DAQ hardware ideas

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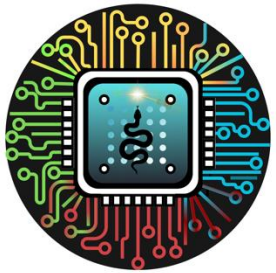
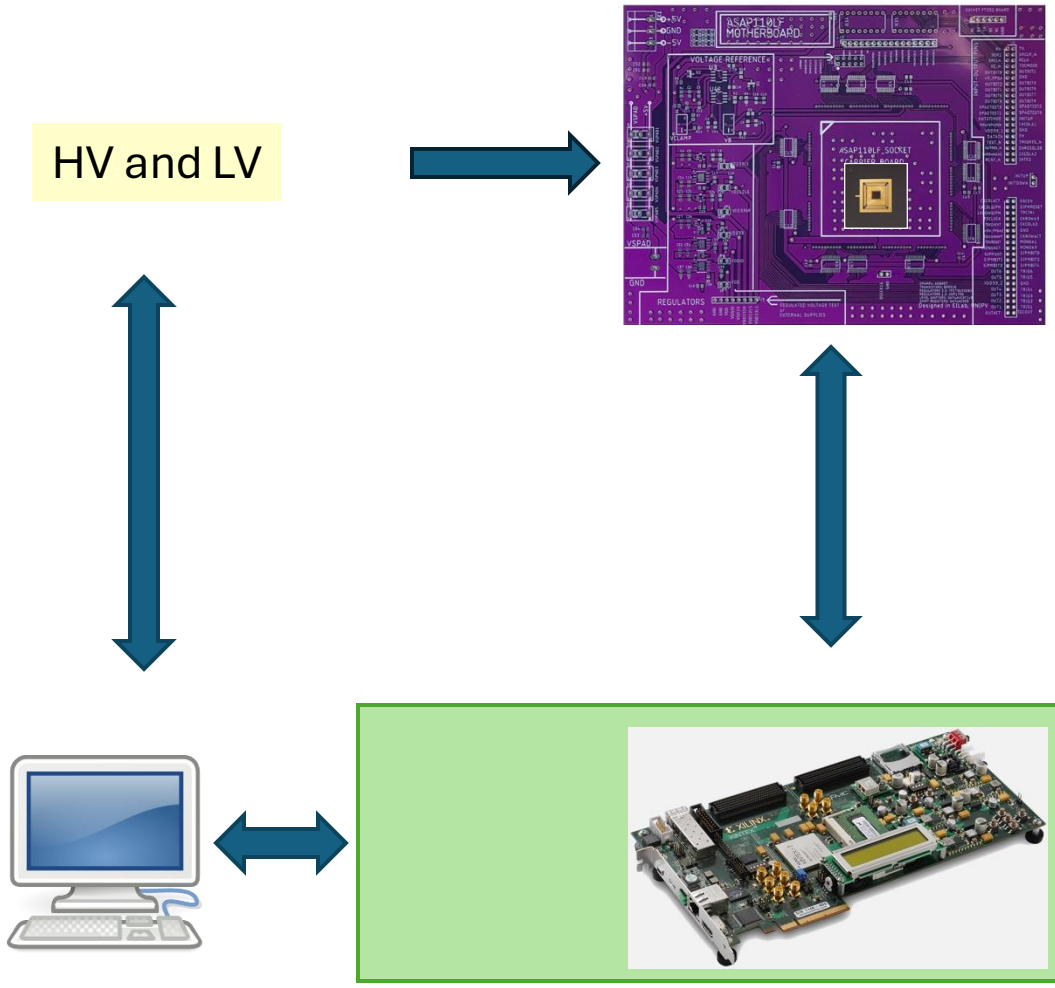


DAQ scheme


HV and LV
ASPIDES chip w/o motherboard
Connection cable
Breakout board
Commercial FPGA board

Requirements and constrains:

- Physical requirements:
  - Distance between the DAQ and the DUT (active irradiation, test beam)
  - Cryo-resistance of the interface cable
  - How many DUTs with the same DAQ? How scalable?
- Electrical requirements:
  - Which transmission protocol between the DAQ and the DUT?
  - How many “wires?”
- Communication with the DAQ PC:
  - Ethernet
  - I2C
  - UART
  - PCI-express
  - A combination?
- Retro-compatibility?
- Cost?

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<5 m
RJ45 (DS), FMC expander in DUNE, FireFly
As many as possible

Parallel (actual), Serial (better), LVDS
As low as possible

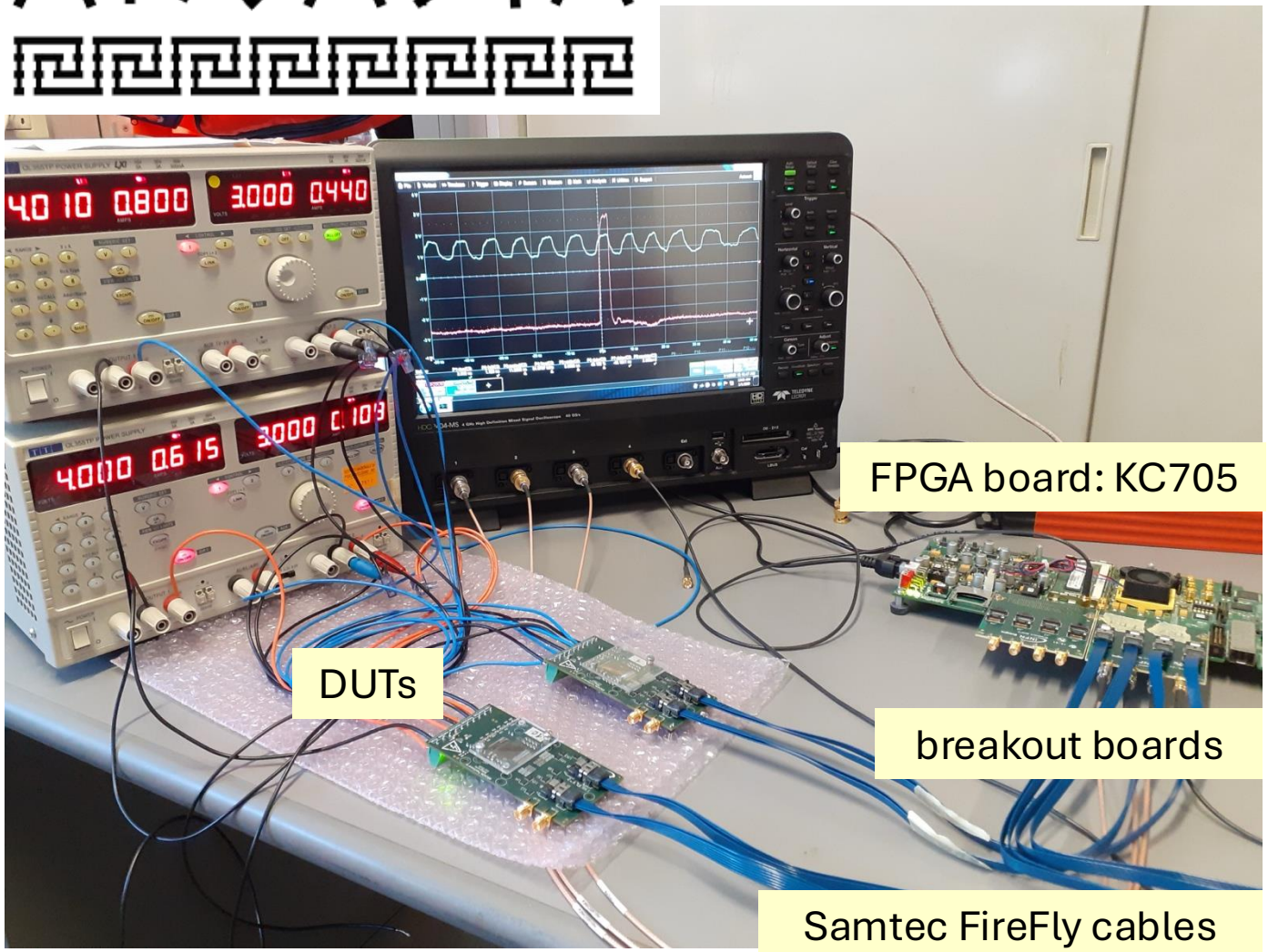
IPBUS 20/30 MB/s polling already available
Easy
Easy
complex

Can be tricky for the number of pins

1 k€ + 4 k€ SJ (BO) + other teams' contributions

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

ARCADIA



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Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

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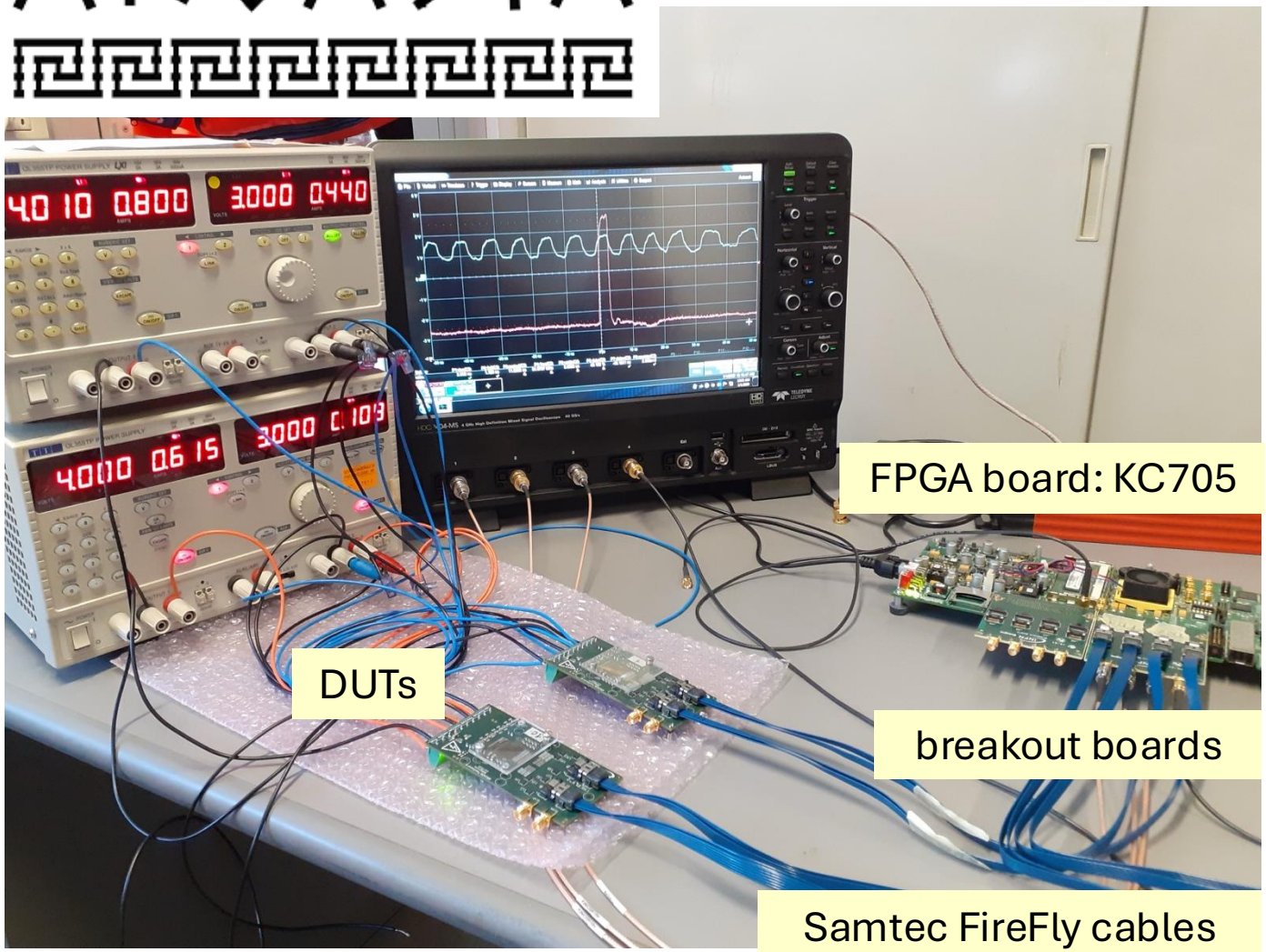

Monolithic fully depleted particle detector CIS 110 nm
24 differential pairs (LVDS)
16 for data with a rate of 640 Mb/s (320 MHz DDR)
8b/10b encoding.
8 lines for clk, rst, testpulse and SPI for config

KC705 Kintex 7 based dev board with **FMC-HPC** (**58 pairs**) and **FMC-LPC** (**34 pairs**). Coax input/output, SFP and ETH connection

Custom breakout boards FMC to FireFly and 2 coax diff I/O. Compatible with both LPC and HPC and agnostic wrt to FPGA

Samtec FireFly PCUE high performance cables. 12 diff pairs up to 28 Gbps. Optical version available

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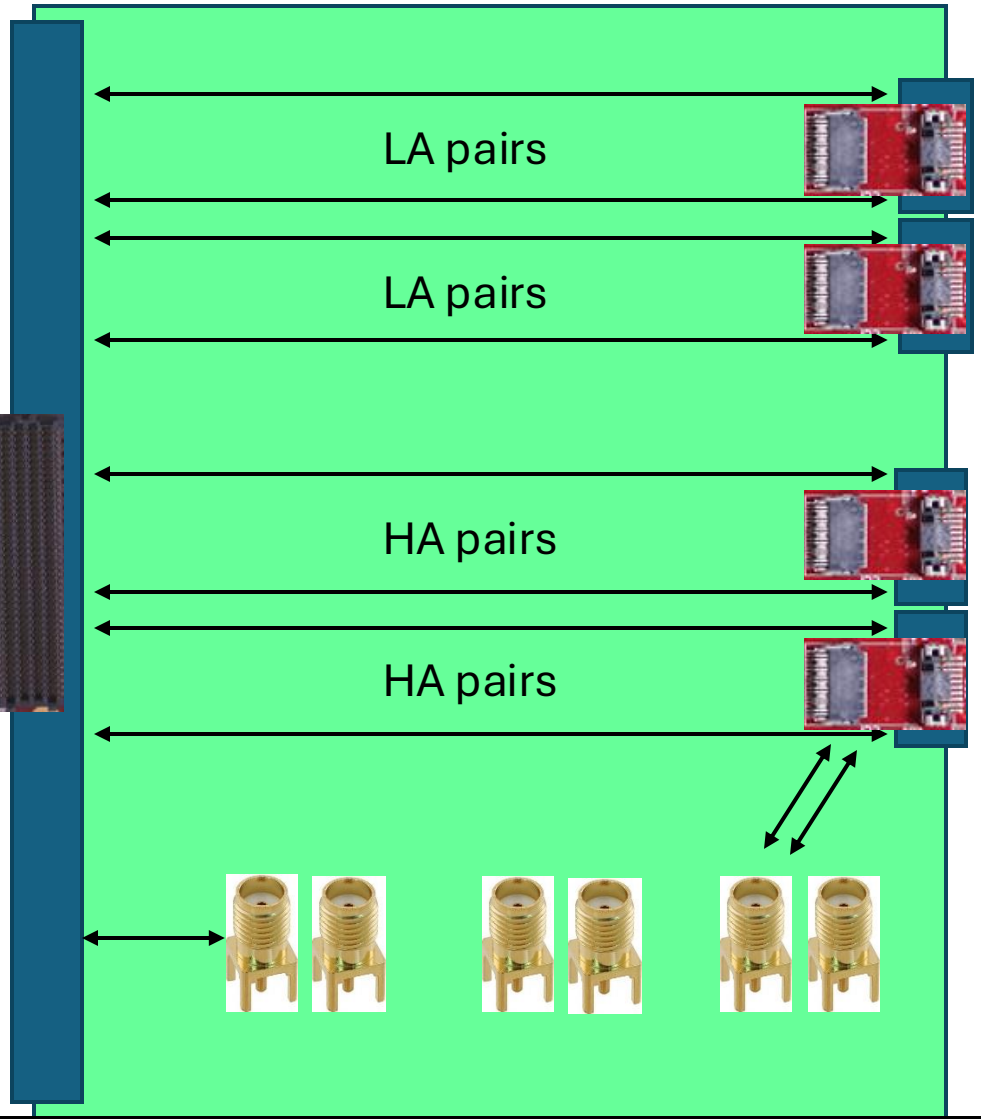
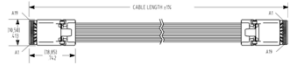
Arcadia- chip board

FMC plug connector

Samtec Firefly



12 LVDS pairs



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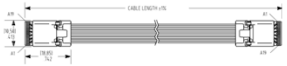

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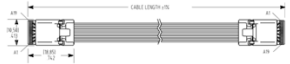
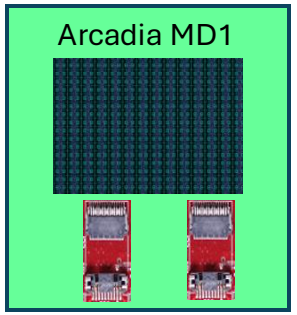
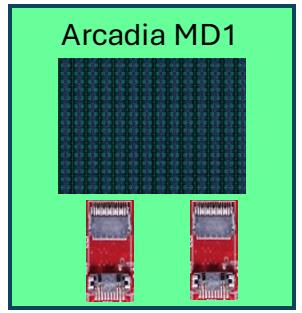




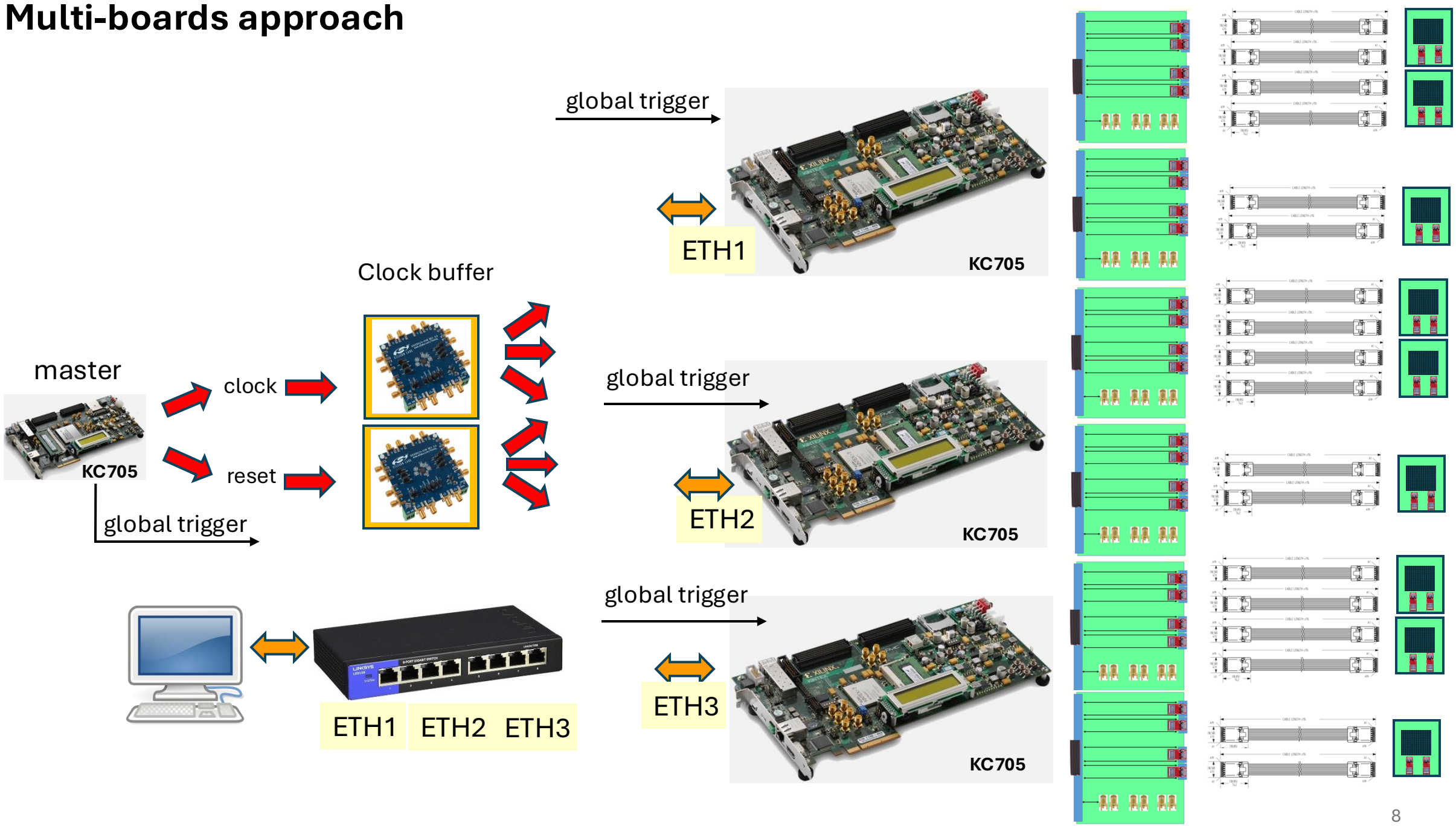


FPGA board: KC705

FMC-HPC: 58 differential pairs + 4 MGTs
FMC-LPC: 34 differential pairs + 1 MGT

SMA connectors for trigger/busy/sync signals

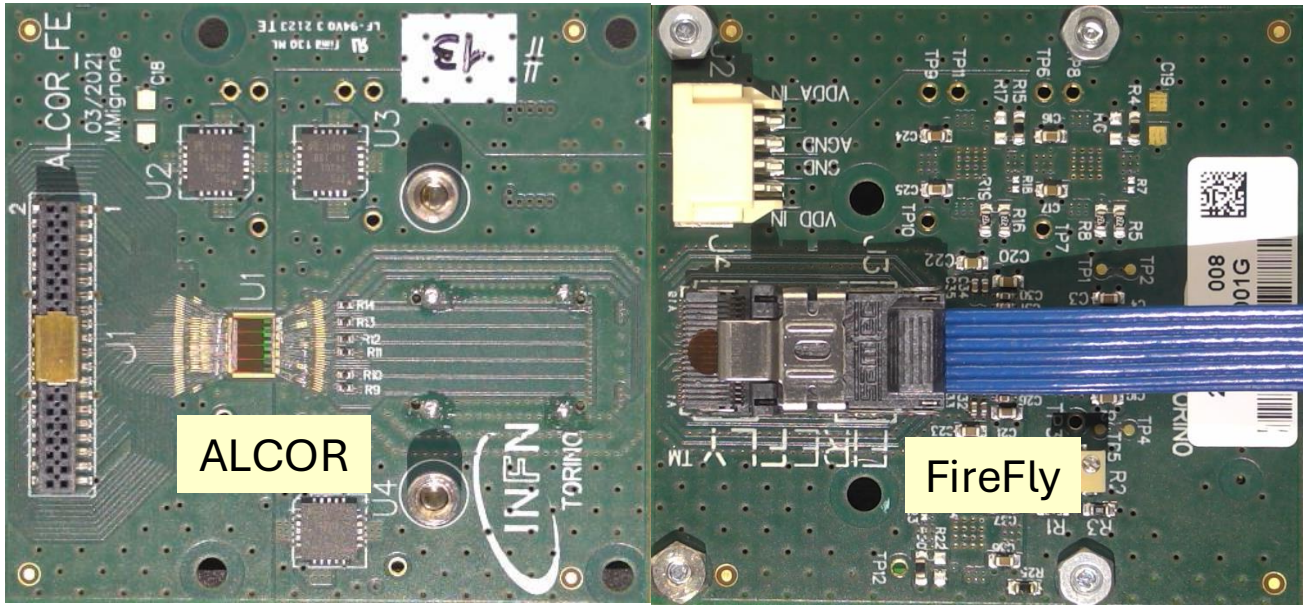
Multi-boards approach



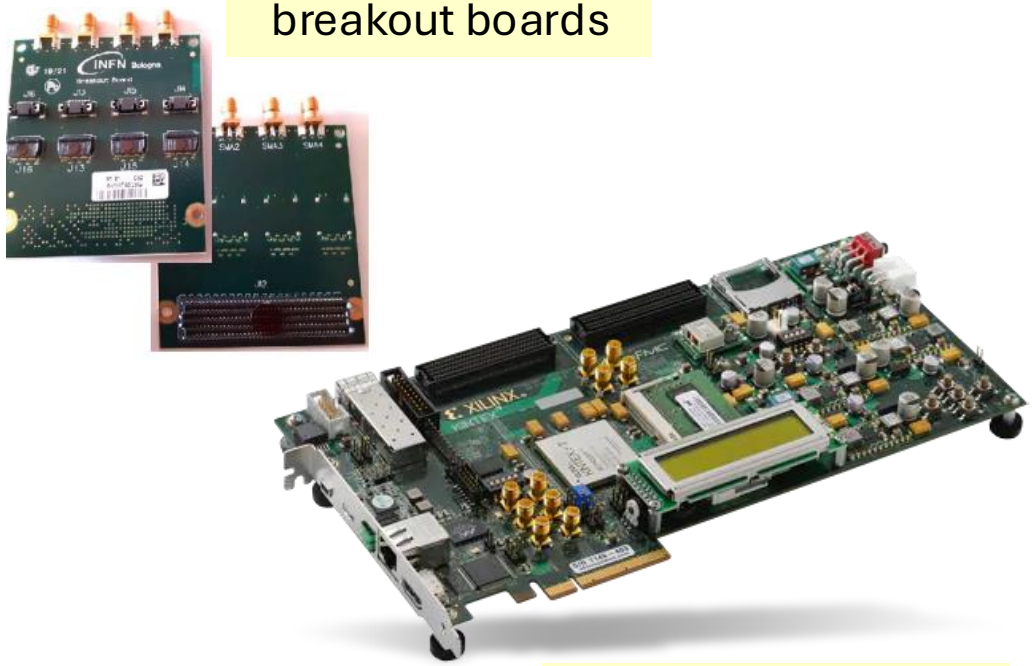
dRICH optical plane based on **SiPMs**

SiPMs readout is based on the ALCOR ASIC (UMC 110 nm):

32-pixel matrix mixed signal ASIC
TDCs based on analogue interpolation with 50 ps LSB (@ 320 MHz)
Fully digital output on 4 LVDS TX data links
SPI-based chip configuration

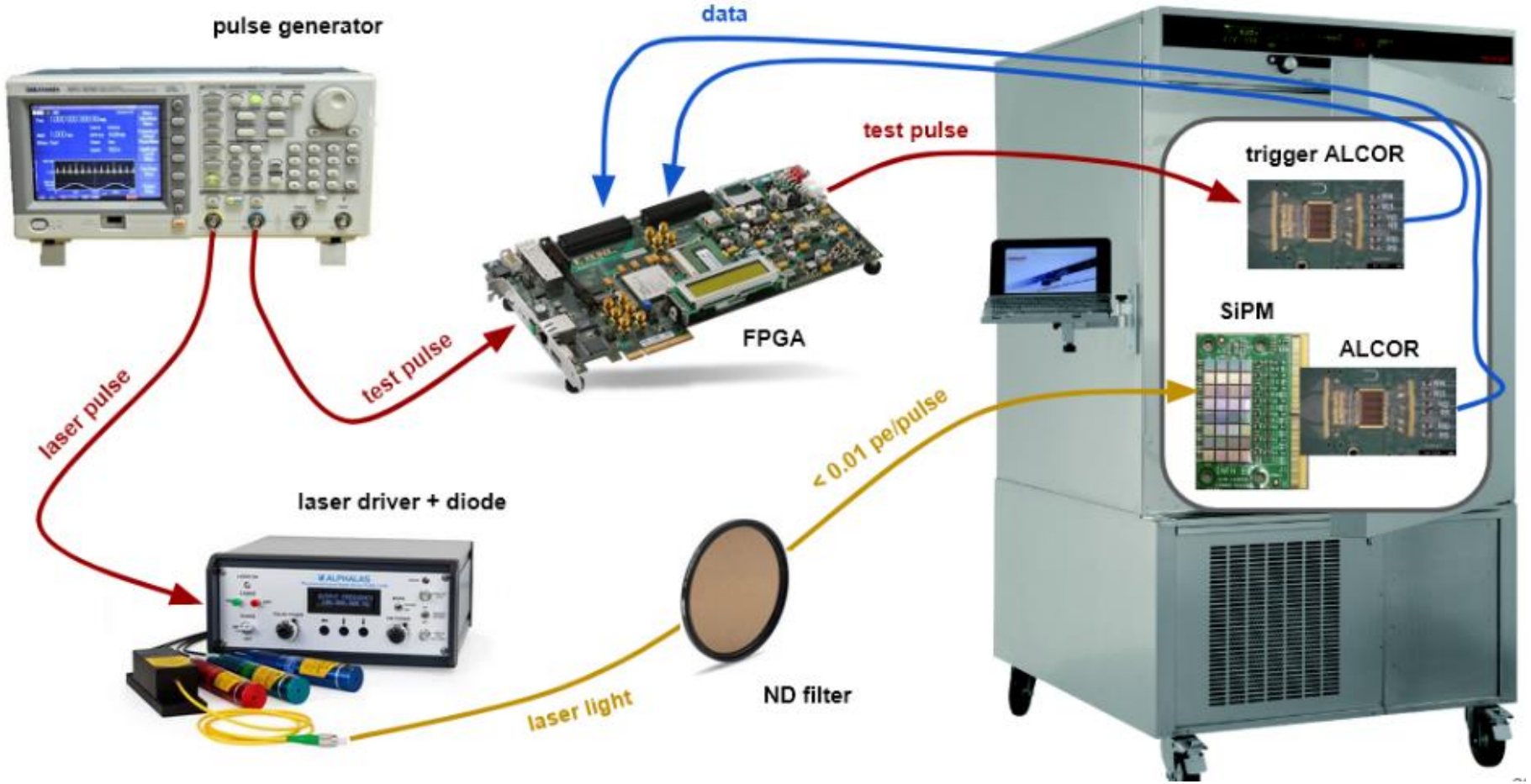


breakout boards

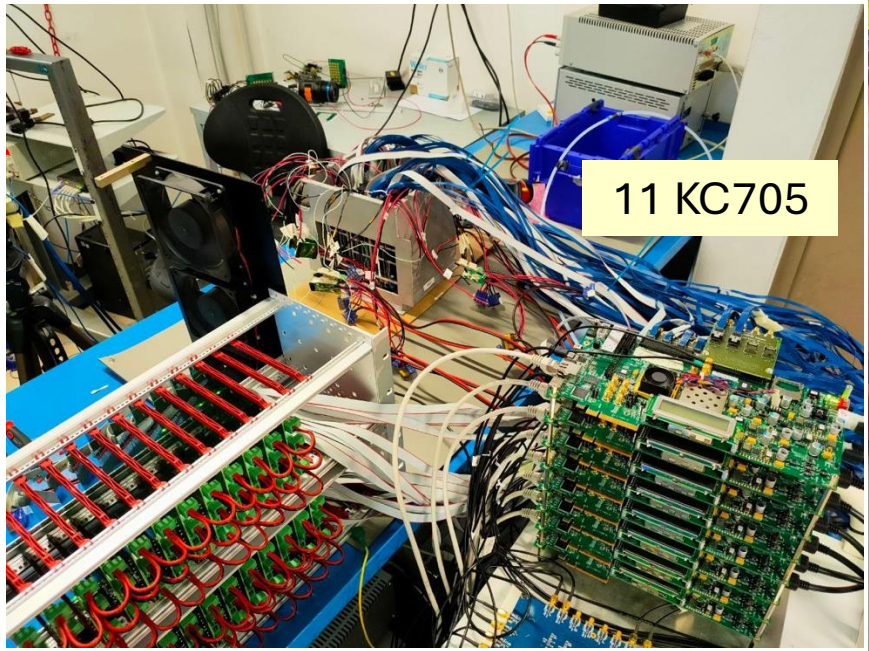


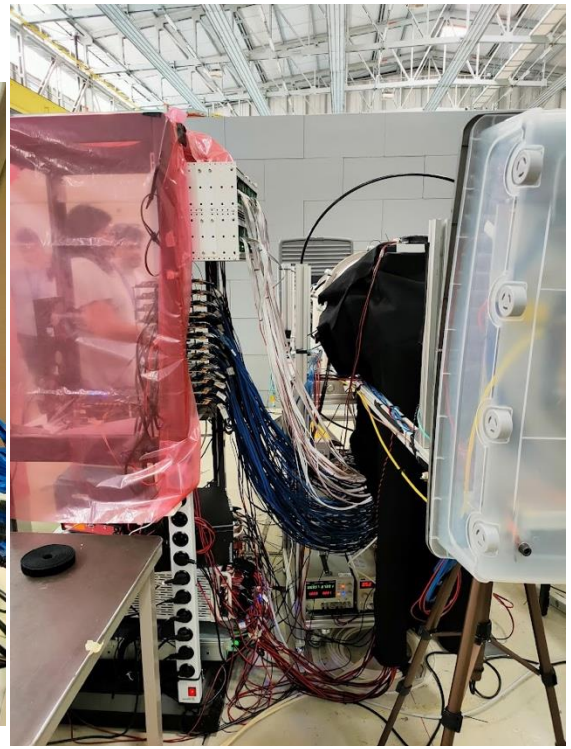
FPGA board: KC705

Setup examples (timing measurement)

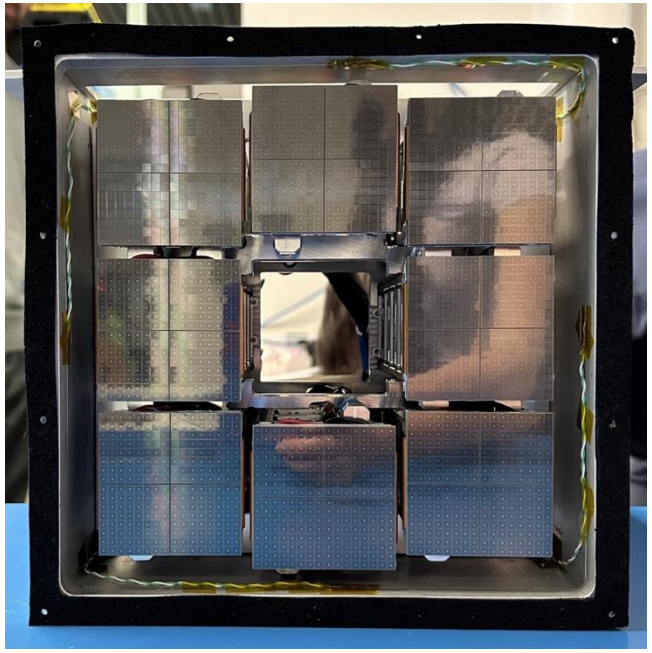


Setup examples (2048 SiPM, 64 ASICS)

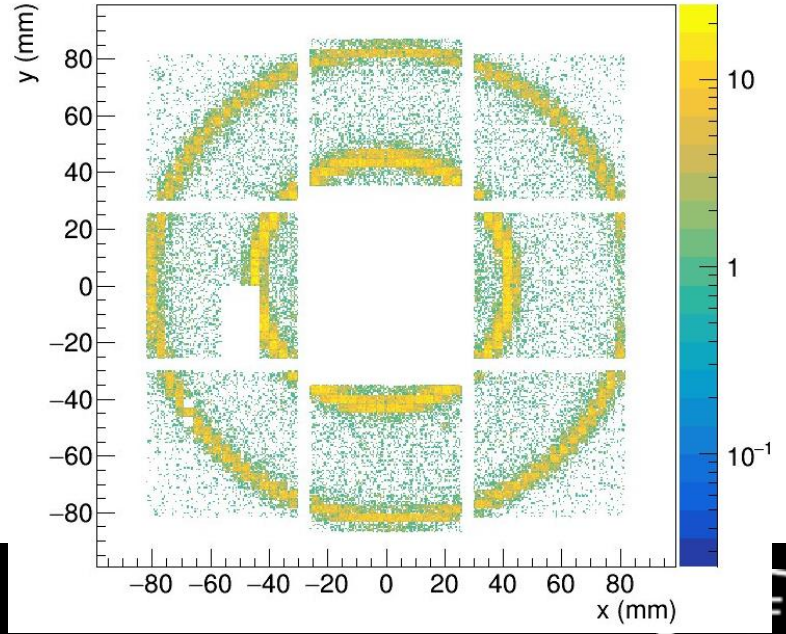




800 Mb/s data rate



dRICH prototype at the 2024 TB



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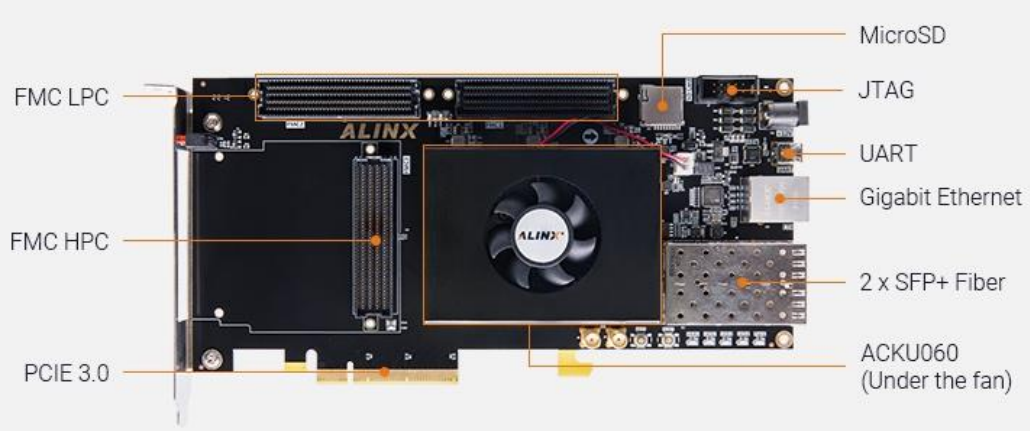
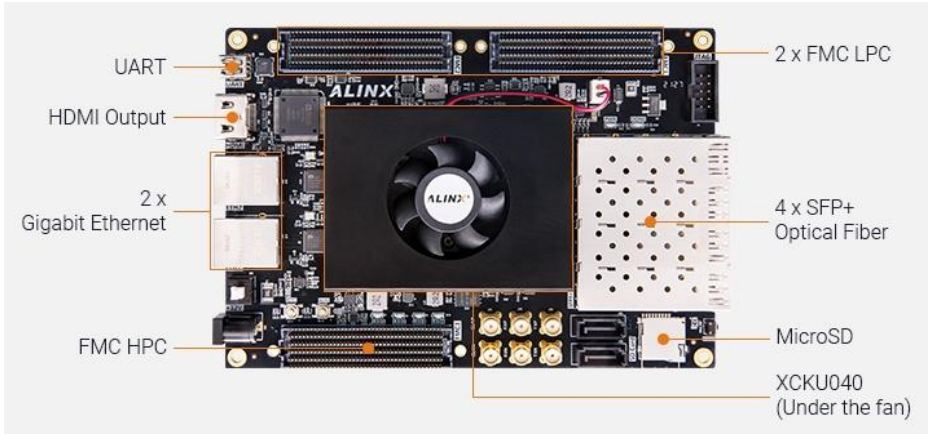
There is a very well known DAQ solution that can ideally work for our purpose but:

- **KC705 deprecated** Kintex7 substituted by Kintex7 US or US+
- VC709 is an alternative with a better FPGA but 1x FMC HPC and very expensive 10 k€

Alinx (Chinese company) alternatives:



AXKU062 Kintex US 2 FMC LPC and 1 FMC HPC
(130 LVDS pairs)
1.216,63 EUR (Mirifica MEPA)



AXKU040 Kintex US 2 FMC LPC and 1 FMC HPC
(123 LVDS pairs)
951,90 EUR (Mirifica MEPA)

Breakout board ≈ 500 EUR
FireFly 2 m cable 80 EUR

Conclusions

- The choice of DAQ HW is strictly dependent on the chip digital interface
- Our suggestion is to implement a register-based approach to reduce the number of wires/pads (less “debuggable”)
- Data output and data rate:
  - How many lines?
  - Parallel or Serial?
    - Fors serial 8b/10b Lvds 320 MHz DDR INFN Torino has the recipe
- Alinx dev boards are proposed as a starting point but if you have any other suggestion…