# WP2 – Testing, data acquisition and integration

R. Santoro


# Proposal submitted

**WP2 – Testing, data acquisition and integration**
*WP2 responsible*: Romualdo Santoro (MI)
*Main WP2 contributors*: BA, BO, MI, NA, PD, PV, TIFPA

This WP will be responsible for the development of the hardware and software test systems for the evaluation of the test chip and the prototype and the demonstrator chips in the laboratory environment. WP2 will also define the measurement procedures for the parameters of interest (DCR, after-pulsing, cross-talk, PDP, QE, time resolution), in agreement with well established practice in the field. In collaboration with WP3, the members of WP2 will design and assemble suitable test boards and acquisition systems also for radiation tolerance characterization and tests in cryogenic conditions. The WP will also be responsible for the integration of 2 or 4 demonstrator chips in a module and its characterization in the laboratory and on a beam line.

# Proposal submitted

**Test chip: ASAP110LF**

**Prototype chip**

**Demonstrator**

Tasks

- Task 2.1 (M1-M4): design and production of the measurement setup for the test chip (also in view of radiation hardness and cryogenic tests)
- Task 2.2 (M5-M12): test chip characterization (including radiation tolerance and cryogenic tests)
- Task 2.3 (M13-M16): design and production of the measurement setup for the prototype chip
- Task 2.4 (M17-M20): prototype chip characterization (including tests after irradiation and in cryogenic conditions)
- Task 2.5 (M21-M28): design and production of the measurement setup and of the module for the demonstrator chip
- Task 2.6 (M29-M35): laboratory characterization of the demonstrator chip
- Task 2.7 (M32-M35): integration of the demonstrator chip in the module
- Task 2.8 (M36-M36): test of the demonstrator module on a beam line

Milestones

- M4: the measurement system for the test chip is ready
- M16: the measurement system for the prototype chip is ready
- M28: the measurement system for the demonstrator is ready
- M35: the module integrating the demonstrator chip is ready

Deliverables

- M4: measurement system for the test chip
- M16: measurement system for the prototype chip
- M28: measurement system for the demonstrator
- M35: module with the demonstrator

# The team: starting point

| WP2 - Testing, data acquisition and integration | | | | |
|---|---|---|---|---|
| | | | | |
| **nome** | **cognome** | **email** | **sezione** | **ruolo/contributo/interesse** |
| Romualdo | Santoro | romualdo.santoro@uninsubria.it | MI | **WP leader** |
| Lodovico | Ratti | lodovico.ratti@unipv.it | PV | caratterizzazione di circuiti integrati |
| Aleksandr | Burdyko | aleksandr.burdyko@uninsubria.it | MI | contributo: design pcb, firmware, qualifica dSiPM |
| Romualdo | Santoro | romualdo.santoro@uninsubria.it | MI | contributo: qualifica dSiPM |
| Gianmaria | Collazuol | gianmaria.collazuol@pd.infn.it | PD | interesse: in firmware readout |
| Nicola | Mazziotta | mazziotta@ba.infn.it | BA | caratterizzazione senore e test |
| Luigi | Rignanese | rignanes@bo.infn.it | BO | design pcb, scelta FPGA, firmware, qualifica dSiPM |
| Davide | Falchieri | davide.falchieri@bo.infn.it | BO | design pcb, scelta FPGA, firmware, qualifica dSiPM |
| Marcello | Campajola | macampajola@na.infn.it | NA | interesse in caratterizzazione del sensore |

# WP2: Starting point

- Setup finalization for the test chip: ASAP110LF (M1-M4)
  - Firmware to assess all structures and documentation → A small team just started: help would be nice
  - GUI and data visualization (?) → No-activity: any interest?
  - Hardware production and distribution → Lodovico is taking care of it
    - 10 chips available
    - FPGA: evaluation kit (obsolete, but there are a lot of boards in Pavia)
  - Any requirement for cryogenic test?
  - Any requirement for radiation hardness test?

→ Feedback would be important!

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  - Standard condition → Preliminary studies
  - Cryogenic test
  - Rad hard test

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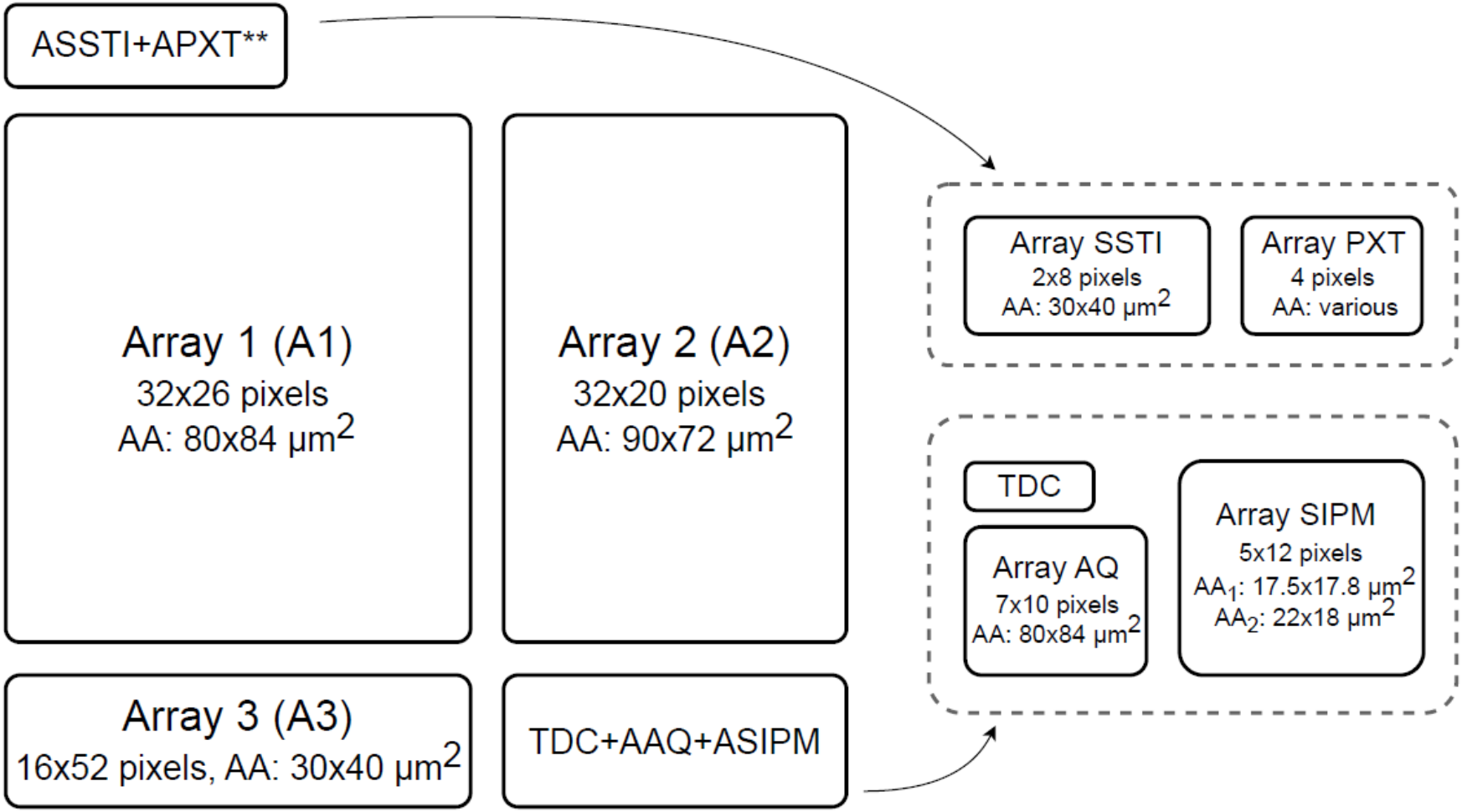
  - Standard condition → Preliminary studies
  - Cryogenic test
  - Rad hard test
- First WP2 meeting: focus on the requirements from Cryogenic and radiation hardness test

# Backup

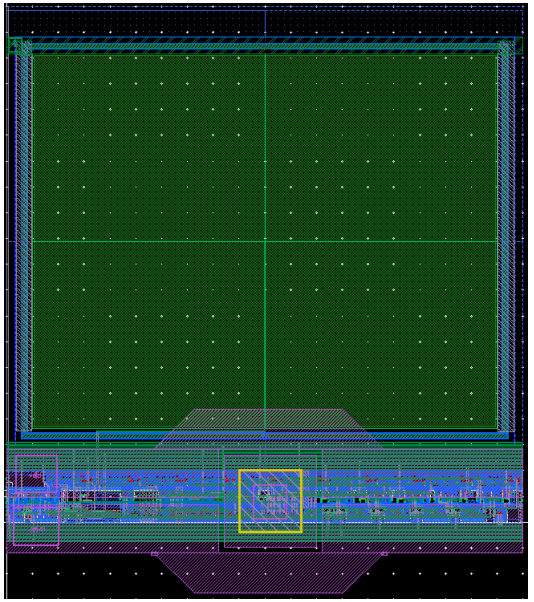
# ASAP110LF chip

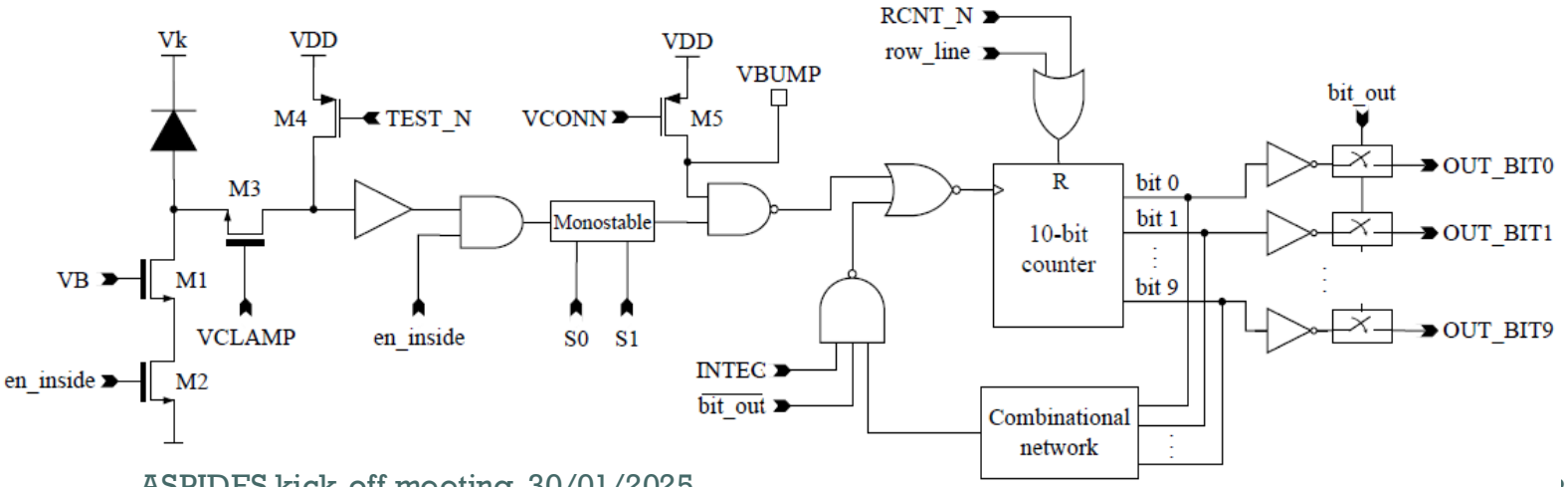


# ASAP110LF chip – Array A2

Array 2 (A2) cell:

- The avalanche is quenched by a passive network
- The monostable circuit modifies the duration of the sensor pulse (400 ps, 750 ps, 2 ns, transparent mode).
- A 10 bit counter automatically counts the pulses.

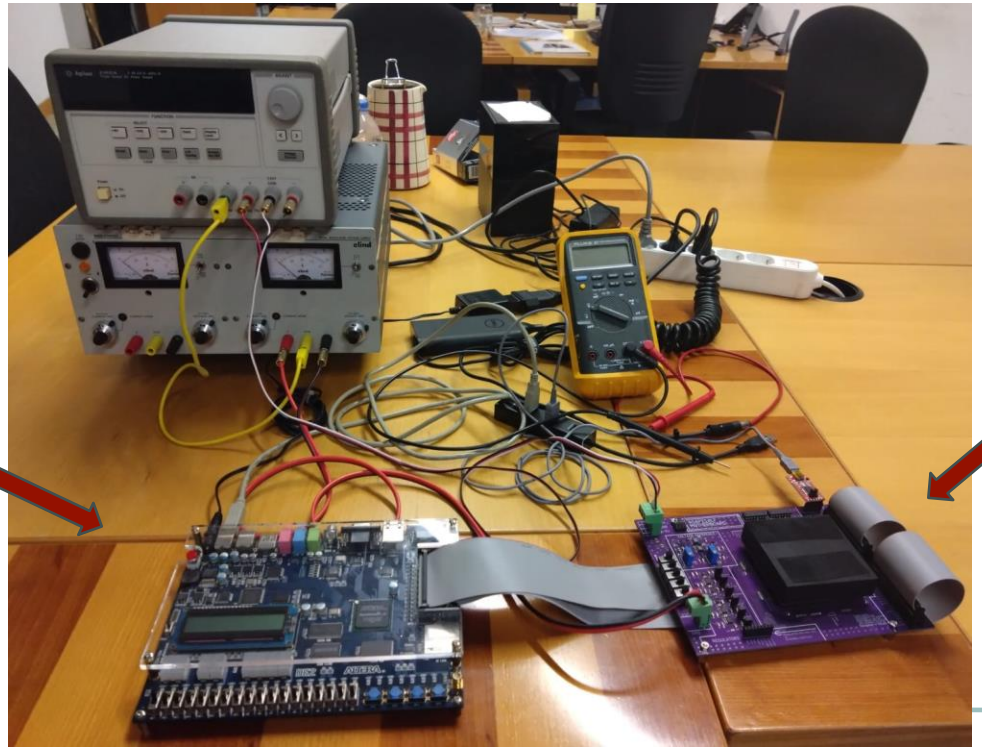




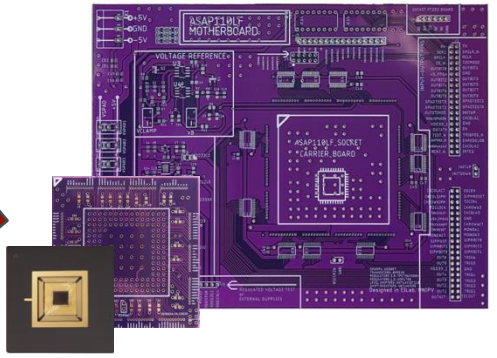
# Test setup

- Two custom boards acting as interface between the FPGA and the chip.
- Firmware developed in VHDL
- Data acquisition based on protocol RS232 (command line)

FPGA: Altera DE2 (education board)



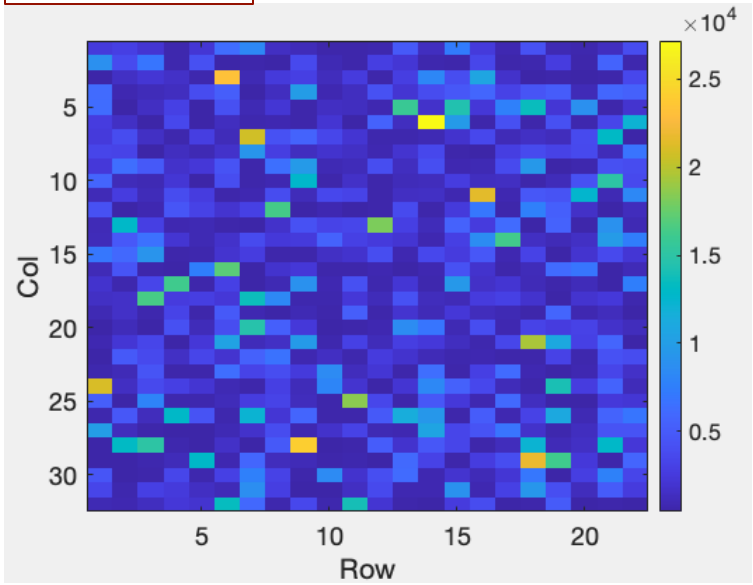
Custom bard + ASAP110LF chip

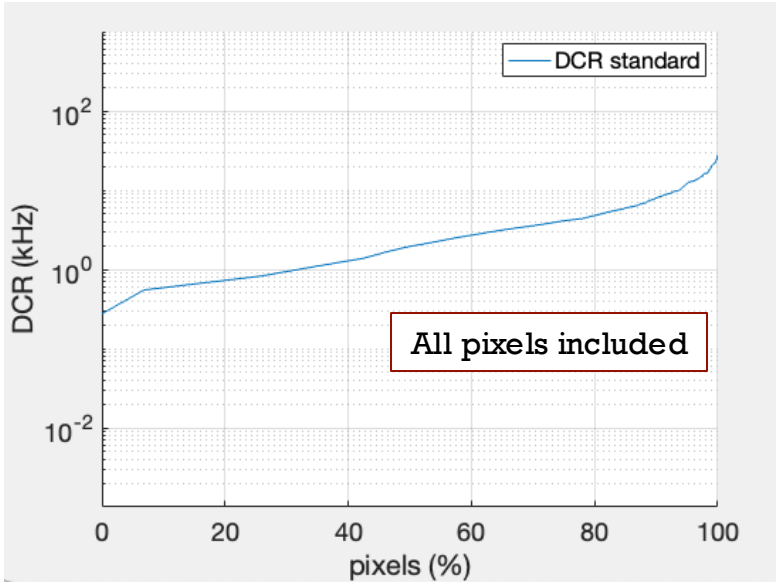


# DCR measurements @ 20V

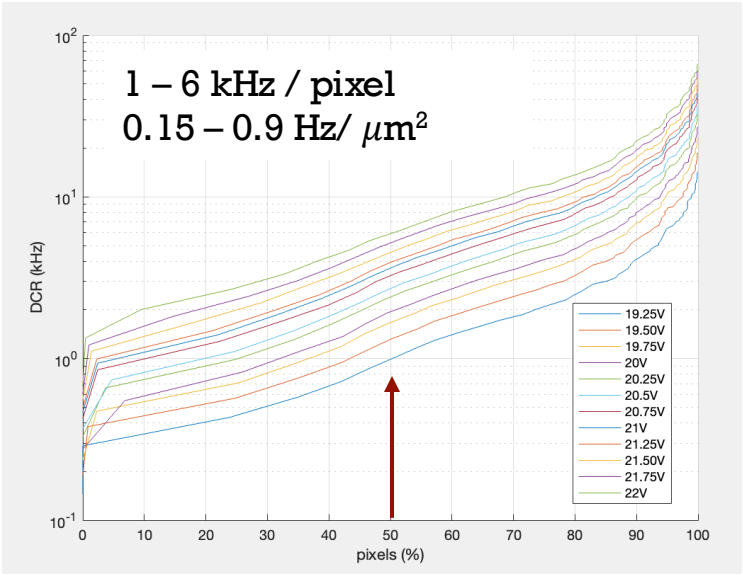
- We are collecting counts in 30k windows (1 ms long). I'm summing counts in 1000 windows -> Average value is the DCR contaminated by AP (DCR standard)

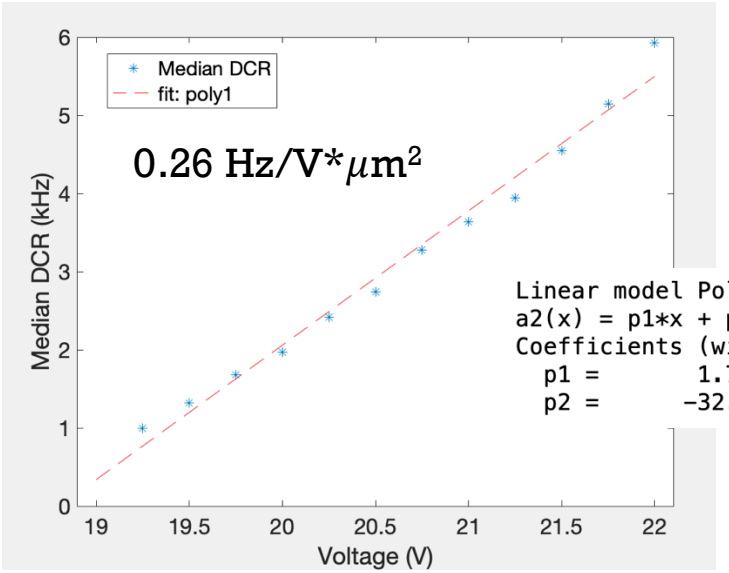
DCR standard



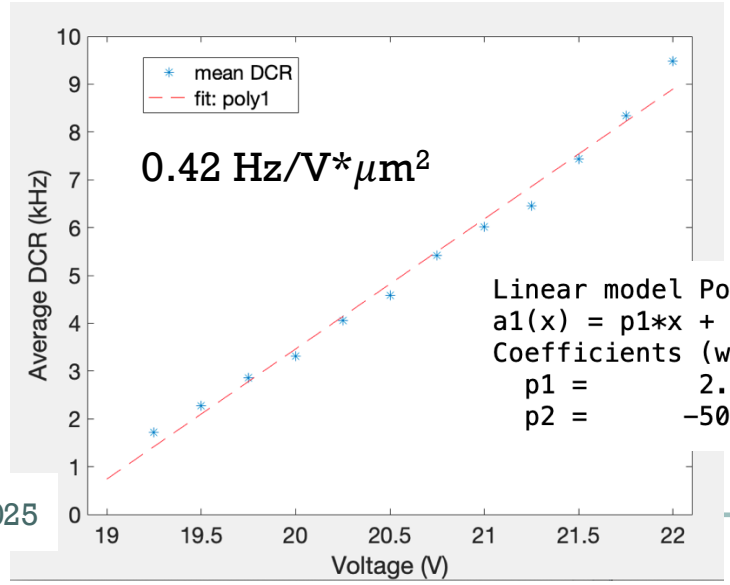



# DCR VS Voltage




```
Linear model Poly1:
a2(x) = p1*x + p2
Coefficients (with 95% confidence bounds):
  p1 =       1.719  (1.569, 1.869)
  p2 =      -32.33  (-35.43, -29.23)
```

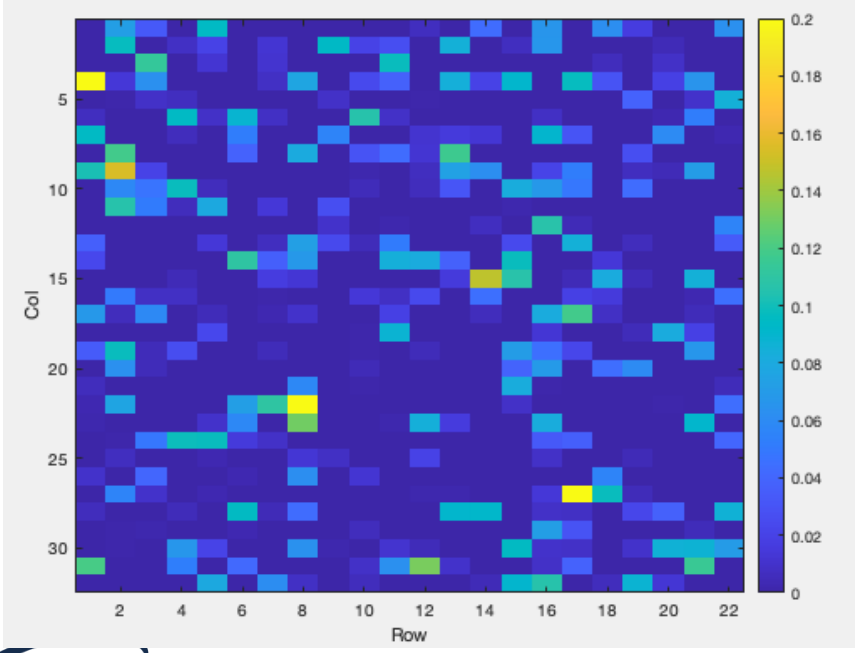



```
Linear model Poly1:
a1(x) = p1*x + p2
Coefficients (with 95% confidence bounds):
  p1 =       2.719  (2.513, 2.926)
  p2 =      -50.93  (-55.19, -46.67)
```

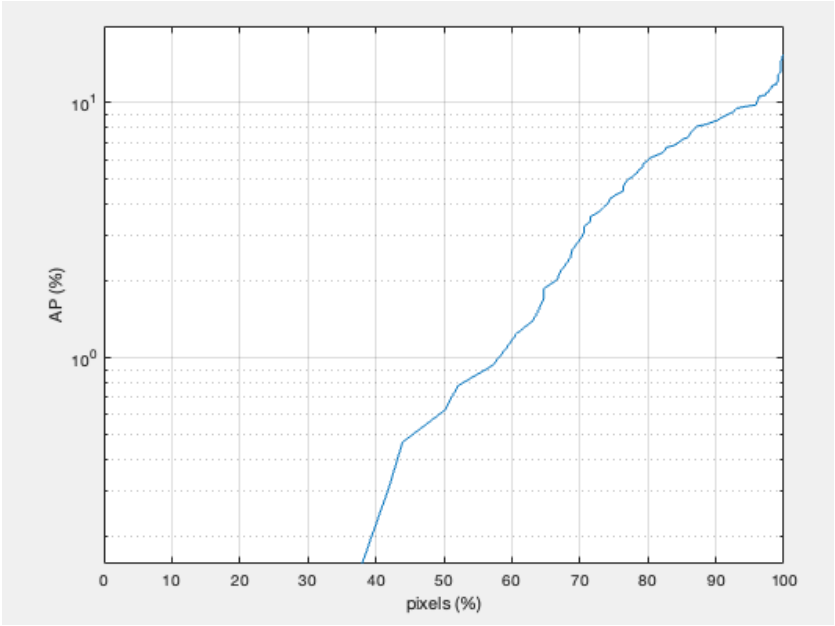
# AP measurements @ 21V

- N pixels with wrong windows (N0=0) -> 15.8% (removed from the plots)
- N pixels not following the Poisson statistic (chi2/ndf > 20) -> 20%

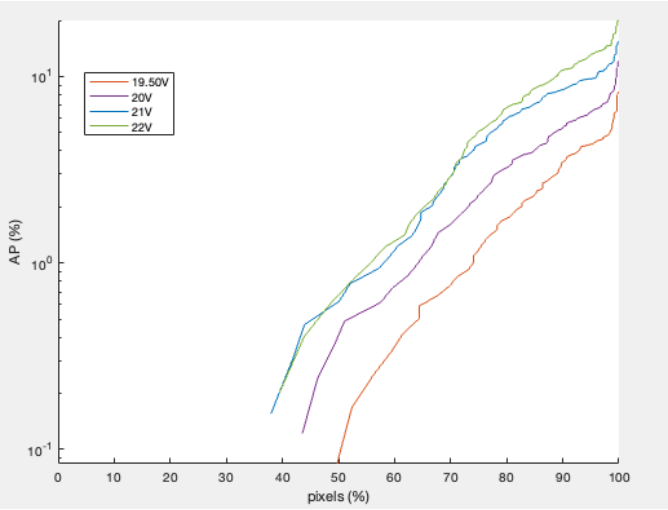
AP in the matrix: all pixels included
(also "wrong windows" and "no-Poisson")

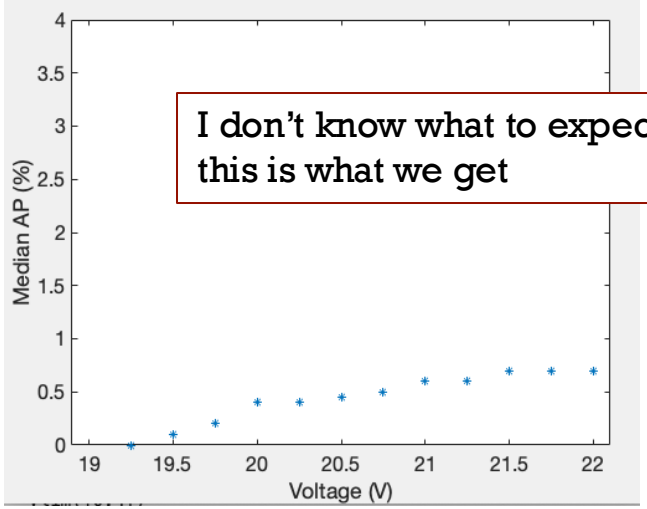



AP, cumulative distribution: only the 64% of all pixels are included in the plot (good pixels)

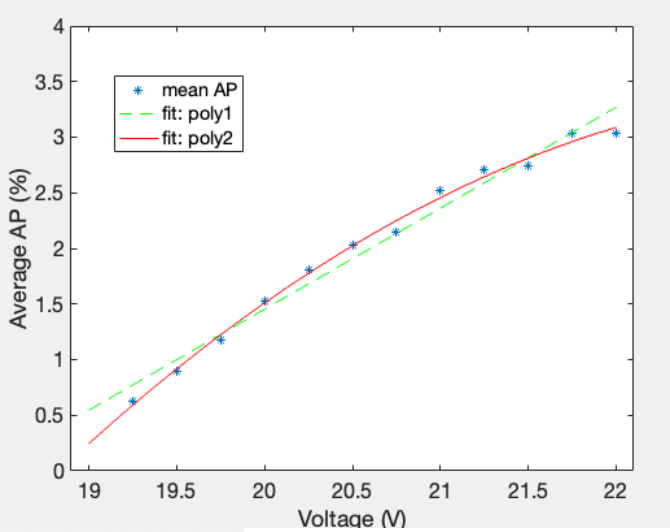


# AP VS Voltage




I don't know what to expect: this is what we get




```
Linear model Poly1:
a1(x) = p1*x + p2
Coefficients (with 95% confidence bounds):
  p1 =      0.9079  (0.8111, 1.005)
  p2 =       -16.7  (-18.7, -14.71)
```