# ASPIDES WP1 – ASIC design and verification

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# ASPIDES: WP1 – ASIC design and verification

WP1: simulation, design and verification of the prototype chip and the demonstrator.

Time: 28 months of the 36 needed by the whole project

### Tasks

- Task 1.1 (M1-M2): draft of the specifications for sensors and integrated readout electronics
- Task 1.2 (M3-M16): simulation, layout, verification and production of the prototype chip
- Task 1.3 (M13-M28): simulation, layout, verification and production of the demonstrator chip

#### Milestones

- M2: specification sheet for sensors and integrated readout electronics drafted
- M10: layout of the prototype chip submitted
- M22: layout of the demonstrator chip submitted

#### Deliverables

- M2: specification sheet for sensors and integrated readout electronics
- M16: prototype chip
- M28: demonstrator chip

### ASPIDES: WP1 – Prototype chip

- Time: November 2025 for MPW
- **Budget:** 50 k€ + 5 k€
  - 50 k€ -> LFoundry CMOS 110 nm (2520€/mm2) -> ~ 16 mm2 (with 4 metal layer option)
  - 5 k€ -> packaging for 10 chips

#### • The metal layer option issue:

- M4 option: no extra cost
- M6 option: 18.800 € extra budged (NO VAT) to be shared with the other "M6 users"
  - According to LFoundry the chance to have another M6 customer is 30% (name cannot be disclosed, extra budget sharing is managed by LFoundry)
  - Silicon area using the 50 k€ with M6 option: 8 mm<sup>2</sup>
  - Silicon area using the 50 k€ + extra with M6 option : total area 16 mm<sup>2</sup>: ASPIDES 11 mm<sup>2</sup> + 5 mm<sup>2</sup> for sponsor

### ASPIDES: WP1 - PDK and DEV tools

#### PDK:

- LF110nm PDK -> leatest release 1.3.2 (July 2022)
  - 2 metal layer options available
  - 2 MOS flavours available: 110 nm (1.2 V), 360 nm (3.3 V)
- SPAD Addon -> release 1.0.0 (June 2019) -> provides abstracts and PV rules for 4 different FBK SPADs
  -> Is it still needed due to our custom cells?

### **DEV tools:**

- Cadence:
  - INFN has a reduced set of licences shared among the sections -> slow design process
  - PDK for Cadence is better developed -> fast layout drawing
- Synopsys:
  - INFN section local licences -> fast design process
  - PDK not as good as Cadence one > slow layout drawing
- Calibre:
  - Physical verification: DRC, LVS, ERC

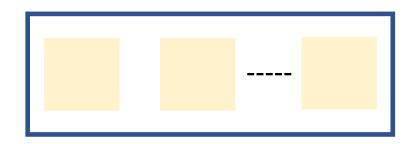
### ASPIDES: WP1 – Resources Sharing

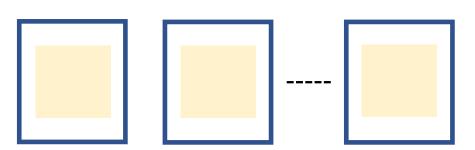
A repository/database should be created to share technical documents, design files, manuals, etc:

- The prototype will contain several parts: dSiPM, aSiPM, transistors for cryogenic characterization, electronic blocks and so on:
  - Are we going to create a common database for sharing?
  - Standard IPs (Bandgap, DAC, ADC, SLSV Rx/Tx, etc.), common/personal?
  - In case of sharing, a database to keep the history of all updates could be usefull, Cliosoft could be a solution.
- We can use Alfresco for documents, but it's not suitable for design files (usually foundries clearly ask for Cliosoft or similar)

# ASPIDES: WP1 – Prototype organizzation

- WP1 participants: BA, BO, PV, TO? How to share the area?
  - We need and estimation of the blocks that each participant wants to prototype
    - 4 equal sections + 1 for common blocks
    - 4 sections of different area + 1 for common blocks
- Prototype organizzation:
  - One common pad-ring shared among all the structures/blocks
  - Several chiplet (area consumption and extra cost for dicing)





### ASPIDES: WP1 – Task 1.1 & Task 1.2

- Task 1.1 (2 Months): draft of the specifications for sensors and integrated readout electronics
  - 1. Collect the specifications starting from the contribution of yesterday (BA, NA, MI)
  - 2. Organize specifications in a shared table: one column for each application and one row for each specification (time resolution, charge resolution, spatial resolution, area, etc.)
  - 3. One meeting (online) to discuss and approve the final specification document
- Task 1.2 (14 Months): simulation, layout, verification and production of the prototype chip
  - 8 months for design, layout and verification -> prototype assembly and verification 1 month
  - For the design the SPAD model is needed -> is it already available?
  - Floor plan (estimation):
    - Collect the number of blocks, area, pins, power domains (A/D) and consumption.