A sub 100-ps LSB Time-to-Digital Converter based on a Pseudo-Differential Ring Oscillator in a 110 nm CMOS Technology

Master's Degree of

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UNIVERSITÀ
DI PAVIA

Supervisor: Prof. Lodovico Ratti

Outline

- **Time-to-Digital Converter (TDC)**
- **Architecture:** Interpolation based TDC
- Resolution Control System
- Simulation Results
- **digital Silicon Photo Multiplier (dSiPM)**
- **Synthesizable dSiPM:** Recursive structure
- **Tools:** Xcelium, Genus and Innovus
- Preliminary Results

Outline

Time-to-Digital Converter (TDC)

Architecture: Interpolation based TDC

Resolution Control System

Simulation Results

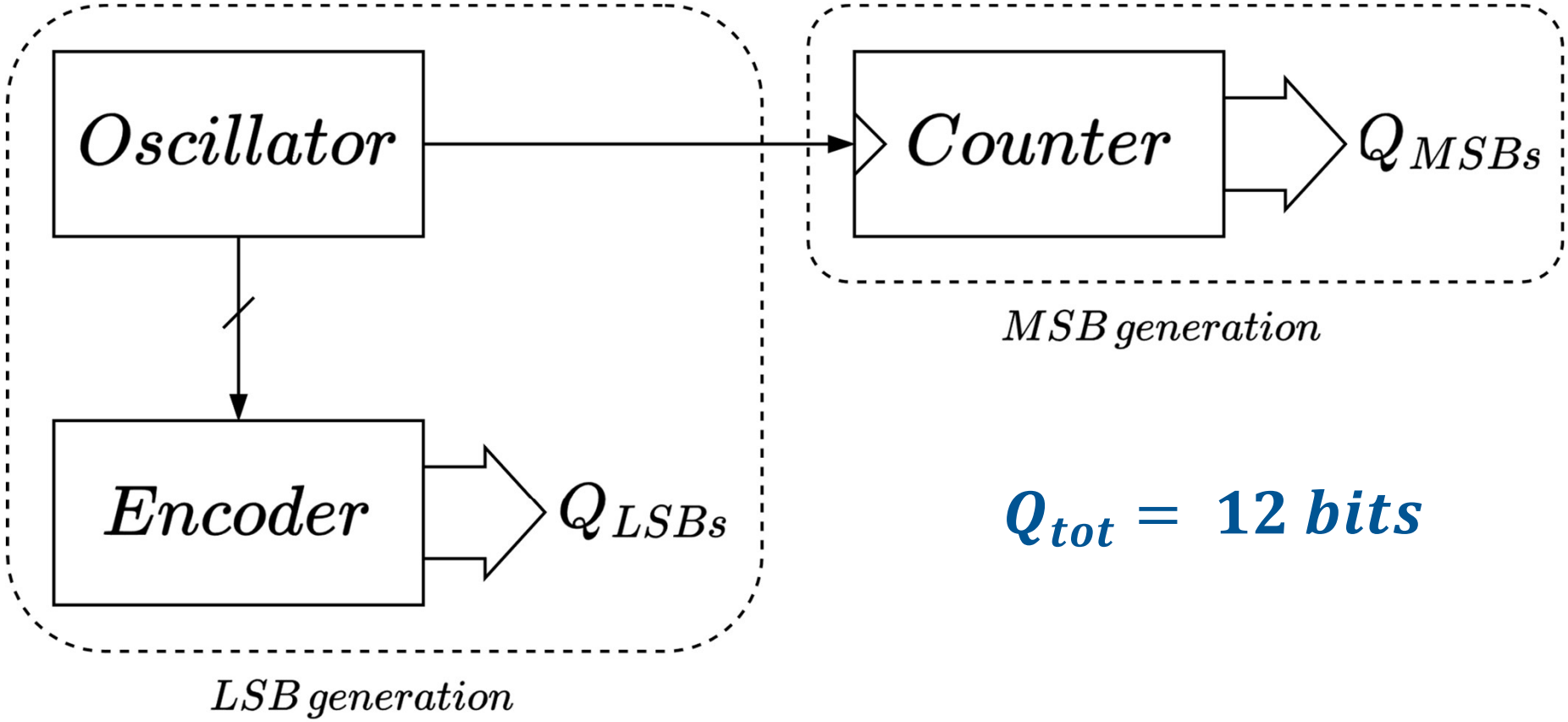
digital Silicon Photo Multiplier (dSiPM)

Synthesizable dSiPM: Recursive structure

Tools: Xcelium, Genus and Innovus

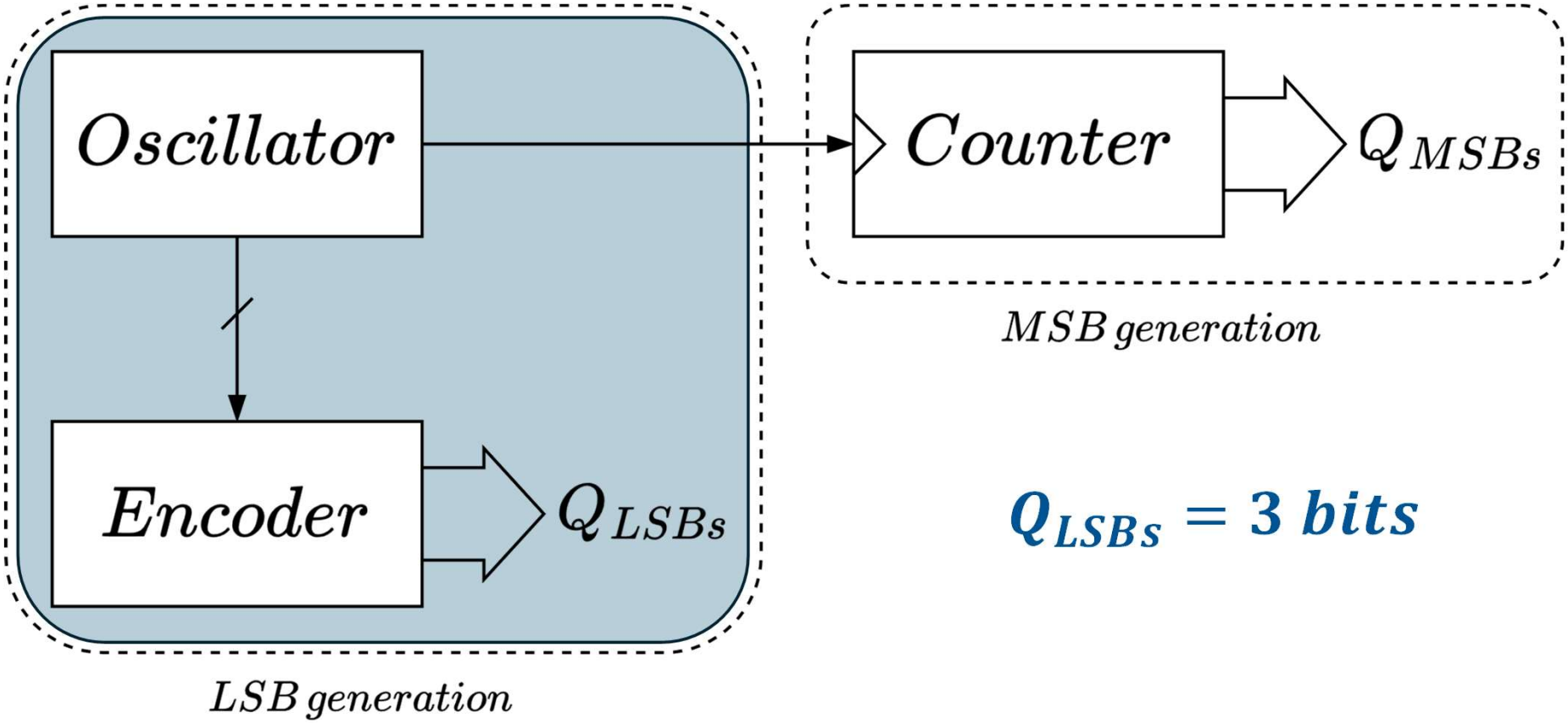
Preliminary Results

Architecture: Interpolation TDC



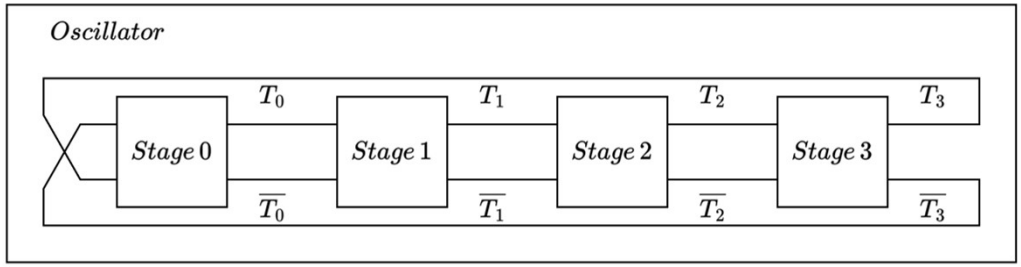
$$Q_{tot} = 12\ bits$$

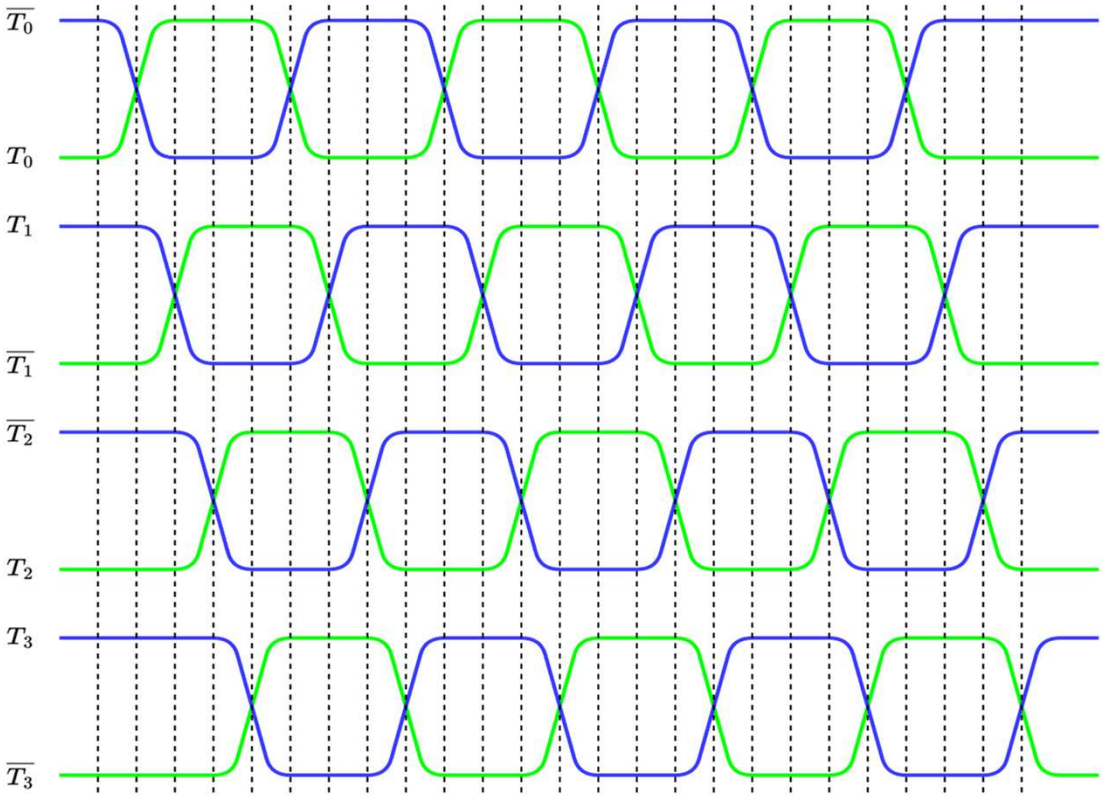
LSBs Generation



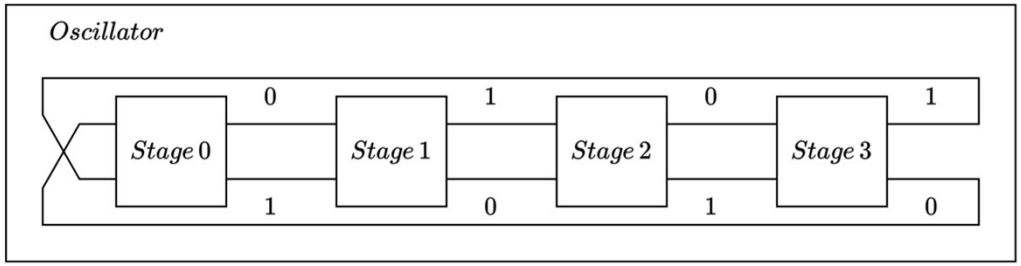
$$Q_{LSBs} = 3\ bits$$

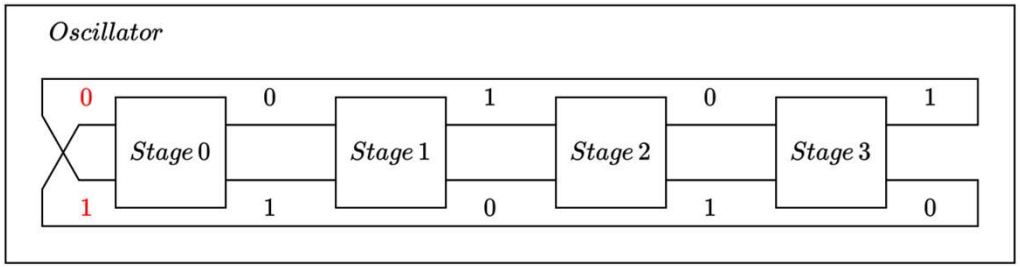
Oscillator Waveforms

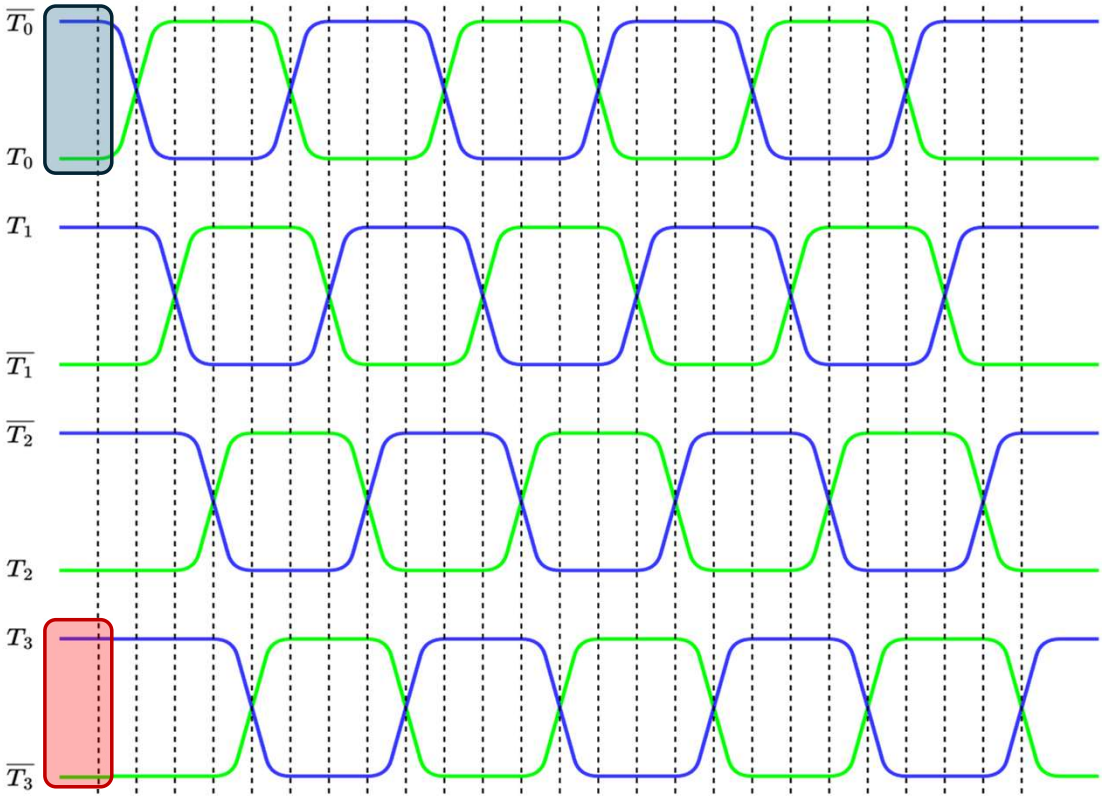


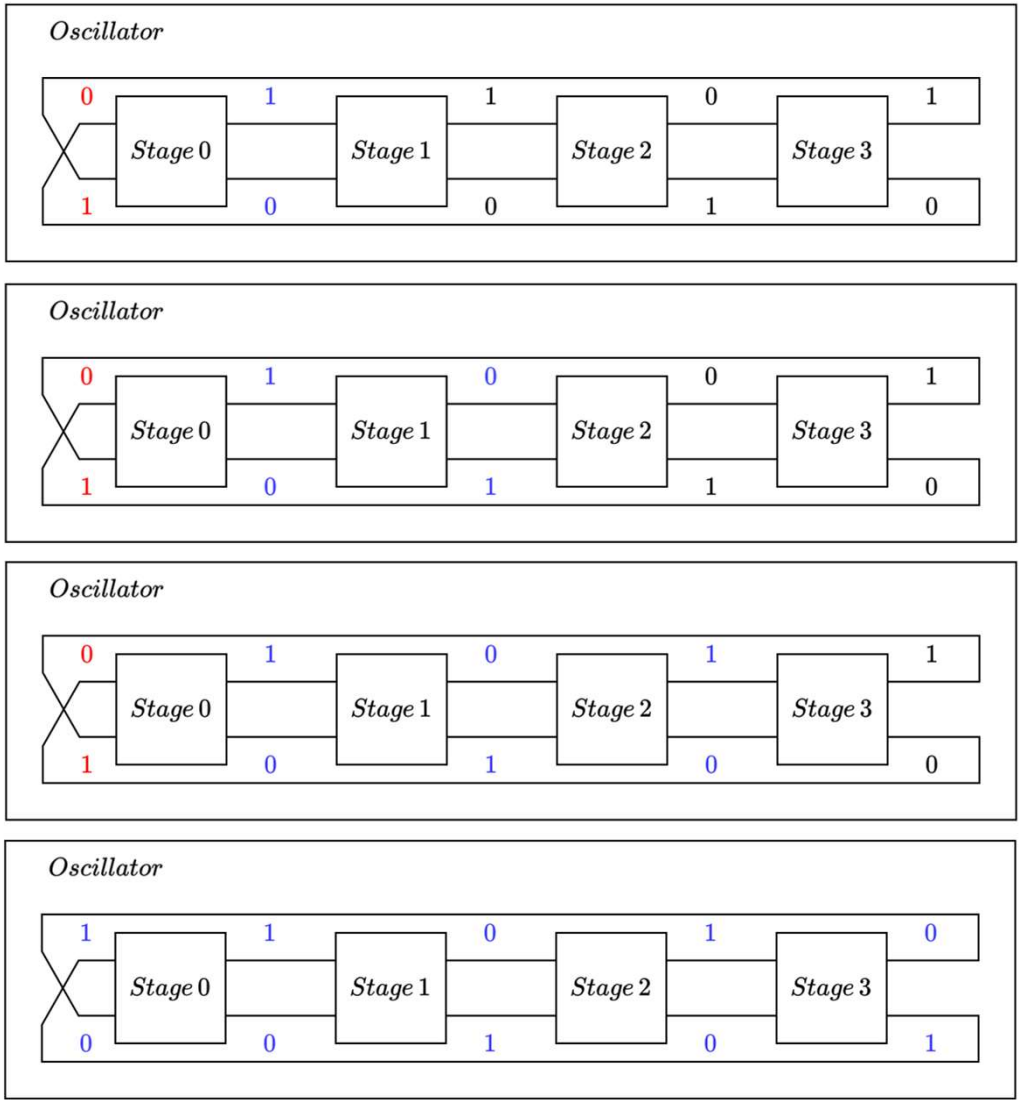


Oscillator Waveforms

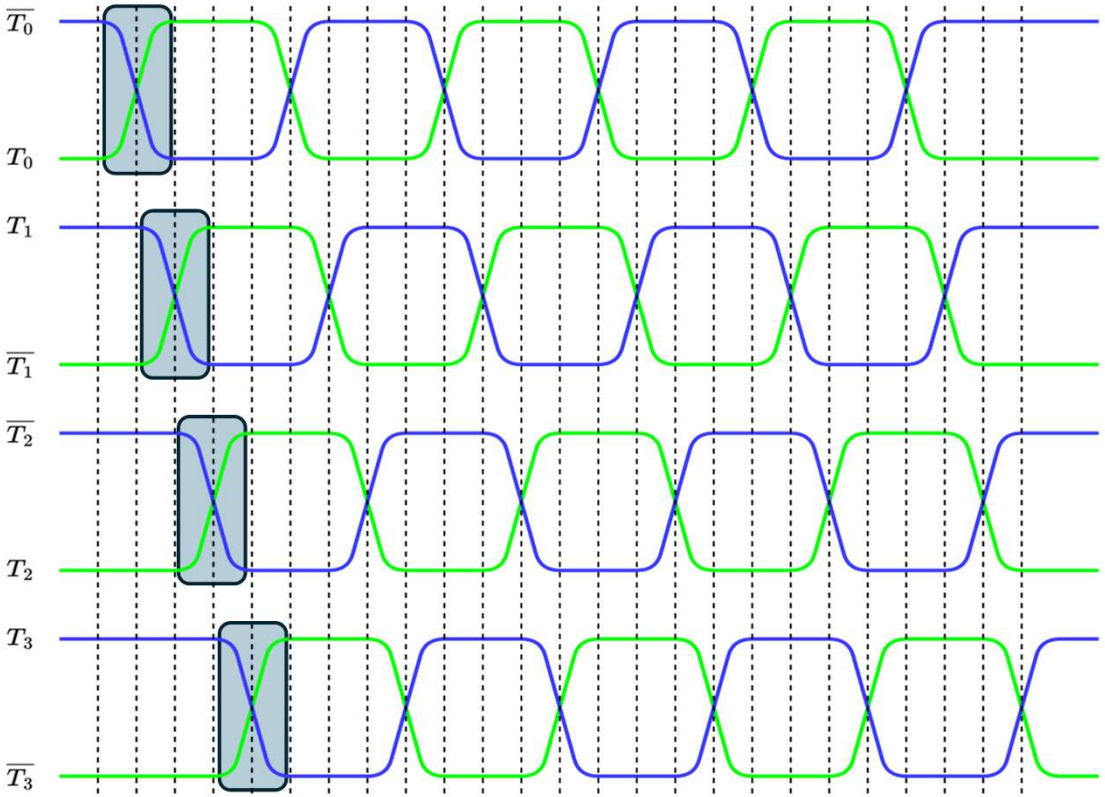




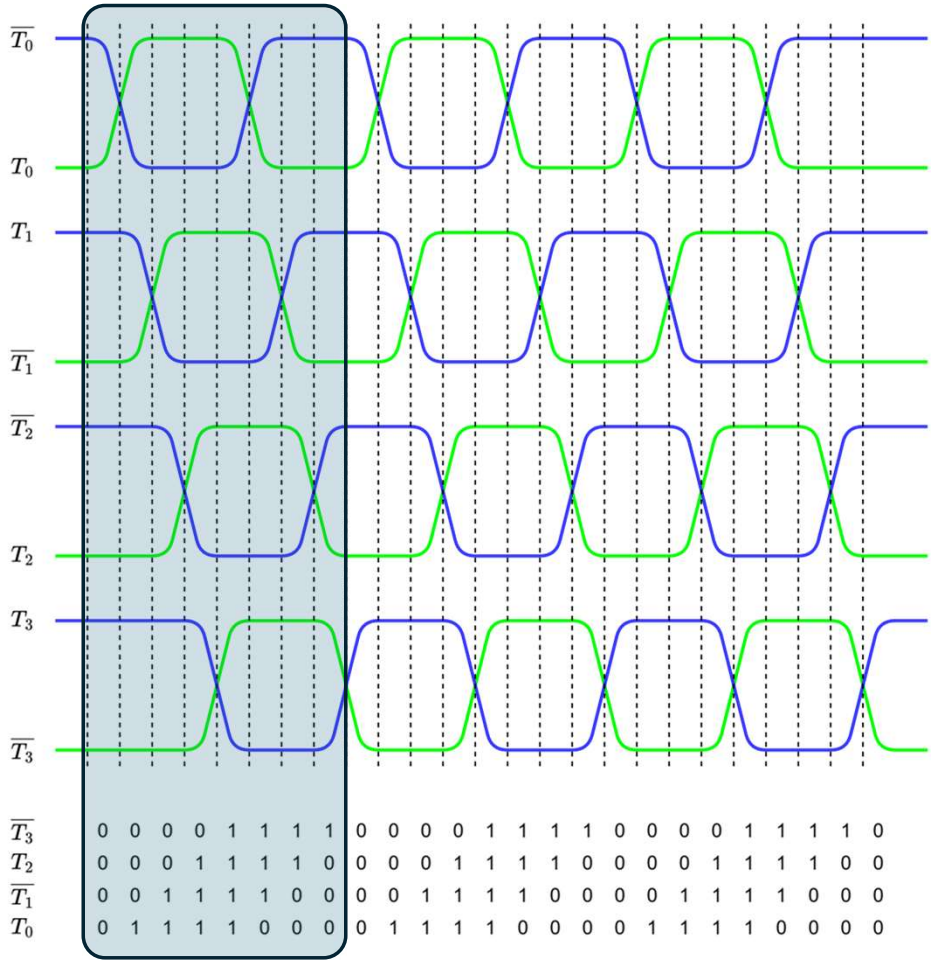




Oscillator Waveforms



Output Decoding

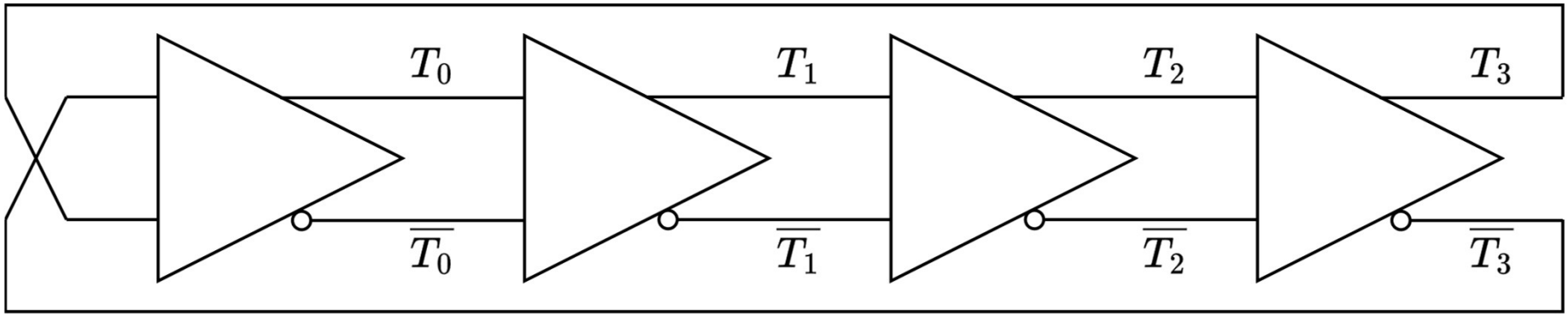


$$LSB: \frac{1}{8} th\ period$$

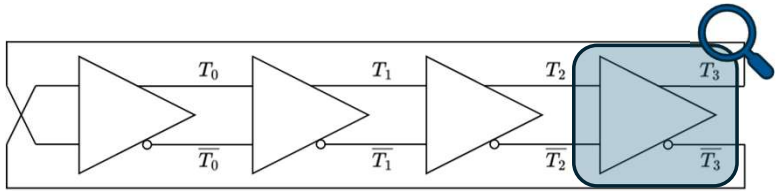
Johnson Encoding

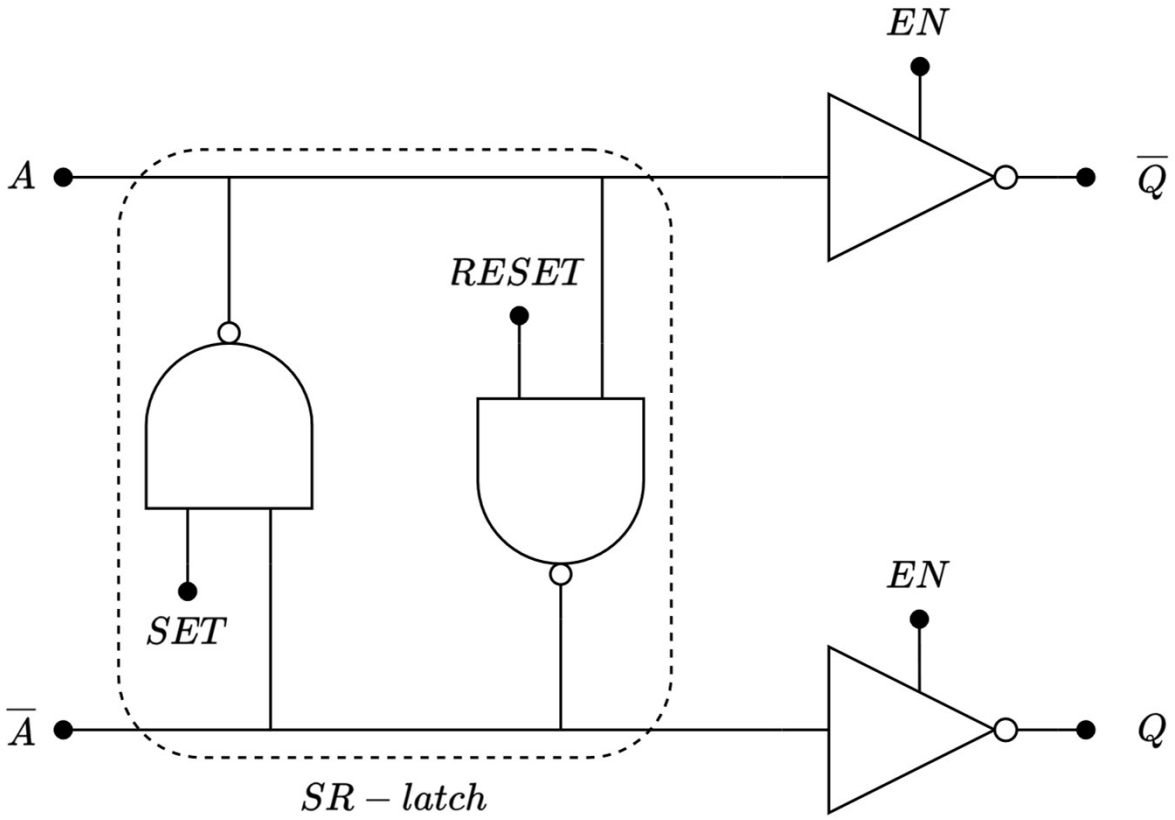
$\overline{T_3}T_2\overline{T_1}T_0$	Binary Code
0000	000
0001	001
0011	010
0111	011
1111	100
1110	101
1100	110
1000	111

Pseudo-Differential Ring Oscillator

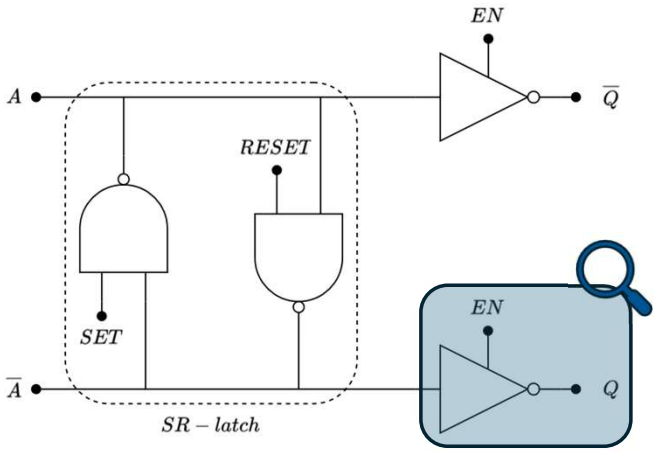


Oscillator Pseudo-Differential Cell

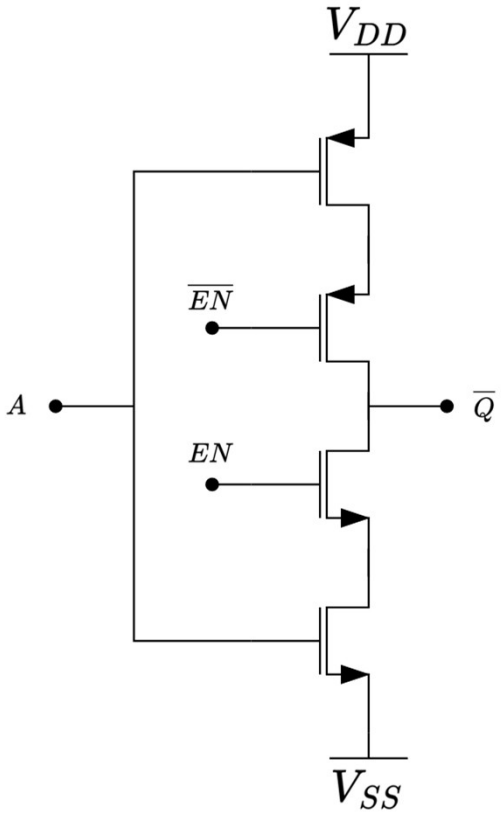




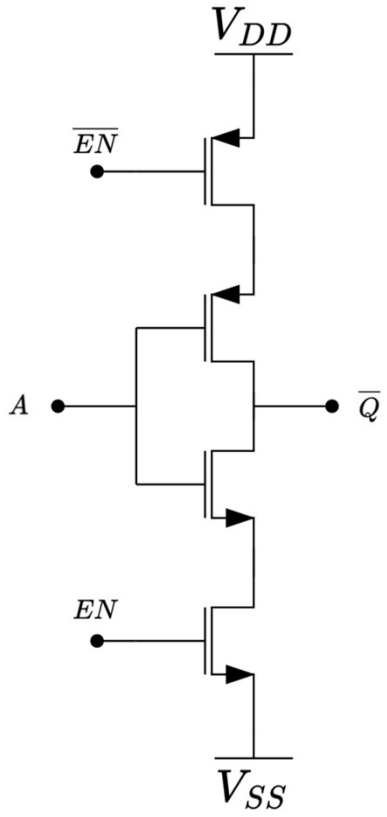
Tri-state Inverter



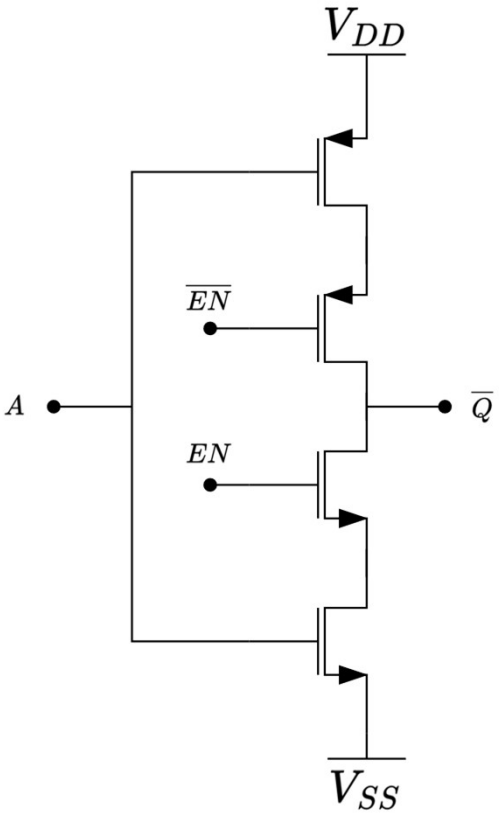
Conventional

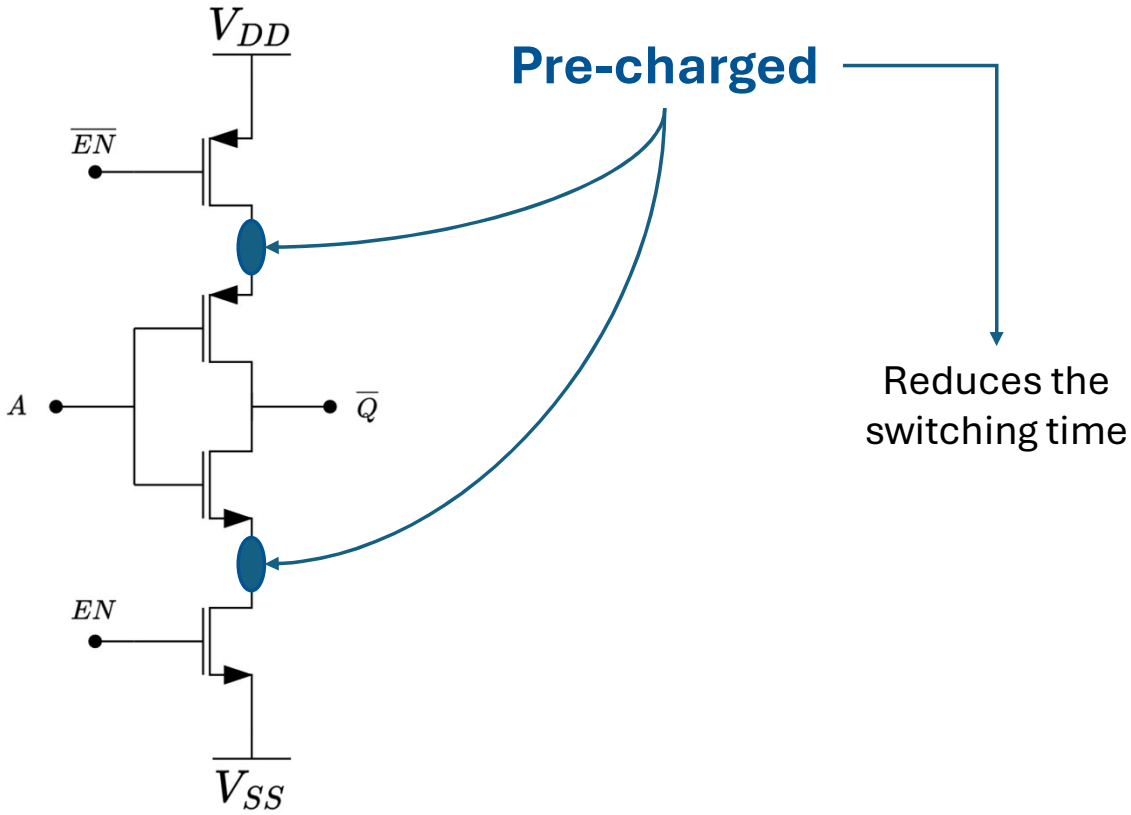


Modified

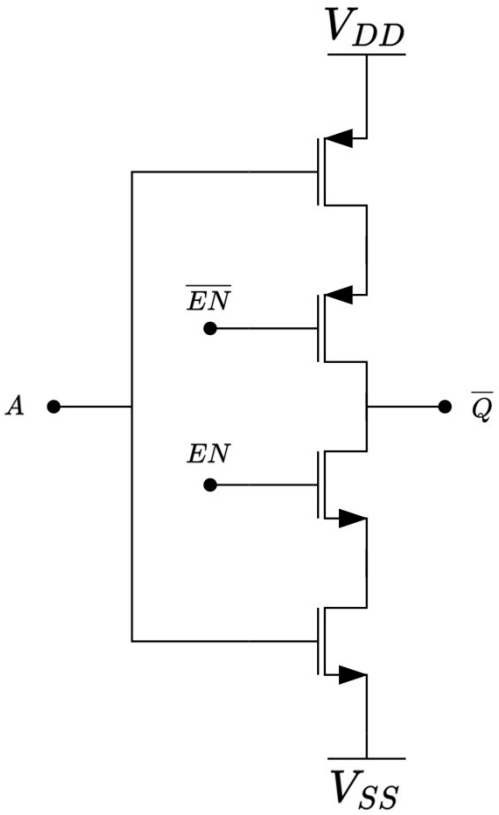


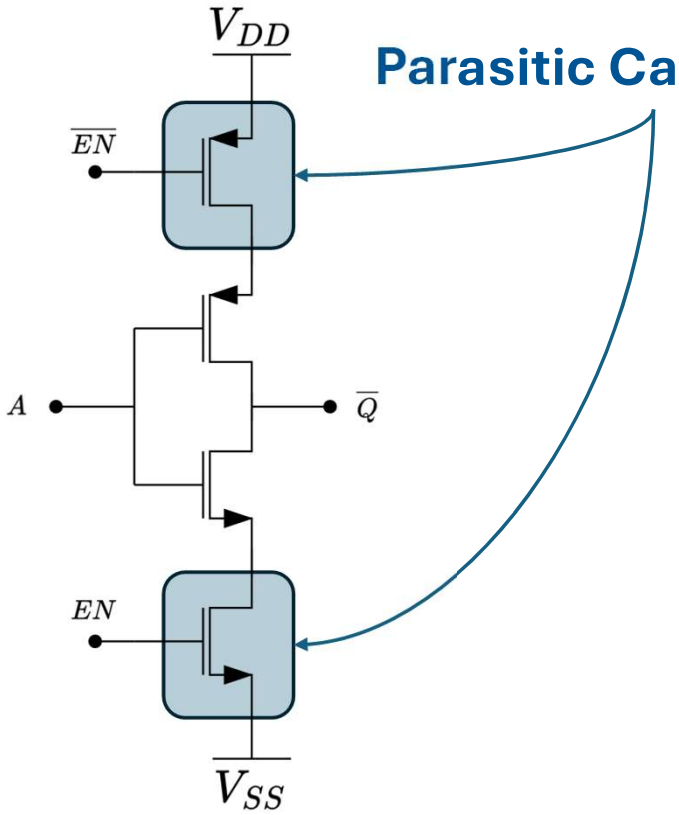
Modified Tri-state Inverter





Modified Tri-state Inverter

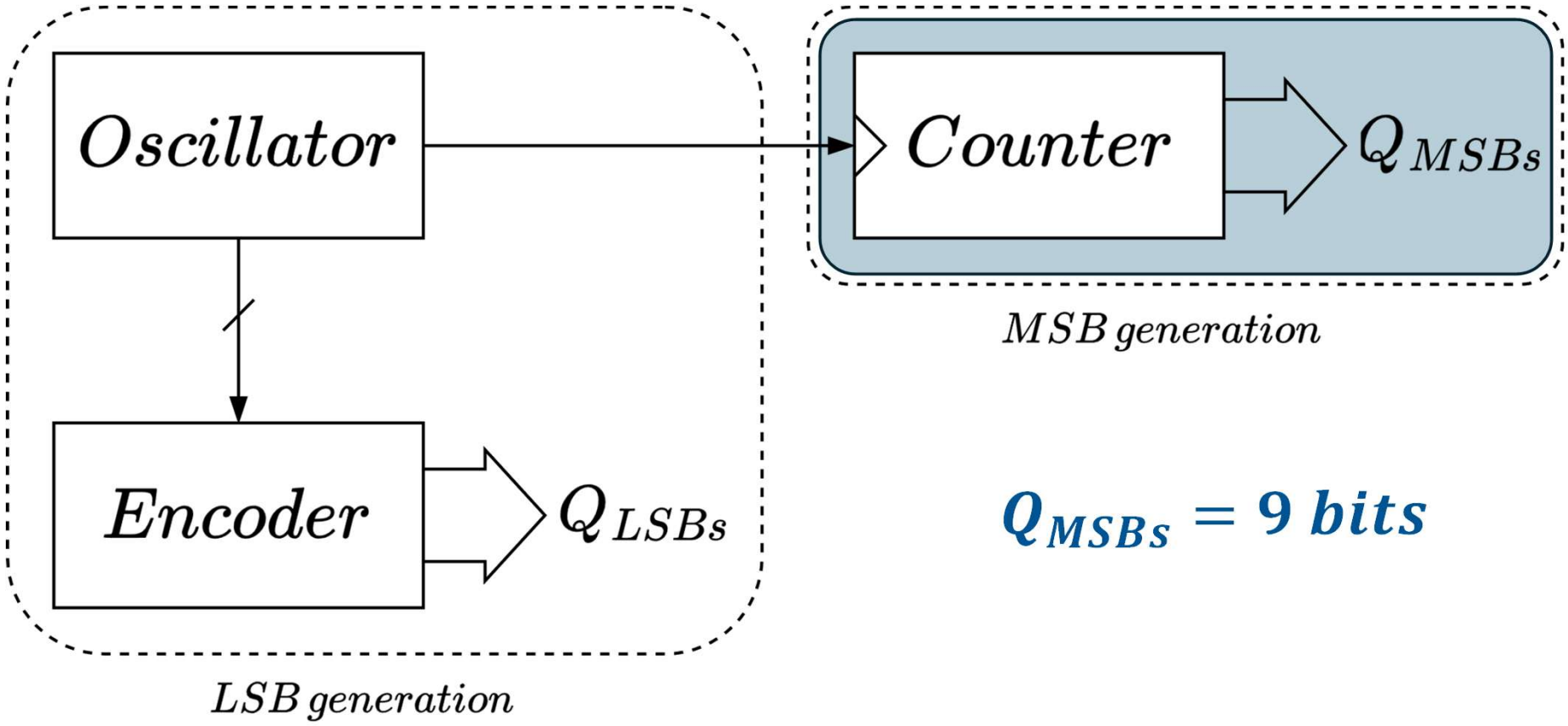




Parasitic Capacitance

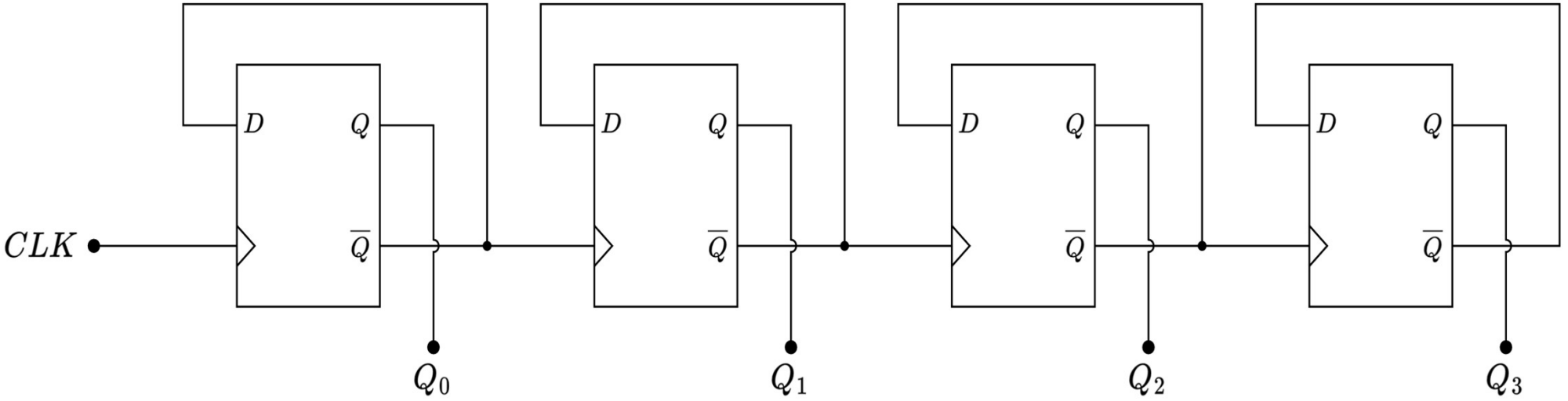
Mitigate the disturbances from the power supply

MSBs Generation



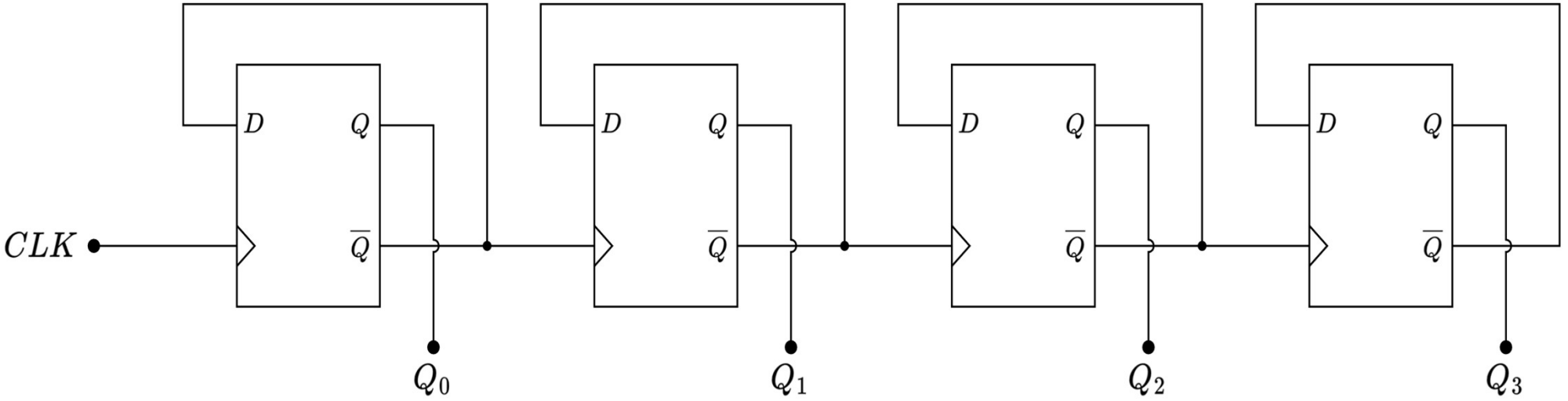
$$Q_{MSBs} = 9\ bits$$

Asynchronous Ripple Counter



$$T_{min} = t_{ckq} + t_{su} \qquad f_{max} = \frac{1}{T_{min}}$$

Asynchronous Ripple Counter (9 bits)



$$T_{min} = t_{ckq} + t_{su} \qquad f_{max} = \frac{1}{T_{min}} \qquad T_d = 9t_{ckq}$$

Outline

Time-to-Digital Converter (TDC)

Architecture: Interpolation based TDC

Resolution Control System

Simulation Results

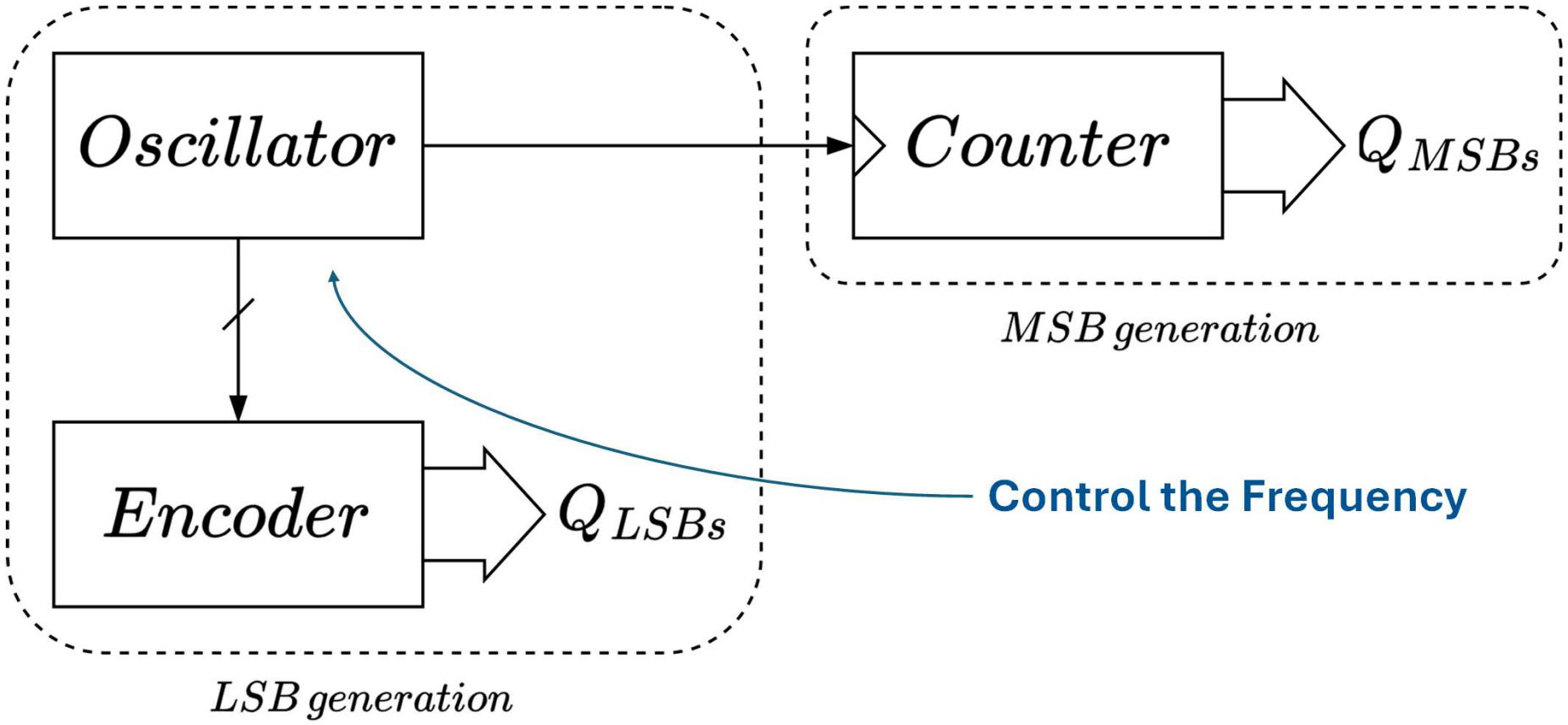
digital Silicon Photo Multiplier (dSiPM)

Synthesizable dSiPM: Recursive structure

Tools: Xcelium, Genus and Innovus

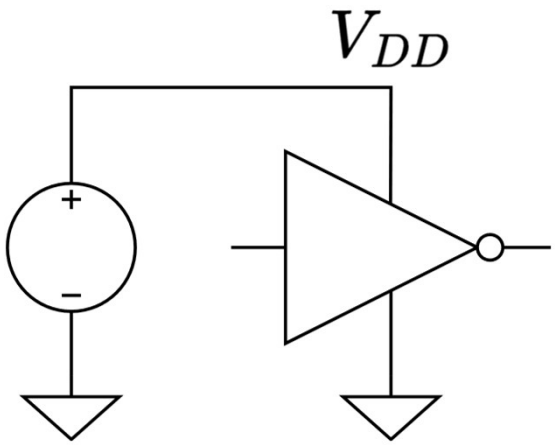
Preliminary Results

Resolution Control System

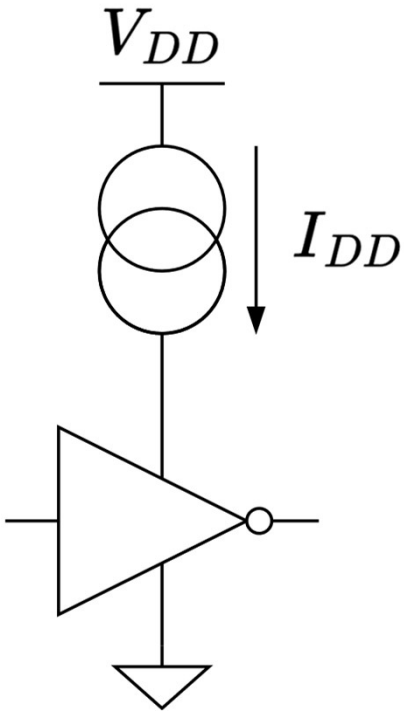


Resolution Control System

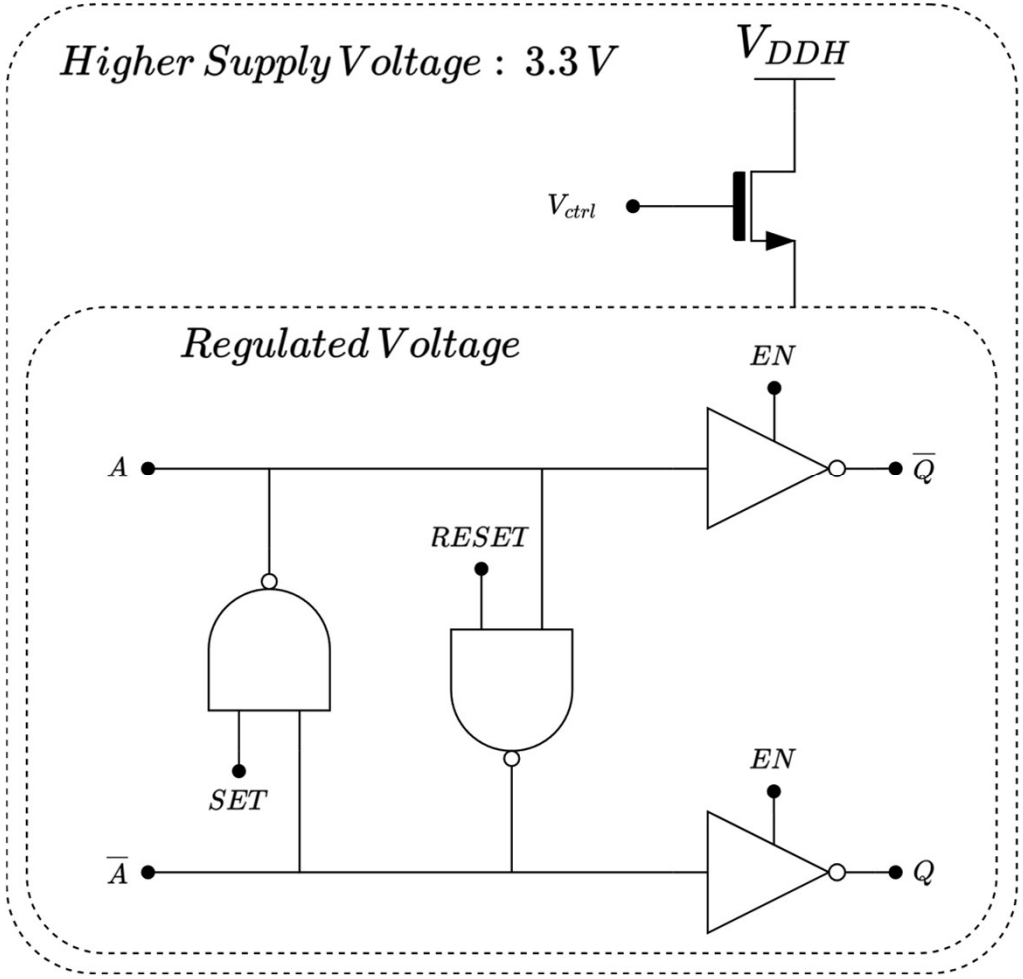
Voltage Control



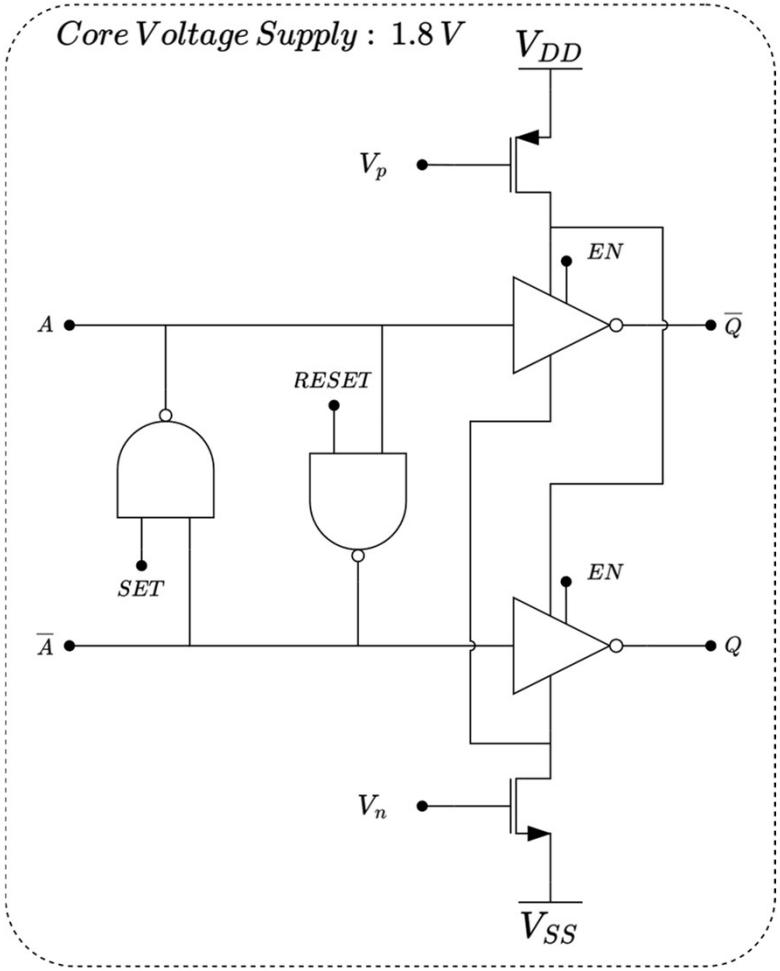
Current Control



Voltage Control System

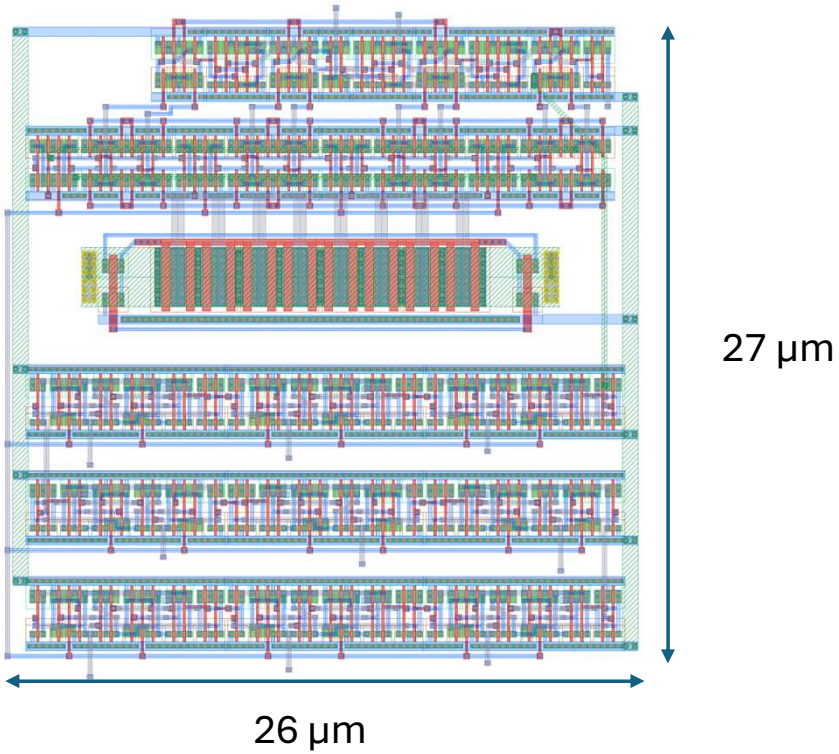


Current Control System

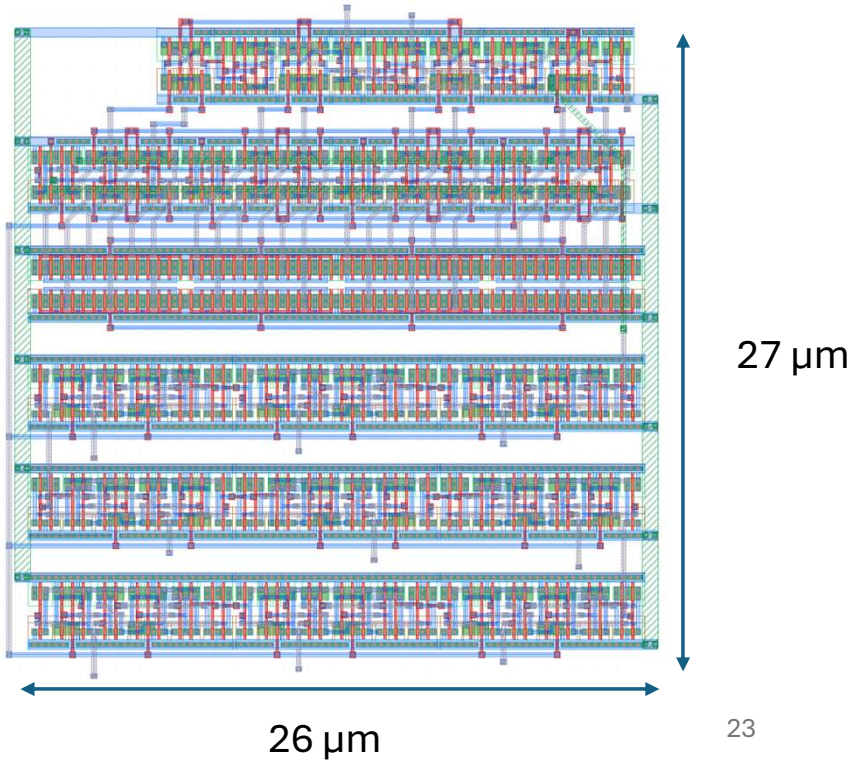


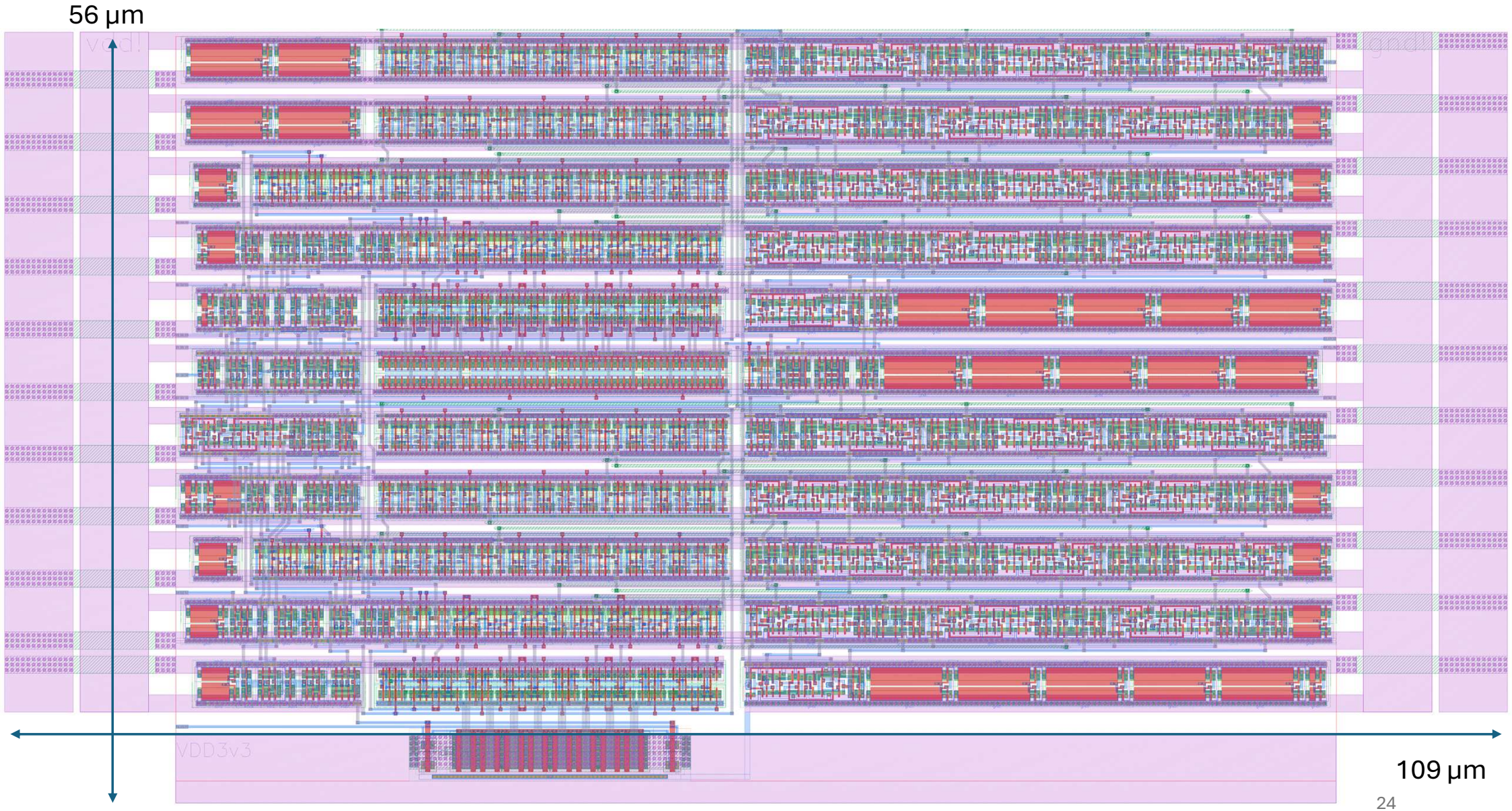
Layout

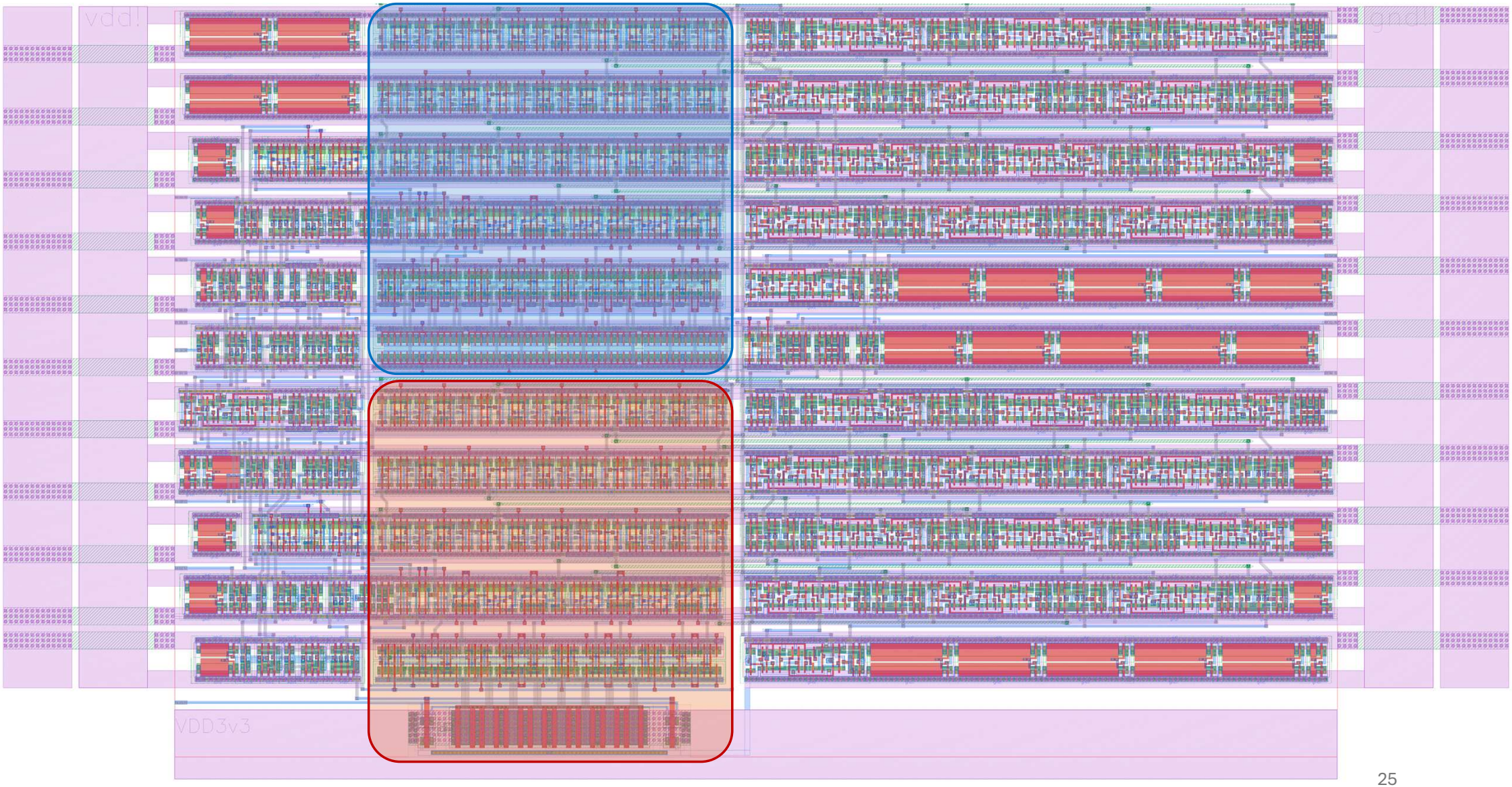
Voltage Control

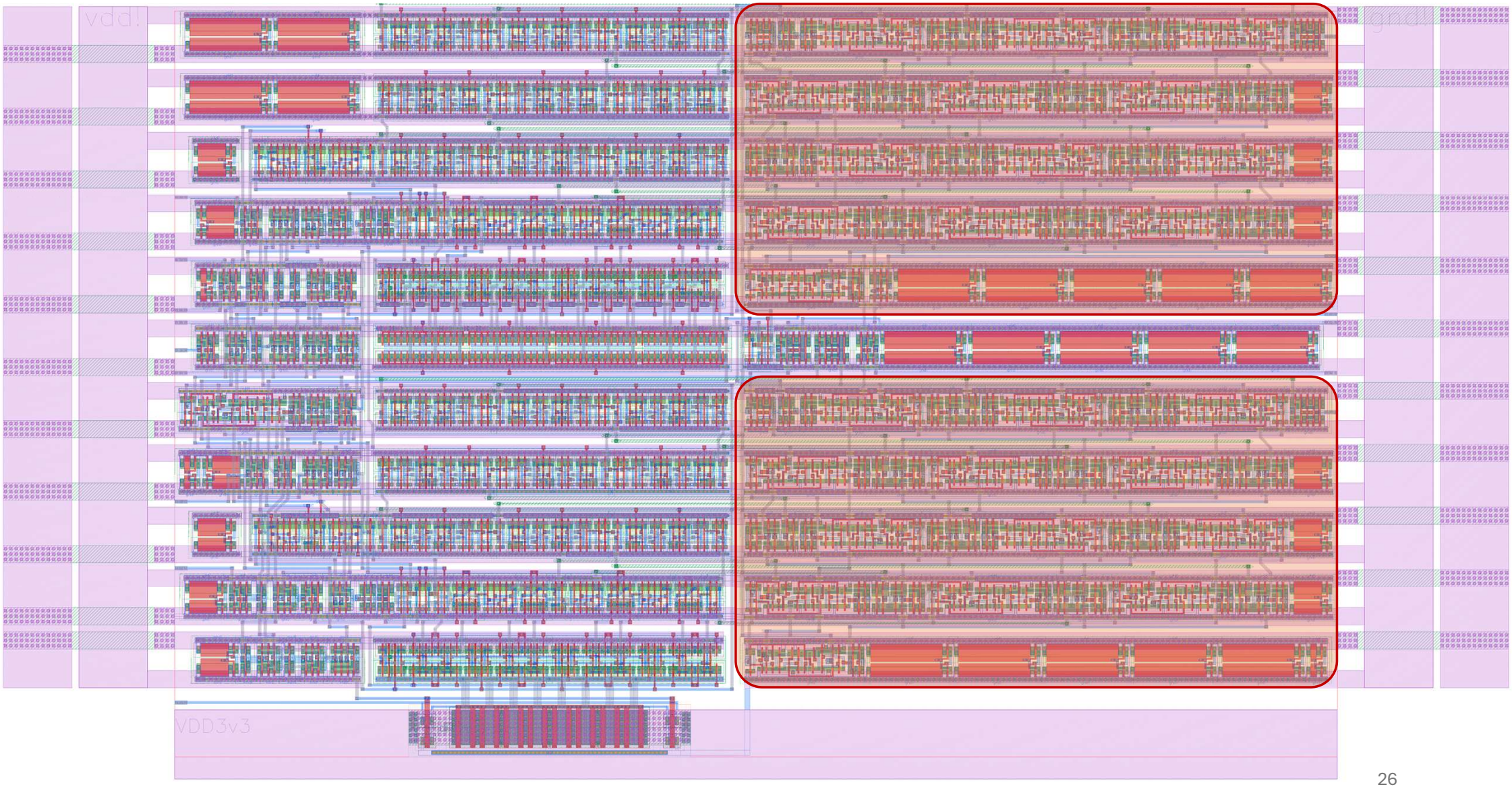


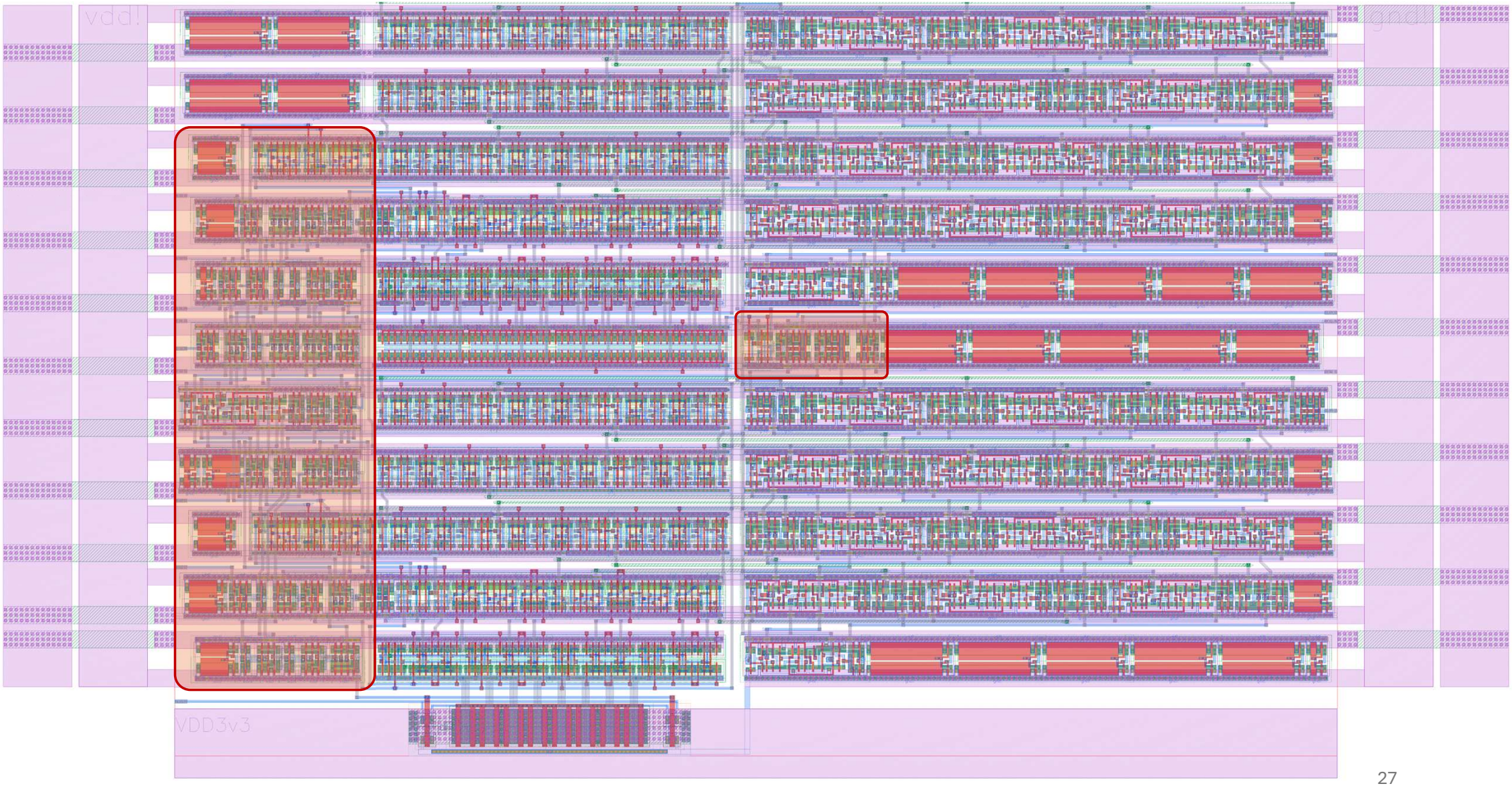
Current Control




56 µm
VDD3v3
109 µm


vdd!
VDD3v3


vdd!
VDD3v3


vdd!
VDD3v3

Outline

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Architecture: Interpolation based TDC

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Simulation Results

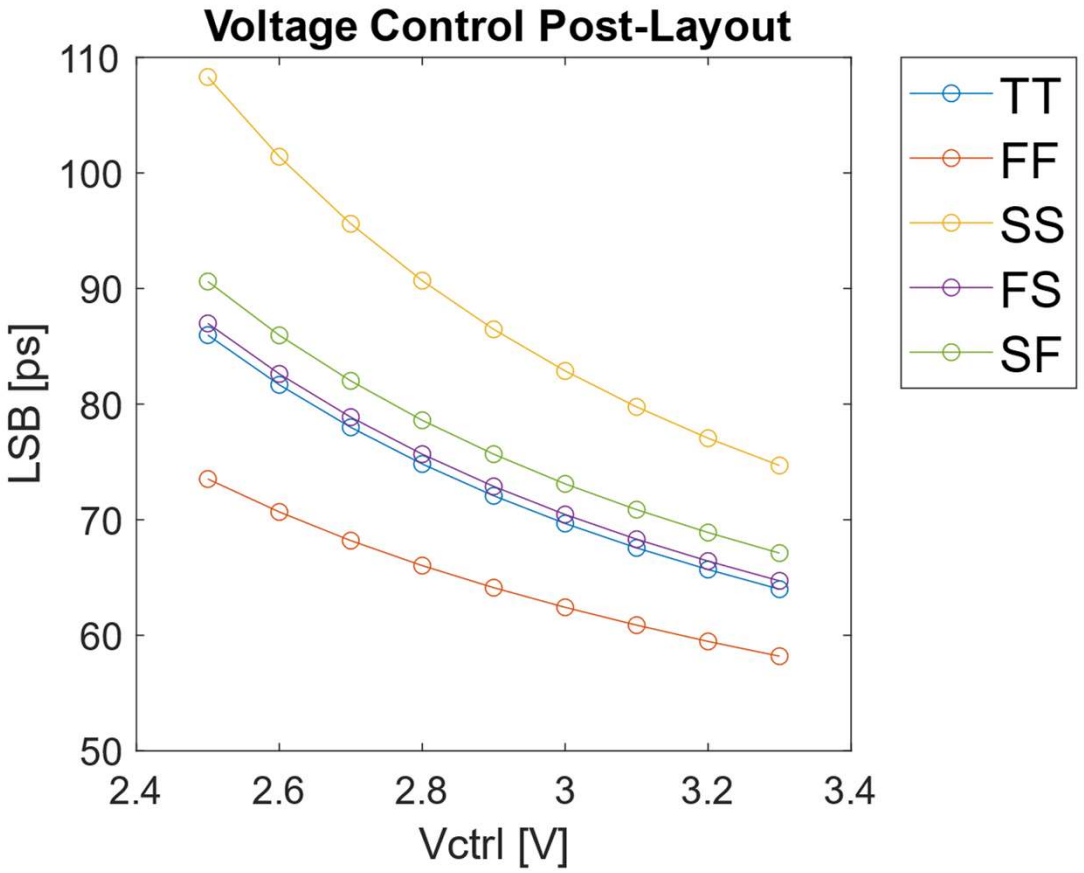
digital Silicon Photo Multiplier (dSiPM)

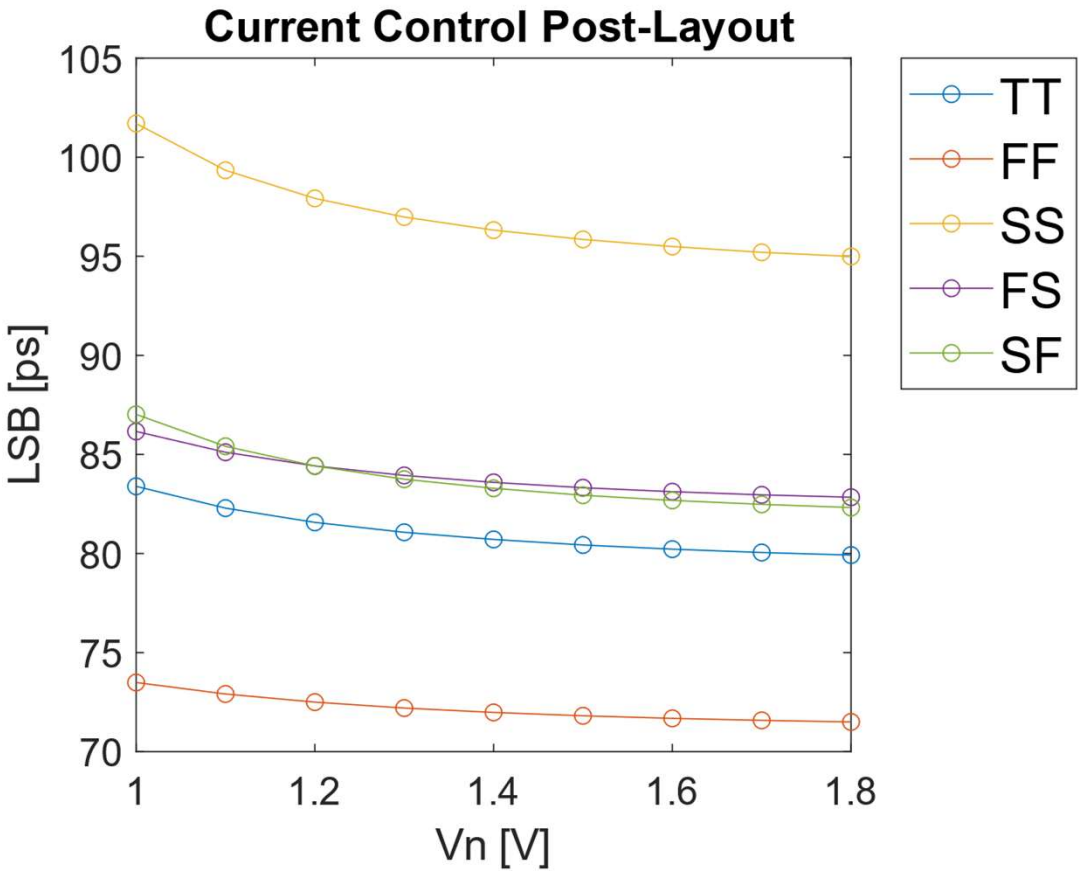
Synthesizable dSiPM: Recursive structure

Tools: Xcelium, Genus and Innovus

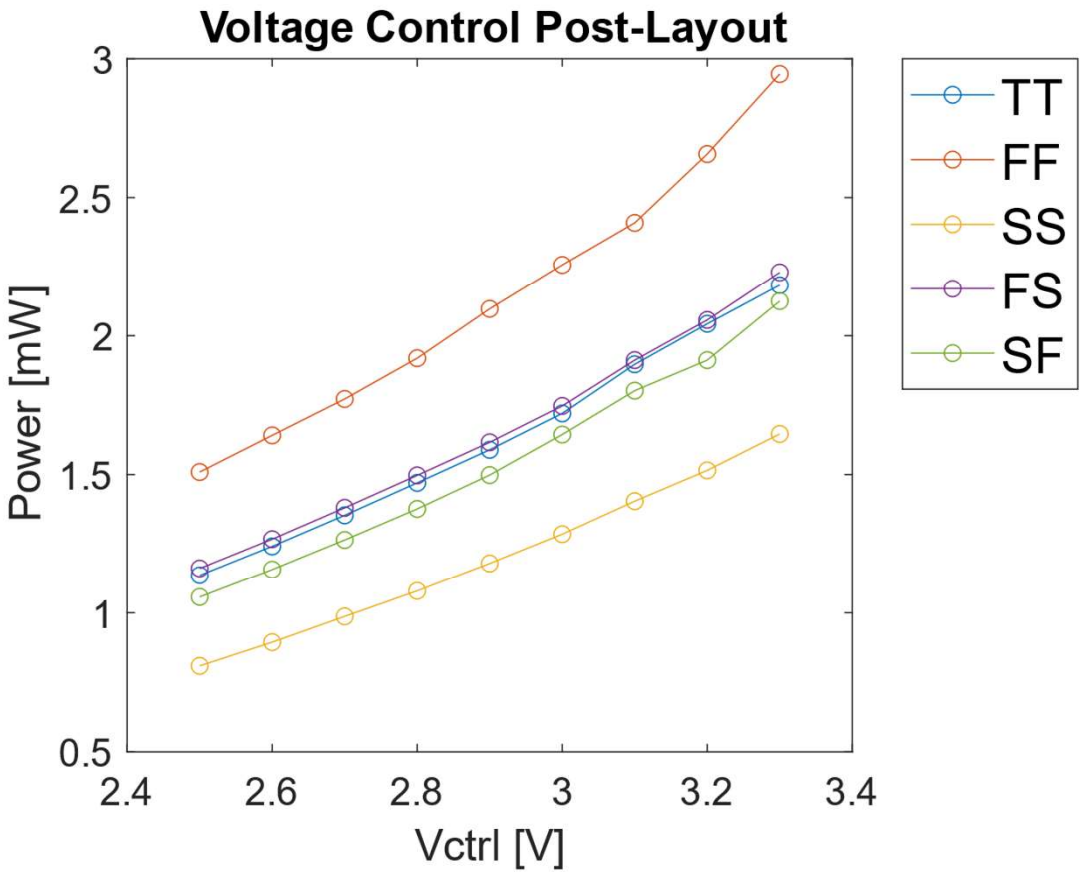
Preliminary Results

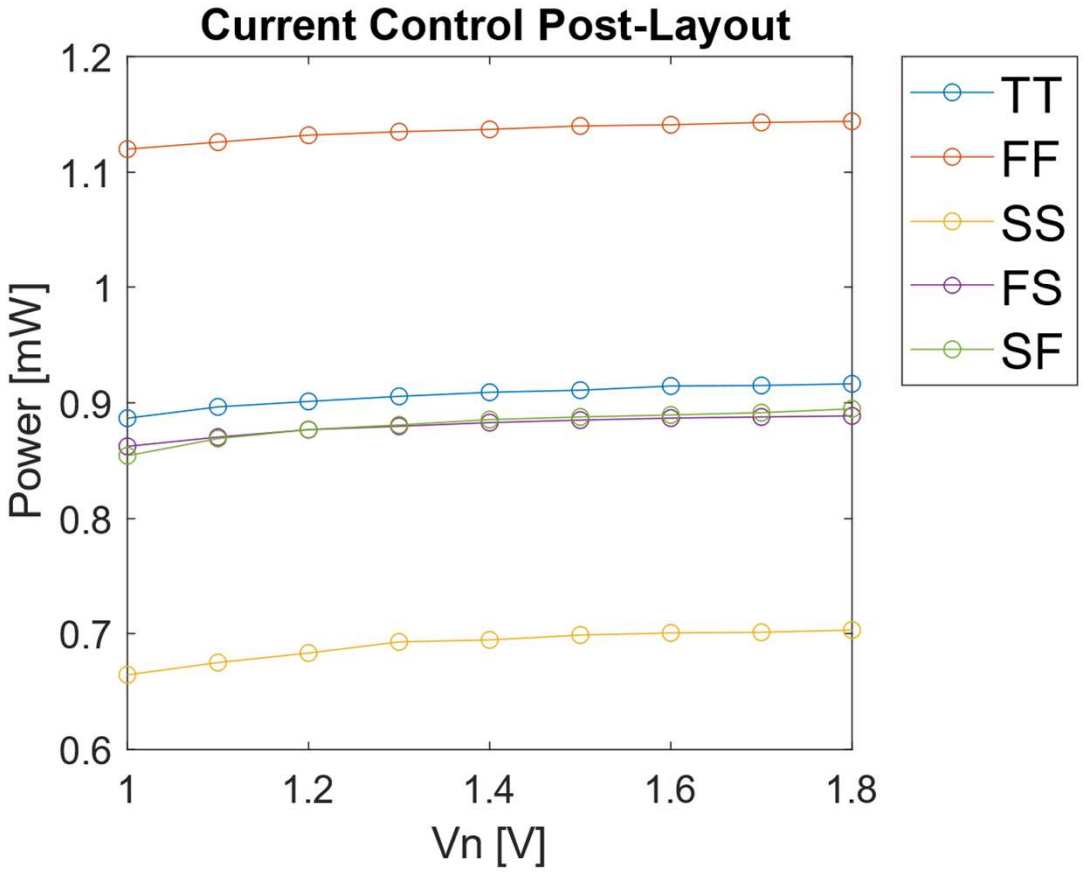
Results: LSB


Voltage Control Post-Layout
LSB [ps]
Vctrl [V]
110
100
90
80
70
60
50
2.4
2.6
2.8
3
3.2
3.4
TT
FF
SS
FS
SF

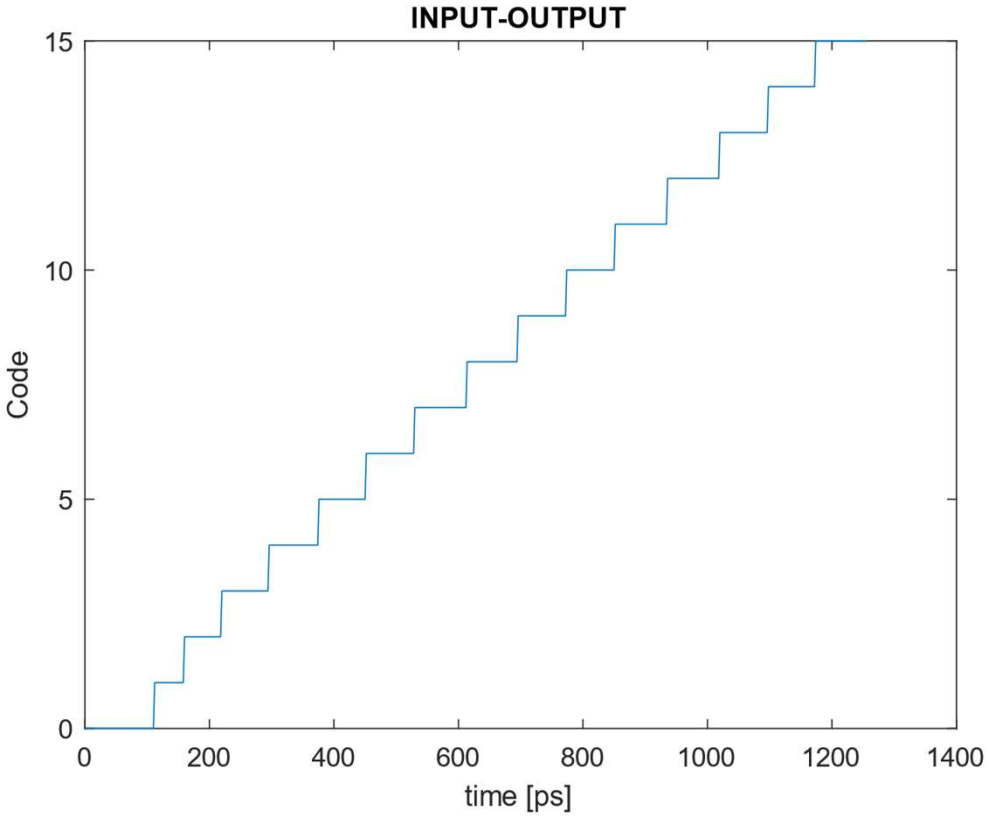

Current Control Post-Layout
LSB [ps]
Vn [V]
105
100
95
90
85
80
75
70
1
1.2
1.4
1.6
1.8
TT
FF
SS
FS
SF

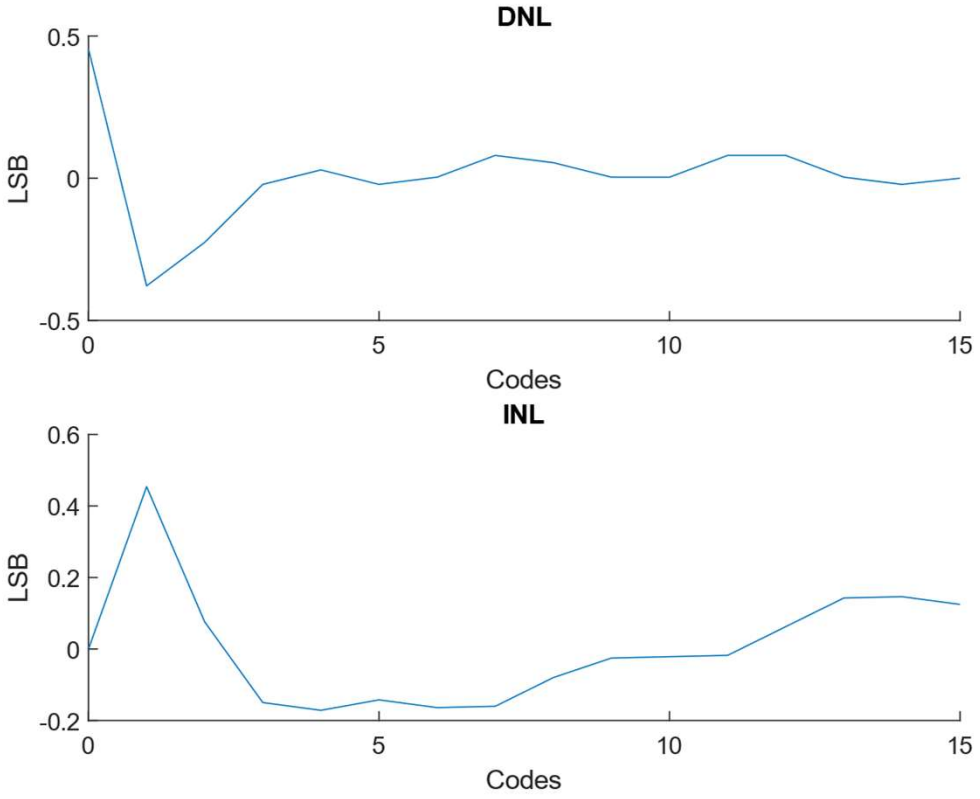
Results: Power



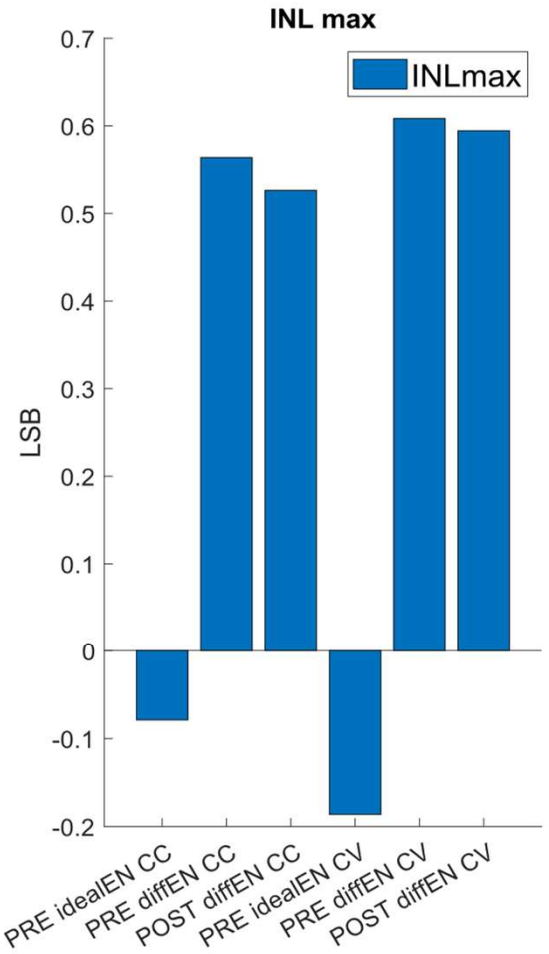


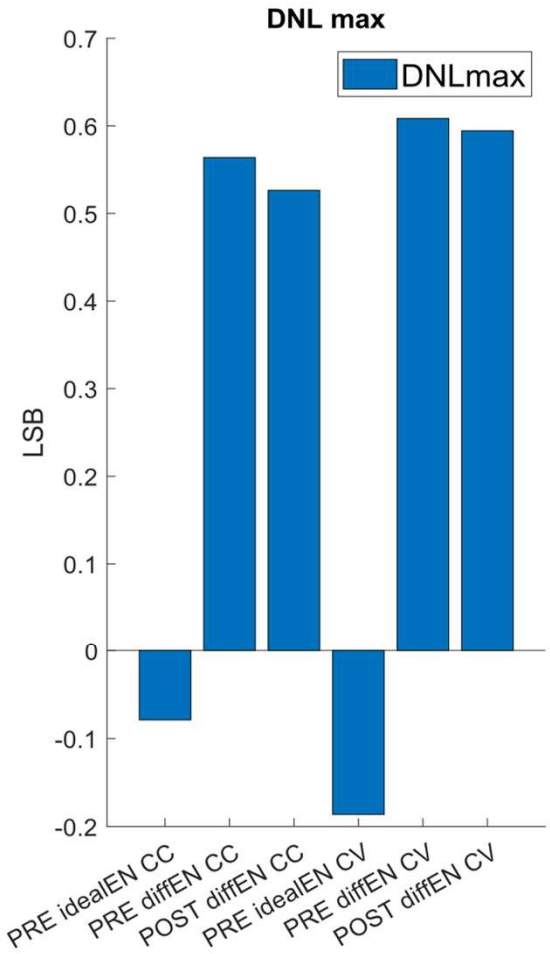
Results: DNL & INL



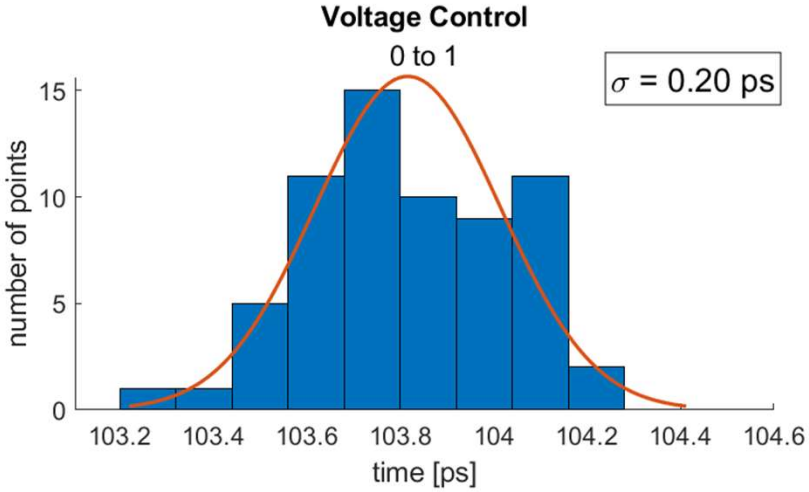


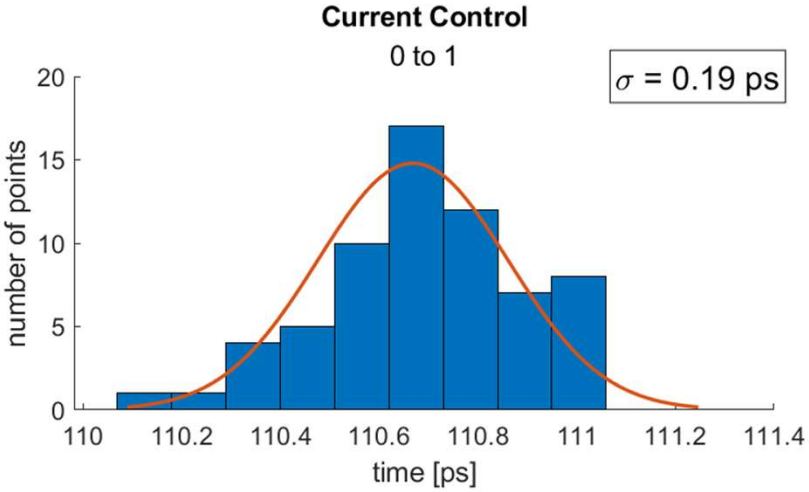
Results: DNL & INL

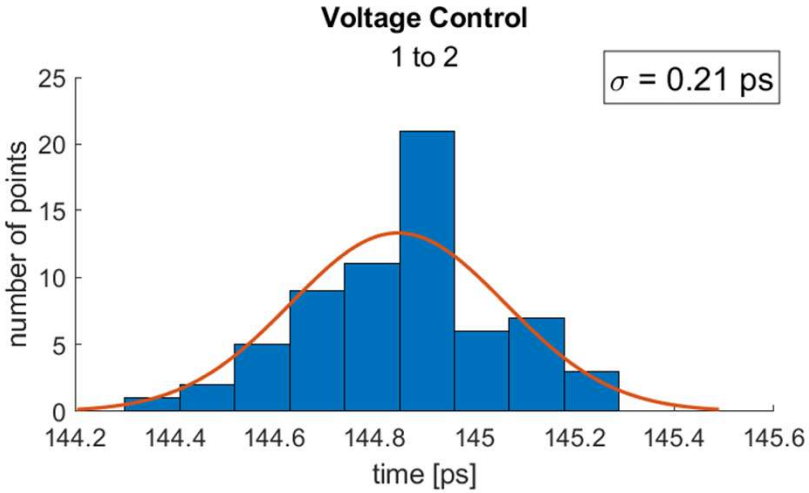


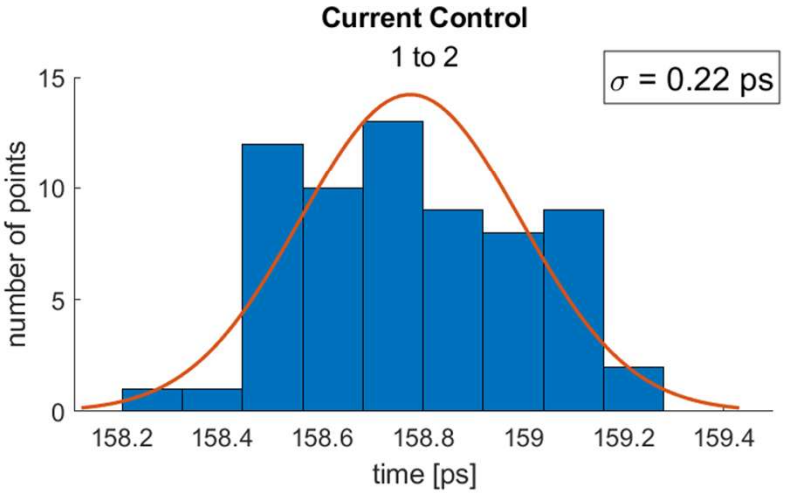


Results: Jitter









Results Summary

	Voltage Control	Current Control
LSB	72.07 ps	80.71 ps
FSR	295.13 ns	330.5 ns
Power	1.589 mW	0.9091 mW

Nominal Condition:

- TT corner
- $V_n = 1{,}4\ V$ $V_p = 0{,}4\ V$ $V_{ctrl} = 2{,}9\ V$

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PhD project of

Tommaso Maria Floris

UNIVERSITÀ
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Supervisor: Prof. Lodovico Ratti

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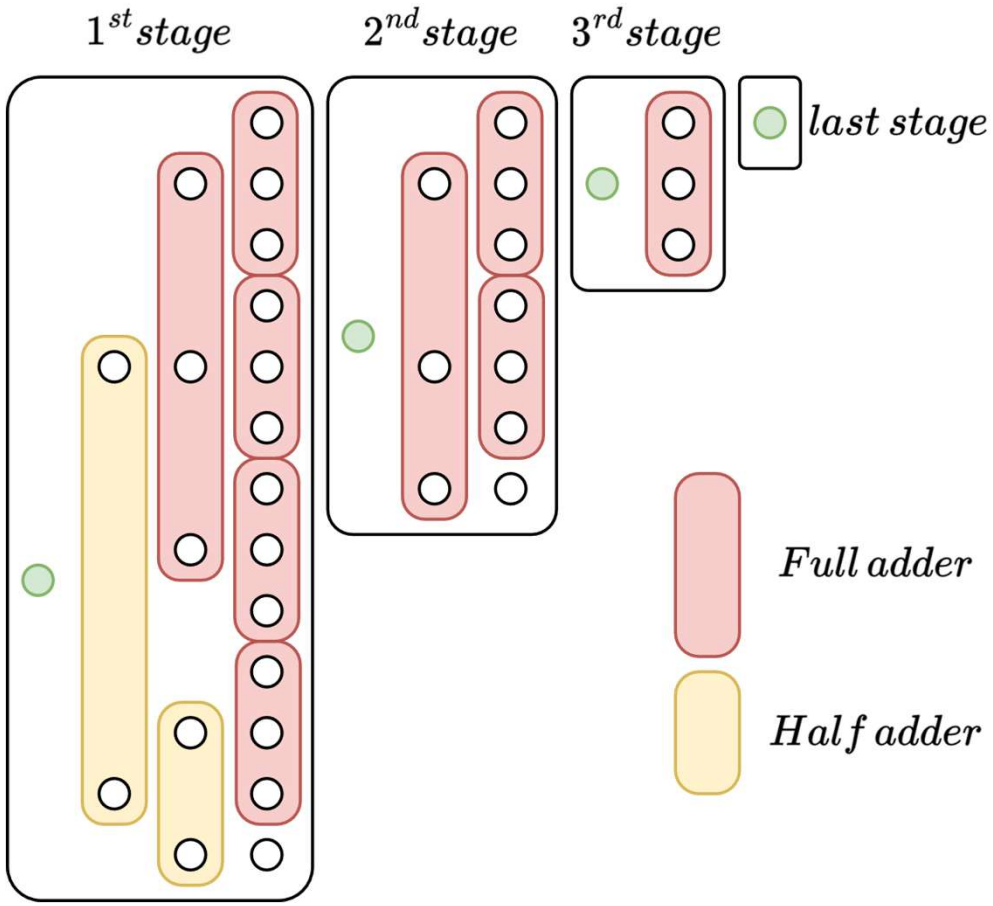
Recursive Structure



- Basic building block: **compressor**
- Each stage is built with the same procedure
- The input of the **first stage** is the binary vector coming from the array
- The input of the following stage is the total **carry vector** of the previous one

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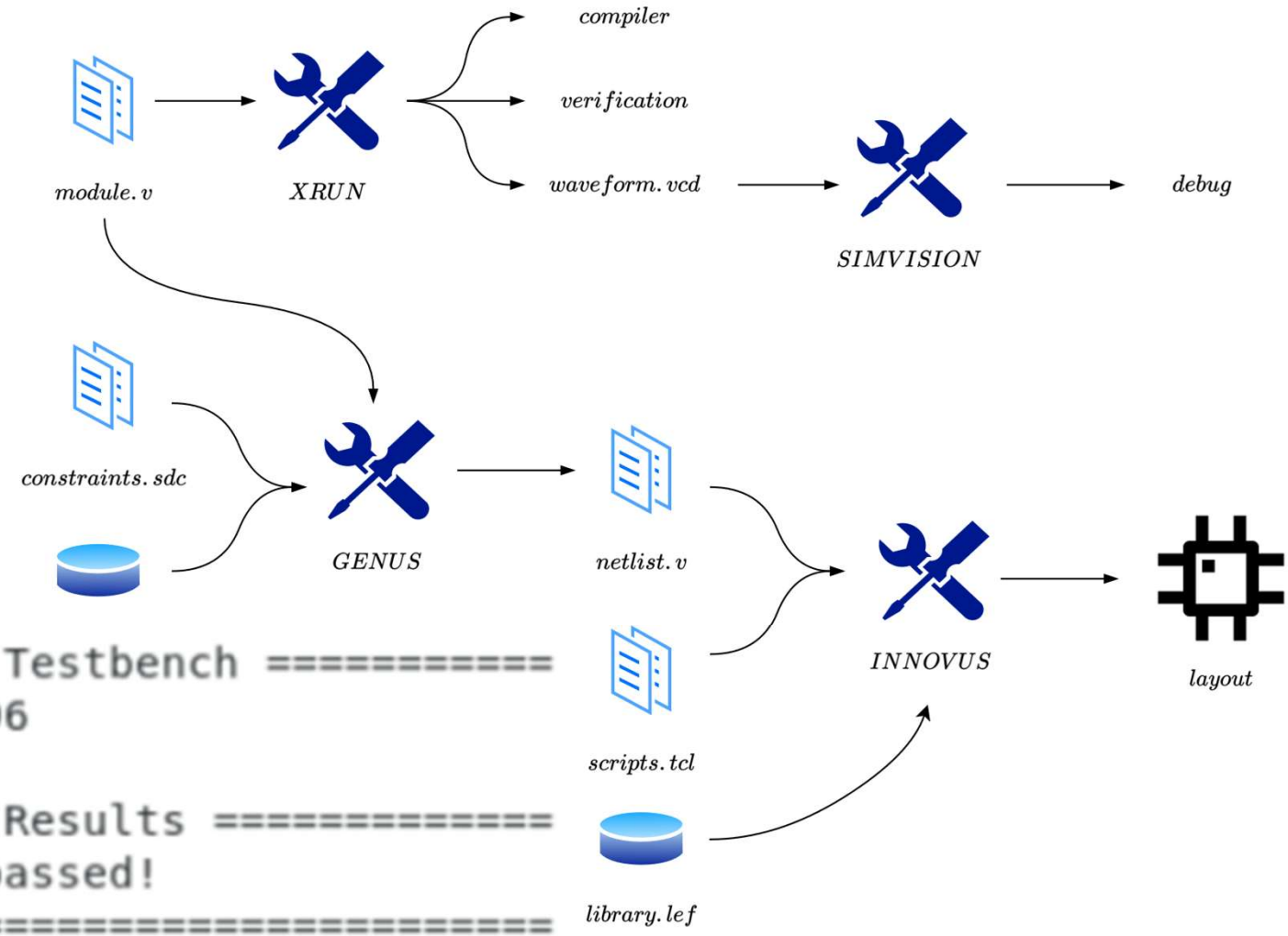
digital Silicon Photo Multiplier (dSiPM)

Synthesizable dSiPM: Recursive structure

Tools: Xcelium, Genus and Innovus

Preliminary Results

Digital synthesis flow




```
========== dSiPM Testbench ==========
INPUT_WIDTH  : 4096
OUTPUT_WIDTH : 13
============ Test Results ============
All 2^4096 tests passed!
======================================
```

Outline

Time-to-Digital Converter (TDC)

Architecture: Interpolation based TDC

Resolution Control System

Simulation Results

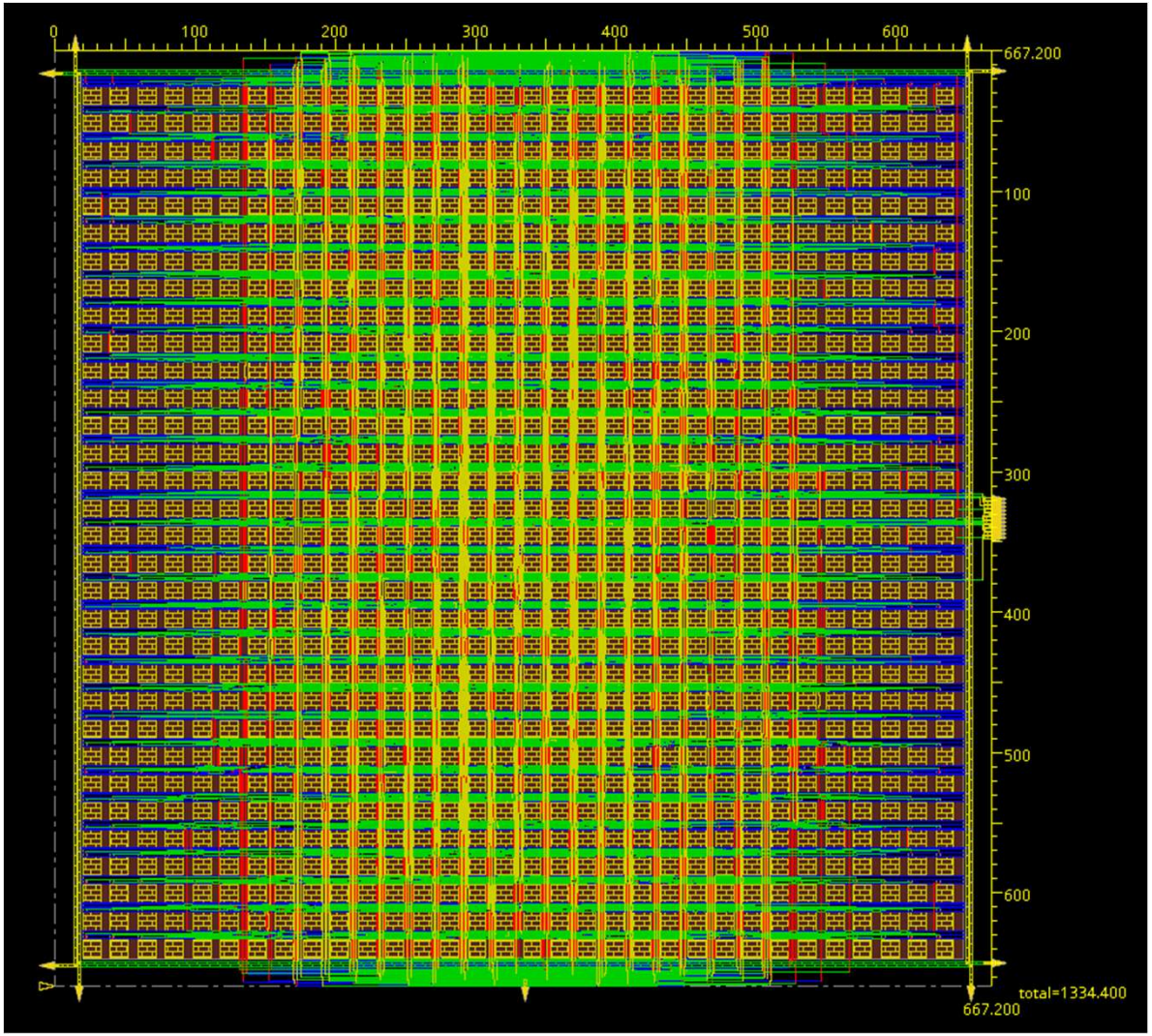
digital Silicon Photo Multiplier (dSiPM)

Synthesizable dSiPM: Recursive structure

Tools: Xcelium, Genus and Innovus

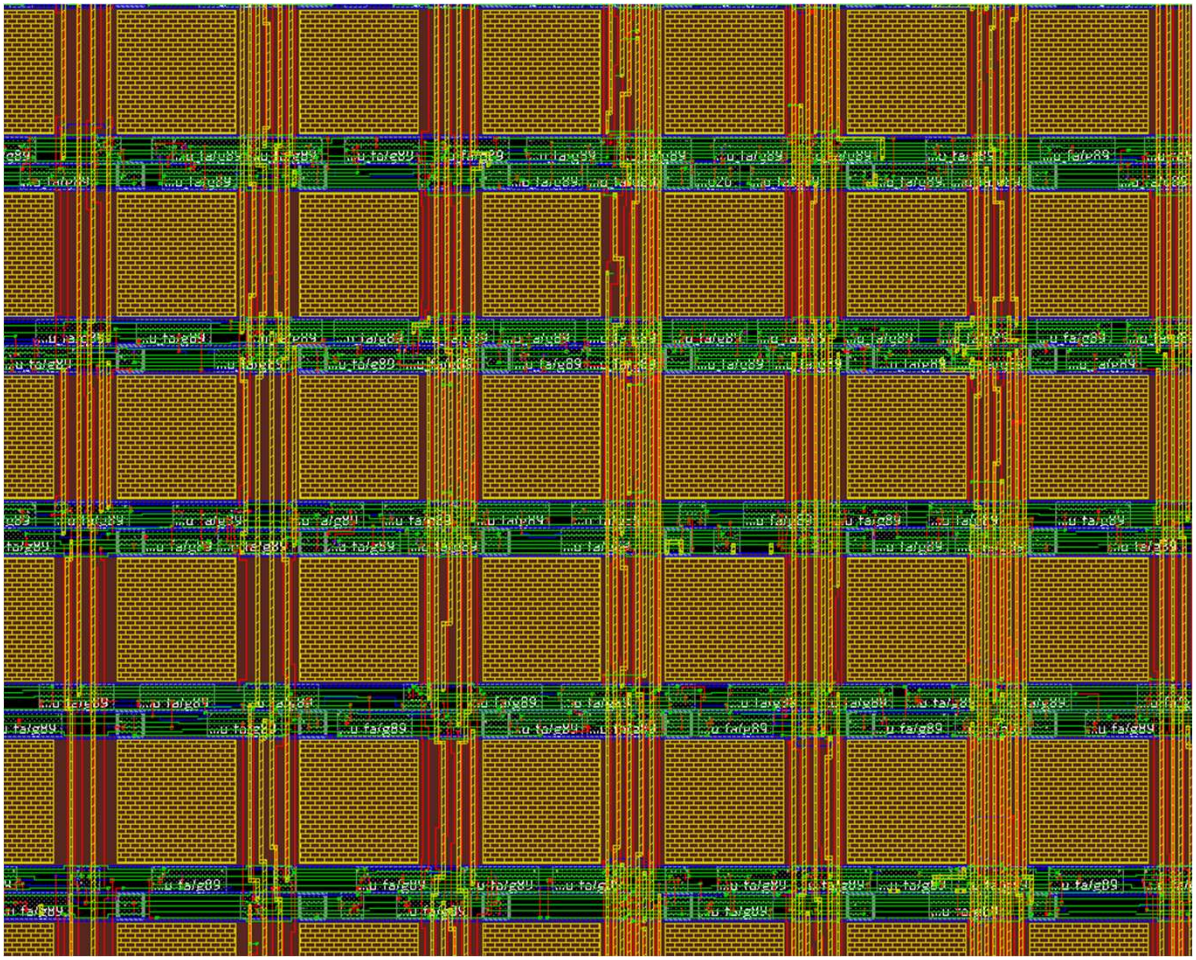
Preliminary Results

32x32 matrix



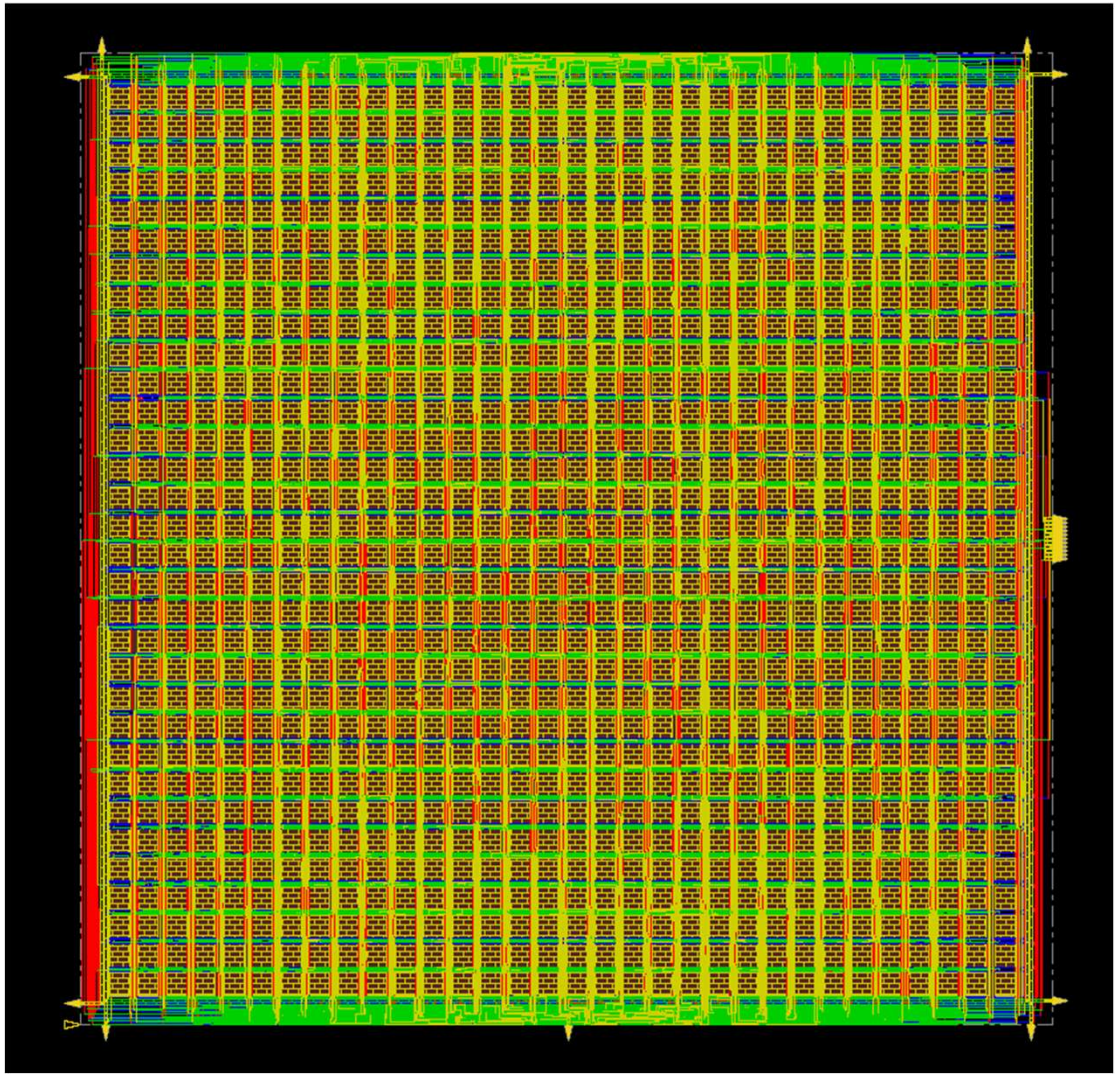
- Matrix shape obtained with a script
- The parameters are:
  - Rows & columns number
  - Width & height of each cell
  - Number of stdCell rows allocated for the digital logic
  - The percentage of the cell area left available for routing

32x32 matrix

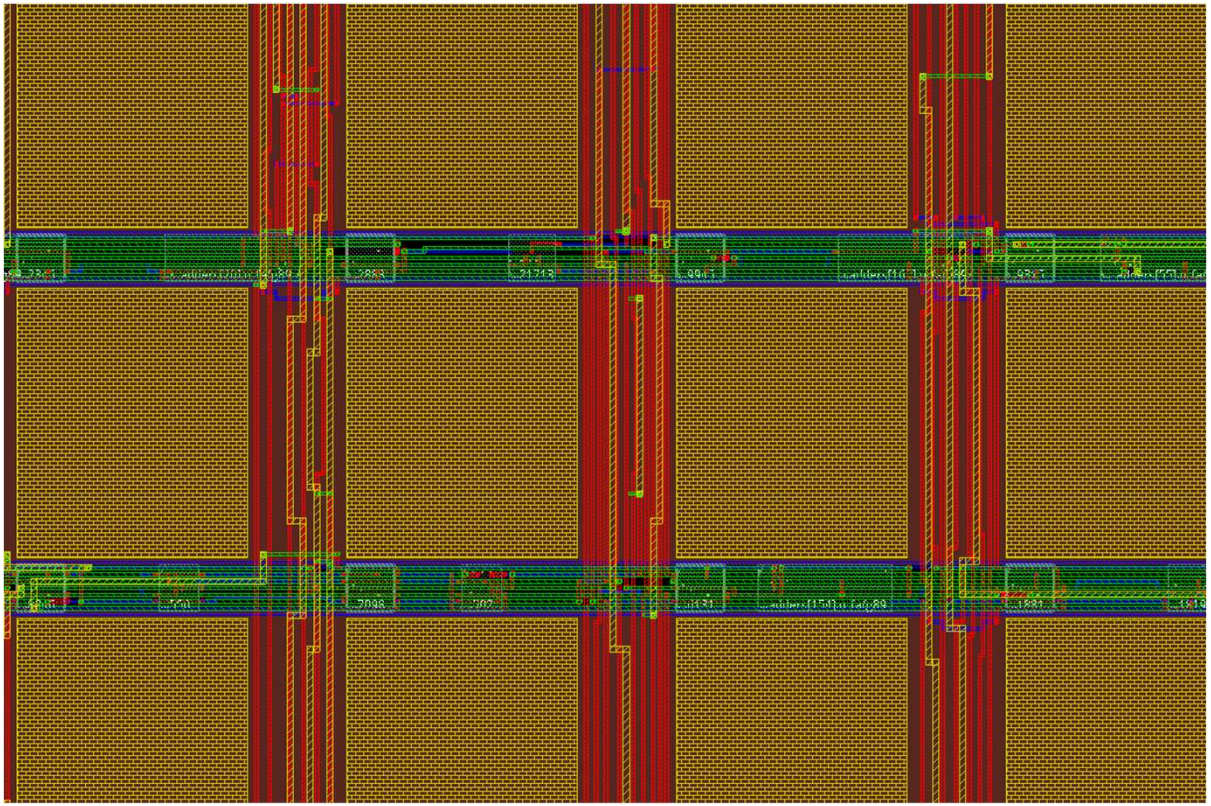
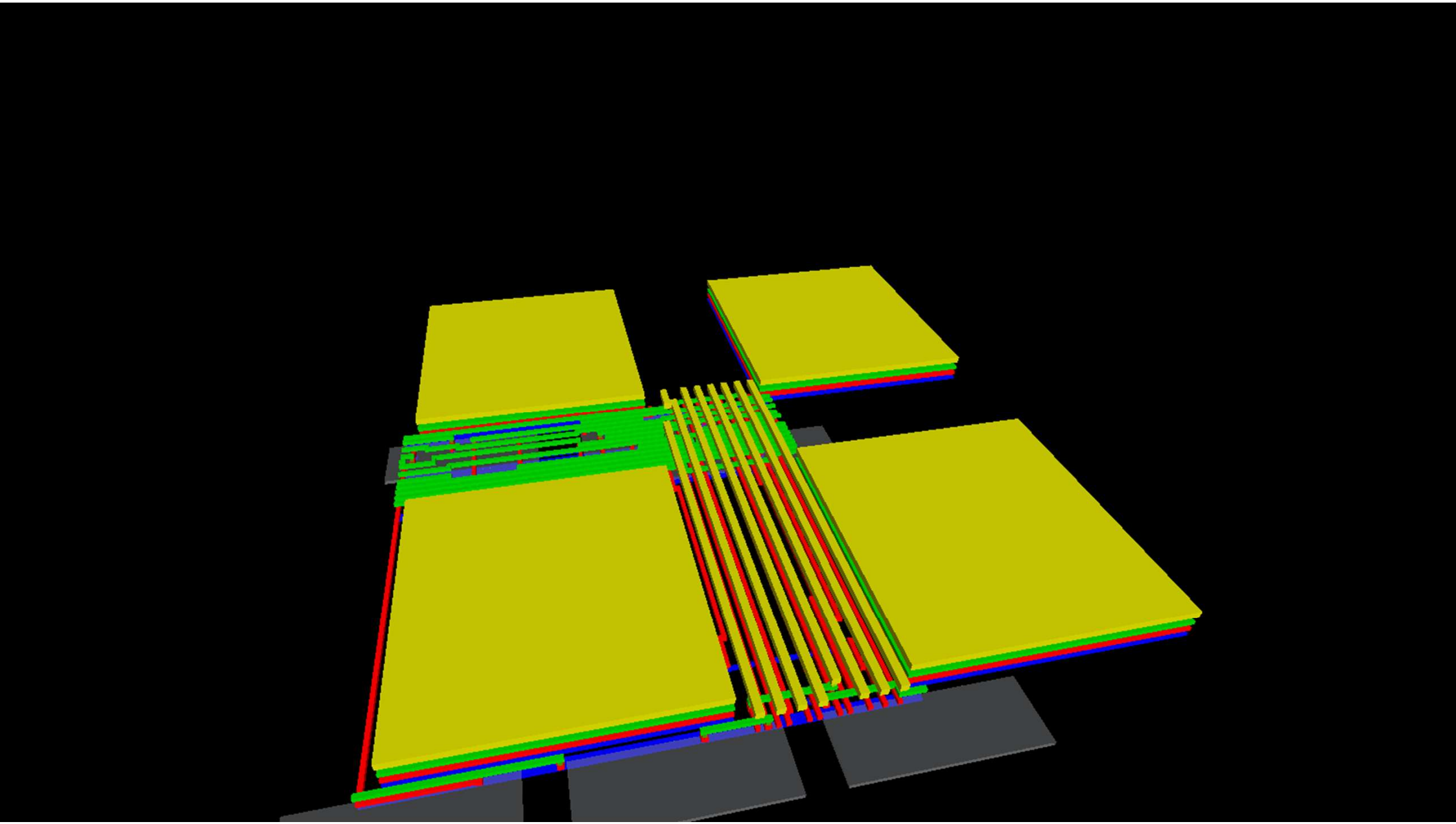


- Cell width & height : 19,6 µm
- Free stdCell row : 2*2,8 = 5,6 µm
- Routing : 0,4*19,6 = 7,84 µm
- Sensor area : 164,64 µm^2
- 42% of the total cell area

32x32 matrix



32x32 matrix



- Cell width & height : 19,6 µm
- Free stdCell row : 1*2,8 = 2,8 µm
- Routing : 0,3*19,6 = 5,88 µm
- Sensor area : 230,5 µm^2
- 60% of the total cell area