A sub 100-ps LSB Time-to-Digital Converter based on a Pseudo-Differential Ring Oscillator in a 110 nm CMOS Technology

Master's Degree of

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Supervisor: Prof. Lodovico Ratti

Outline

Time-to-Digital Converter (TDC) Architecture: Interpolation based TDC **Resolution Control System** Simulation Results digital Silicon Photo Multiplier (dSiPM) Synthesizable dSiPM: Recursive structure **Tools:** Xcelium, Genus and Innovus **Preliminary Results**

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Time-to-Digital Converter (TDC)

Architecture: Interpolation based TDC

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Architecture: Interpolation TDC



LSBs Generation



Oscillator Waveforms



 $\overline{T_3}$

Oscillator Waveforms





Output Decoding



$LSB: \frac{1}{8}th \ period$

Johnson Encoding

$\overline{T_3}T_2\overline{T_1}T_0$	Binary Code
0000	000
0001	001
0011	010
0111	011
1111	100
1110	101
1100	110
1000	111

Pseudo-Differential Ring Oscillator



Oscillator Pseudo-Differential Cell



Tri-state Inverter

 $A \bullet$

 $\overline{A} \bullet$

SET



Modified Tri-state Inverter



Modified Tri-state Inverter



MSBs Generation



Asynchronous Ripple Counter



$$T_{min} = t_{ckq} + t_{su}$$
 $f_{max} = \frac{1}{T_{min}}$

Asynchronous Ripple Counter (9 bits)



 $T_{min} = t_{ckq} + t_{su}$ $f_{max} = \frac{1}{T_{min}}$ $T_d = 9t_{ckq}$

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Resolution Control System



Resolution Control System

Voltage Control

Current Control





Voltage Control System



Current Control System



Layout

Voltage Control

Current Control







27 µm

56 µm

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Preliminary Results

Results: LSB



Results: Power



Results: DNL & INL



Results: DNL & INL





Results: Jitter





Results Summary

	Voltage Control	Current Control
LSB	72.07 ps	80.71 ps
FSR	295.13 ns	330.5 ns
Power	1.589 mW	0.9091 mW

Nominal Condition:

• TT corner

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$$V_n = 1,4 V$$
 $V_p = 0,4 V$ $V_{ctrl} = 2,9 V$

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A synthesizable digital Silicon Photon Multiplier with N input bits in a110 nm CMOS Technology

PhD project of Tommaso Maria Floris



Supervisor: Prof. Lodovico Ratti

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Recursive Structure



- Basic building block: compressor
- Each stage is built with the same procedure
- The input of the **first stage** is the binary vector coming from the array
- The input of the following stage is the total carry vector of the previous one

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Digital synthesis flow



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- Matrix shape obtained with a script
- The parameters are:
 - Rows & columns number
 - Width & height of each cell
 - Number of stdCell rows allocated for the digital logic
 - The percentage of the cell area left available for routing



- Cell width & height : 19,6 µm
- Free stdCell row : 2*2,8 = 5,6 μm
- Routing: 0,4*19,6 = 7,84 µm
- Sensor area : 164,64 µm^2
- 42% of the total cell area





- Cell width & height : 19,6 µm
- Free stdCell row : 1*2,8 = 2,8 μm
- Routing: 0,3*19,6 = 5,88 µm
- Sensor area : 230,5 µm^2
- 60% of the total cell area

