ASAPLF110 test chip characterization

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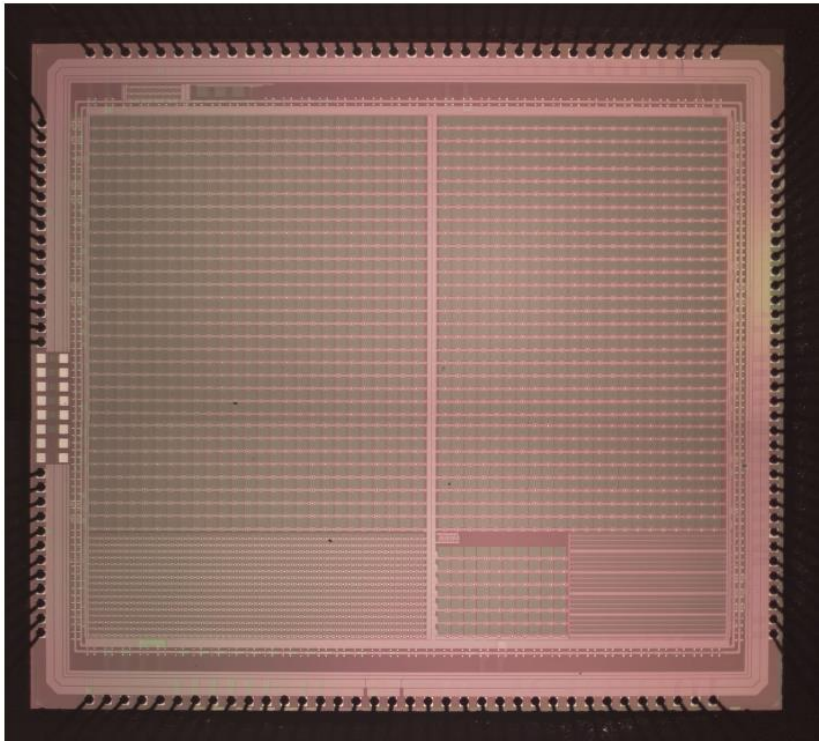
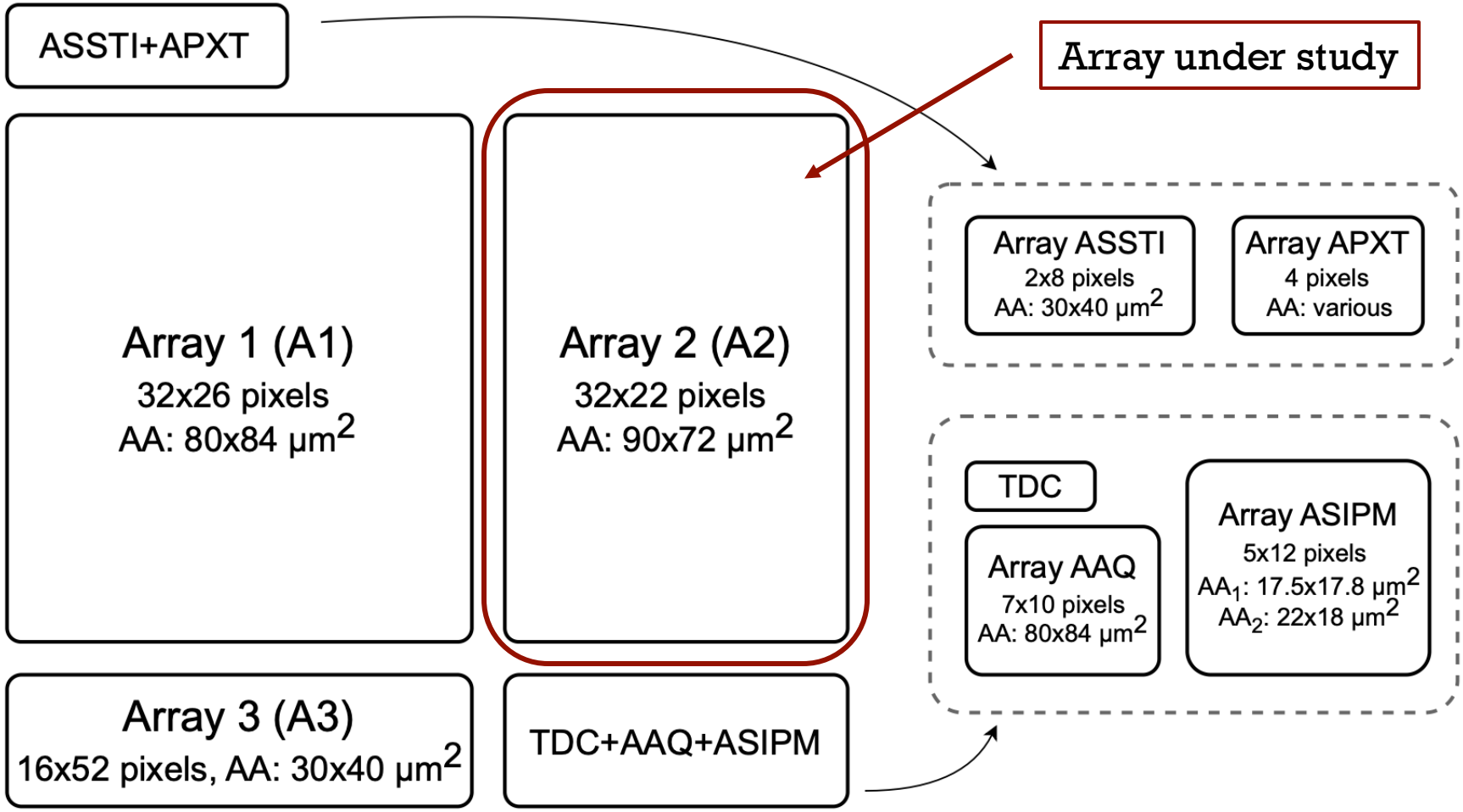
ASAPLF110: a technology characterization platform

A test chip (ASAPLF110) with the same technology of interest is available from a previous project:



- 110 nm CIS technology;
- 136 pads involving supplies, voltage references and I/O digital signals.
- fully digital detection system embedding various SPAD arrays with different readout circuits;
- availability of single sensors enabling direct extraction of the I-V characteristics featured by the SPADs
- in-chip time to digital converter for DCR and afterpulsing characterization
- digital SiPMs based on a parallel counter architecture

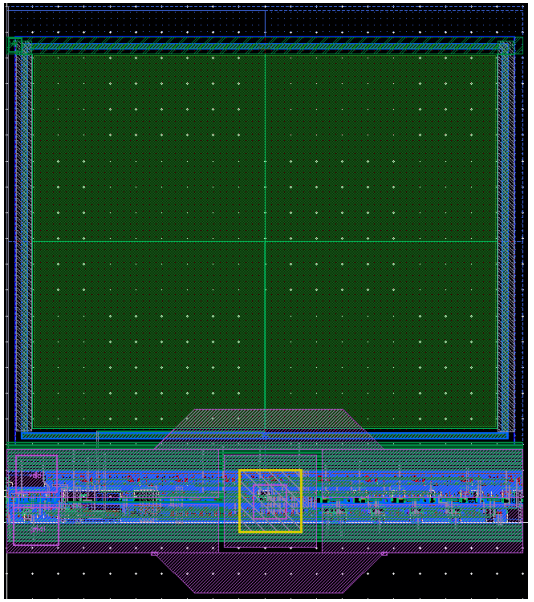
ASAP110LF chip - Design

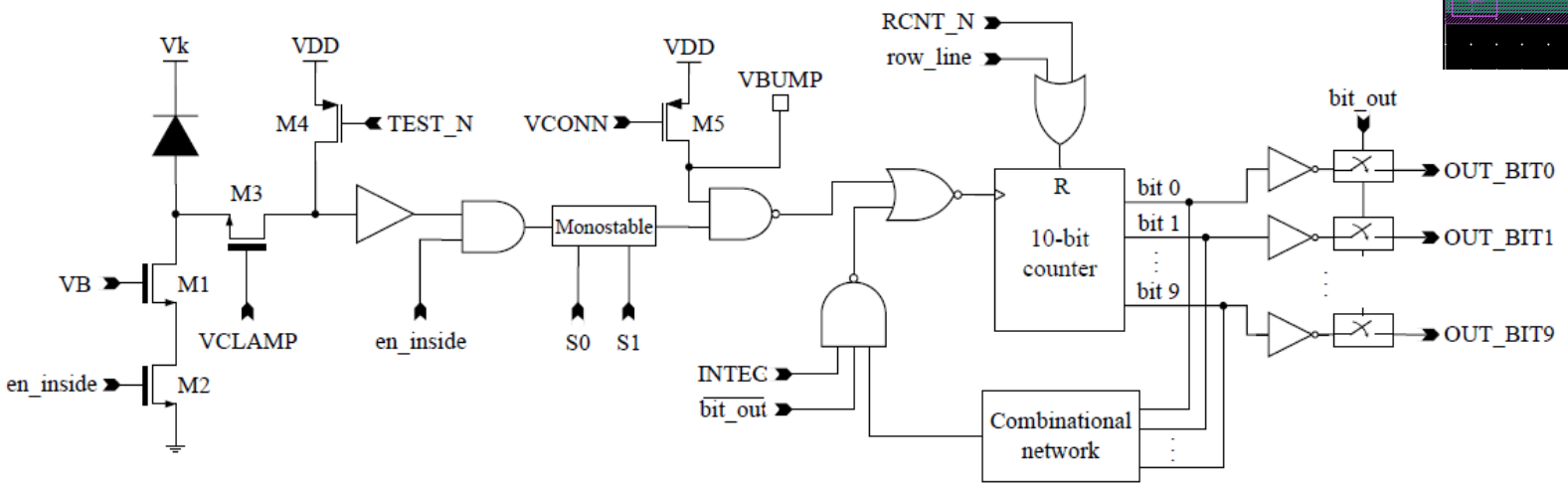


ASAP110LF chip – Array A2

Array 2 (A2) cell:

- SPADs array: 32x22 pixels, 90x72μm^2
- The avalanche is quenched by a passive network
- The monostable circuit modifies the duration of the sensor pulse (400 ps, 750 ps, 2 ns, transparent mode).
- A 10 bit counter automatically counts the pulses.

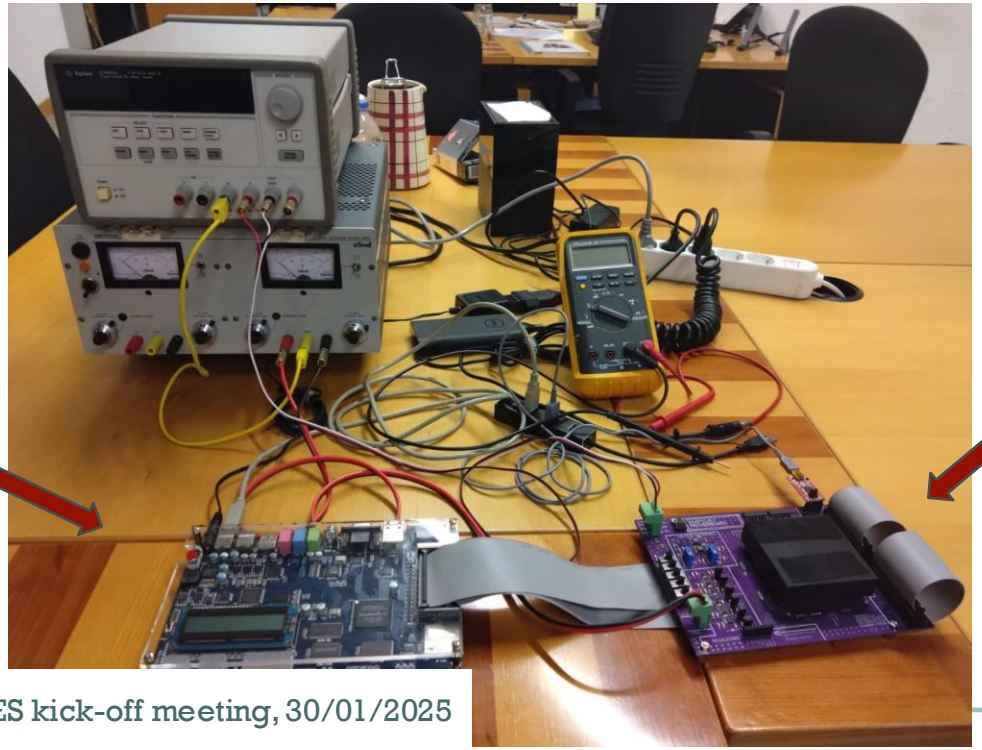




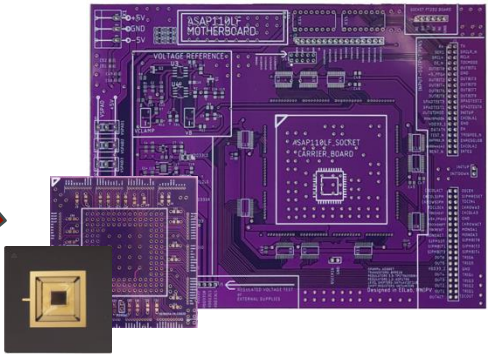
Test setup

- Two custom boards acting as interface between the FPGA and the chip.
- Firmware developed in VHDL
- Data acquisition based on protocol RS232 (command line)

FPGA: Altera DE2
(education board)

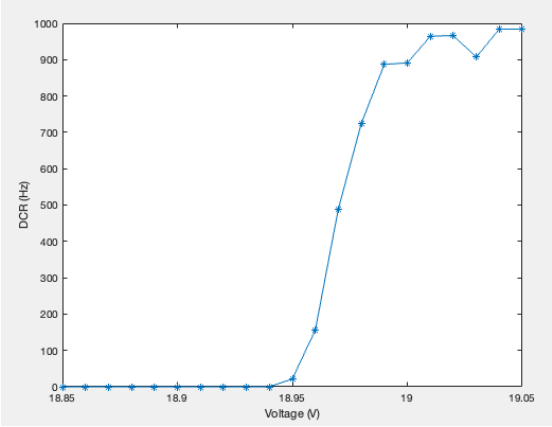


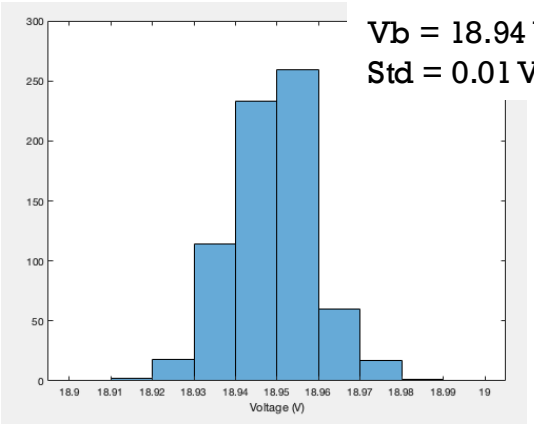
Custom bard +
ASAP110LF chip

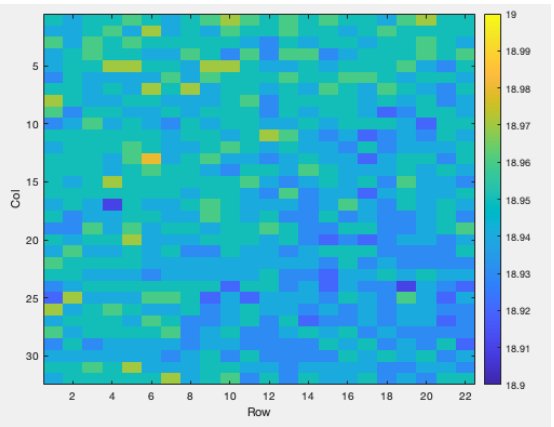


First test results

- Breakdown voltage
  - DCR VS voltage using 500 ms long gate windows
  - Scan performed with dV = 10 mV
  - Vb defined as the minimum voltage with DCR > 0 (Vb measured with IV-curves is 500 mV lower: ref. G. Torilla PhD thesis)

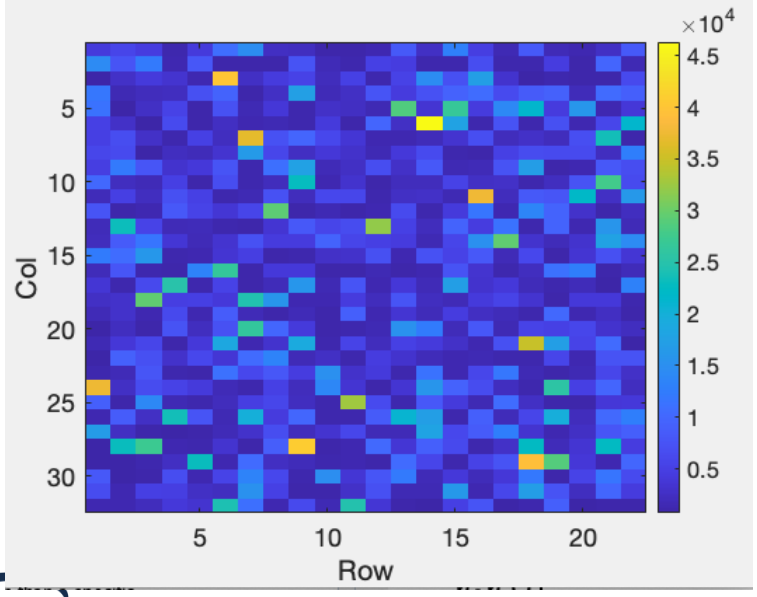


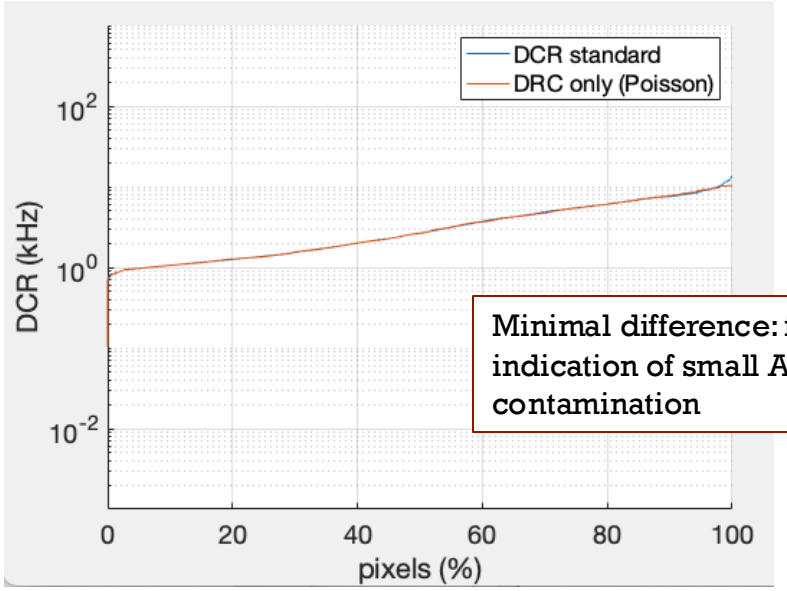




First test results

- Breakdown voltage
- DCR @ 21V: measured with two methods
  - Count rates measured in 30k windows (1 ms long): average value is the DCR contaminated by AP (DCR standard)
  - Assuming DCR follows Poisson distribution, I'm measuring the probability of having 0 counts in 1ms long windows (μ of the Poisson distribution)

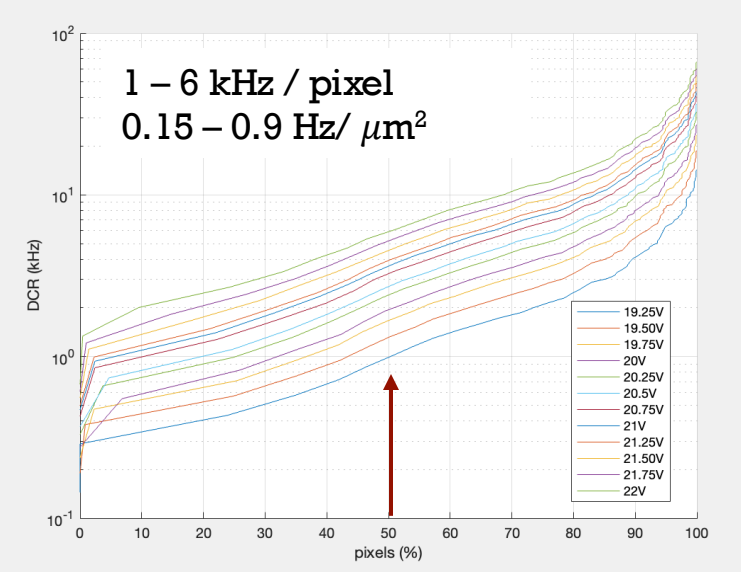


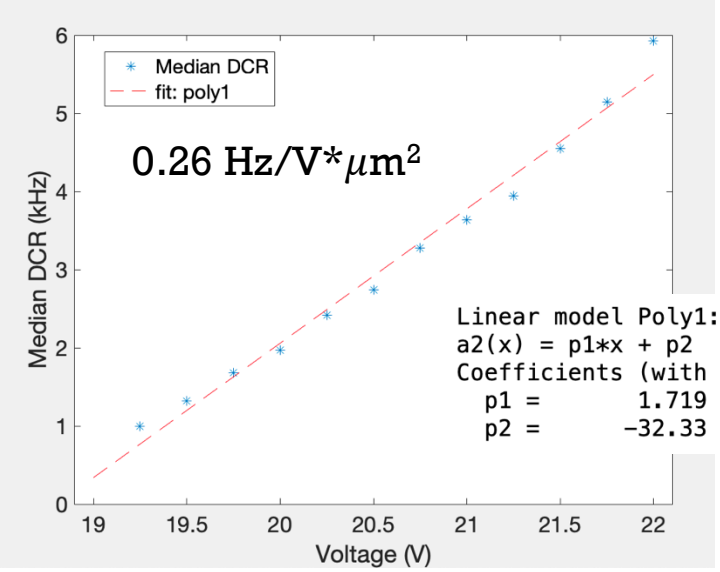


Minimal difference: first indication of small AP contamination

First test results

- Breakdown voltage
- DCR @ 21V
- DCR VS bias voltage





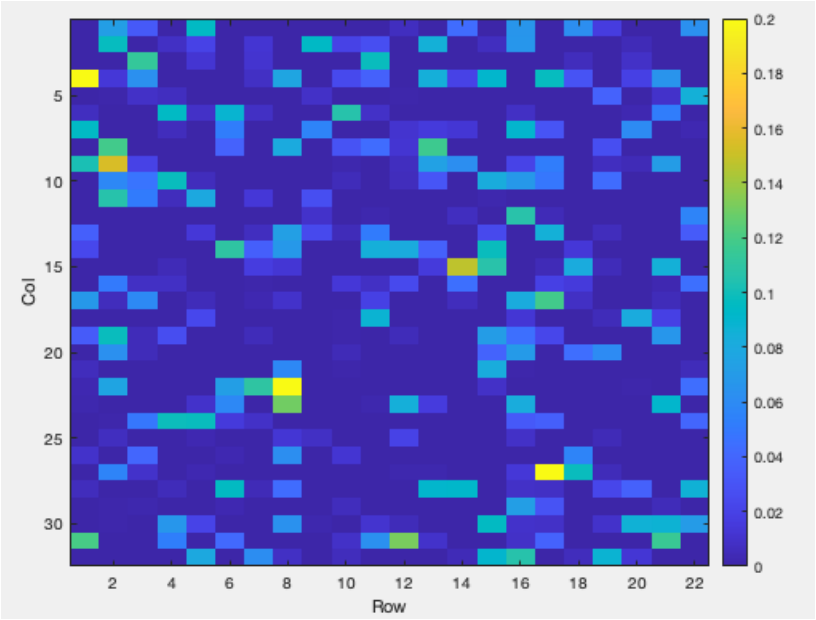
First test results

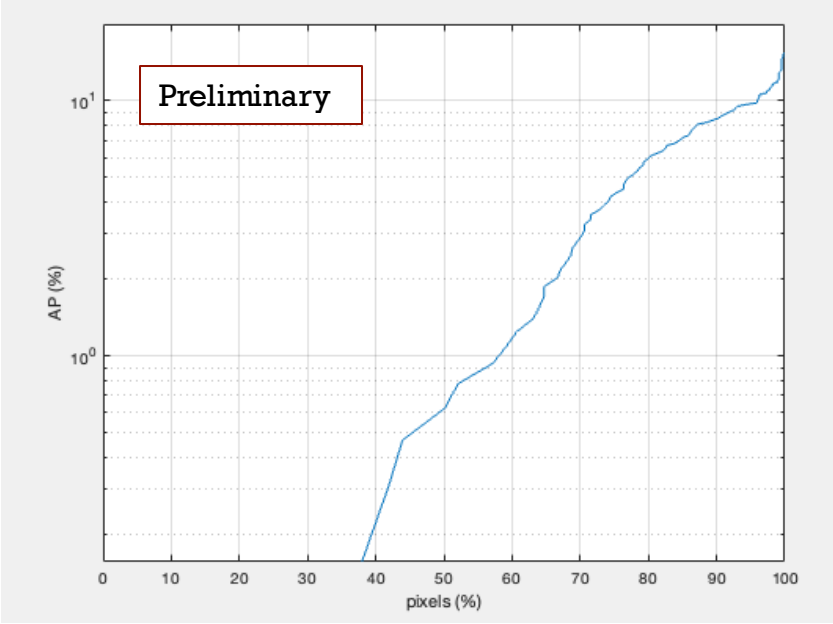
- Breakdown voltage
- DCR @ 21V
- DCR VS bias voltage
- AP @ 21V
  - Spurious pulses in gated windows N_{tot} have both DCR and AP
  - Assuming DCR follows Poisson distribution: the probability of having 0 counts in gated windows allows to measure the DCR alone:
  - AP can be measured as follows:

$$AP = \frac{N_{tot} - N_{DCR}}{N_{tot}}$$

First test results

- Breakdown voltage
- DCR @ 21V
- DCR VS bias voltage
- AP @ 21V



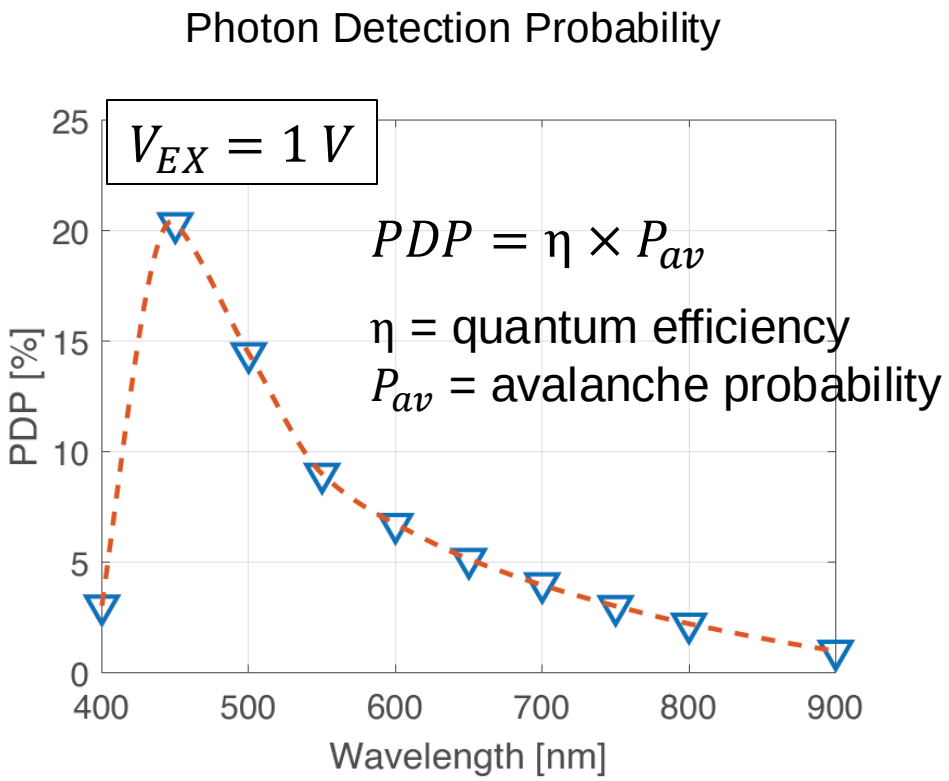


First test results

- Breakdown voltage
- DCR @ 21V
- DCR VS bias voltage
- AP: alternative strategies under study (i.e. Time interval)
  - Unfortunately, TDCs are not available for A2
  - Statistical methods based on Poisson assumption

First test results

- Breakdown voltage
- DCR @ 21V
- DCR VS bias voltage
- AP @ 21V
- PDE: from PhD thesis (G. Torilla)
  - We are preparing a setup in Como for this type of measurements
  - We are in contact with a company, but we have not yet finalised the offer



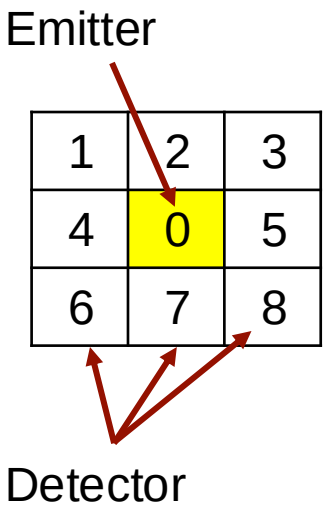
First test results

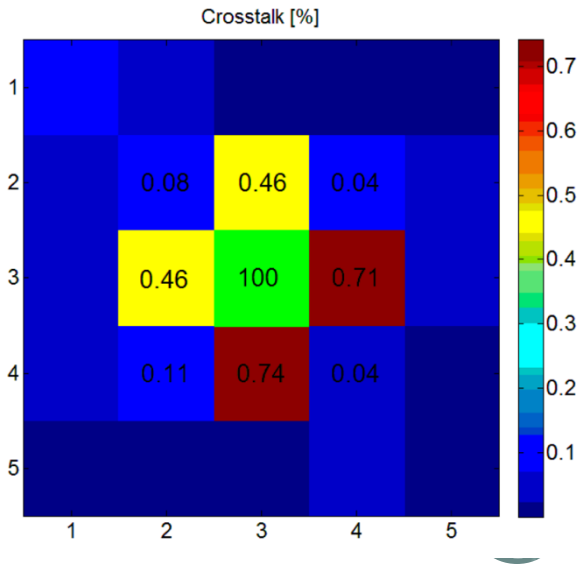
- Breakdown voltage
- DCR @ 21V
- DCR VS bias voltage
- AP @ 21V
- PDE @ 1 V over
- Cross talk: just started
  - A small team on the subject to implement the strategy in the firmware

Crosstalk: Method1

- In each measurement we consider two SPADs at the time (Emitter-Detector pair)
- It is a three-step procedure (Method1)
  - Spurious count rate for the Emitter while all detectors are OFF (M0)
  - Spurious count rate for one of the Detectors (i.e. 5) while the Emitter is OFF (M5)
  - Spurious count rate for the same Detector while the Emitter is ON (M5*)
- The probability to induce a spurious effect in Detector 5 is:

$$XT_5 = (M5^*-M5)/M0$$

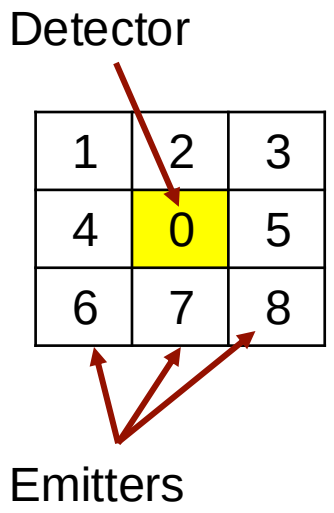




Crosstalk: Method2

- This time the central SPAD is considered the detector, while all the others are the emitters
- It is a two-step procedure
  - SPAD0 ON all others OFF (M0)
  - SPAD0 ON all others ON (M0*)

XT=(M0*-M0)/M0*



Crosstalk - Method2 @ 21V

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- It is a two-step procedure
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  - SPAD0 ON all others ON (M0*)

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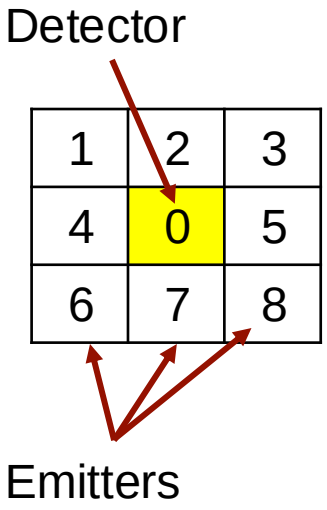

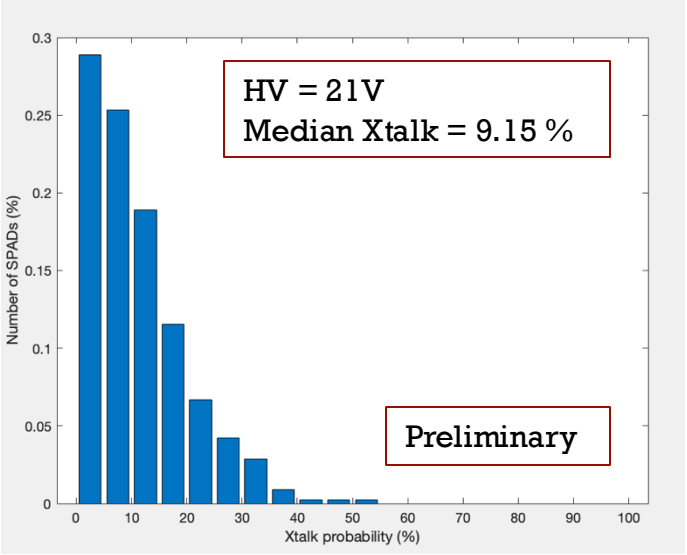

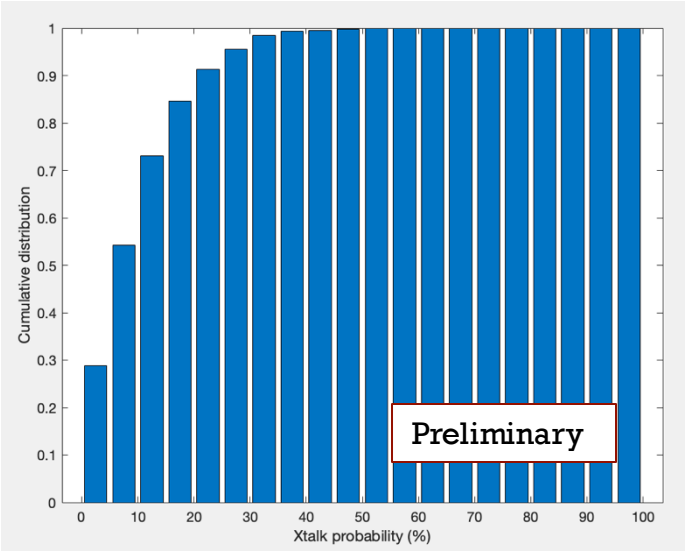

Crosstalk - Method2 @ 21V

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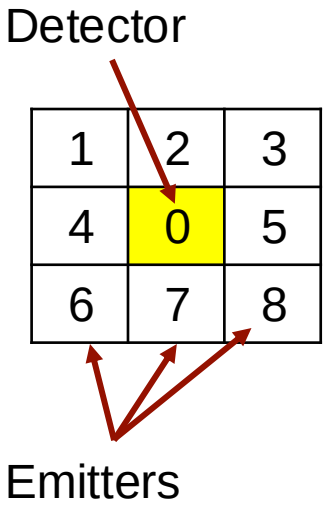
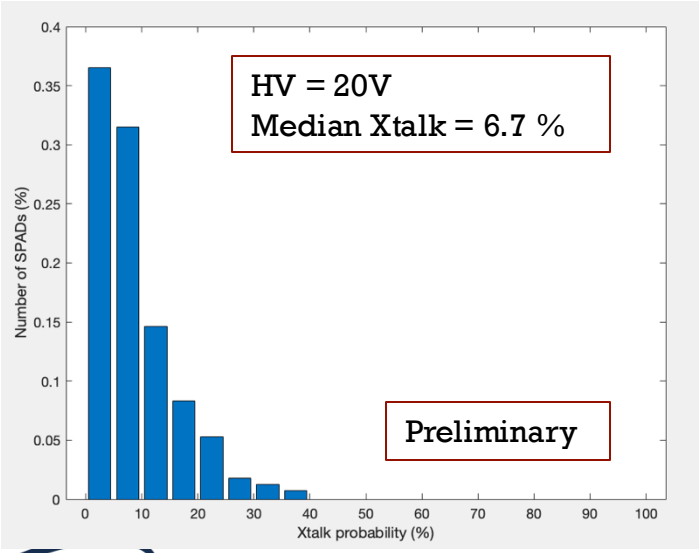
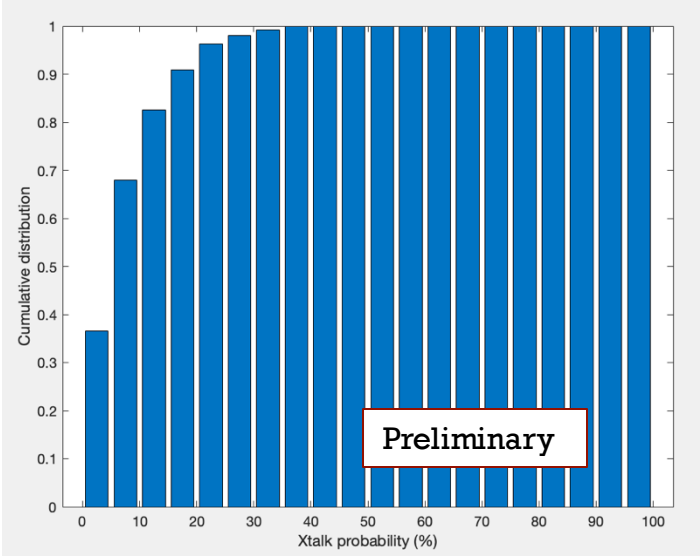
XT=(M0*-M0)/M0*





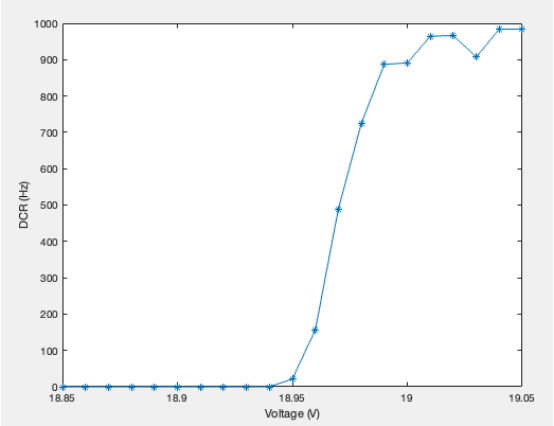


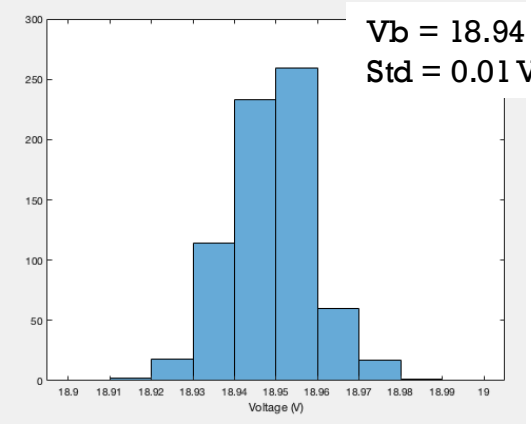
Summary

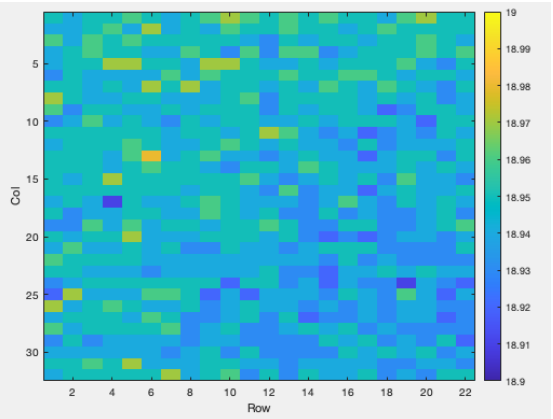
- In this talk I've summarized some tests recently performed just to get familiar with the system: there is still a lot to understand!
- The firmware is well advanced, but it requires some improvements
  - Deep understanding and new functionalities
- WP2 will collect inputs to improve the current setup and is the place where discussions will take place to define the requirements for the next setup: people interested in the discussions and willing to contribute can add their name in the google-doc
  - Tests methodology
  - Firmware implementation
  - Software and GUI
  - Discussion on the results

Backup

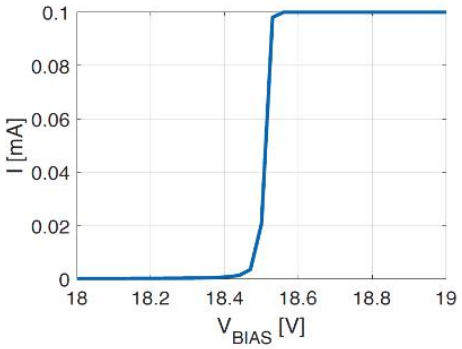
Vb (A2)



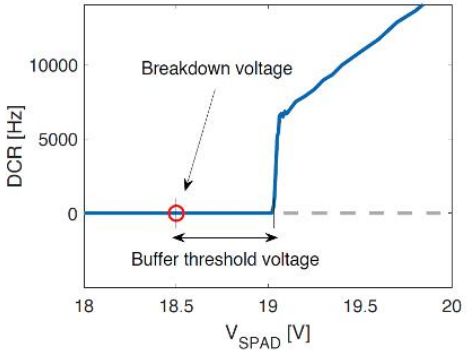


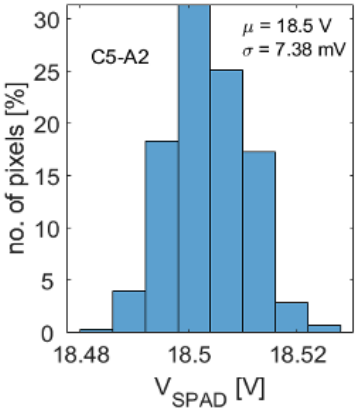


I-V curve measurements (single devices)



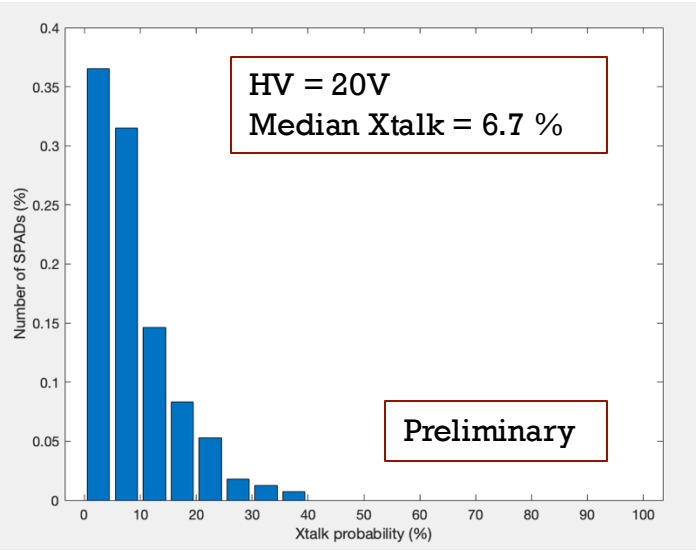
Breakdown voltage extraction (sensors in arrays)



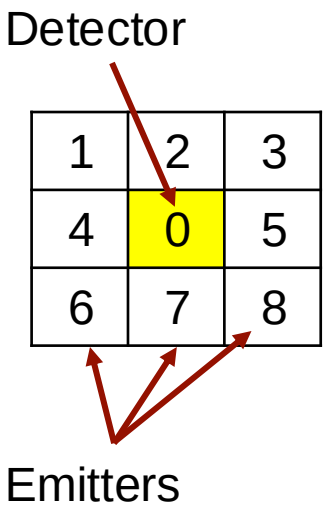


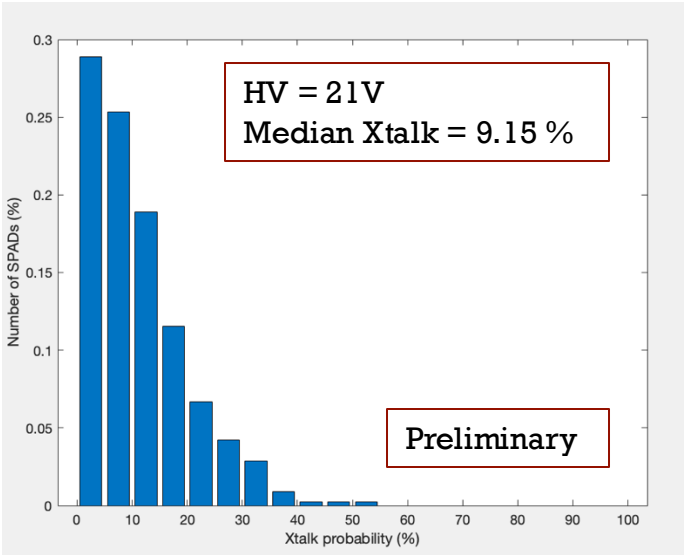
Ref: Gianmarco

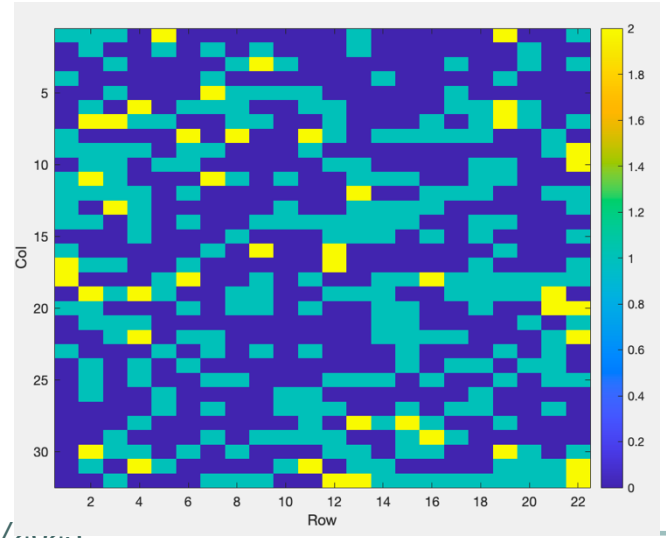
Crosstalk: Method2




```
xt20 =

  struct with fields:

    idxBadEv: [237×1 double]
    idxGoodEv: [397×1 double]
      idxOver: [70×1 double]

>> xt21

xt21 =

  struct with fields:

    idxBadEv: [104×1 double]
    idxGoodEv: [450×1 double]
      idxOver: [150×1 double]
```







SPADs “Faulty” in the two measurements: yellow SPADs behave incorrectly in both measurements