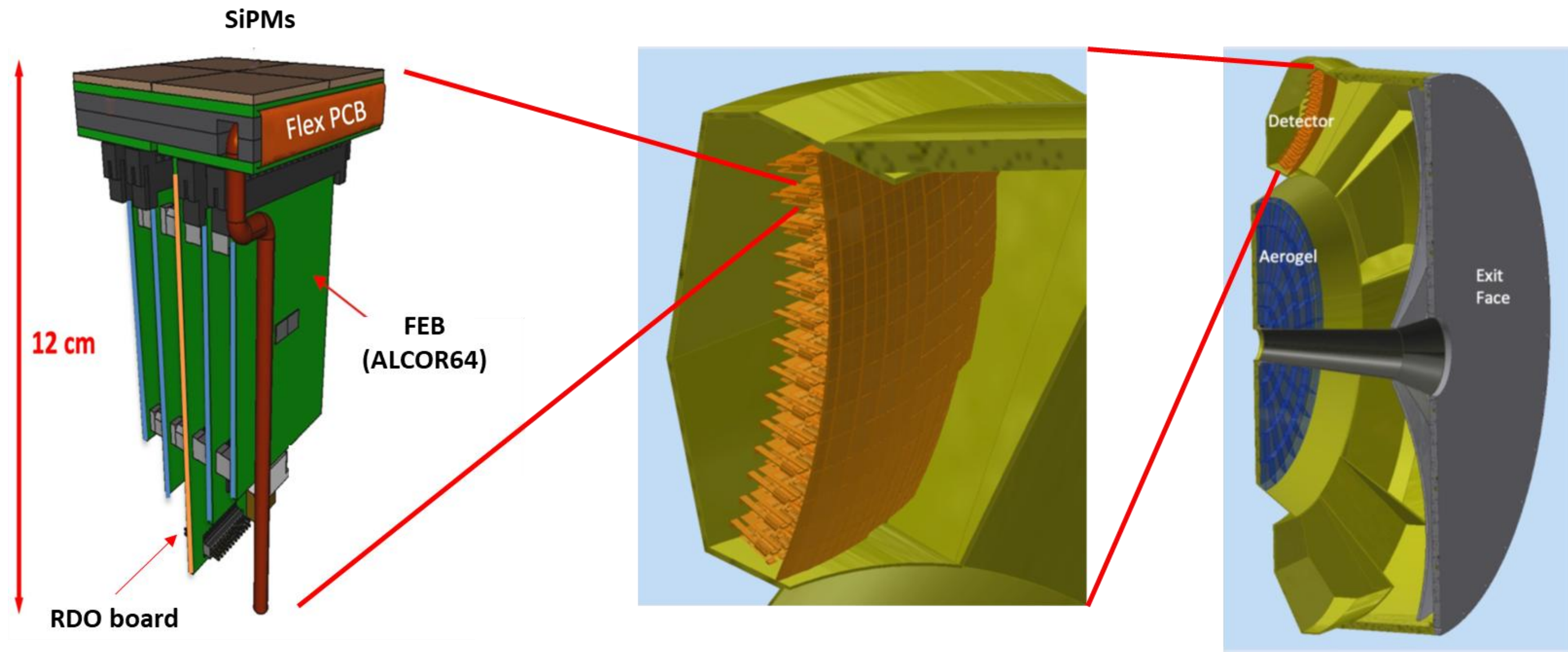
# Radiation tolerance tests of key electronic components of the dRICH RDO




Sandro Geminiani (UniBo and Bologna INFN)

ePIC general meeting-20/01/2025

# The PDU radiation environment

The dRICH-PDUs are exposed on a moderate dose of radiation, which causes:

- SiPMs degradation.
- **Lower reliability on Electronic component functioning.**

**Expected radiation exposure, including a 5 safety factor** (ref data: https://wiki.bnl.gov/EPIC/index.php?title=Radiation_Doses):

$$\mathbf{TID_5 \cong 2.3\ krad}$$
$$\mathbf{(\ for\ 1000\ fb^{-1}\ )}$$

$$\mathbf{\phi_5(p + n > 20MeV) \cong 700\ Hz/cm^2}$$

- **Cumulative effects:** during the component life, the **integrated TID increases component power consumption** up to a final damage.
- **Single Event Effects (FEE): localized event induced by a single particle**, producing ionization through nuclear collision:

**Transient (SET):** spurious signals propagating in the circuit.

**Static (SEU):** errors overwriting memory location.

**Permanent (SEL, …):** destructive events (permanent damage)

# The PDU radiation environment

The dRICH-PDUs are exposed on a moderate dose of radiation, which causes:

- SiPMs degradation.
- **Lower reliability on Electronic component functioning.**

**Expected radiation exposure, including a 5 safety factor** (ref data: https://wiki.bnl.gov/EPIC/index.php?title=Radiation_Doses):

$$\mathbf{TID_5 \cong 2.3\ krad}$$
$$\mathbf{(\ for\ 1000\ fb^{-1}\ )}$$

$$\mathbf{\phi_5(p+n>20MeV) \cong 700\ Hz/cm^2}$$

- **Cumulative effects:** during the component life, the **integrated TID increases component power consumption** up to a final damage.
- **Single Event Effects (FEE): localized event induced by a single particle**, producing ionization through nuclear collision:

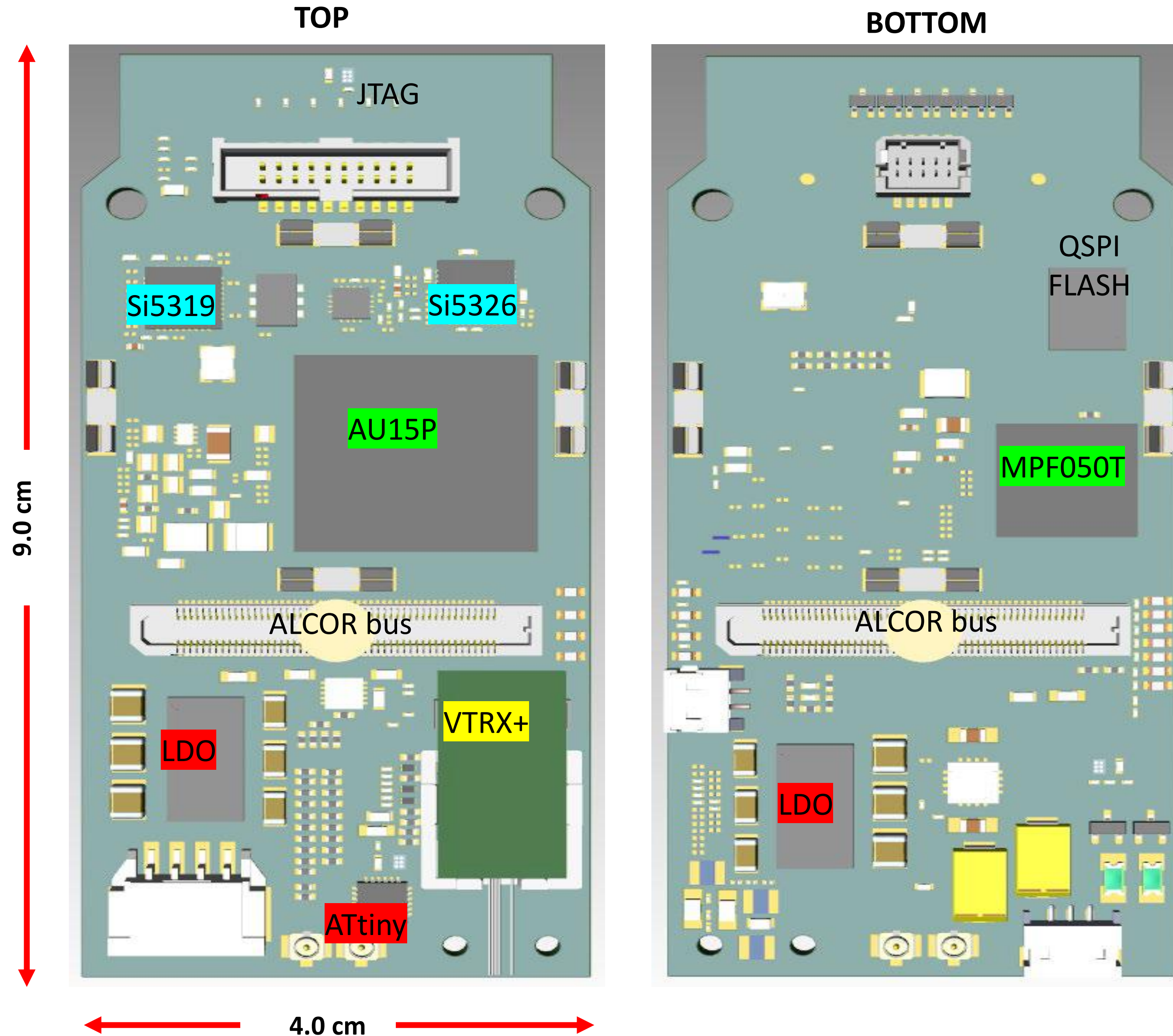
**Transient (SET):** spurious signals propagating in the circuit.

**Static (SEU):** errors overwriting memory location.

**Permanent (SEL, …):** destructive events (permanent damage)

**IMPORTANT to estimate SEU and (potential) SEL occurrences for both RDO card and ALCOR FEBs !**

# The RDO Board




**FPGAs**

- **AU15P**: **AMD Artix Ultrascale+** main FPGA interfacing with ALCORs.
- **MPF50T**: **Microchip PolarFire** FPGA responsible for the AU15P configuration (see later …).

**Clock multiplier**

- **Si5319** and **Si5326** from **SiLab**.

**Power management**

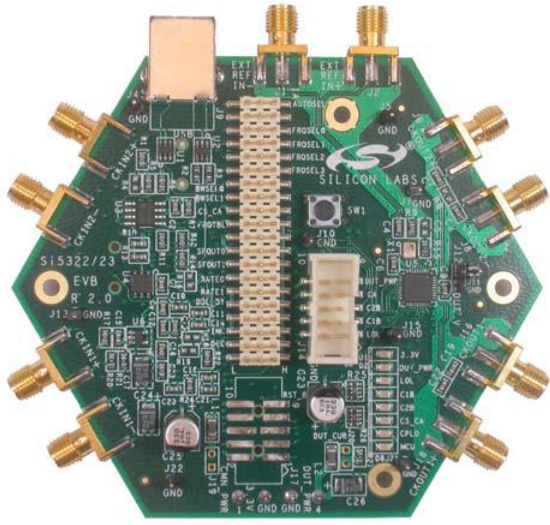
- **2 LDOs LTM4709** for different power rails.
- **Micorchip ATtiny417** µcontroller, controlling power consumption.

**Data link**

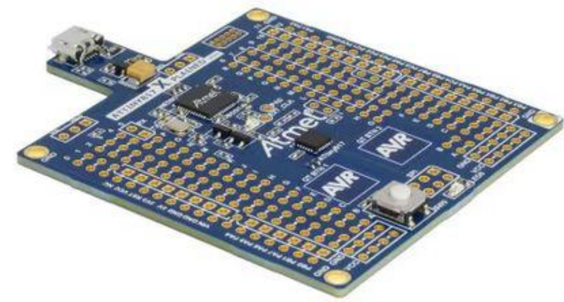
- **VTRX+**: optical transceiver.

# Proton irradiation campaign (@Proton Irradiation facility in Trento)

**Si5326-EVB**



**ALINX XCAU15P**

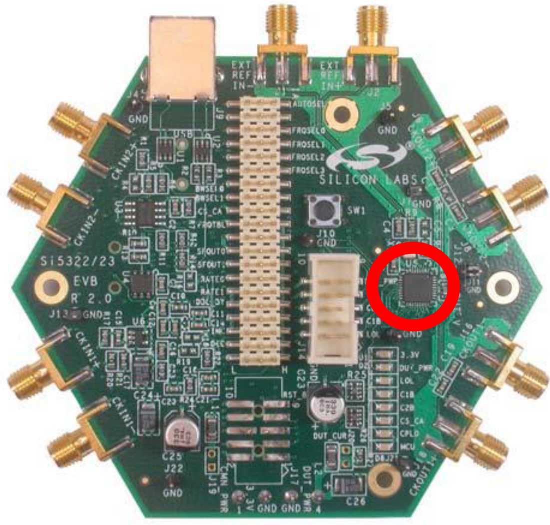


**ATtiny817-EVB**

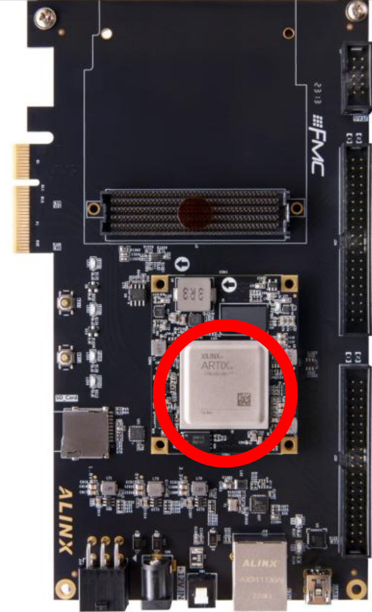
***Waiting for the RDO…***

# Proton irradiation campaign (@Proton Irradiation facility in Trento)

Si5326-EVB



ALINX XCAU15P



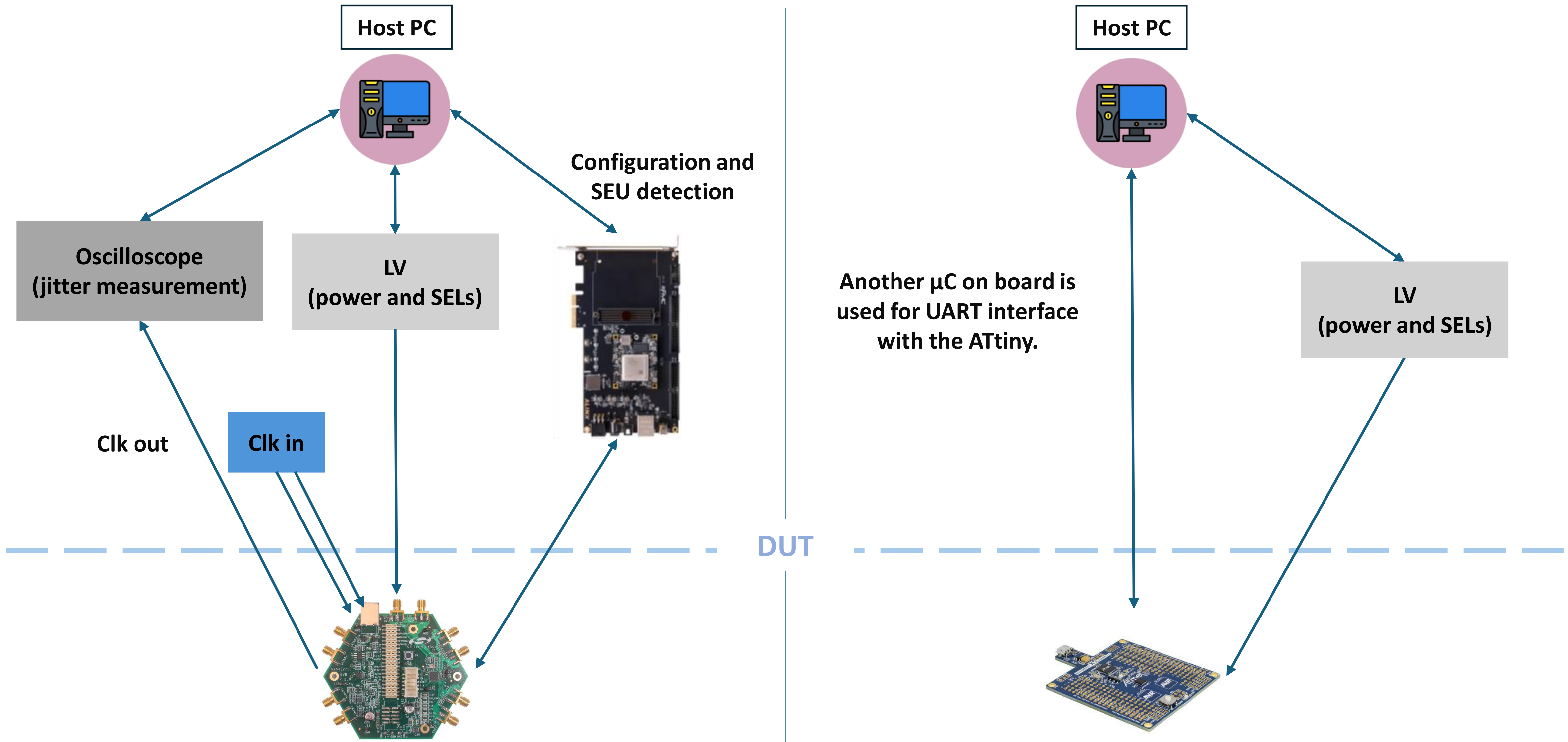
ATtiny817-EVB

**Irradiation session :**

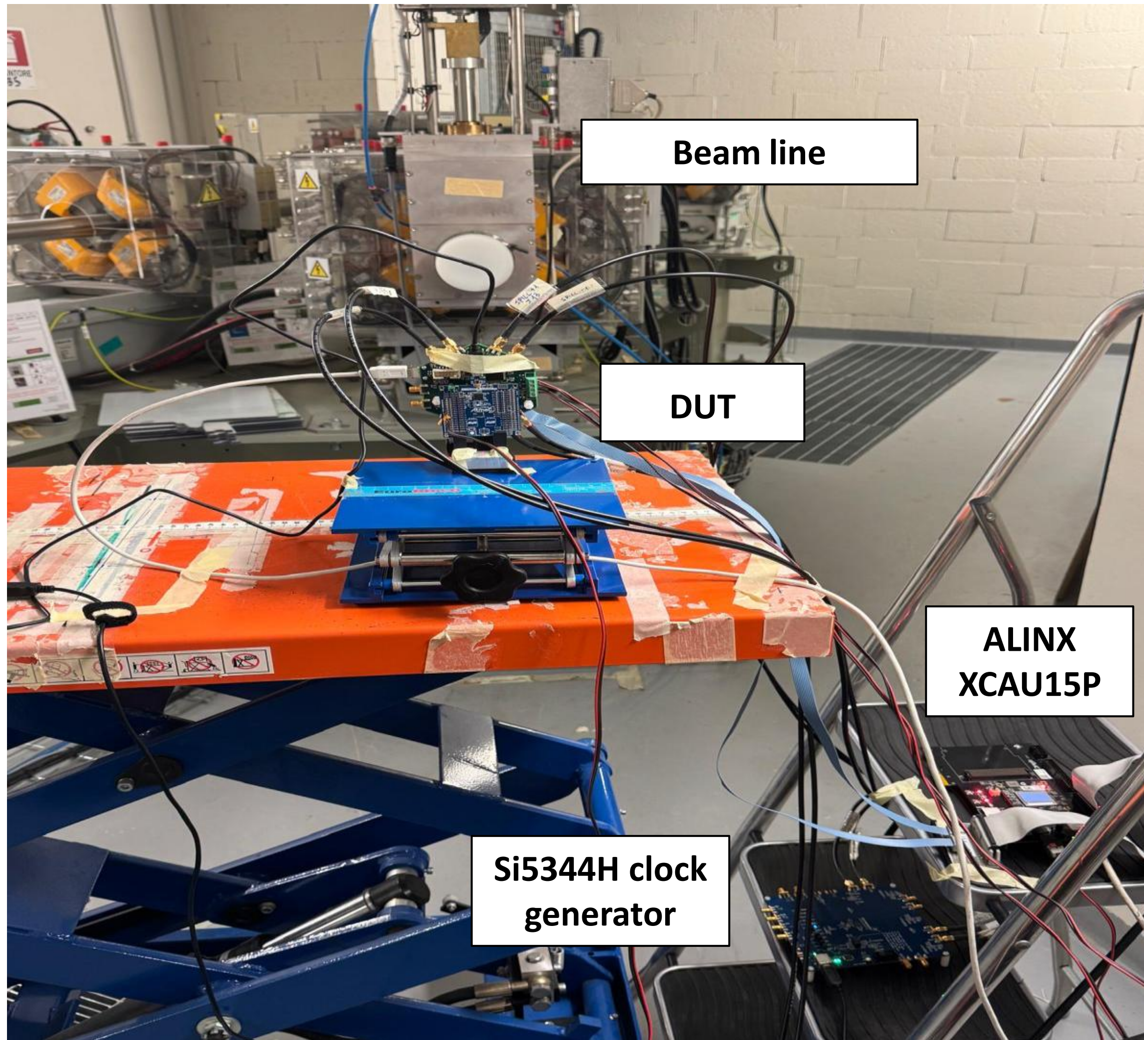
- **Si5326** and **ATtiny EVBs** on a proton beam at 100 MeV kinetic energy (using a $10^8$ Hz/cm$^{-2}$ flux).
- **ALINX XCAU15P board** on a proton beam at 70 MeV kinetic energy (using a $10^6/10^7$ Hz/cm$^{-2}$ flux).

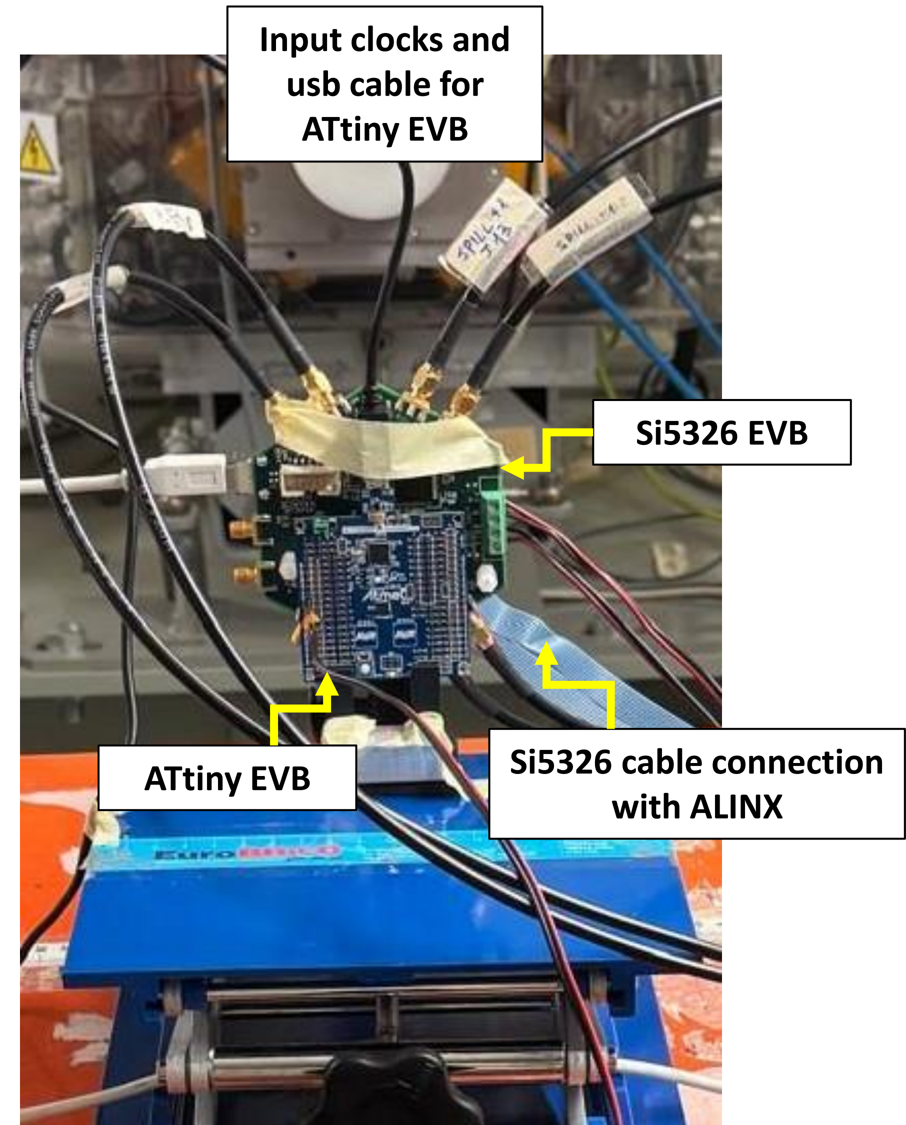
**Purpose**: estimating **SEE/TID sensitivity** for selected components waiting for first RDO prototypes.

# Si5326 and ATtiny setup



# Si5326 and ATtiny setup



# Results

## ATtiny817 µcontroller

- **Monitored memory:** 6.6/8 KB of **FLASH (53 Kb)** and 450/512 B of **SRAM (3.6 Kb).**
- **21 SEUs** detected on **SRAM**, while **0 SEUs** on **FLASH** memory after 1026 s.
- The **ATtiny crashed in the last run** (TID effect or SEL?).
- **TID = 23 krad (dose rate = 1-2 krad/min)**
- **SRAM**: $\sigma_{SEU} = (3.89 \pm 0.54) \cdot 10^{-14} \frac{\text{cm}^2}{\text{bit}}$
- **FLASH memory** (limit @ 95% C.L.): $\sigma_{SEU} < 3.83 \cdot 10^{-16} \frac{\text{cm}^2}{\text{bit}}$

**MTBF in the dRICH system for ATtiny417:**

**SRAM (256B): 4.0 h**
**FLASH (4kB): > 26 h**

## Si5326 clock multiplier

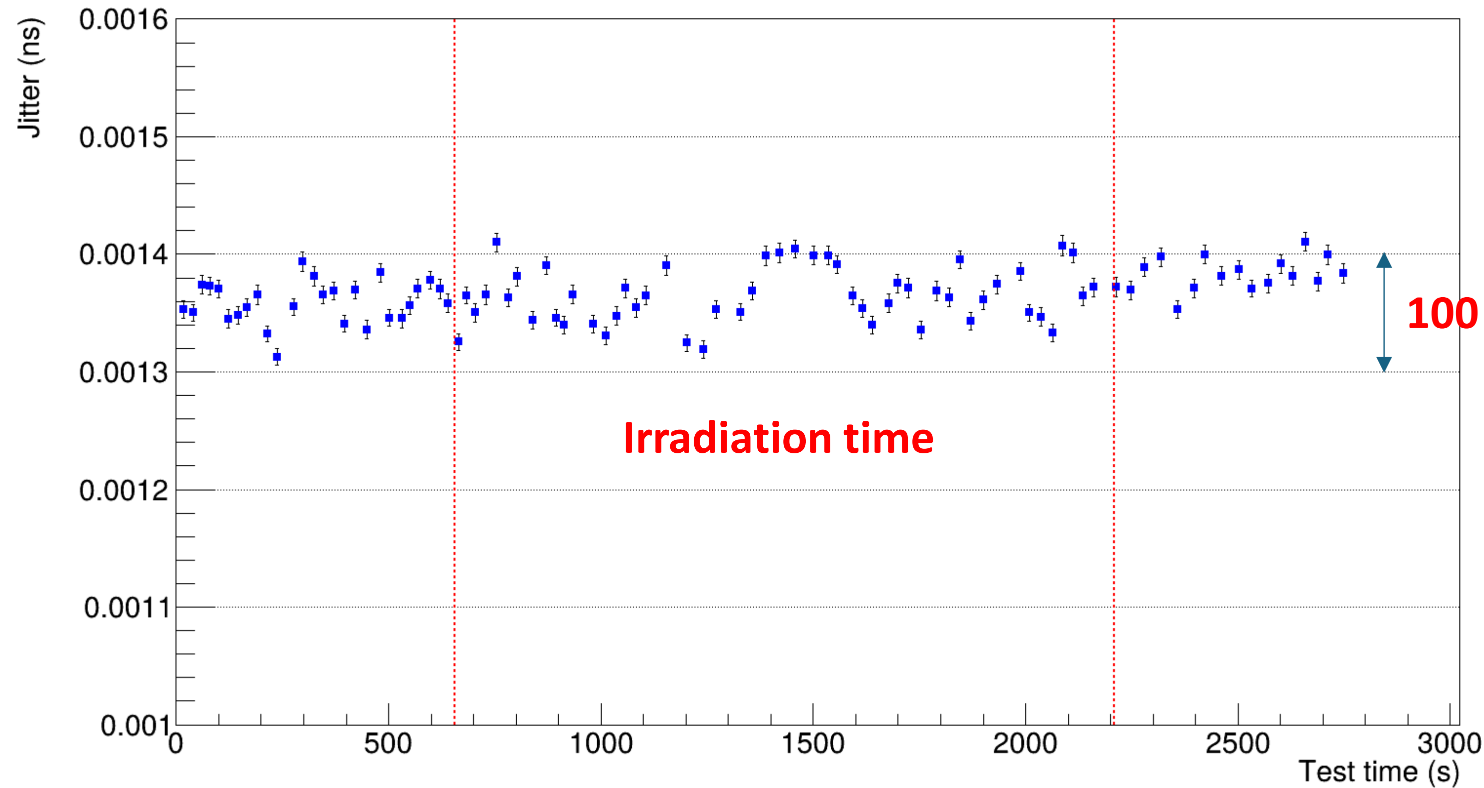
- **Monitored memory: 2007/2048 bits** of configuration memory.
- **19 SEUs** and **0 SELs** detected after 1553 s.
- **TID = 42 krad (dose rate = 1-2 krad/min)**
- Besides the SEUs, the device did not **lose the PLL lock keeping the out clock period stable.**
- $\sigma_{SEU} = (2.11 \pm 0.50) \cdot 10^{-14} \frac{\text{cm}^2}{\text{bit}}$

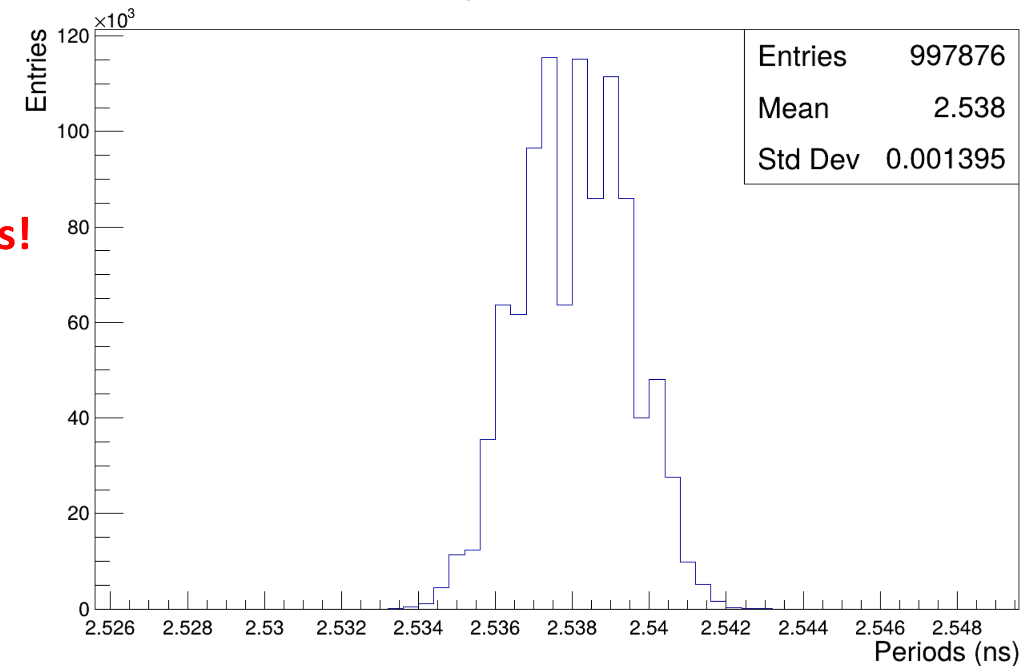
**MTBF in the dRICH system for both Si5319 and Si5326:**

**3.8 h**

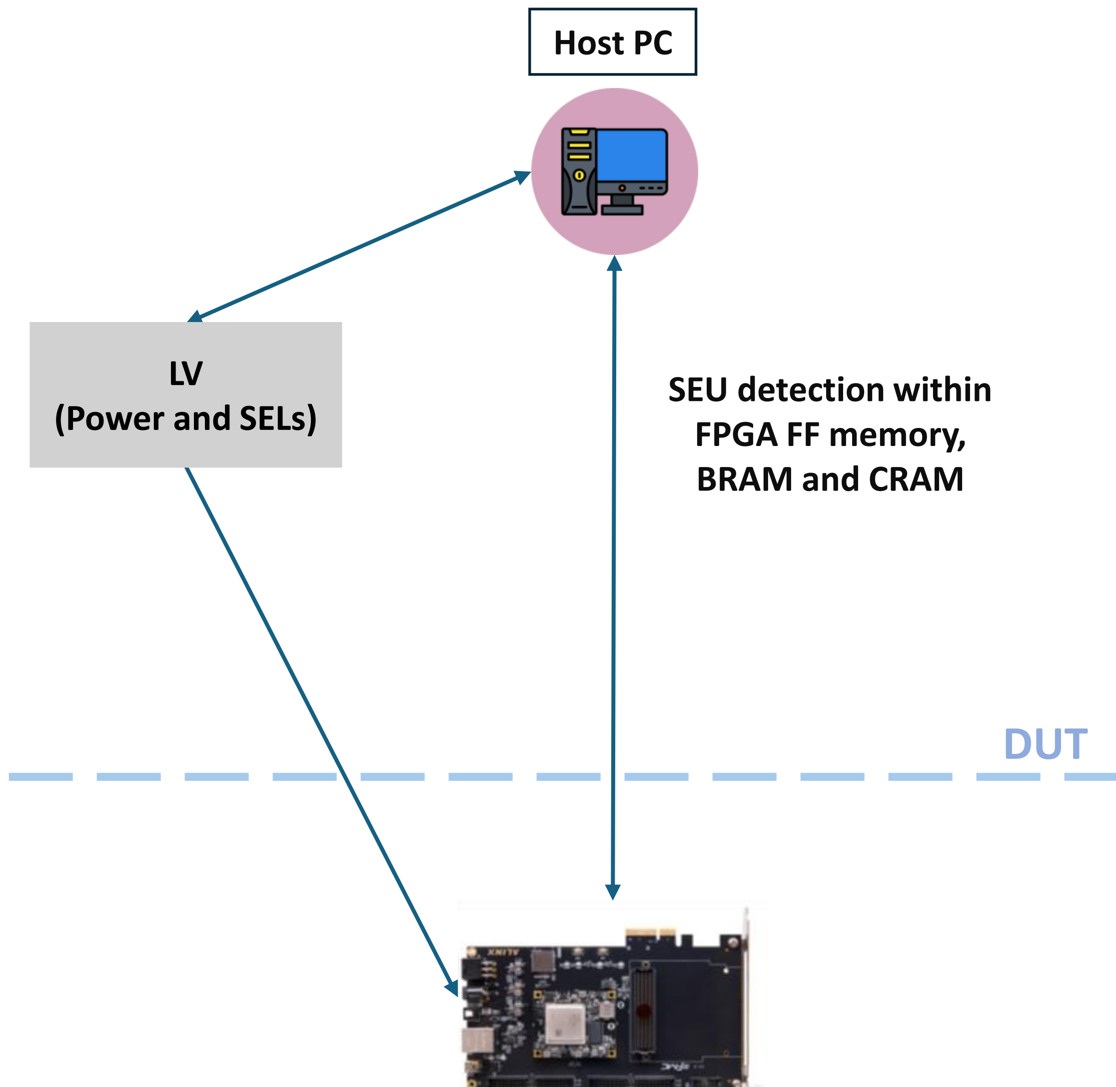
**MTBF = Mean Time Between Failure**

# Jitter and Period of the out clock



# ALINX XCAU15P setup




The AU15P checks its own memory:

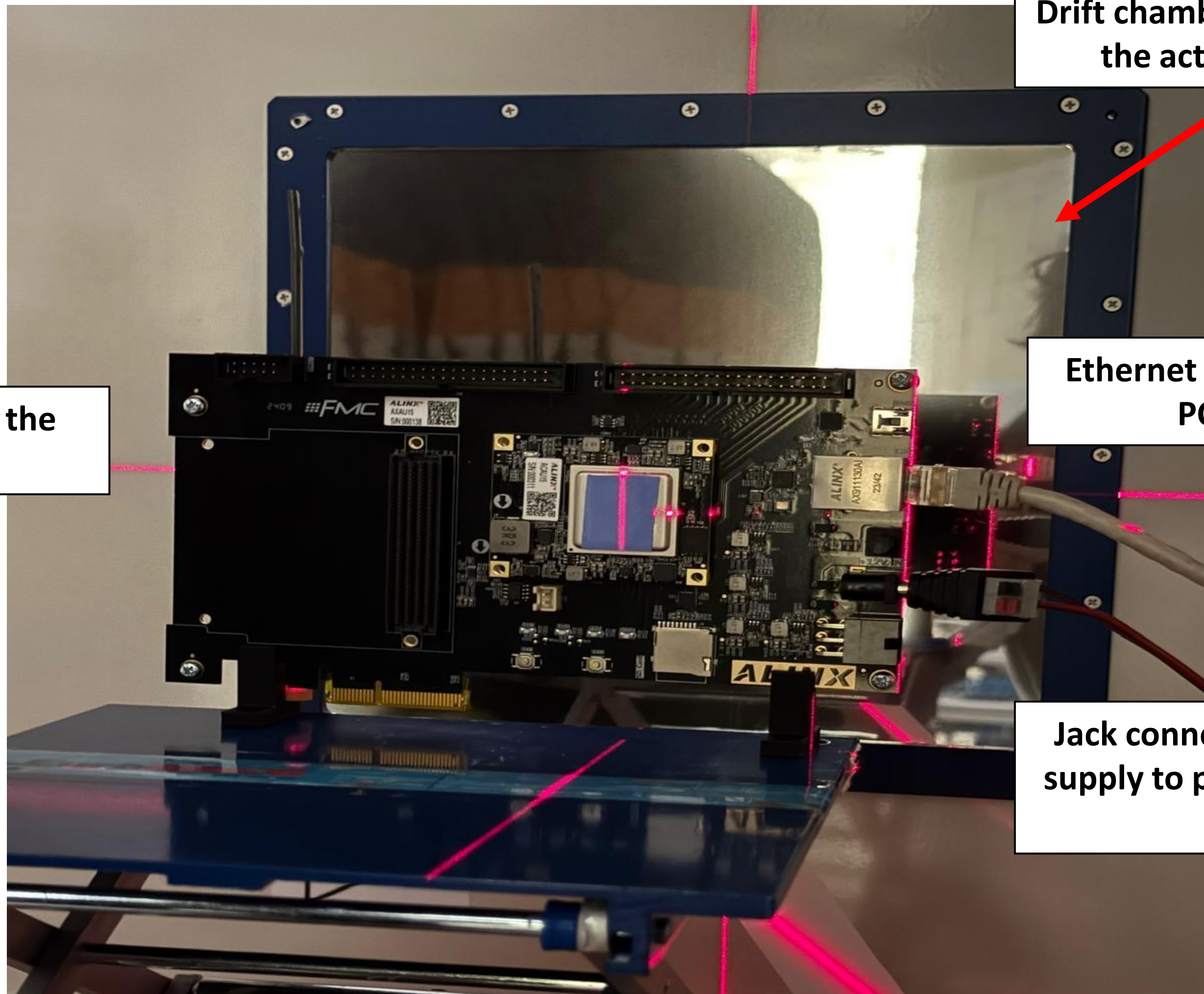
- **FF chains** and **Block RAM buffer** were configured with a **fixed pattern** and checked continuously (communication via IPbus over Ethernet link).
- **Configuration RAM** was checked by the **Soft Error Mitigation (SEM) IP core** by AMD (ref: https://www.xilinx.com/products/intellectual-property/sem.html).

The SEM IP is configured in **«Mitigation and testing»** mode:

- It **locates the errors** through ECC and CRC approaches.
- It **corrects the error** if the location is identified.
- **It checks all the configuration memory.**

# ALINX XCAU15P setup

ALINX XCAU15P aligned to the beam.




Drift chamber monitor to measure the actual proton fluence.

Ethernet Connection to the Host PC to detect SEUs

Jack connection to the LV Power supply to power up the FPGA and detect SELs.

# Results

- **Monitored memory: 8/156 Kb** of **FF memory**, **3.6/5.1 Mb** of **BRAM** and **33/33 Mb** of **CRAM**.
- **0 SEUs** detected on **FF memory** and **69 SEUs** on **BRAM** after 2560s.
- **70 corrected SEUs**, **11 uncorrected SEUs** and **1 dead link** detected on **CRAM** after 2560 s.
- **No SEL** detected after 3706 s.
- **TID = 6.36 krad (dose rate = 10-500 rad/min)** after 3706 s.

**FF memory** (limit @ 95% C.L.): $\sigma < 3.5 \cdot 10^{-14} \frac{\text{cm}^2}{\text{bit}}$

**MTBF in the dRICH system (156 Kb):**
**> 3.6 min**

**BRAM**: $\sigma_{\text{SEU}} = (1.78 \pm 0.21) \cdot 10^{-15} \frac{\text{cm}^2}{\text{bit}}$

**MTBF in the dRICH system (5.1 Mb):**
**2.1 min**

**SEU cross section and MTBF (33 Mb) in the dRICH system for CRAM :**

| | $\sigma_{\text{SEU}} \left(10^{-16} \frac{\text{cm}^2}{\text{bit}}\right)$ | **MTBF** (min) |
|---|---|---|
| **COR** | $(1.96 \pm 0.25)$ | **2.9** |
| **UNCOR** | $(3.09 \pm 0.94) \cdot 10^{-1}$ | **18** |
| **TOTAL** | $(2.30 \pm 0.28)$ | **2.5** |

# Conclusions and outlook

1. We integrated $\mathbf{TID \sim 2.8 \cdot TID_5}$ for the AU15P, $\mathbf{TID \sim 10 \cdot TID_5}$ for the ATtiny and $\mathbf{TID \sim 18 \cdot TID_5}$ for the Si5326.

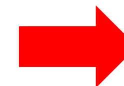
No significative cumulative effect or SEL during all the tests, besides the **ATtiny crash.**

**Devices tested up to a TID largely exceeding expected TID @dRICH: no destructive effects seen for $\mathbf{TID \leq TID_5}$**

2. **Si5326: MTBF = 3.8 h** and the jitter analysis showed the **out clock is very stable.**

**The RDO AU15P will control the chip configuration every t ≪ 3.8 h.**

3. **ATtiny**: **SRAM MTBF = 4 h** and **FLASH MTBF > 26 h**.



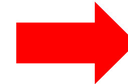
**The FLASH MTBF is a safety limit and key RAM registers will be implemented with TMR checks.**

# Conclusions and outlook

4. Ultrascale+ **FPGA SEUs cross sections estimated by AMD**:
   - BRAM: $\sigma_{SEU} = (9.82 \pm 1.77) \cdot 10^{-16} \frac{cm^2}{bit}$
   - CRAM: $\sigma_{SEU} = (2.67 \pm 0.48) \cdot 10^{-16} \frac{cm^2}{bit}$

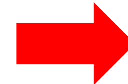
**Our CRAM estimate is compatible** with the AMD one while our **BRAM estimate differs for a factor** $\sim$**2**. Then, our estimates for MTBFs are:

**FF MTBF > 3.6 min** and **BRAM MTBF = 2.1 min**



**They are manageable at the AU15P firmware level using TMR,CRC and reset features.**

**CRAM MTBF = 2.5 min**



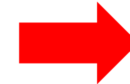
**The RDO MPFT50 as a FLASH based FPGA will work as scrubber, ensuring fast SEU correction.**

# Conclusions and outlook

4. Ultrascale+ **FPGA SEUs cross sections estimated by AMD**:
   - BRAM: $\sigma_{SEU} = (9.82 \pm 1.77) \cdot 10^{-16} \frac{cm^2}{bit}$
   - CRAM: $\sigma_{SEU} = (2.67 \pm 0.48) \cdot 10^{-16} \frac{cm^2}{bit}$

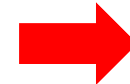
**Our CRAM estimate is compatible** with the AMD one while our **BRAM estimate differs for a factor** $\sim$**2**. Then, our estimates for MTBFs are:

**FF MTBF > 3.6 min** and **BRAM MTBF = 2.1 min**



**They are manageable at the AU15P firmware level using TMR,CRC and reset features.**

**CRAM MTBF = 2.5 min**



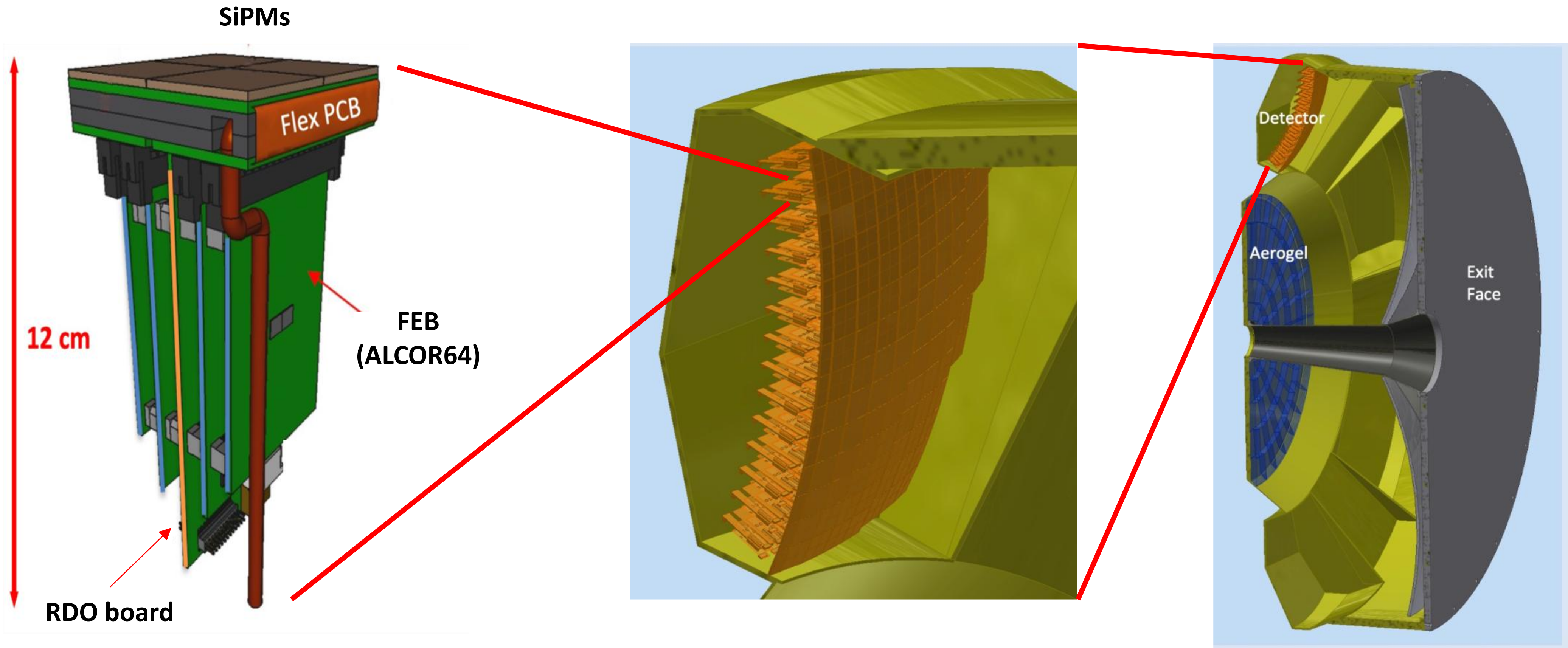
**The RDO MPFT50 as a FLASH based FPGA will work as scrubber, ensuring fast SEU correction.**

**No showstoppers identified for tested RDO components. SEU mitigation strategies needed in firmware design, as expected!**

# Thank You for Your attention!

# Backup slides

# The RDO within the dRICH




**Photon Detection Unit (PDU):**

- 4 matrices (64SiPMs each)
  - 4 ALCOR64 FEBs
    - **1 RDO board**

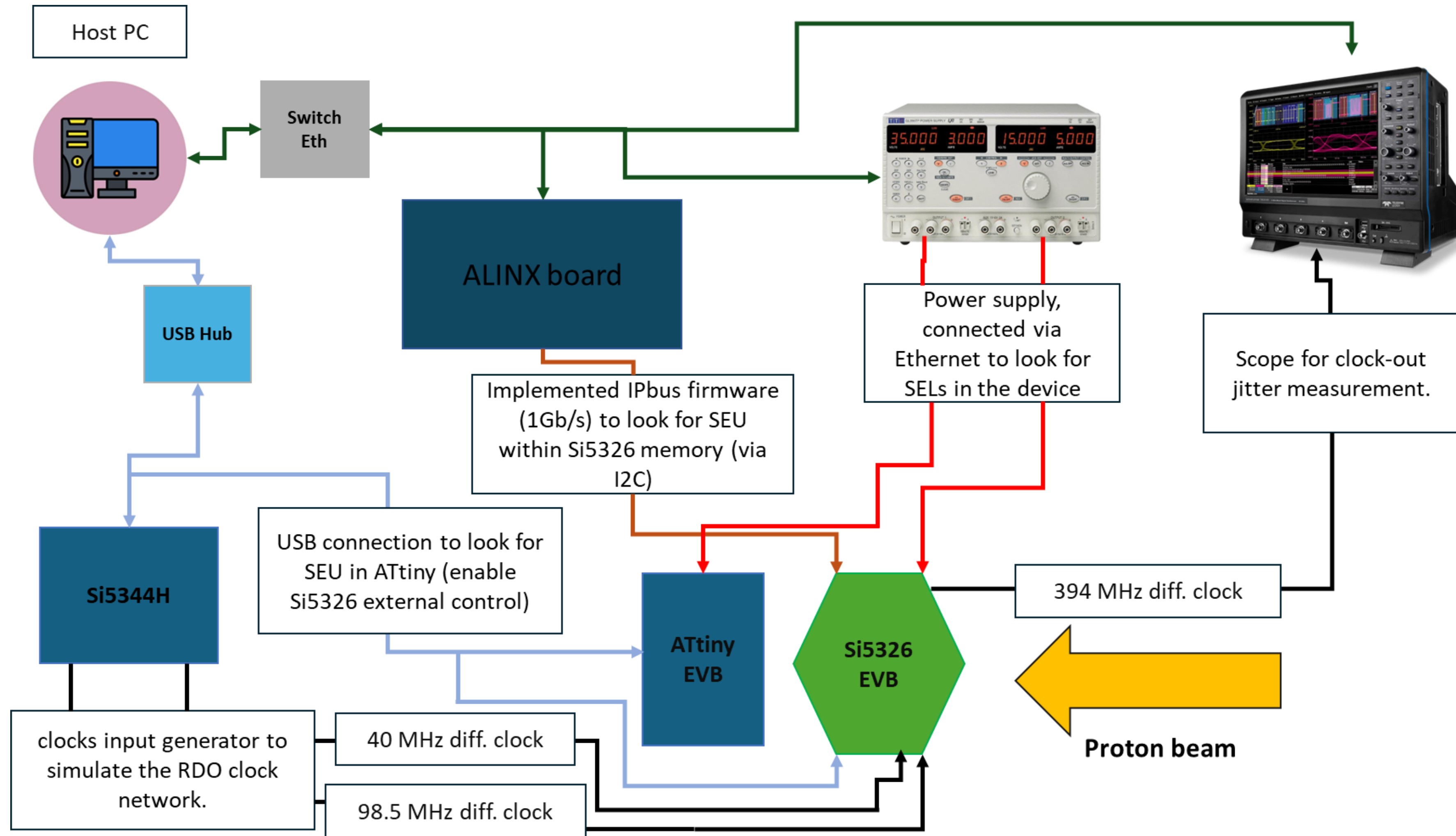
**Detector Box:**

- 208 PDUs

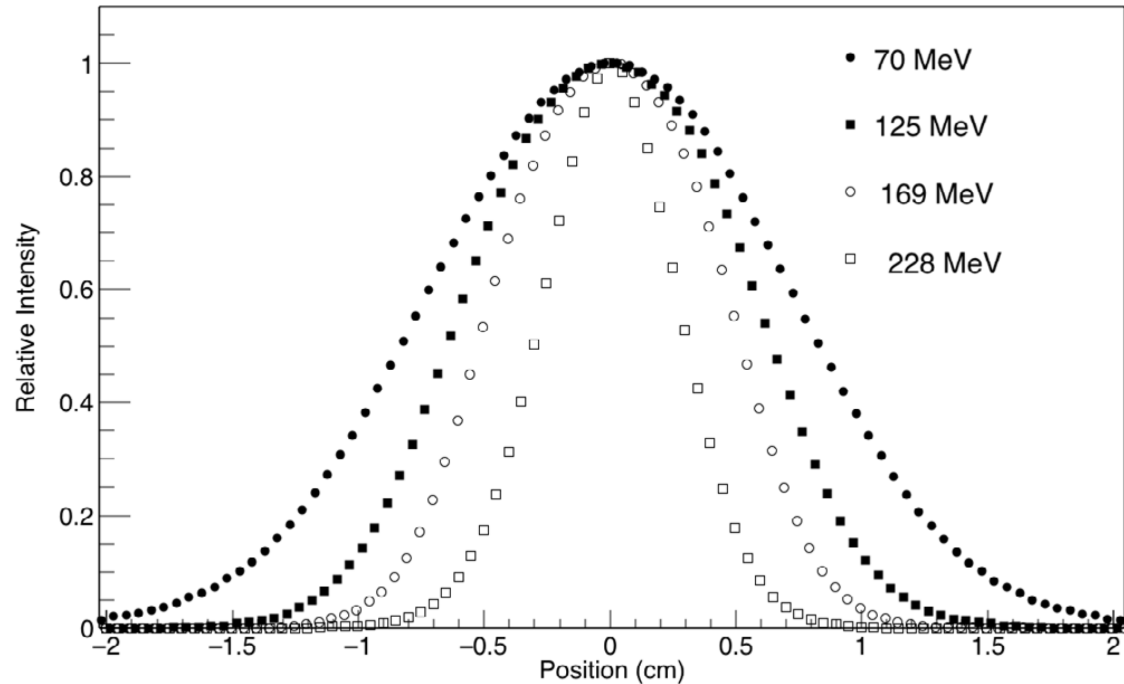
**dRICH detector:**

- 6 sectors for 1248 PDUS

# Si5326 and ATtiny setup



# Devices and TIFPA beam



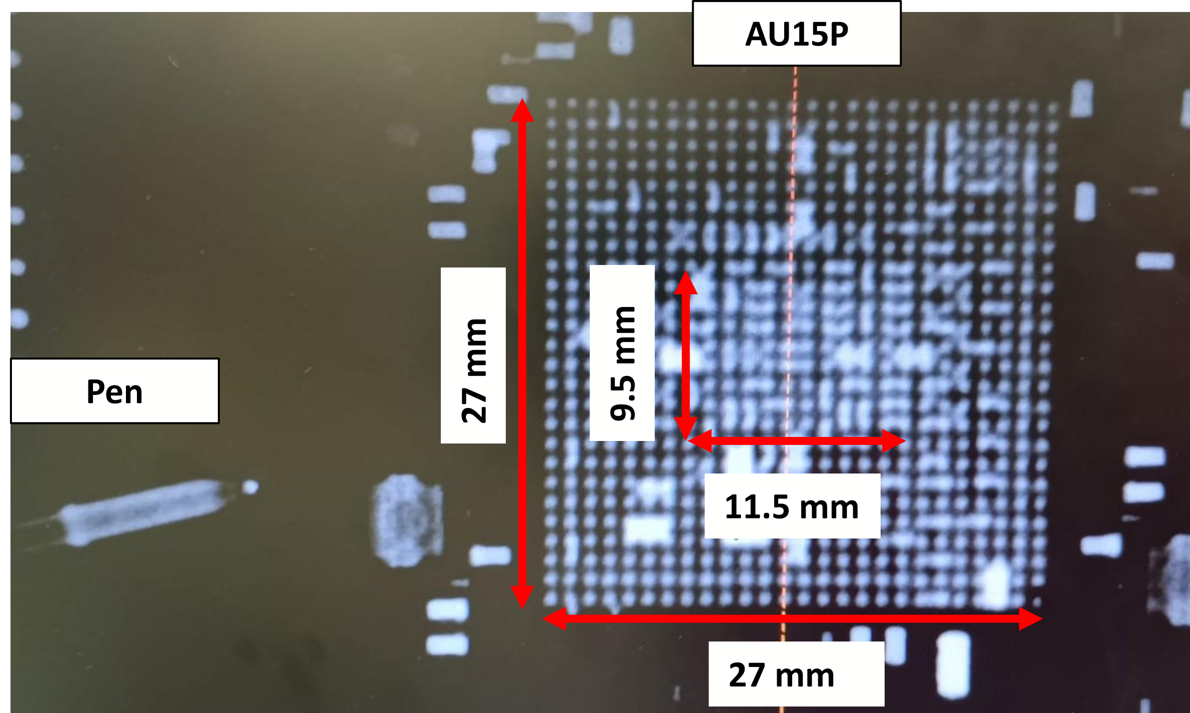

Ref: https://www.sciencedirect.com/science/article/pii/S0168900217306654

| DUT | **Area** ($cm^2$) |
|---|---|
| ATtiny817 | 0.16 |
| Si5326 | 0.36 |
| AU15P Die | $\sim\frac{7.29}{6.67}$=1.09 |

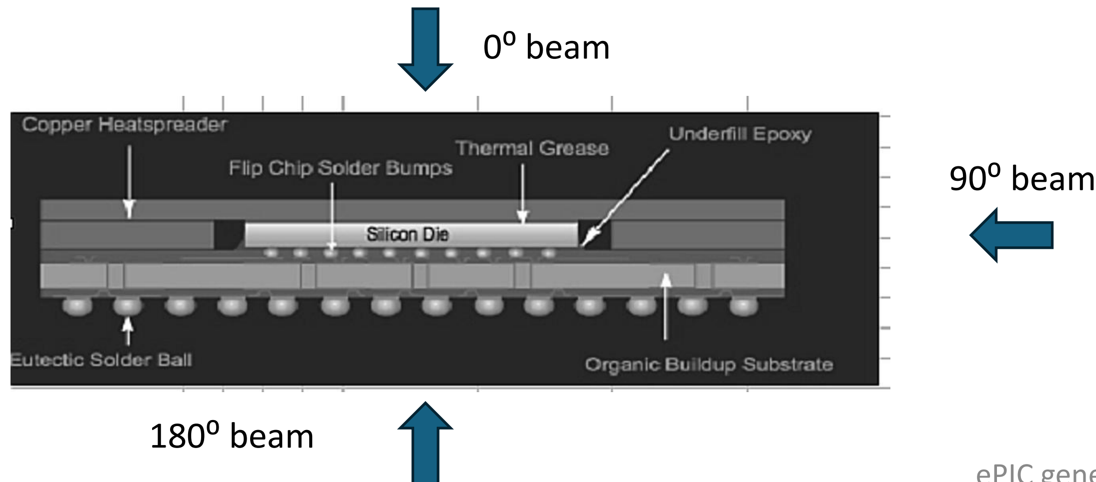
| $E$ (MeV) | $\sigma_x$ (mm) | $\sigma_y$ (mm) | Asymmetry (%) |
|---|---|---|---|
| 70.2 | 6.93 | 6.91 | 0.1 |
| 73.9 | 6.63 | 6.74 | 0.8 |
| 82.7 | 6.28 | 6.41 | 1.0 |
| 90.8 | 6.04 | 6.15 | 0.9 |
| 100.0 | 5.63 | 5.73 | 0.8 |

| Energy [MeV] | Range [$g/cm^2$] | FWHM [mm] | Intensity [p/s] |
|---|---|---|---|
| 70 | 4.1 | 16.2 | 3.83E+06 |
| 74 | 4.5 | 15.9 | - |
| 83 | 5.5 | 15.2 | 7.50E+06 |
| 91 | 6.5 | 14.6 | 9.94E+06 |
| 100 | 7.72 | 13.7 | 1.19E+07 |

# AU15P die and Flip-Chip package effect




0° beam




90° beam

180° beam

The ~**2 factor** for the BRAM SEU cross section can be **explained due to the effect of the FPGA package**? Such an effect was shown for CRAM bits for a Virtex-II FPGA (ref: https://www.researchgate.net/publication/3430143).