

# Trigger and DAQ: Challenges and Opportunities **2026 Update: European Strategy for Particle Physics**

Jun 23–27 2025, Venice Lido

Thea Klæboe Årrestad (ETH Zürich) **Dorothea vom Bruch (CPPM Marseille)** 

FJZURICH

![](_page_0_Picture_5.jpeg)

## **Timelines and synergies**

![](_page_1_Figure_1.jpeg)

## FCC-ee TDAQ challenges

- FCC-ee at Z-pole:
  - highest instantaneous luminosities ever achieved
  - each sub-detector must be capable of read-out at 50 MHz
  - physics rate ~100 kHz, large background rate in innermost layers
- Aim is "trigger-less" design: software -based online selection

#241 #95

![](_page_2_Figure_7.jpeg)

![](_page_2_Figure_9.jpeg)

## FCC-ee TDAQ challenges

- TDAQ requirements highly dependent on detector technology. Potential challenges:
  - TPC cannot read out every 20 ns, hardware-based first filtering might be necessary
  - Noise from increasingly granular
  - Limited by single read-out ASIC data transmission capacity

#241

#### <u>Rate estimates, FCC-ee Z-pole (F. Bedeschi)</u>

Subdetector	Untriggered
Idea vertex	~1 TB/s
Idea DCH	~500 GB/s
Idea DR Calorimeter	~10 TB/s
Idea Luminometer	~20 GB/s
Idea Muon System	~400 MB/s
Total	11.7 TB/s

### **Extreme hit rates in inner layers**

2) Fine granularity, but noisy

![](_page_3_Picture_14.jpeg)

![](_page_3_Picture_15.jpeg)

![](_page_3_Picture_16.jpeg)

## **Read-out of vertex detectors**

- Large background from incoherent pairs creation (mostly forward,  $\bullet$ but substantial fraction within vertex detector acceptance)
- For vertex detector  $\rightarrow$  200 MHz/cm<sup>2</sup> for innermost layer
  - Untriggered: 24.4 Gbit/s / 2-chip module
  - 2.2 Tb/s for Layer 1 (x10 less in Layer 2)
- Current MAPS technology cannot match this rate, all FCC-ee detector concepts foresee MAPS
  - Max readout speed achievable on chip  $\rightarrow$  3.2 6.4 Gbit/s (current ARCADIA)
- Trigger-less readout seems extremely challenging (also: can we even handle this output?)
- Need on-detector compression!

![](_page_4_Figure_10.jpeg)

### See Fabrizio's and Daniela's talk

![](_page_4_Picture_13.jpeg)

![](_page_4_Figure_14.jpeg)

![](_page_4_Picture_15.jpeg)

![](_page_5_Figure_0.jpeg)

- Increased
  - 130→<sup>⊆</sup> 1
    - 250 TI ( x10 ŀ
  - O(1) P
- Full read

![](_page_5_Figure_6.jpeg)

 Tracker readout impossible at full rate (even with) infrastructure constraints)

0101

- To keep trigger rates at acceptable levels, offline algorithms must be migrated to trigger!
  - Track readout+hardware trigger for outer layers (>20 cm)

Abada, A., Abbrescia, M., AbdusSalam, S.S. et al. FCC-hh: The Hadron Collider

![](_page_5_Figure_12.jpeg)

![](_page_5_Figure_13.jpeg)

## How do we address these? **Opportunities for novel designs**

- FCC-ee in streaming trigger less mode faces significant challenges
  - ~ 160 Pb/year for FCC-ee detectors
  - material and power budgets
  - offline-like resolution, requiring real-time calibration and alignment
- FCC-hh can read out calorimeter and muon systems at full rate with tomorrows technology
  - **PU=1,000** scenario
- Must invest in the current and upcoming experiments to develop workflows that harness emerging hardware technologies!

Must reduce data directly at source, aggregate and stream to offline, while staying within tight

Can learn from HL-LHC LHCb & ALICE, EIC ePIC how to do real time physics extraction with

Tracker (probably) not! Will need compression/reconstruction at-source and/or track trigger for a

![](_page_6_Picture_15.jpeg)

![](_page_7_Figure_1.jpeg)

### Example vertex detector inner layer from before (#241 FCC-ee):

![](_page_7_Picture_4.jpeg)

32 bits pixel data in inner layer @ 200 MHz/cm<sup>2</sup>

### 24.4 Gbit/s

## **Two options:**

![](_page_8_Figure_1.jpeg)

## **Two options:**

![](_page_9_Figure_1.jpeg)

## Fast Machine Learning for HEP

ML on specialised hardware (ASICs, FPGAs) could help us address our data processing challenges

HEP tasks not well-represented by industry-driven tools

Have developed our own tools!

![](_page_10_Figure_4.jpeg)

## ML inference at low latency **HEP Tools and Communities**

![](_page_11_Picture_1.jpeg)

![](_page_11_Picture_2.jpeg)

![](_page_11_Picture_3.jpeg)

#### Co-processing kernel (Xilinx accelerators/SoCs)

#### HEP hardware ML libraries:

![](_page_11_Picture_7.jpeg)

#### **ASICs**

![](_page_11_Picture_10.jpeg)

![](_page_11_Picture_11.jpeg)

![](_page_11_Picture_13.jpeg)

![](_page_11_Picture_14.jpeg)

![](_page_12_Figure_0.jpeg)

### 2024: Neural hardware triggers making decisions in LHC experiments!

![](_page_13_Figure_1.jpeg)

![](_page_13_Figure_6.jpeg)

## **Frontend reduction**

![](_page_14_Figure_1.jpeg)

2 solutions: <u>frontend reduction</u> or higher capacity transfer

### ESPPU26 #<u>11</u> #<u>95</u> #<u>247</u> #<u>233</u> #<u>93</u> #<u>211</u> #<u>272</u>

## **Smart Pixels**

https://fastmachinelearning.org/smart-pixels/

- Reduce silicon data via in-pixel intelligence
  - frontend filtering: discard low-pt track data (< 2 GeV)
  - feature extraction: Extract particle position and angle in pixel front-end ASICs from charge in single pixel layer
- Bandwidth savings of 57-75%!

![](_page_15_Picture_8.jpeg)

![](_page_15_Picture_9.jpeg)

![](_page_15_Picture_12.jpeg)

![](_page_15_Figure_13.jpeg)

## **Reconfigurable logic in ASIC design The Embedded FPGA framework**

- Pathway to implementing ML "at source"
  - Fully reconfigurable logic on detector frontend
- Open source (FABulous, OpenFPGA)
  - potential to apply to variety of subsystems/ fields (SuperKEKB, FCC-ee, DUNE, freeelectron lasers)

#### ESPPU26 #95Eol

![](_page_16_Picture_8.jpeg)

![](_page_16_Picture_9.jpeg)

![](_page_16_Picture_11.jpeg)

![](_page_16_Picture_12.jpeg)

## **ML compression: Calorimeter data concentrator**

10,000 ECONs with ML inside going live in HL-LHC

![](_page_17_Figure_2.jpeg)

Di Guglielmo et Al, IEEE TNS 68.8 (2021)

![](_page_17_Picture_5.jpeg)

![](_page_18_Figure_1.jpeg)

## Wireless data transmission **Reducing material budget for detector readout**

- Increase Gbps w/o increasing material
- Send single signal to several receivers, saves cabling
- Cost reduction, simplified installation/ repair, reduction in dead material
  - Especially important for future tracking detectors

Few Gbps possible with 802.11ac/ad WiFi!

### <u>Wirel</u>

![](_page_19_Figure_7.jpeg)

![](_page_19_Picture_9.jpeg)

## Intelligent back-ends

![](_page_20_Figure_1.jpeg)

![](_page_20_Picture_2.jpeg)

## **Real-time tracking**

- - reduce rate by x10 by filtering low momentum hits
  - final track candidates and determine track parameters
  - Track quality with BDT implemented with  $\Lambda$ Conifer

![](_page_21_Figure_5.jpeg)

#### C. Brown, Vertex2023

• HL-LHC CMS will read out tracks with  $p_T > 2$  GeV and run L1 track reconstruction

• Offline like reconstruction: track seeding, building and Kalman Filter to identify

![](_page_21_Figure_11.jpeg)

![](_page_21_Picture_13.jpeg)

# Hardware jet building and flavour tagging

![](_page_22_Figure_1.jpeg)

### HL-LHC CMS will run with **FPGA** track finding, particle flow, jet clustering and flavour tagging in $< 12 \, \mu s$

<u>Object tagging for Phase-2 CMS</u>

![](_page_22_Picture_5.jpeg)

![](_page_22_Picture_6.jpeg)

## **Real-time track triggers** BELLE-II

- •Belle-2 uses neural track hardware trigger for reconstruction of vertex, and azimuthal and polar angles of single particle track
- •ML for GNN-based offline tracking
  - •Work ongoing on bringing this to the hardware trigger

#### arxiv:411.13596

![](_page_23_Figure_5.jpeg)

![](_page_23_Figure_6.jpeg)

# **Trigger-less design: LHCb Run-3**

- Run 3 event selection entirely in software, heterogeneous platform FPGA-based DAQ cards (low-level bit manipulations)

  - high-speed dedicated network cards (memory ops for transfer)
  - GPUs for data processing (large-scale parallel problems)
- Lessons learned in Run3:
  - Expertise in Low-level network simulations
  - Architecture that supports fast adaptation to emerging tech
  - Full read-out, track reconstruction and lepton PID at 30 MHz
- Run-4 R&D:
  - Early track reconstruction on FPGA boards (RETINA)
  - Investigating emerging processors as GPU alternative (ALLEN)

Aaij, R., Albrecht, J., Belous, M. et al. Allen: A High-Level Trigger on GPUs for LHCb.

#### ESPPU26 #127 #148

![](_page_24_Figure_14.jpeg)

![](_page_24_Picture_17.jpeg)

## Heterogeneous TDAQ architecture

- ALICE, CMS & LHCb deploy heterogeneous software triggers with CPU and GPU architectures since LHC-Run 3
  - independently developed software frameworks, integrated with experiment software
  - Collaboration crucial to share common tools and experience with emerging processors

### ESPPU26 #127 #148 #64

![](_page_25_Figure_5.jpeg)

![](_page_25_Figure_6.jpeg)

### **Real-time alignment & calibration Reaching the FCC-ee precision needs**

- High quality alignment & calibration crucial to minimise systematic uncertainties at future colliders and experiments
- Will need to cope with
  - high channel counts
  - timing-based reconstruction for 4D alignment
  - test case in ePIC and LHCb Run5
- Need fast calibration (limited buffering)
  - heterogeneous software frameworks developed for HLTs and advanced distributed computing techniques

#### ESPPU26 <u>#127</u> <u>#17</u>

LHCb's real-time alignment & calibration system deployed in 2018

![](_page_26_Figure_10.jpeg)

((~7min),(~12min),(~3h),(~2h)) - time needed for both data accumulation and running the task

https://iopscience.iop.org/article/10.1088/1748-0221/14/04/P04013

![](_page_26_Figure_13.jpeg)

![](_page_26_Figure_14.jpeg)

### **DRD7: R&D Collaboration on Electronics and On-Detector Processing**

![](_page_27_Picture_1.jpeg)

- **WP7.1**: Data density and power efficiency
- WP7.2: Intelligence on the detector
- WP7.3: 4D and 5D techniques
- **WP7.4**: Extreme environments
- **WP7.5**: Backend systems and COTS components
- **WP7.6**: Complex imaging ASICs and technologies
- WG7.7: Tools and Technologies
- Extend to include:
- •Real-time inference on specialized hardware.
- Heterogeneous real-time software tools
- in close collaboration with the Fast Machine Learning Foundation, CERN NGT and EuCAIF AI-RDs

![](_page_27_Picture_15.jpeg)

![](_page_27_Figure_16.jpeg)

![](_page_27_Picture_17.jpeg)

### **AI R&D collaborations EuCAIF** proposal for scalable, robust AI through cross-domain collaboration

- Al for Data Processing: Front-end electronics, trigger
- calibration, system monitoring.
- Al for Detector Optimization: Differentiable programming, reinforcement learning to maximize detector performance
- Al for Event Reconstruction: Tracking, calorimetry, end-to-end foundation models.

# Al for Detector and Accelerator Control: Accelerator performance,

![](_page_28_Picture_10.jpeg)

## Conclusion

#### Exciting challenges ahead to make sure TDAQ is not the precision bottleneck

- read-out of increasingly granular detectors within tight material, power budgets
- high fidelity on-detector compression for high-precision triggers or to reduce steaming data load for processing and storage
- Al/ML tools are essential to meeting these challenges
  - Must develop and maintain versatile heterogeneous frameworks and platforms
- Cross-experiment organisational support for frontend/backend ML developments represented in DRD collaborations/AI-RDs

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![](_page_29_Figure_9.jpeg)

![](_page_29_Figure_10.jpeg)