European Strategy for Particle Physics

PARALLEL 6 / **DETECTOR TECHNOLOGIES**

ASICs
Lessons Learnt & Perspectives

Frank Simon, KIT IPE

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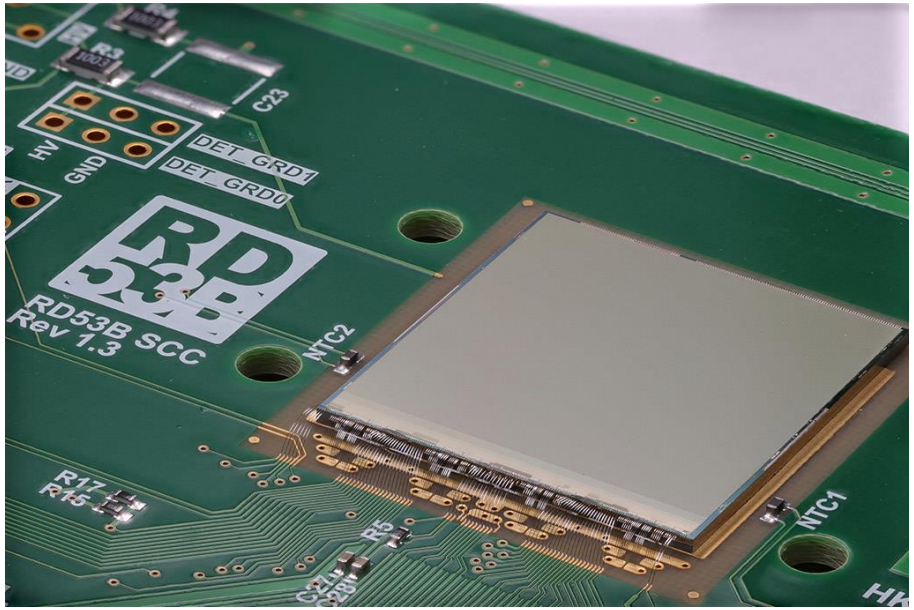
Setting the Stage

01

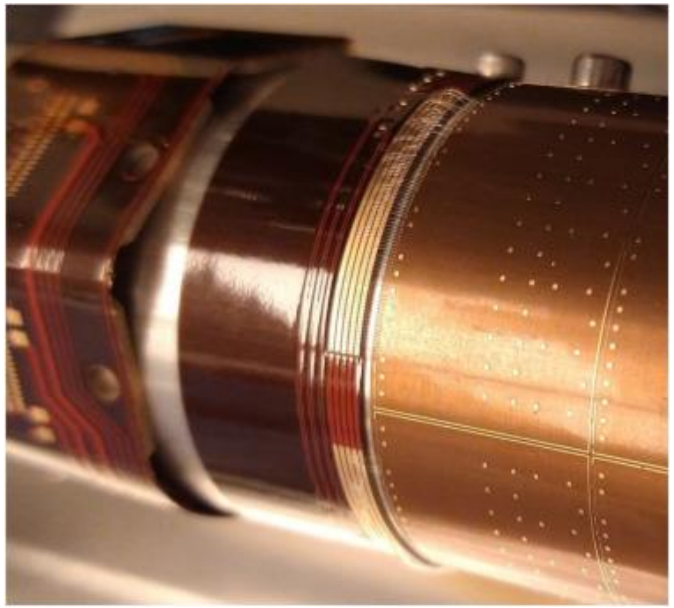
ASICs in High Energy Physics
Setting the Stage

Application-**S**pecific **I**ntegrated **C**ircuits are key elements of modern HEP detectors.
Two “classes” of applications:

Readout / on-detector data processing



Monolithic CMOS sensors



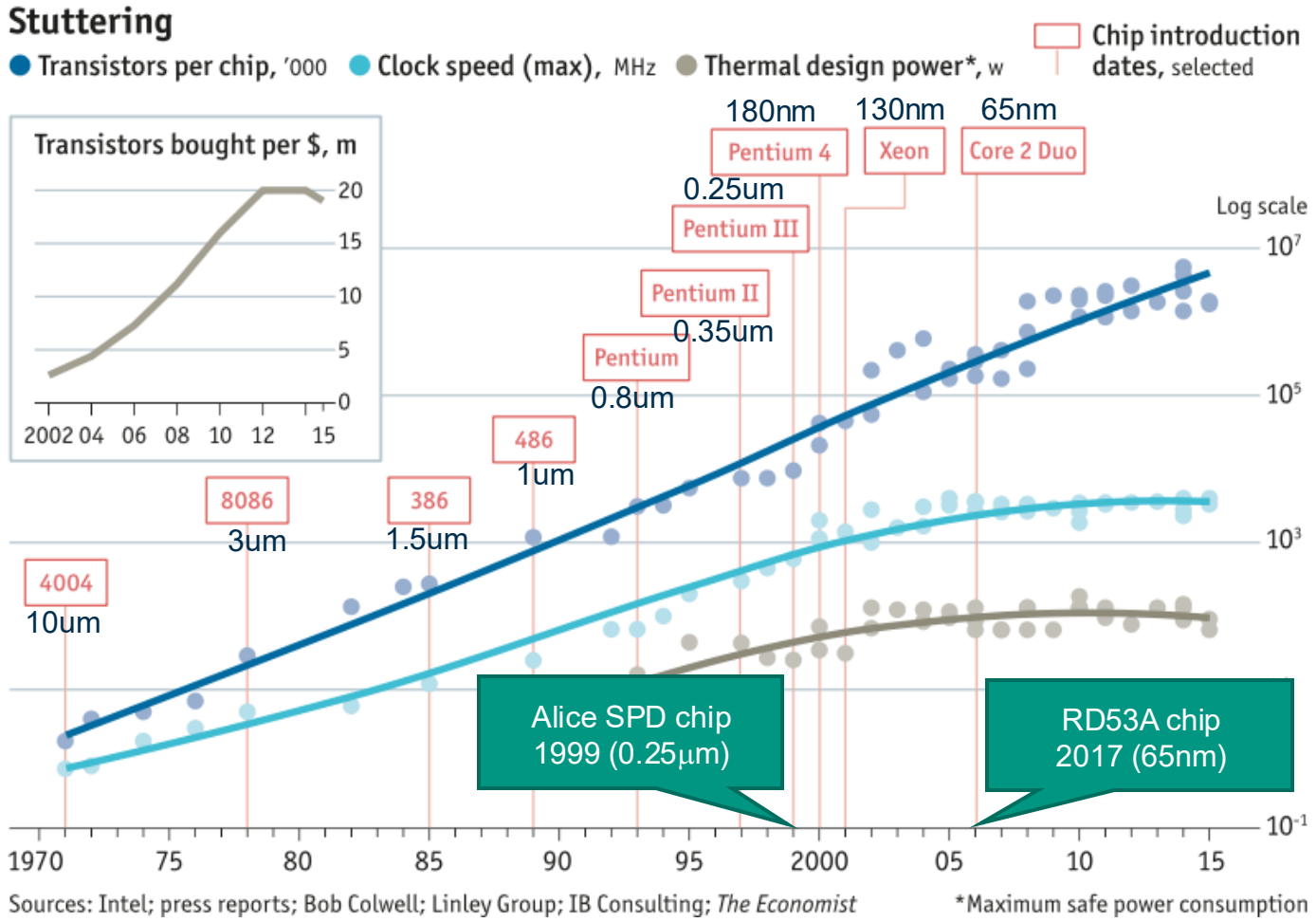
Perspectives on Technology Evolution
Setting the Stage

Modern microelectronics technology is evolving rapidly – driven by industry.

- Development in HEP has failed to keep up with this evolution.
  - In the late 1990ies: Using latest technologies.
  - Today: ~ 10 -- 15 years behind in technology adoption. A contributing factor: qualification for HEP time and resource intensive.

Selected consequences:

- Cannot fully exploit potential of modern FPGAs (used in back end) in terms of IO speed, advanced functionalities.
- Technology support at foundries a risk. Requires selection of long-lived nodes.

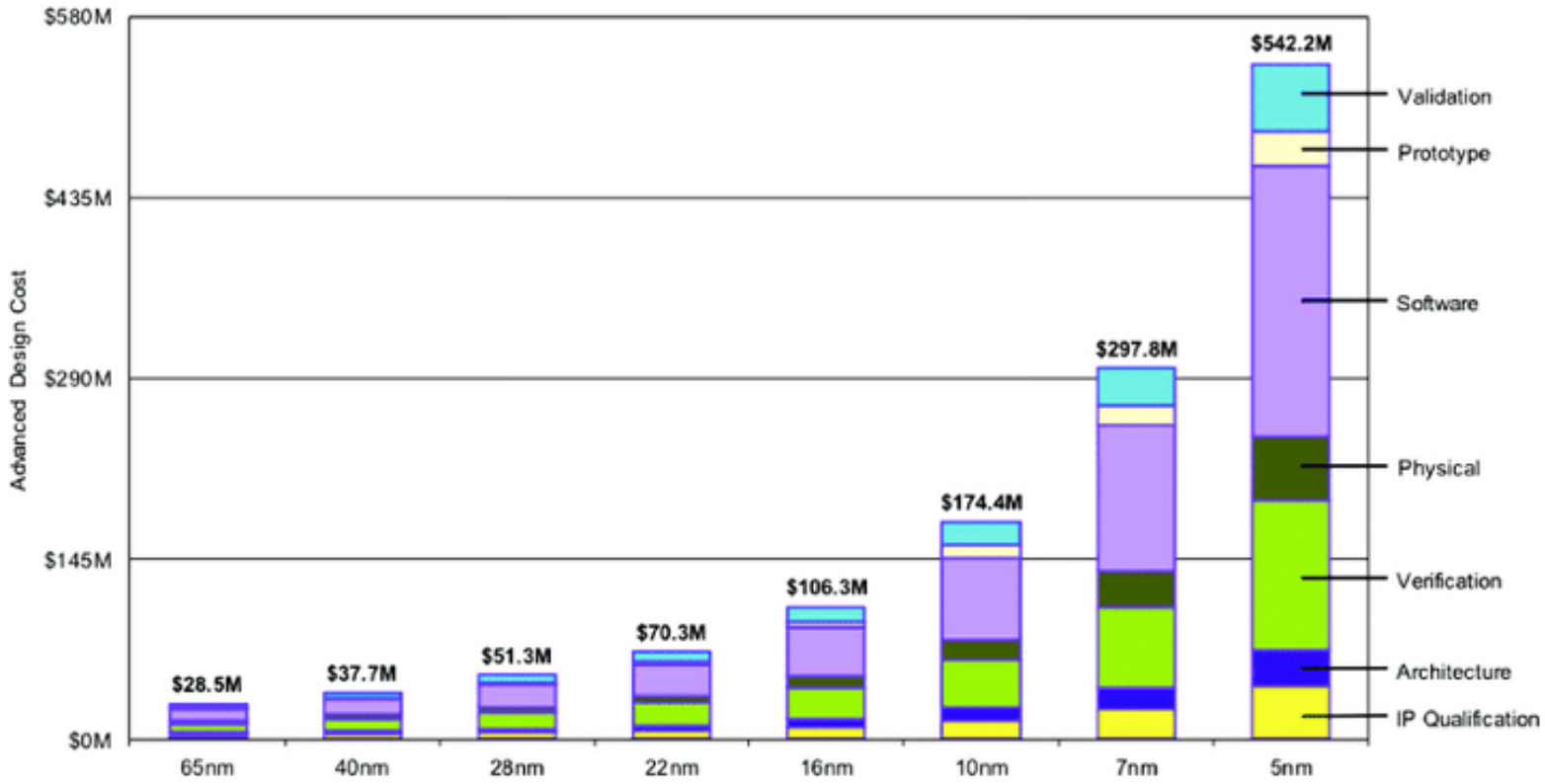


taken from M. Campbell, SPC 2019

Perspectives on Technology Evolution
Setting the Stage

Adopting modern technologies comes with significant hurdles:

- Increasing cost and complexity with smaller technology nodes:
  - development effort and tools
  - one-off production cost (masks)
- Specific HEP requirements
  - in particular: significant radiation hardness
  - long-term availability of process to support our long development and application cycles



taken from Semiconductor Engineering, 2023 / IBS 2018

Lessons learnt

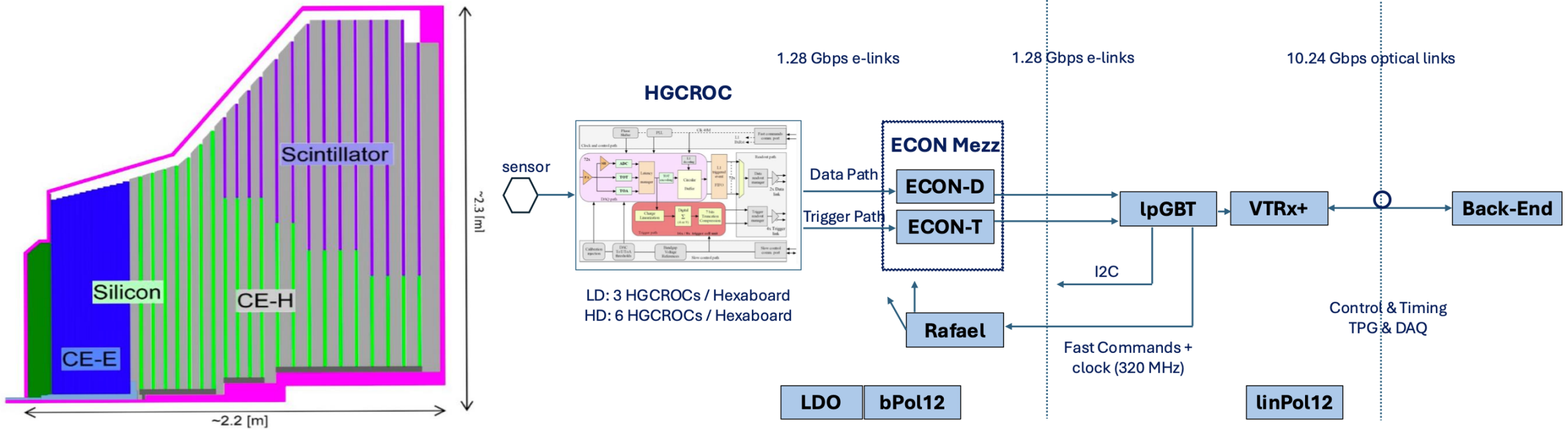
02

The Phase II Challenge
Overview

ASICs are the heart of the electronics system of all Phase II detectors

- In total ca. 50 ASICs: Common, ATLAS, CMS – with varying complexity.
  All require radiation tolerance and high speed.
  - Triplication in digital circuits, use of radiation-hard design techniques

One example: The CMS HGCAL

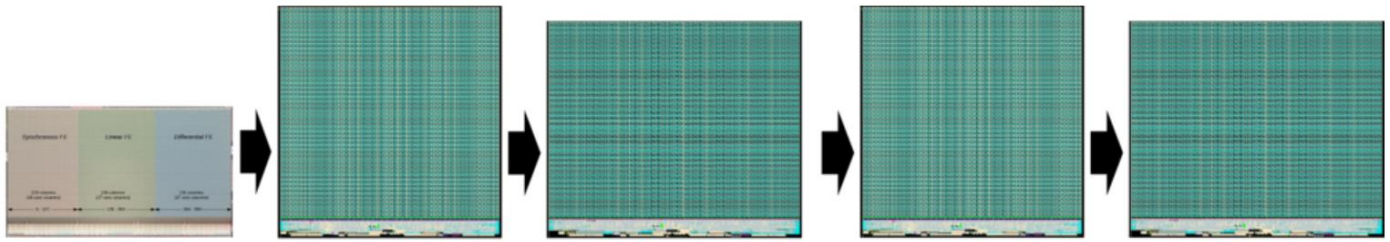


The Phase II Challenge
Pixel Readout as Example

Arguably most complex ASIC project of the Phase II upgrades – joint ATLAS & CMS development, organized in the RD53 collaboration

- mixed-signal ASIC in 65 nm technology, high rate, high radiation tolerance.
- Slight variations for ATLAS and CMS – different front-ends.
- A collaboration of 24 institutes, ~ 100 involved people over 10 years.

Collaboration formed 2013 – originally foreseen for a 3 year R&D program. Collaboration ended in 2024.



Parameter	Value (CMS/ATLAS)
Technology	65 nm CMOS
Max. hit rate	3.0 GHz/cm^2
Trigger rate	750 kHz / 1 MHz
Trigger latency	12.5 µs
Pixel size (chip)	50 x 50 µm^2
Pixel size (sensor)	50 x 50 µm^2 or 25 x 100 µm^2
Pixel array	432 x 336 pixels / 400 x 384 pixels
Chip dimensions	21.6 x 18.6 mm^2 / 20 x 21 mm^2
Detector capacitance	< 100 fF (200fF for edge pixels)
Detector leakage	< 10 nA (20nA for edge pixels)
Min. threshold	1000 e-
Threshold spread	< 100 e- RMS
Calibration pulse resolution	10 e-
Noise	< 150 e- RMS, with sensor
Charge measurement	4 bit TOT, max 1% deadtime at 3.0 GHz/cm^2
Radiation tolerance	1 Grad over 10 years at -15°C
SEE tolerance	SEU rate, innermost: ~100Hz/chip
Power	< 1W/cm^2, Serial powering
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Temperature range	-40°C ÷ 40°C (Nominal operation=-20°C ÷ -10°C)

Delivering Phase II ASICs
A Reviewers Perspective: Challenges encountered

Now on the home stretch: Designs (almost) finished, many produced or in production.

But:

- At the point of the TDR effort, the start of HL-LHC was foreseen for mid-2026.
  Today, it is 4 years later.
- Almost all more complex ASICs required one or more prototyping iteration more than foreseen and were delayed by several years compared to the original planning. In some cases, versions used in production have some minor bugs.

Typical issues:

- Design bugs that render ASIC inoperable in specific conditions.
- Use of a library item that turned out to be buggy or poorly documented.
- Subtle mistakes that result in problems on the percent level (for example randomly on startup).
- Issues that appear under certain radiation and temperature conditions.
- ...

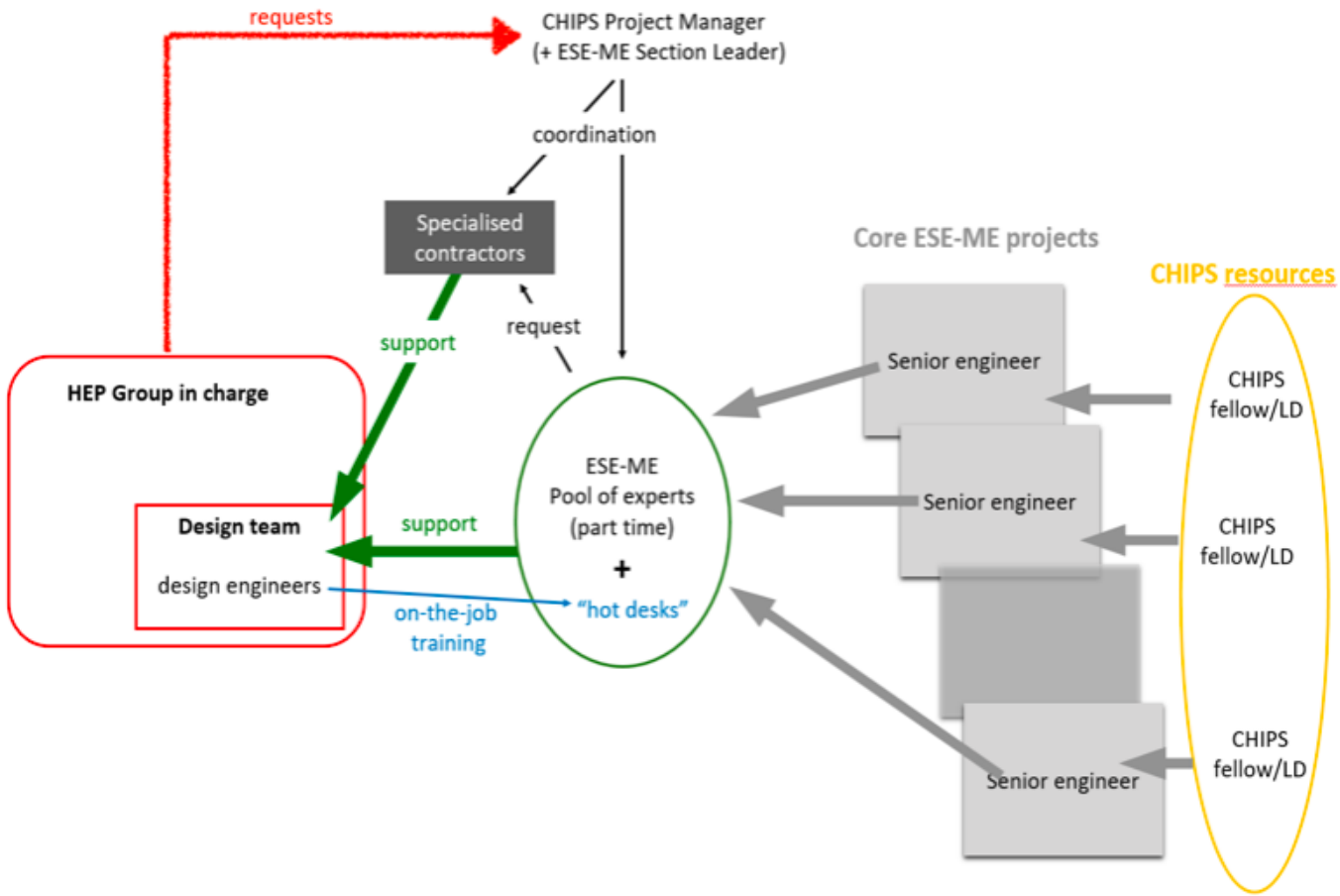
Delivering Phase II ASICs
Measures taken

A main driver of the delays: Lack of critical mass of experienced personnel

- ASIC engineering experts, in particular with experience in complex projects using the full tool sets incl. modern verification tools and workflows
- Loss of personnel in participating institutes: Contracts running out, shift to other projects, changing academic interests, ...

CERN's response: The **CERN-HEP IC design Platform and Services (CHIPS)** initiative.

- Began operations in 2020, following discussions in the LHCC, SPC.
- Recently extended.
- Has been instrumental to bring Phase II ASICs to the stage where they no longer drive the critical path of the upgrades



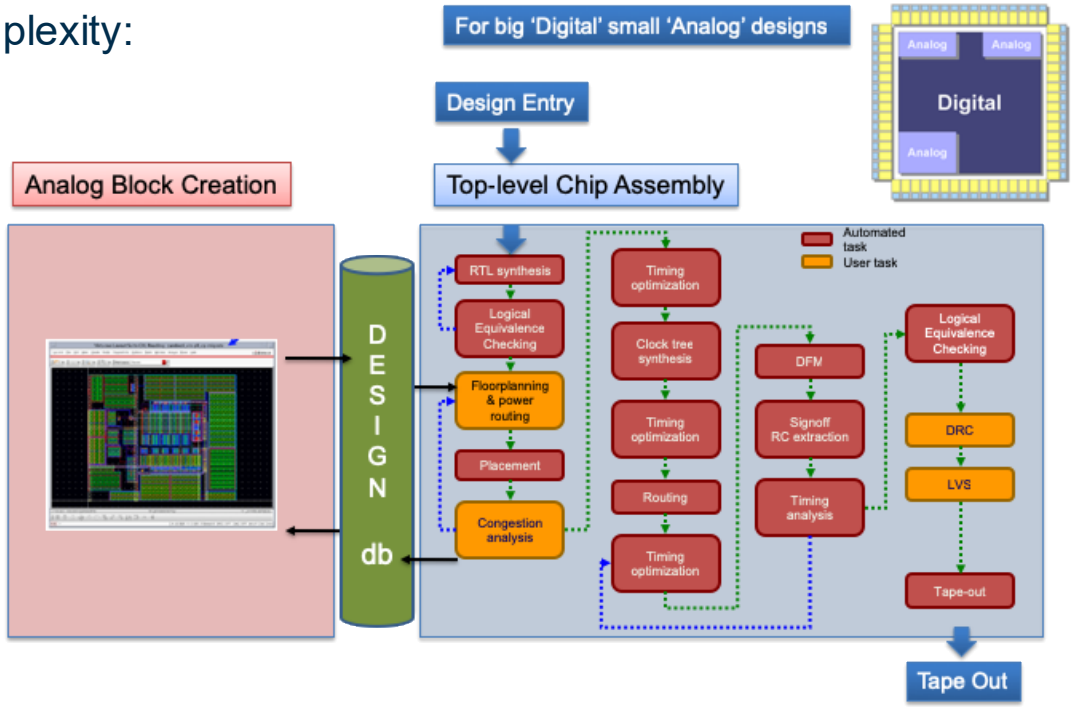
Limits of the HEP Model
A personal Perspective – and Lessons learned

A change in design paradigm for mixed-signal ASICs with increasing complexity:
From analog-on-top to digital-on-top. Consequences:

- System-on-chip design, requiring significantly more simulation and verification in design process. Different skill set than “classical” analog design, and generally more resources.
  But: strong mitigation of risk if followed consistently

Common HEP approach with small groups at universities hits limits:

- Conflict of academic interest (focus on designing new features) with project needs (adherence to schedule, mitigation or risks)
- Reliance on students: Thesis needs satisfied with implementation of new features, project needs with bug fixing. New features frequently turn into the next bug.
- Desire (and external pressure) for ownership – several solutions for similar problems – fragmentation of overall effort in the community, duplication.
- Changing personnel driven by short-term contracts.



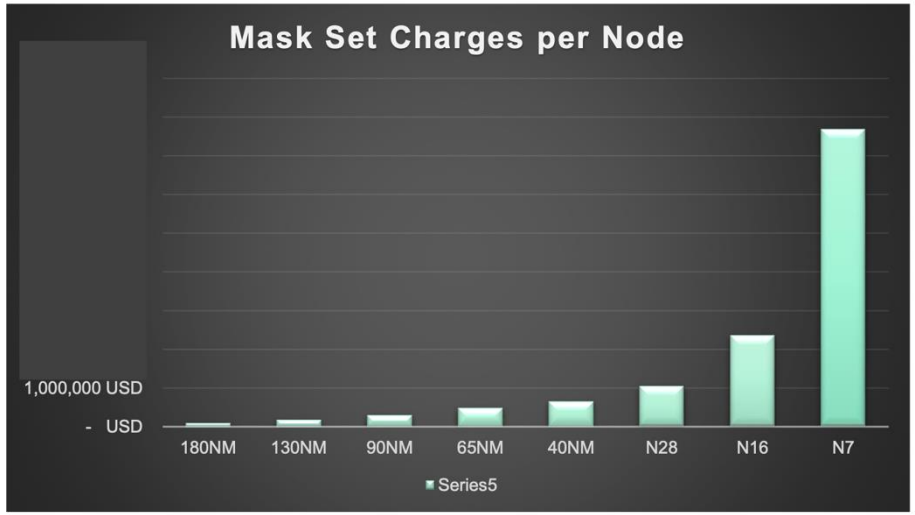
The Path forward

03

Common Submissions, Tools and Frameworks
Central Elements for ASIC Development in the Community

Pooling resources – coordinating common submissions:

- Offset cost in most technologies prohibitively high for R&D projects: Multi-project wafers to enable R&D projects.
  - Requires coordination and advance planning, development of roadmap for future submissions.



Paul Malisse, TWEPP '23

Access to professional state-of-the-art design tools, software licences, PDKs

- Europractice as low-cost framework for purely academic development
- Commercial licenses a to enable other activities

Access to foundries, supporting legal framework

- CERN foundry access service

- Establish Commercial Contracts with silicon vendors
- Establish NDAs that allow for collaborative work. Example: HEP-specific 3-way NDA for 28 nm technology
- Organize prototyping Multi Project Wafer runs, for sharing fabrication costs
- Coordinate silicon fabrication: MPW, Engineering & Production runs

Bringing Experts together
Hubs for ASIC Development: DRD7 WG 7.7

Concept being developed in the DRD7 Collaboration to address the challenges of ASIC development in HEP.
Main motivation:

- Effective support of technologies and tools for the HEP community is both essential and demanding.
- Models adopted in the past might not allow to keep pace with current and future technologies and requirements.

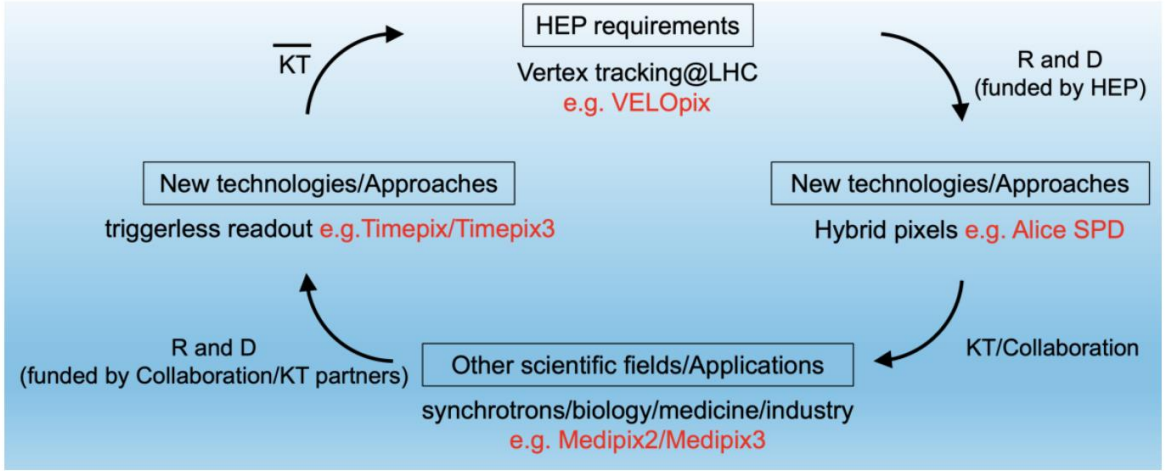
Key Goals of a hub-based structure:

- Establish and maintain access to cutting-edge technologies and EDA software tools through regional collaboration.
- Ensure a professional approach to prototyping and fabrication cycles, including best practices in design, verification, and foundry submissions.
- Facilitate collaborative work across distributed teams and enable IP block sharing.
- Implement rigorous project review and submission processes to manage risks and control changes.

First step:
A task force has been established to discuss new cooperative models. Process driven by lessons learned from LHC and HL-LHC ASIC projects – recognizing the need for enhanced design and verification support in future ASIC projects.

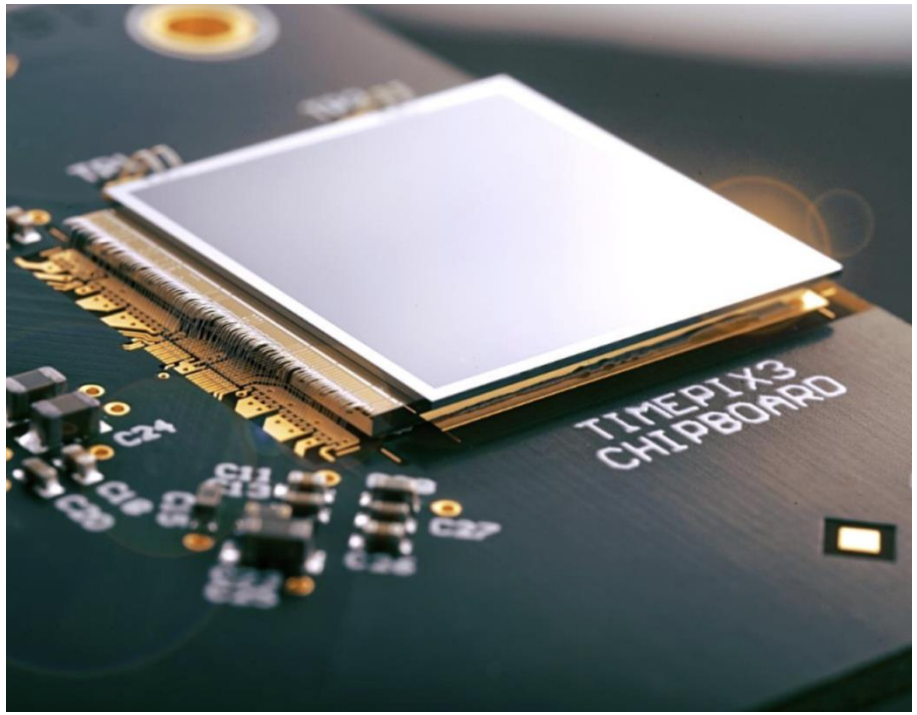
MediPix/TimePix
A Model for Experiment-Agnostic Development

An example of an HEP-driven development that evolved into much broader applications



- Further generalizing activities can add additional dynamics, new ways of funding developments: Fewer developments with higher volumes – involving communities well outside of HEP.

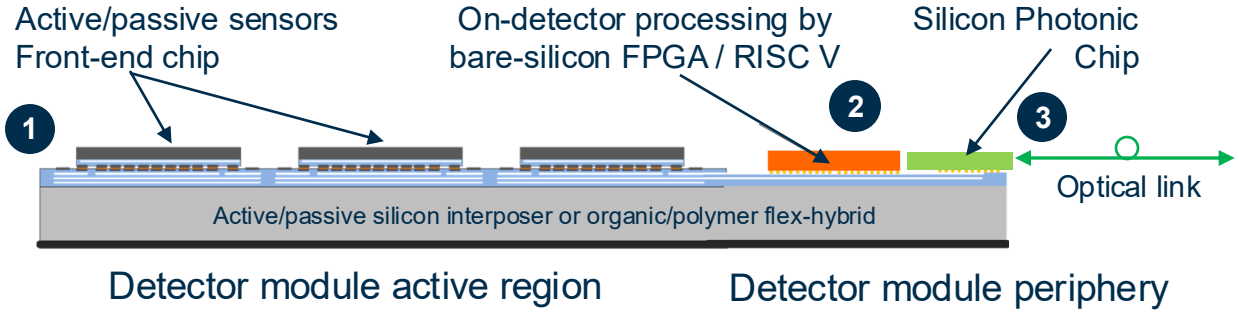
ESPPU input #161: “Call for a new approach to detector developments involving microelectronics”



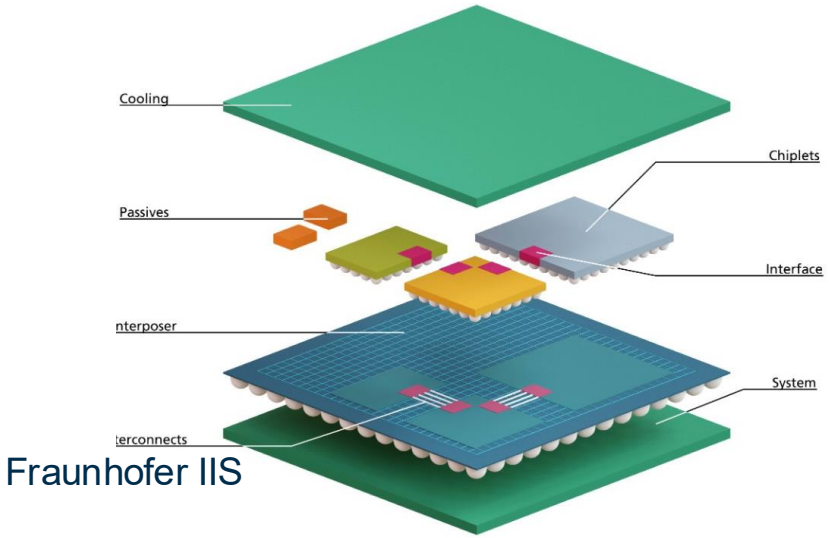
Interconnect & Packaging Technologies
Increasing Integration, exploiting different Technologies

It's not just silicon: Packaging and interconnect technologies. Modern technologies such as through-silicon vias, redistribution layers, ... extend possibilities further.

- Turning chips into systems:
  - Today: connections with sensors
  - Next: Full integration of data transmission (silicon photonics), programmable on-detector intelligence ("eFPGAs")



- Chiplet technology: Combining small "chiplets" into larger ASICs – each potentially produced in a different technologies, optimised for requirements, cost and availability, increasing flexibility in re-use of existing designs.



Fraunhofer IIS

Personnel: Development, Engineering, Testing...
The Basis of Success

A highly specialized field of electronics – driven by industry, growing rapidly.

- Finding and retaining expert personnel is a massive challenge: Cannot compete in terms of salary
- Need a spectrum of expertise and type of personnel
  - Design / IP development
  - Verification
  - Testing
  - ...

To address the needs of the field, we need to maintain, and in some cases build, an environment that attracts top experts

- Requires career paths fitting to the sub-field, recognition of technical contributions, ...

Conclusions

04

Conclusions

- ASICs are essential elements of HEP detector systems
  - No detectors without them: all throughout the readout and control chain.
  - Sensors.
  - Intelligence on the front-end.
- The field has fallen behind industry in terms of technology nodes, driven by increasing cost and complexity.
- ASICs were a major factor in Phase II delays: Development model of HEP hitting its limits.

As a community, we need to rethink and change our approach to ASICs.
There is scope for disruptive functionalities revolutionizing detectors
- but only if the community is able to reorganize.

- Need to adopt new strategies to keep up / catch up:
  - Modern approach for design and verification.
  - Common designs, coordination and collaboration across experiments, and across fields:
    Forming new partnerships.
- Personnel is essential: Highly specialized (and sought-after) skills required:
  Need an inspiring environment, recognition and attractive career paths
  – and appropriate structures in the community.