Semiconductor Technologies for Vertex Detectors, Silicon Trackers and Timing

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Challenges for an HET e^+e^- collider

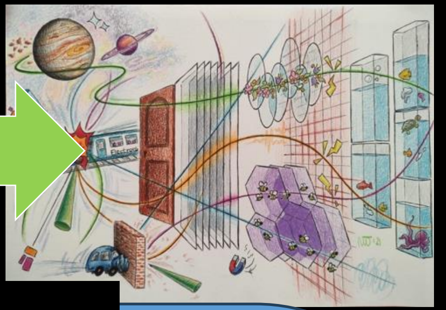
- Vertex Detectors
  - **Resolution** (single point: 3 μm, time: 5 ns)
  - **Hit rate/density** (up to 200 MHz/cm^2)
  - **Power** consumption (50 mW/cm^2)
  - **Radiation** hardness (TID: 100 kGy, NIEL: few 10^{13}/ cm^2)
  - **Material budget** (0.15%- 0.3% of a radiation length per layer)
- Trackers
  - Small number of O(10 μm) silicon detectors layers
  - gaseous detectors
- TOF wrappers to provide PID
- High granularity calorimeters

- Goals lead to conflicting requirements
  - Higher spatial resolution/ Smaller pixels / More channels/ More power
  - Better timing resolution/more power
  - Power consumption/cooling
- Ultimate detector performance must address system considerations

	ITS3	ALICE 3 VTX	ALICE 3 TRK	ePIC	FCC-ee
Single-point res. (μm)	5	2.5	10	5	3
Time res. (ns RMS)	2000	100	100	2000	20
In-pixel hit rate (Hz)	54	96	42		few 100
Fake-hit rate (/pixel/event)	10^{-7}	10^{-7}	10^{-7}		
Power cons. (mW / cm^2)	35	70	20	<40	50
Hit density (MHz/cm^2)	8.5	96	0.6		200
NIEL (1 MeV n_{eq}/cm^2)	$4 \cdot 10^{12}$	$1 \cdot 10^{16}$	$2 \cdot 10^{14}$	few 10^{12}	10^{14} (/year)
TID (Mrad)	0.3	300	5	few 0.1	10 (/year)
Material budget (X_0/layer)	0.09%	0.1%	1%	0.05%	˜0.3%
Pixel size (μm)	20	10	50	20	15-20

Future hadron colliders will also require unprecedented levels of radiation hardness

ECFA detector roadmap



Implementation of the ECFA roadmap for Solid State Detectors

DRDT3.1: Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors

DRDT3.2: Develop solid state sensors with 4D-capabilities for tracking and calorimetry

DRDT3.3. Extend capabilities of solid state sensors to operate at extreme fluences

DRDT3.4. Develop full 3D-interconnection technologies for solid state devices in particle physics.

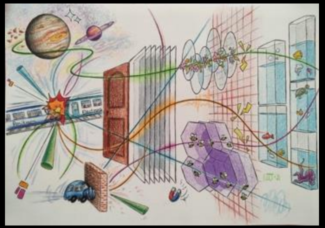
DRD3

- **WG1:** Monolithic CMOS Sensors
- **WG2:** Sensors for Tracking & Calorimetry
- **WG3:** Radiation damage & extreme fluences
- **WG6:** Non-silicon based detectors
- WG7: Interconnect and device fabrication
- **WG4:** Simulation
- **WG5:** Characterization techniques, facilities
- **WG8:** Dissemination and outreach

https://indico.cern.ch/event/1214410/

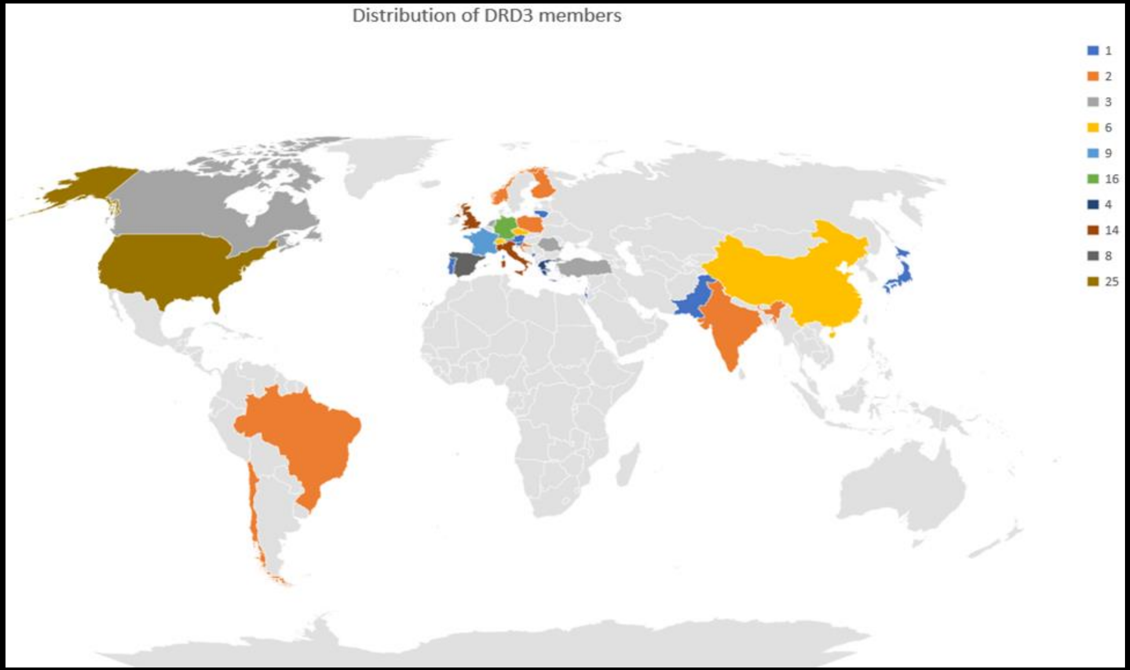
DRD3

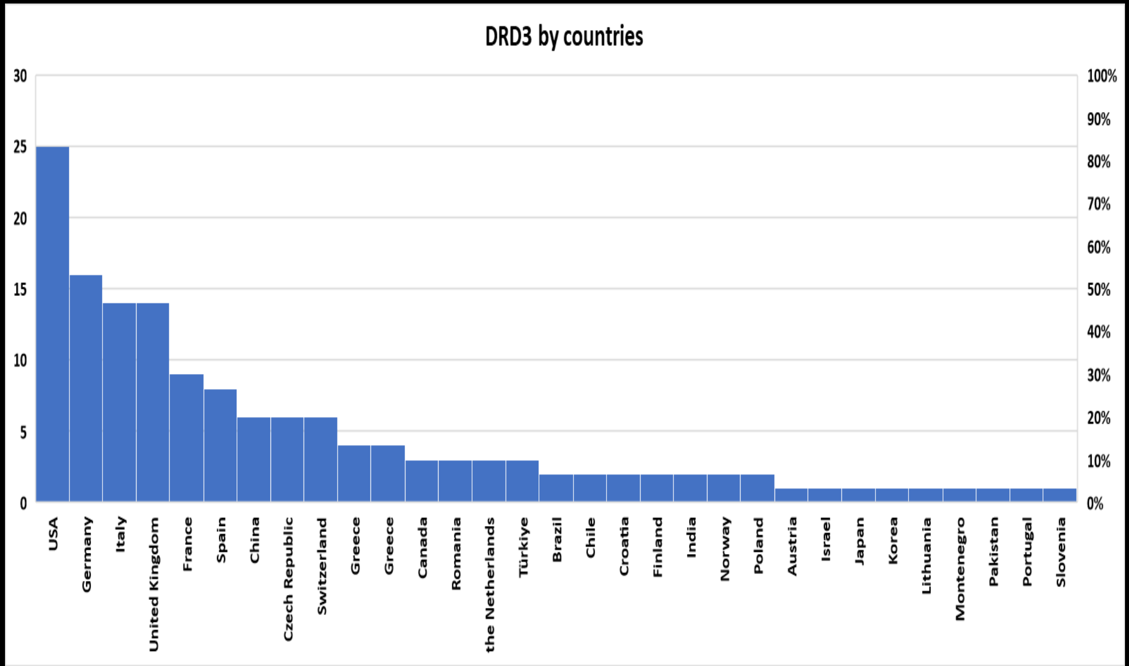
DRD3



- Huge: 145 institutions / 700++ people in the community e-group
- Highly International

Large interests from the community:
- Integration of RD39,RD42, RD48,RD50 groups
- But even larger number of institutions from outside these communities

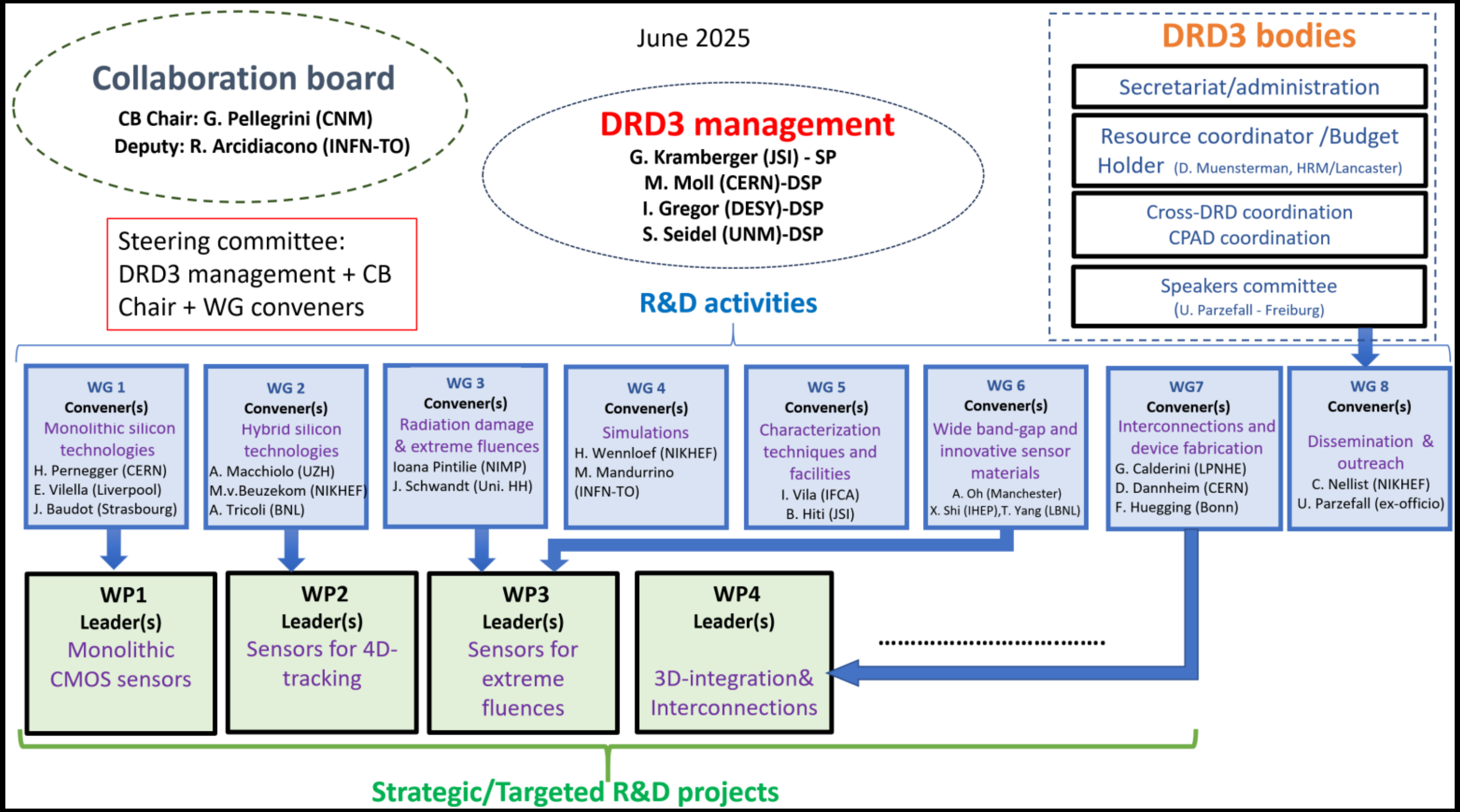




- Coordinated efforts also in the US and other countries
- Many inputs for the ESPPU process: #17, #32, #68, #70, #75, #78, #94, #95, #101, #102, #131, #145, #148, #157, #211, #245

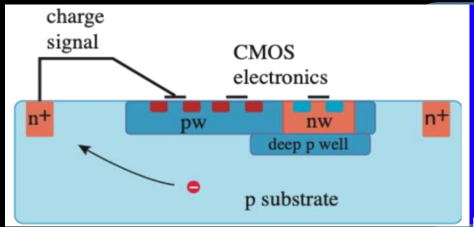
DRD3 collaboration

https://indico.cern.ch/category/17387/

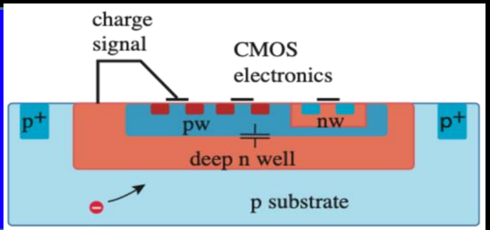


- <u>The third DRD3 week</u> took place at NIKHEF June 2-6:
  - Extensive scientific discussions held across numerous Working Groups (WGs)
  - First set of Work Package (WP) projects prepared and ready for CB approval
  - Several new institutes have joined the collaboration
  - R&D efforts continue actively, despite significant commitments to HL-LHC
  - Many new measurements presented and discussed

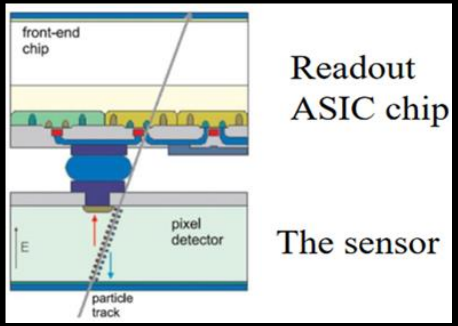
R&D Path for Solid State Detectors



Monolithic devices (all in one) – CMOS 55-180 nm processes



Hybrid devices



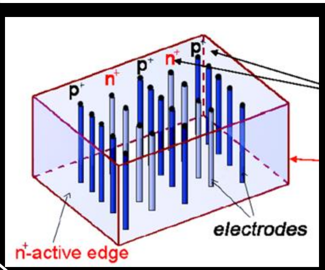
- Small electrode
  - MAPS
  - With gain
  - Without Gain

Optimized for rates/power/position resolution

- Large electrode
  - Without Gain
  - With gain
  - Large area passive devices (strip)

Optimized for radiation hardness/timing

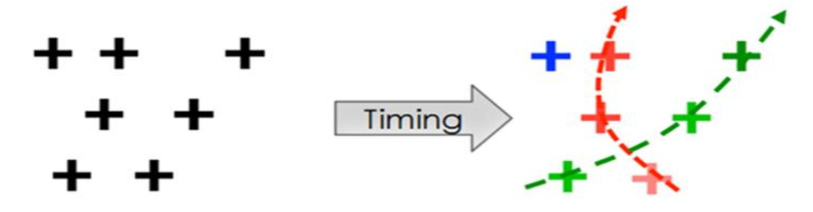
- Planar
  - Large area passive devices (strip)
  - With Gain (LGADs)
- 3D devices
  - Trench 3D
  - Column 3D
    - With Gain ?

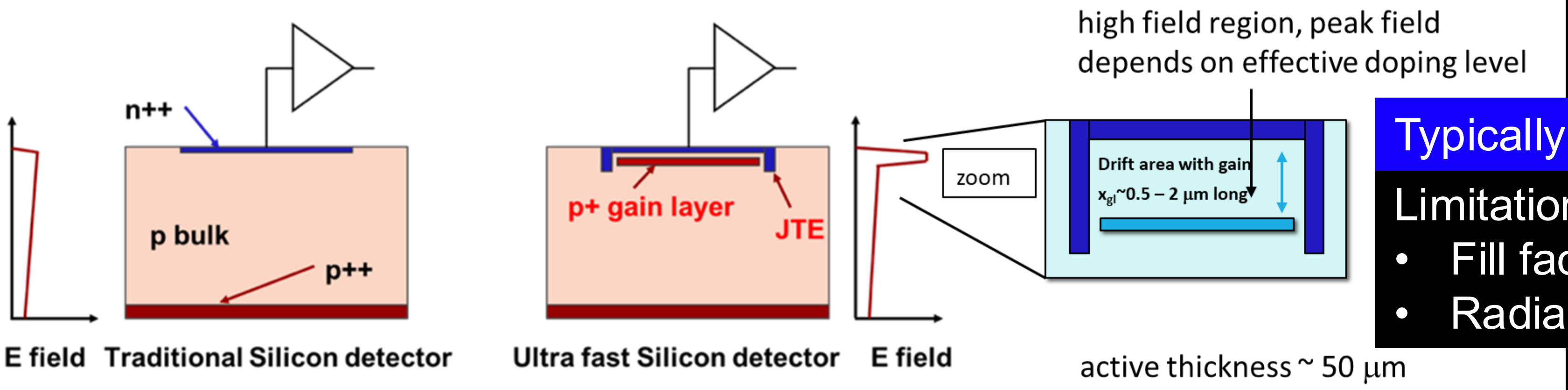


Red	Ideas
Orange	Recent research
Green	Proven/demonstrated

LGADs: Towards 4D tracking

- 4D tracking with ~10-30 μm position and ~10-30 ps time resolution simultaneously for every hit brings benefits in dense particle environment for tracking and PID





Typically 20-55 μm thick with 20 fC signal (G~40)

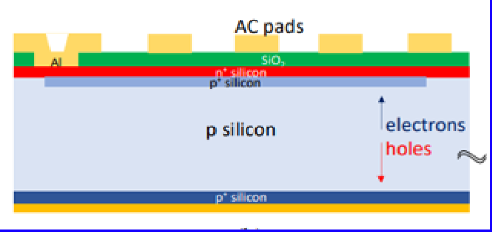
Limitations for conventional LGADs:

- Fill factor (large cell devices) due to JTE
- Radiation hardness – currently to ~3e15 cm^{-2}

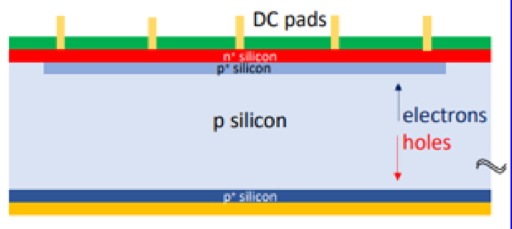
DIRECTION OF RESEARCH:

- Improve Radiation hardness: carbon in gain layer co-implantation (to reduce acceptor removal), compensated LGADs (exploit removal of acceptors and donors to maintain constant gain during operation)
- Improve Fill factor: different technologies

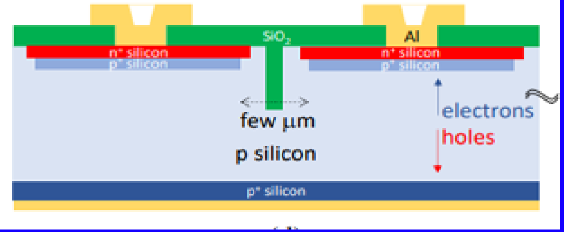
AC-LGADs



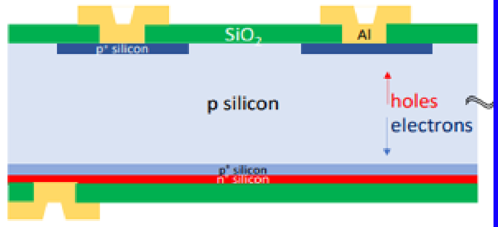
RSD-LGADs



Trench isolated LGADs



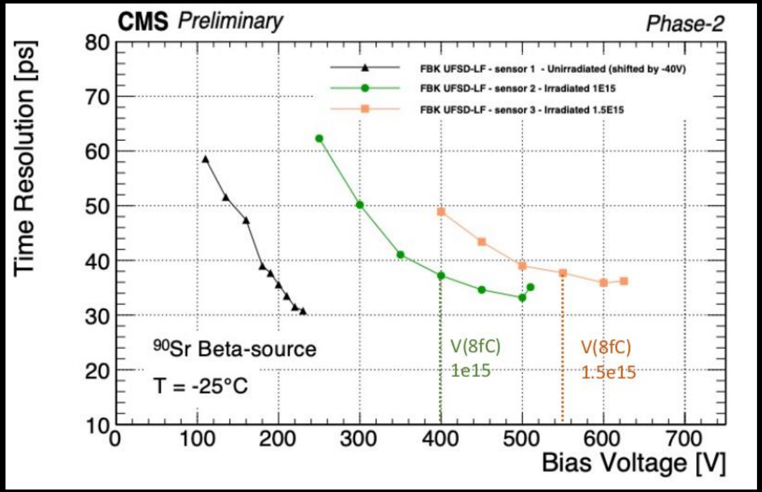
Inverse LGADs



Impact also beyond Particle Physics

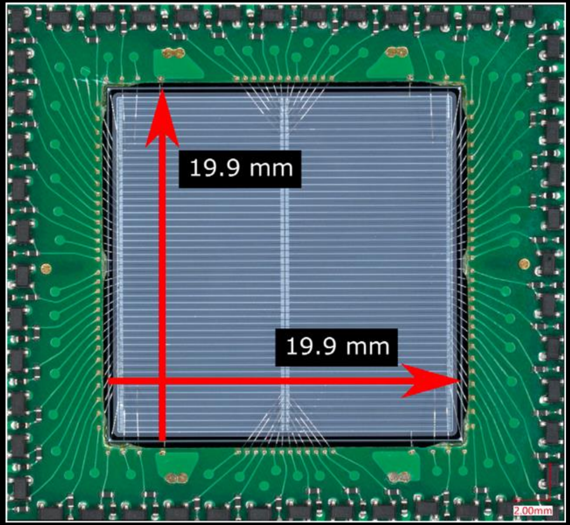
Large volume production

- IME (China Institute of Microelectronics) sensors for ATLAS High Granularity Timing Detector
- HPK
- FBK Technology Transferred to LFOUNDRY
  - Custom process on 8” wafers
  - Deep gain layer
  - Carbon co-implantation



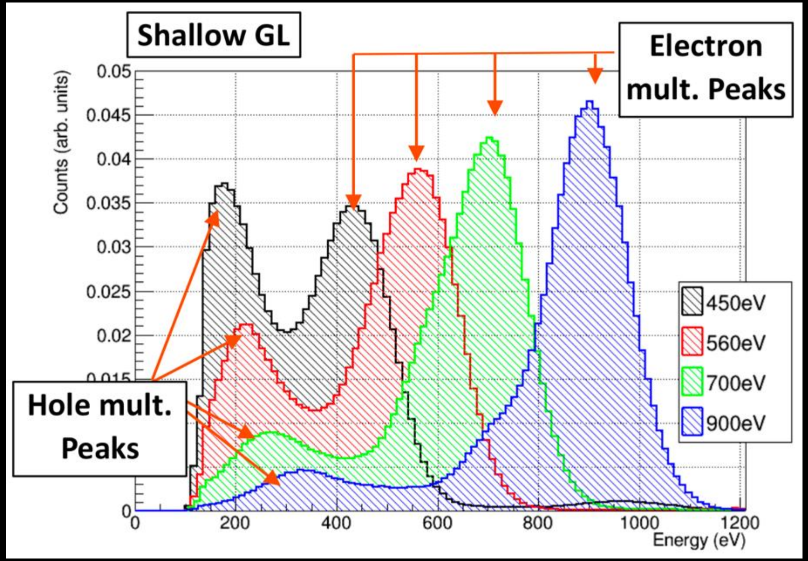
LGADs for Light and Heavy Ions

- Sensors used in T0 system of HADES fixed target experiment at GSI
- Strip LGADs operating in HADES with $\sigma(t) \approx 100$ ps for 4.5 GeV protons



Detection of soft X-rays: 250 eV - 2 keV

- Gain allow lower photon detection limit in counting detectors
- Gain improves SNR of integrating detectors
- Thin entrance window and gain structure must be developed



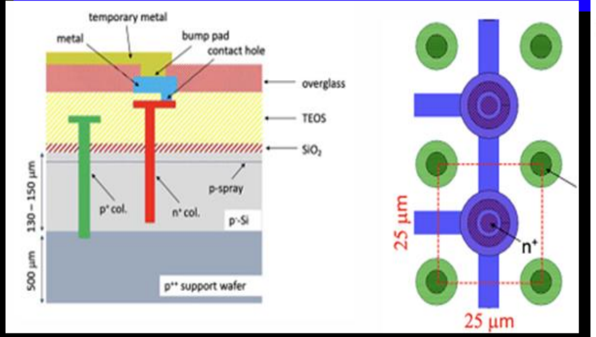
3D detectors: Towards 4D Tracking

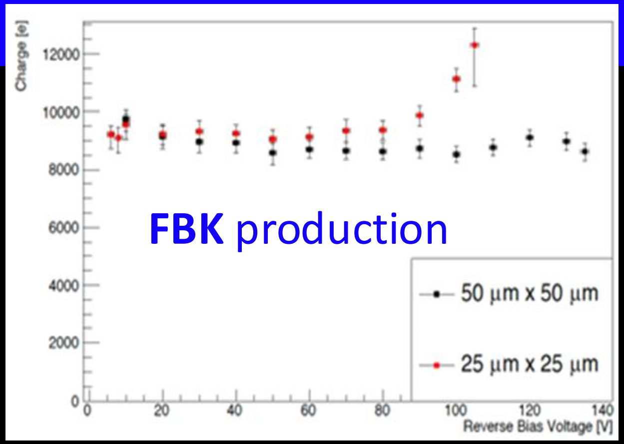
3D technology as timing detectors:

- Fill factor ~100% (inclined tracks)
- Fast (small distance) and can be thick
- Radiation tolerance up to ~1e17 cm^{-2} (at higher bias voltages)
- Technology is mature-latest 3D detectors are done in single sided processing

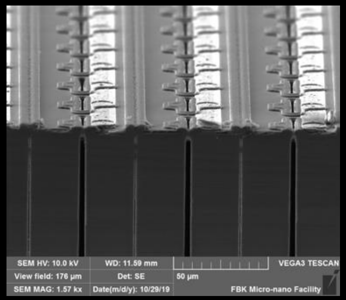
DIRECTION OF RESEARCH:

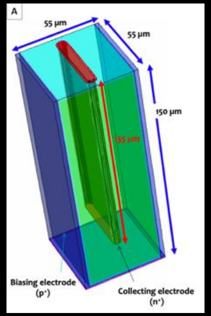
- 3D sensors with gain
- Sensors produced in a 25 µm x 25 µm with a very small column width show amplification ("silicon wire proportional chamber")



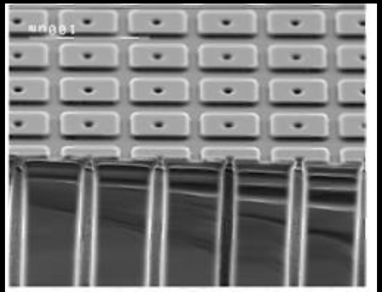


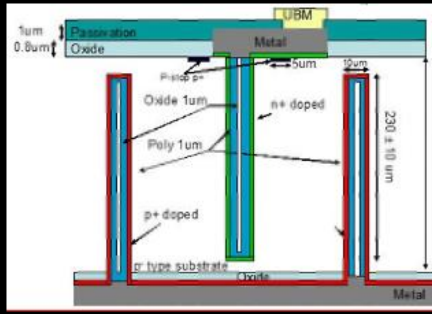
Trench 3D (INFN – FBK/IMECAS)



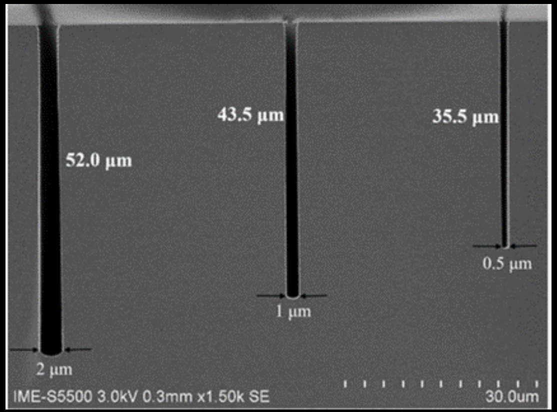


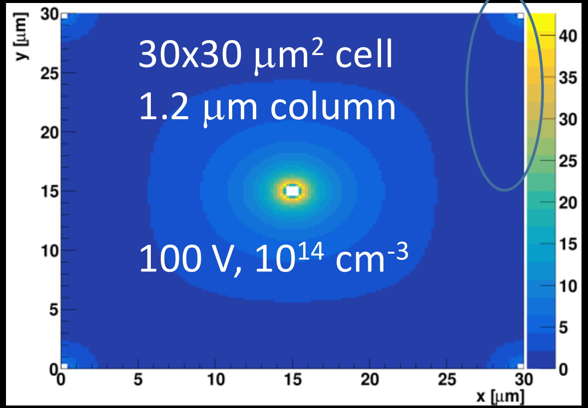
Column 3D (CNM/FBK/Sintef/ IMECAS)





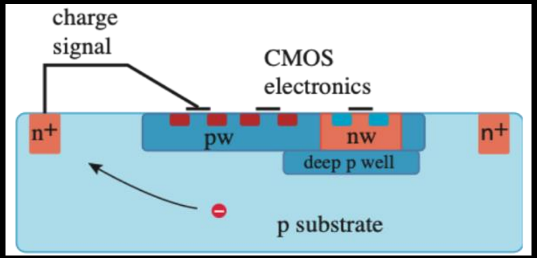
IMECAS - 8" CMOS process with aspect ratio of **>70**





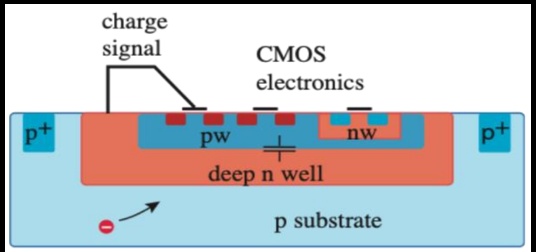
Monolithic Detectors

SMALL ELECTRODE



- $C \approx 3$ fF
- Low analogue power
- Difficult lateral depletion, requiring process modification of radiation hardness
- Threshold ≈ 100 e-

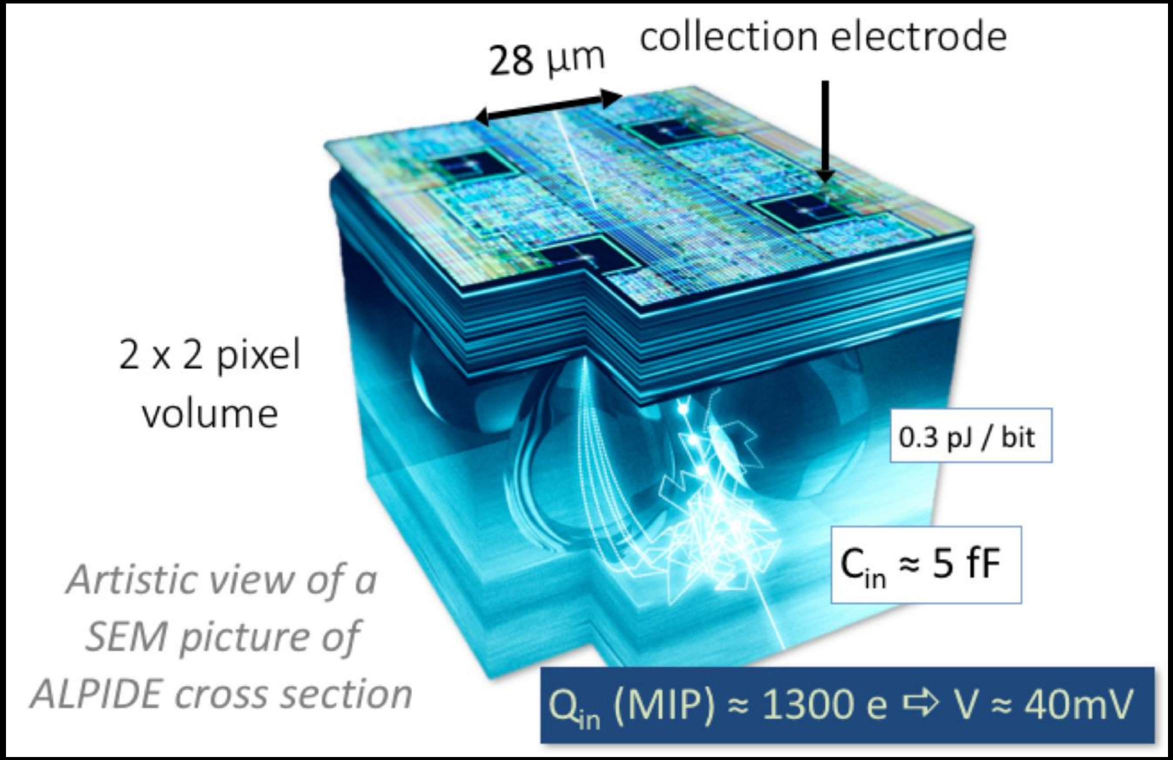
LARGE ELECTRODE



- $C \approx 300$ fF
- Strong drift fields, short drift path, large depletion depth
- Higher power, slower
- Threshold ≈ 500-1000 e-

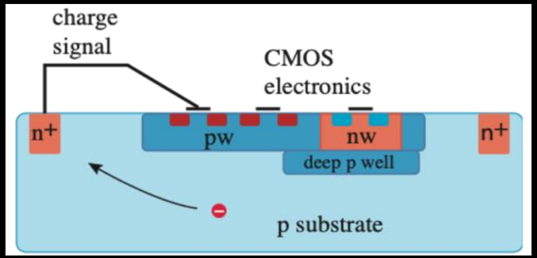
$$\tau \propto \frac{C}{g_m} \qquad ENC_{thermal} \propto \frac{kTC}{g_m}$$

Operational experience from ALICE ITS2 (SMALL ELECTRODE)



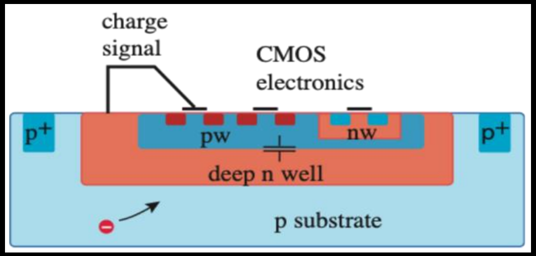
Monolithic Detectors

SMALL ELECTRODE



- C ≈ 3 fF
- Low analogue power
- Difficult lateral depletion, requiring process modification of radiation hardness
- Threshold ≈ 100 e-

LARGE ELECTRODE



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$$\tau \propto \frac{C}{g_m} \qquad ENC_{thermal} \propto \frac{kTC}{g_m}$$

Directions of research:

- Achieve very high spatial resolution (3 μm – easier for SMALL ELECTRODE)
- Achieve excellent time resolution (CMOS with gain)
- Support high data rates
- Improve radiation tolerance
- Minimize power consumption
- Maintain low material budget
- Enable coverage of large detector areas
- Control and reduce costs

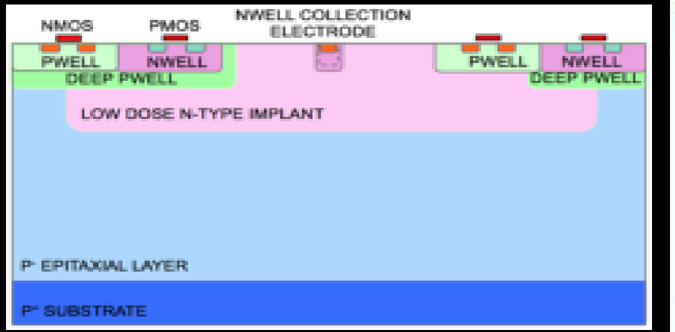
Integrate all requirements

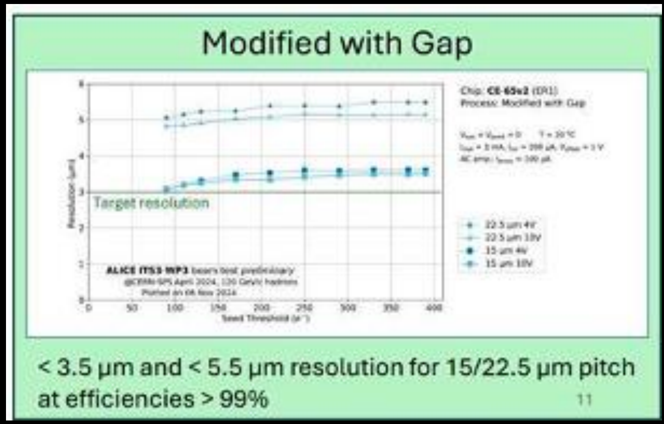
Challenges using commercial processes:

- Limited active depth (typically 60–80 e⁻h/μm)
- Thinner epitaxial layers at smaller nodes
- Cost escalation at smaller nodes; MPW may not be available
- Difficulty identifying vendors accommodating our requirements
- Restricted access to process information for device simulation
- Access constraints related to licensing (e.g., -PDKs)
- Limited availibility for high resistivity material, process modifications and additional processing needs such as backside processing and metallization

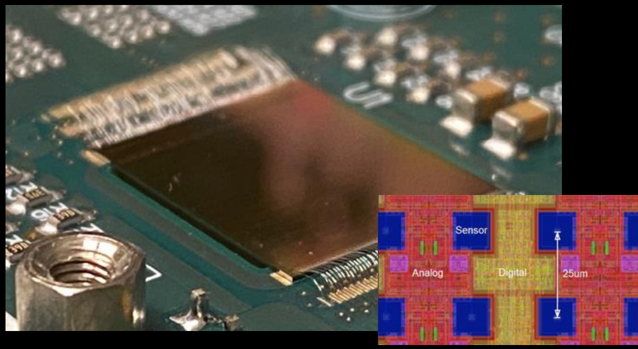
MAPS Process and architecture

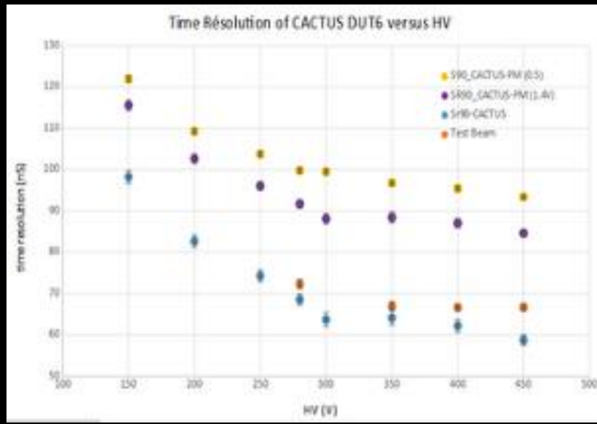
- Modified processes to achieve uniform efficiency over the cell (important for small electrodes)
  - Process modifications in Tower 180 (MALTA) successfully ported in TPSco 65





- Several sensors and readout architecture pursued
  - ARCADIA (LF11is technology)
    - MD3 chip: FD-MAP, Pixel pitch: 25 µm
    - Electronics: analog and digital, with in-pixel threshold and data storage
    - Architecture: event-driven
    - Low (High) power: 10-30 (100) mW/cm^2
  - Octopus (TPSco65):
    - Standard process, pitch ≳ 20 µm, and ADC or TOT
    - Standard/Modified process pitch ≲ 15 µm, with binary readout
  - Versatile Tracker (TPSco65):
    - Fixed collection pitch, Tuneable front-end, Programmable periphery
  - Cactus/MiniCactus chips LF15A technology
    - prototype to explore timing
  - NAPA (TPSco65) in the US

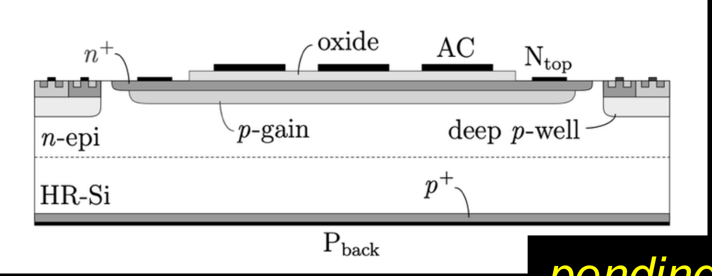




MAPs with gain

- Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays (LF11is technology)

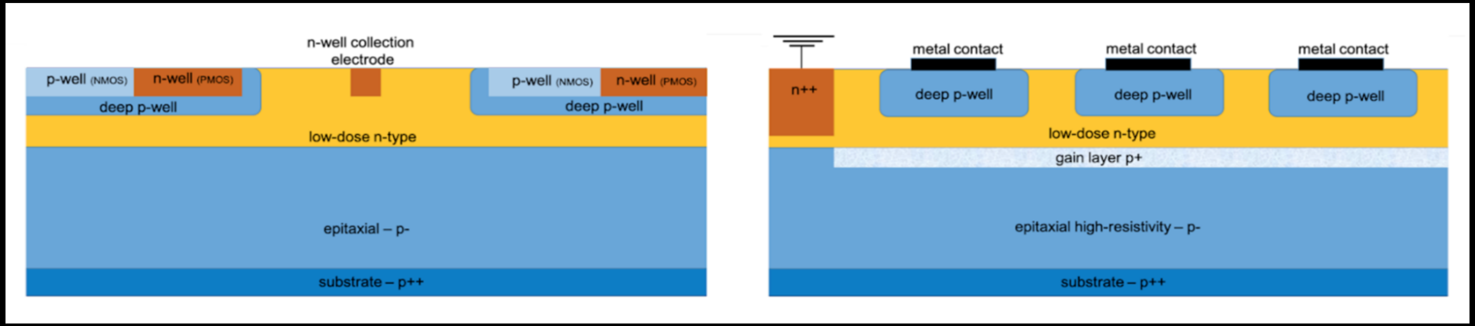
ALICE 3 time of Flight system
σ(t) ~ 20 ps



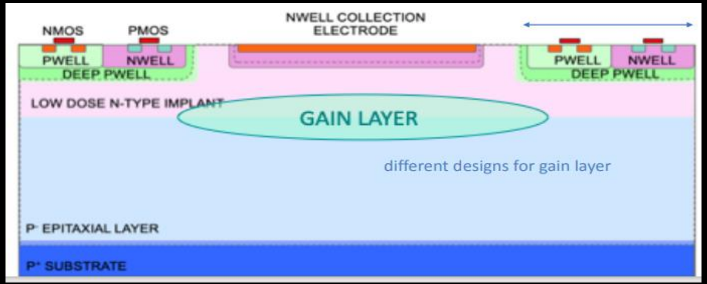
pending patent

Monolithic AC LGAD for IDEA silicon wrapper

- Development of monolithic AC-LGADs with SkyWater (Fermilab)
  - Targeting 10 ps and 5 µm spatial resolution

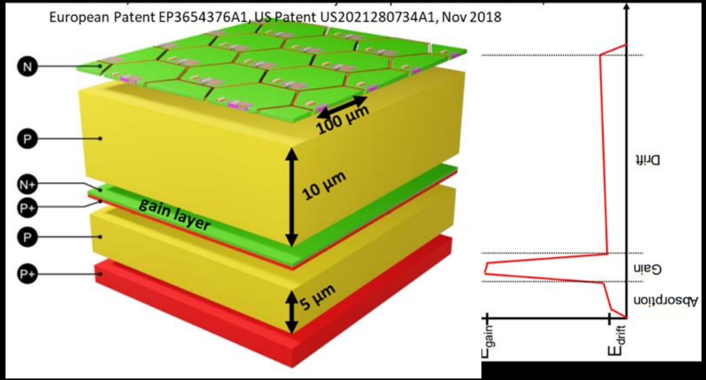


- CASSIA (CERN)



"deep junction" gain layer design In TJ180 aiming then transfer to TPSco 65

PicoAdd SiGe130 nm (Uni-Geneve)

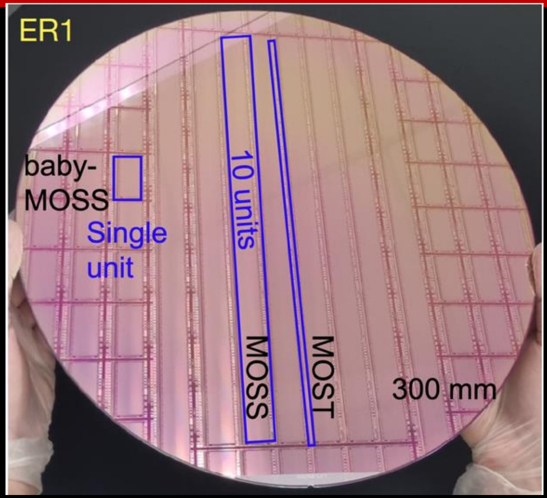


- SiGe bipolar amplifiers – fast (good timing)
- CMOS for digital electronics (monolithic)
- Gain-layer removed from the surface allowing very good spatial resolution without dead area

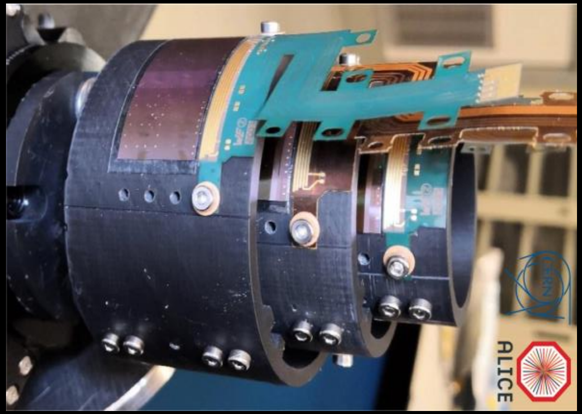
MAPs and material

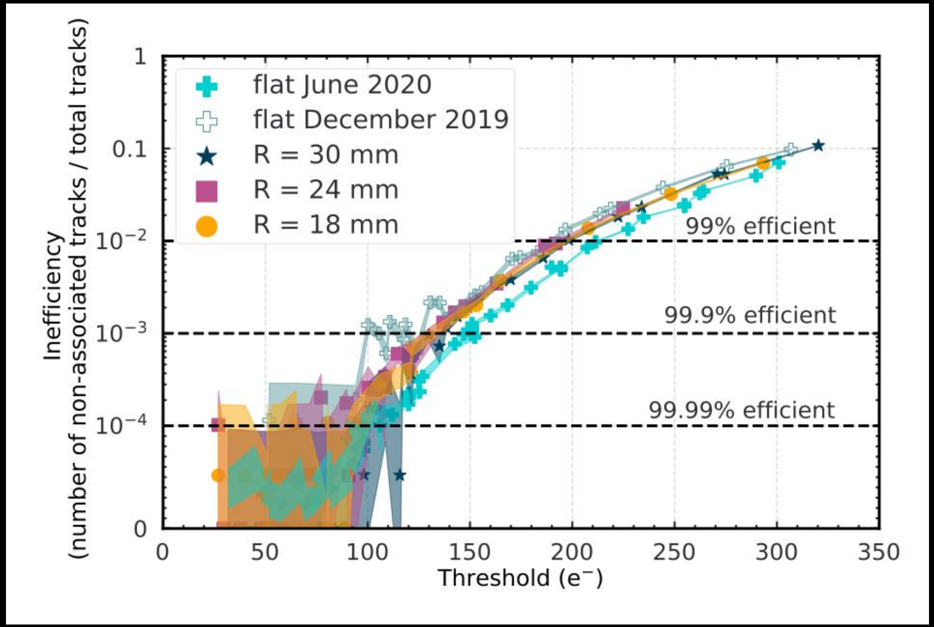
ITS3

- Ultralight stitched large sensors(wafer area) thinned down to 40-50 μm
- Flexibility of silicon allows foldable vertex detector (ALICE ITS 3)
- Fine pitch 65 nm TPSCo technology, 18 – 22.5 μm pixel pitch, modified design electrode, ITS-3



ITS3 "engineering model 1" made of 3 layers of dummy silicon, 40-50 μm thick



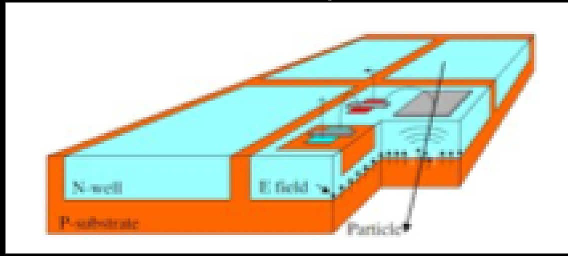


ALICE 3

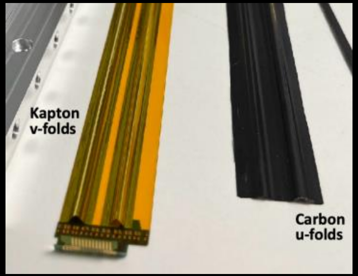
- 3 layers of wafer-size, ultra-thin, curved, CMOS MAPS inside the beam pipe in secondary vacuum
- σ(pos) ~ 2.5 μm

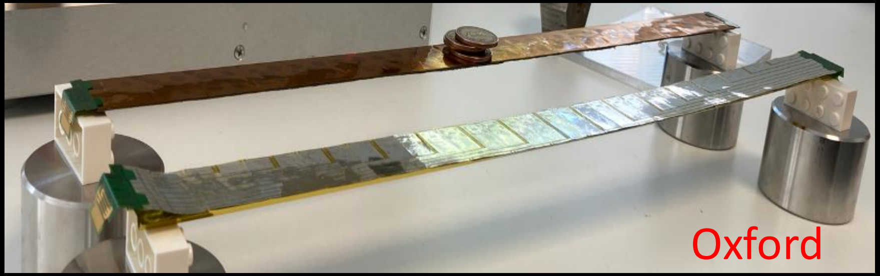
MAPs and material

- MU3e
  - Mupix11 chips based on HV-CMOS technology (KIT- Heidelberg)
  - Thinned to 50 µm (Vertex) and 70 µm (Tracker)
  - 80 Ωcm resistivity (380 Ωcm for first prototype modules)



Kapton-Aluminum flexes produced by LTU (Kharkiv)





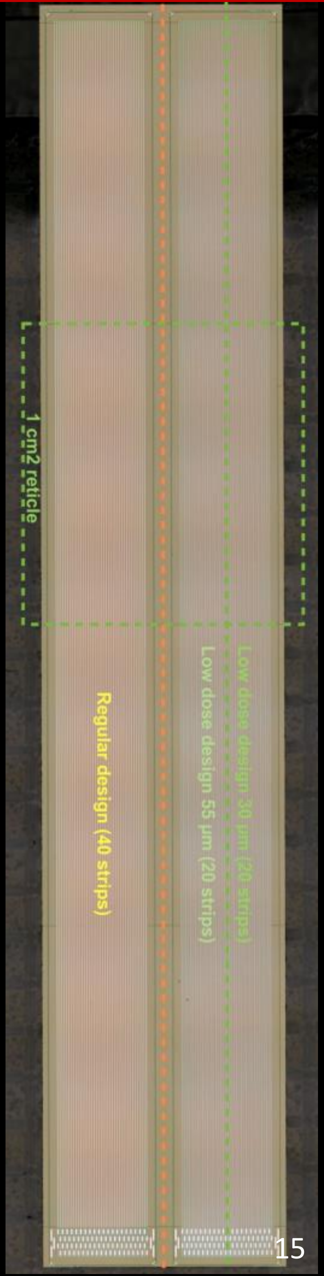
Chips glued on Al/Kapton flex supported by a Kapton tape with a v-fold (vertex) or by 25 µm Carbon-fibre support structure (tracker) to achieve 0.1% X_0/layer

Large area CMOS strip detectors

- Reduced material budget
- Easier integration
- Potentially low cost and availability

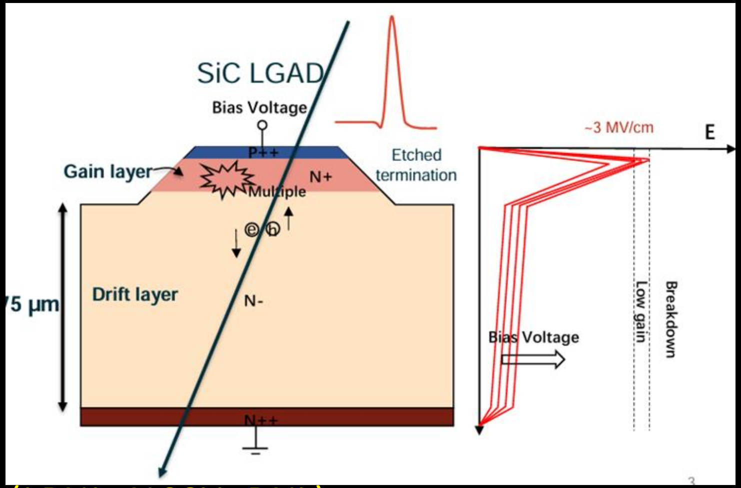
LFA150 nm –
Resistivity of wafer: >2000 Ω·cm
ASIC can be implemented

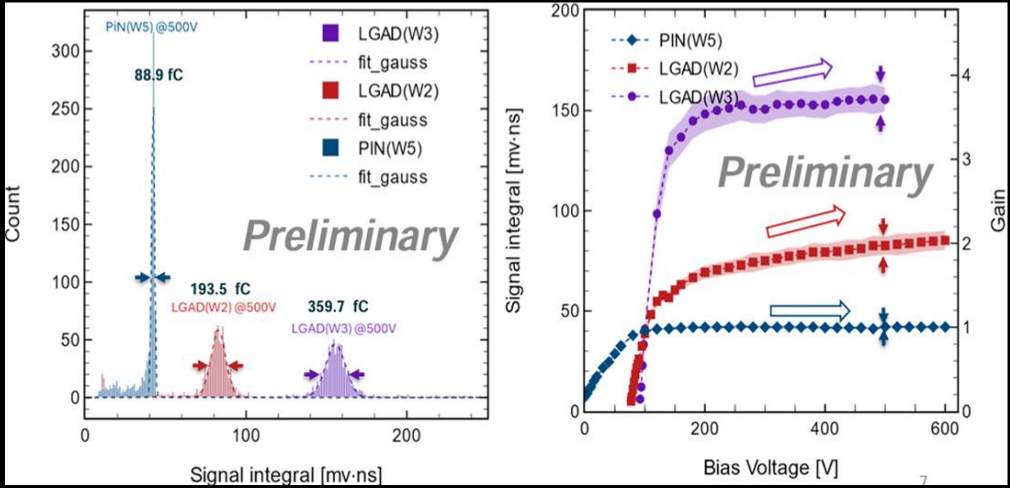
(Dortmund, Freiburg, DESY, Bonn)



Silicon carbide developments

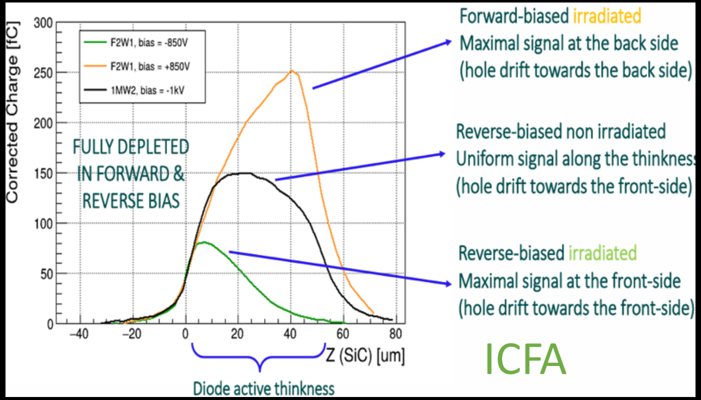
Gain achieved with SiC-LGADs





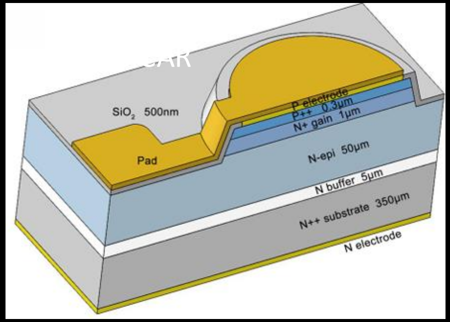
(LBNL, NCSU, BNL)

Irradiated SiC detectors in forward bias – discovery of charge multiplication

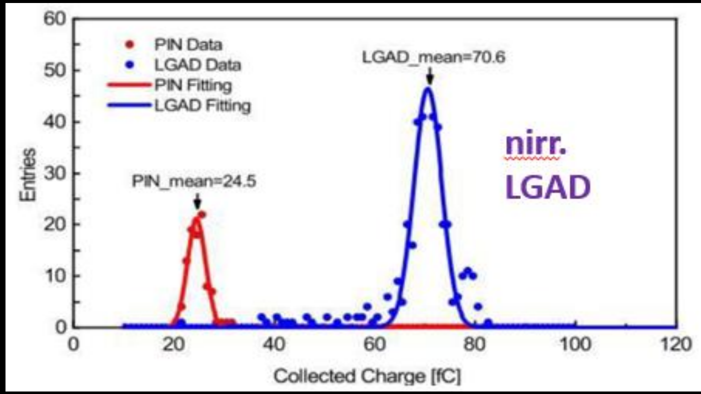


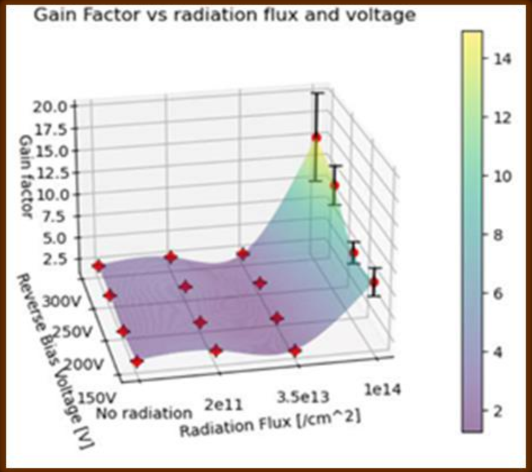
ICFA

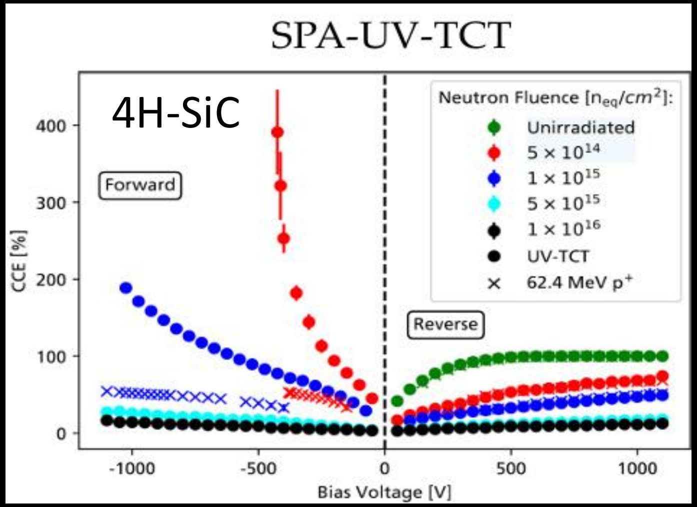
Gain increases with irradiation!



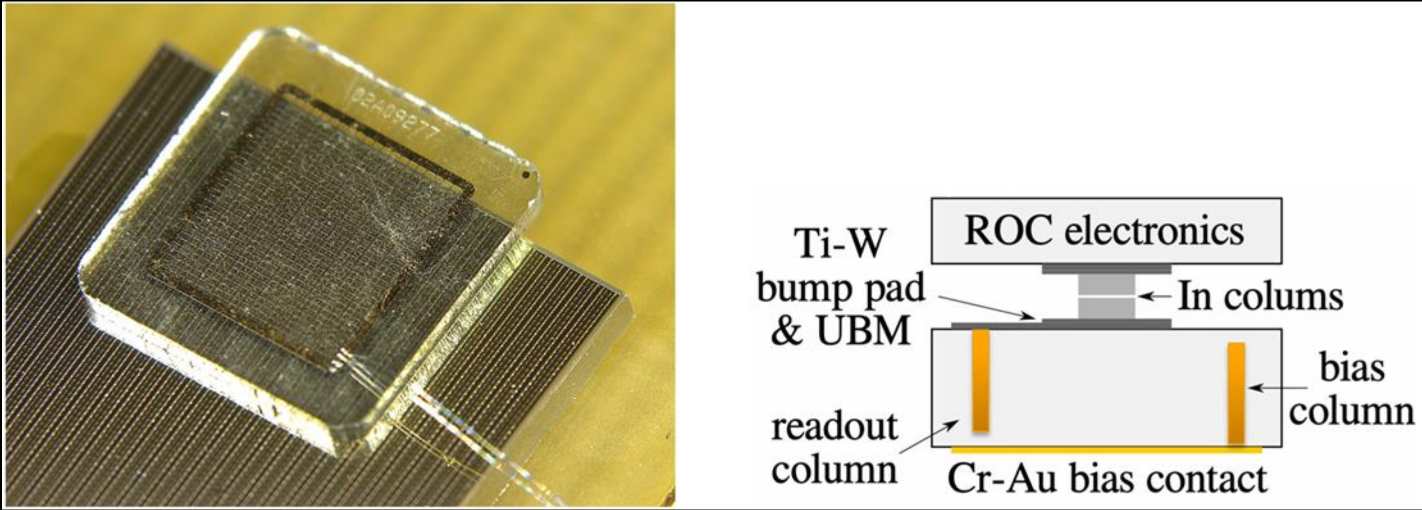
IHEP, Shanghai, Hefei

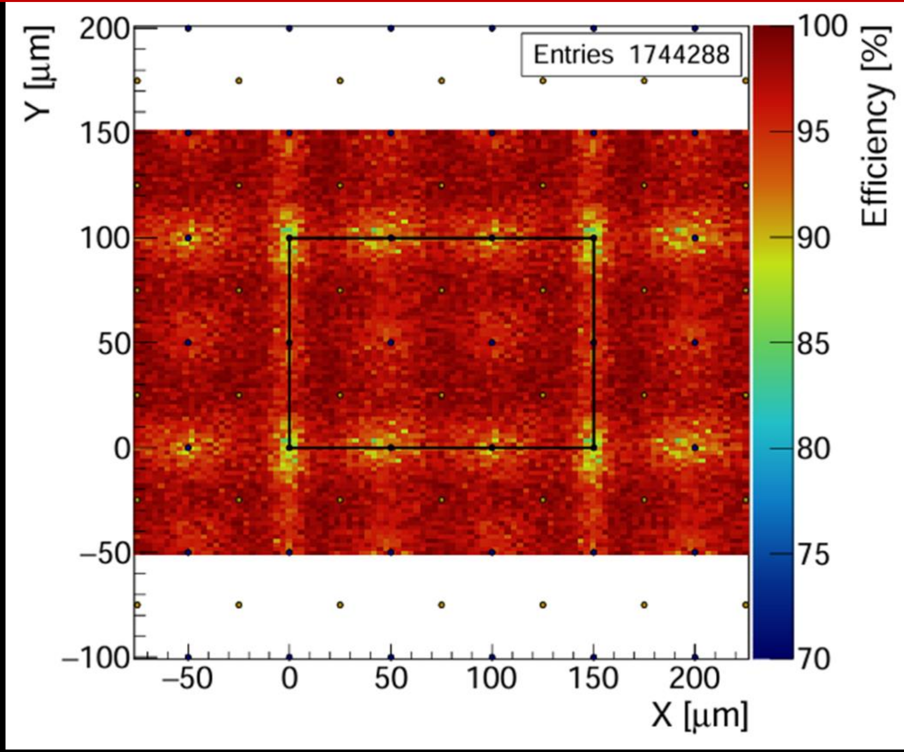


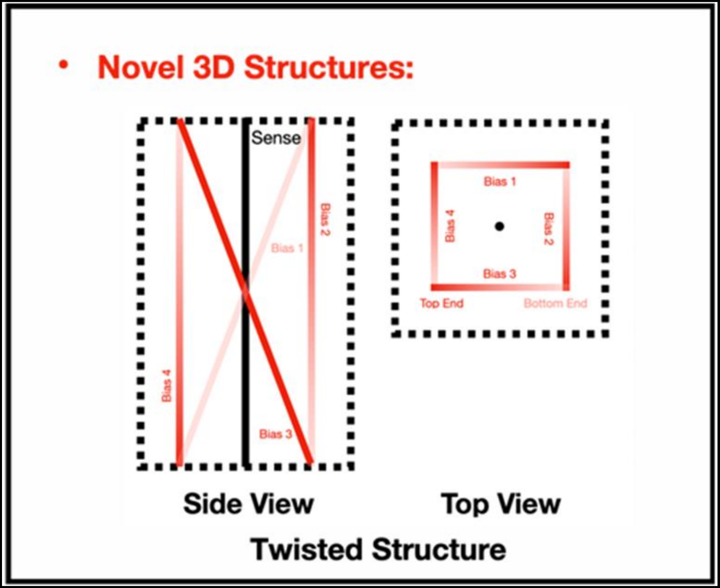


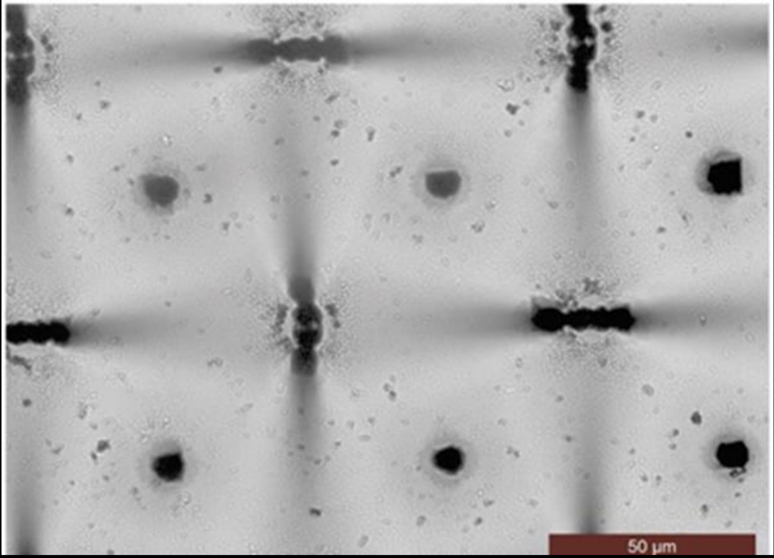


Diamond detector developments









3D electrodes made with laser (graphitization when focused light pulls through the diamond – slow)

Twisted structure would improve timing performance and reduce the impact of the pCVD grains.

DRD3 Projects

WP1

- OCTOPUS- Fine-pitch CMOS pixel sensors with precision timing for vertex detectors at future Lepton-Collider experiments
- TPSCo 65nm CMOS with high precision timing (IP2I)
- Development of MAPS using 55nm HVCMOS process for future tracking detectors (IHEP)
- Radiation hard read-out architectures (CERN)
- CASSIA - CMOS Active Sensor with Internal Amplification (CERN)
- Towards large electrode CMOS sensors with intrinsic amplification for ultimate timing performance (Saclay)
- TPSCo 65nm MCMOS with high precision timing

WP2

- Novel silicon 3D-trench pixel detectors based on 8-inch CMOS process (IME)
- LGAD based timing tracker development for future electron collider (IHEP)
- Development of very small pitch, ultra rad- hard 3D sensors for tracking + timing applications at FBK (FBK)
- Development of Ultra Fast-Time Low Mass Tracking Detectors (FNAL/BNL)
- Development of TI-LGADs for 4D Tracking (UZH)

WP3

- Radiation damage in Si PiN and LGAD sensors (NIMP)
- Radiation hardness of 25 μm 3D diamond detectors (Manchester)
- SiC LGAD Detector (IHEP)
- Development of radiation-hard GaN devices for MIP detection (Carleton)
- Graphene/SiC Detector (CAS)

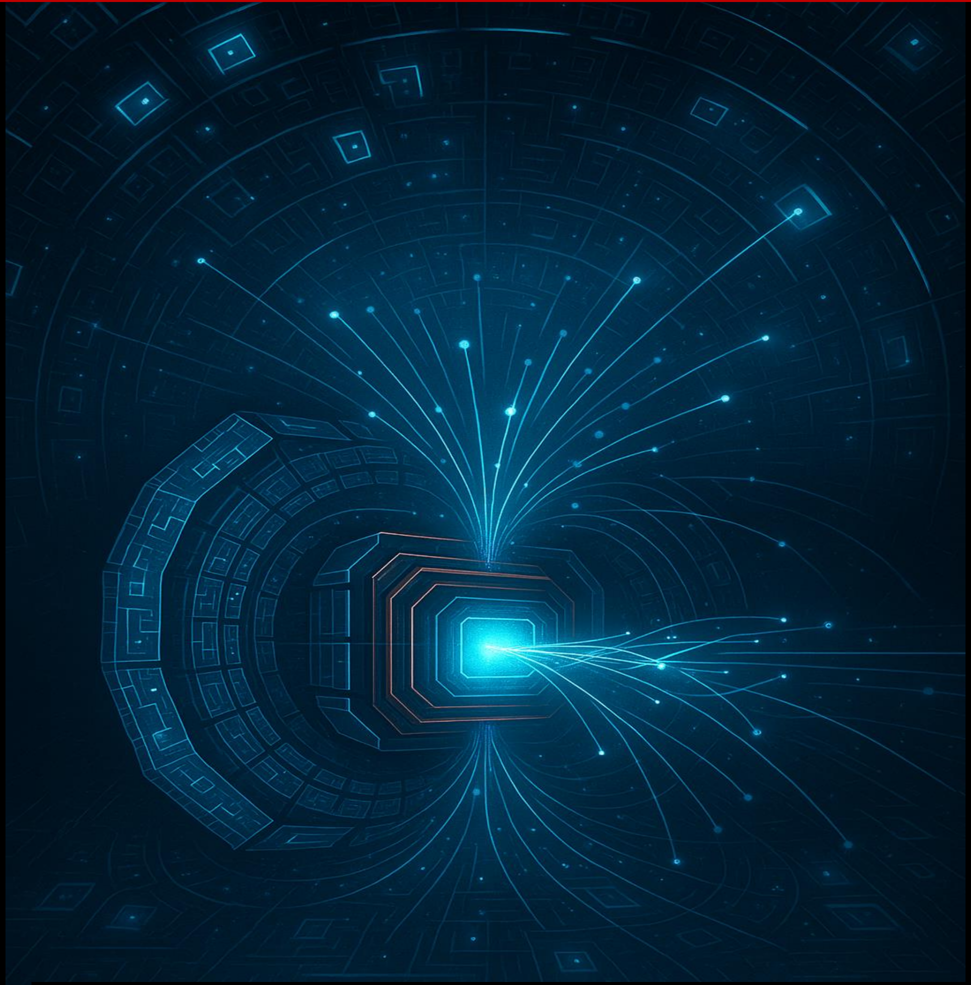
WP4

- In-house plating, hybridization and module-integration technologies for pixel detectors (CERN,FBK)

Reviewed by CB
In CDS but not very thoroughly reviewed or input is missing
presented at the 3rd DRD3 meeting

CONCLUSIONS

- Impressive range of activities, despite a significant portion of the community still deeply engaged with HL-LHC construction
- Steady progress across multiple fronts
- Active evaluation of several promising technologies:
  – LF 110, LF 150
  – TPSCo 65
  – TJ 180
  – TSI 180
- Strong focus on ITS3, ePIC, and ALICE 3 creates great opportunities to accelerate R&D — though this intensity can also create some tension around coordination and resource balance across projects



SILICON IS AT THE AHEART OF DISCOVERY

Many thanks to the working group on Detector Instrumentation and Gregor Kranberger (the spokeperson of DRD3)

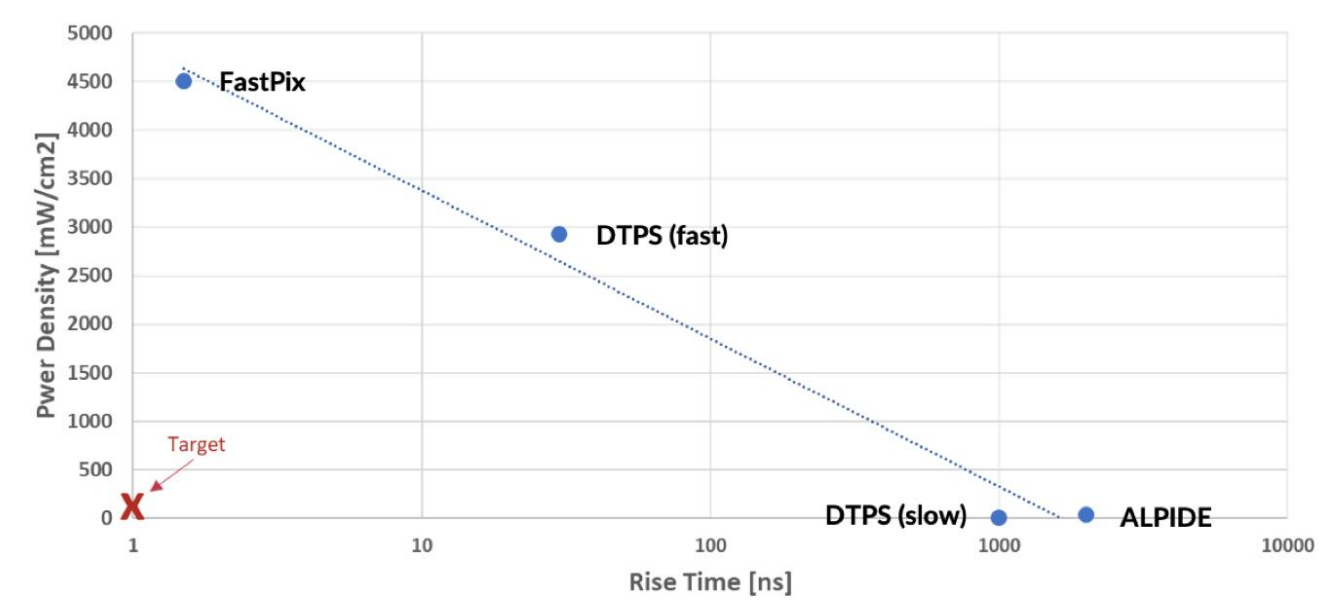
MAPS technologies

- **TPSCo 65 nm**
  - 10 µm epitaxial layer
  - 7 metal layers, 300 mm wafers with stitching
  - Wafers can be thinned to < 50 µm
  - Pixel pitches below 20 µm
- **LF11IS (Automotive CMOS Imaging)**
  - 6 metal layers on high-resistivity substrates
  - Supports Front-Side Illuminated (FSI) and Back-Side Illuminated (BSI) process flows
  - Stitching options available
- **IHP 130 nm (SiGe BiCMOS)**
  - Combines Silicon-Germanium Heterojunction Bipolar Transistors (HBTs) with CMOS
  - State-of-the-art analog and RF performance
- **LFoundry 150 nm (LF15A)**
  - Mixed digital / high-performance analog CMOS
  - High-voltage capability
  - Up to 6 metal layers, with optional top metal for large pixel matrix power distribution
- **TSI 180 nm (High-Voltage CMOS)**
  - 7 metal layers
  - Suitable for power and signal integration in complex systems
- **TowerJazz 180 nm (CMOS Imaging)**
  - Cost-effective process for imaging applications on 200 mm wafers
  - 6 metal layers + optional thick top metal for enhanced signal and power routing
  - Ideal for prototyping and manufacturing

Target Specs and State of the art

Chip name	Technology	Pixel pitch [μm]	Pixel shape	Time resolution [ns]	Power Density [mW/cm2]
Target Specification	?	25 x 100	Sq / rect	1	< 20
ALPIDE [2][3]	Tower 180 nm	28	Square	< 2000	5
FastPix [4][5]	Tower 180 nm	10 - 20	Hexagonal	0.122 – 0.135	>1500
DPTS[6]	Tower 65 nm	15	Square	6.3	53
Cactus [7]	LF 150 nm	1000	Square	0.1-0.5	145
MiniCactus [8]	LF 150 nm	1000	Square	0.088	300
Monolith [9][10]	IHP SiGe 130 nm	100	Hexagonal	0.077 – 0.02	40 - 2700

No design fulfills all target specification → The need to develop a custom design

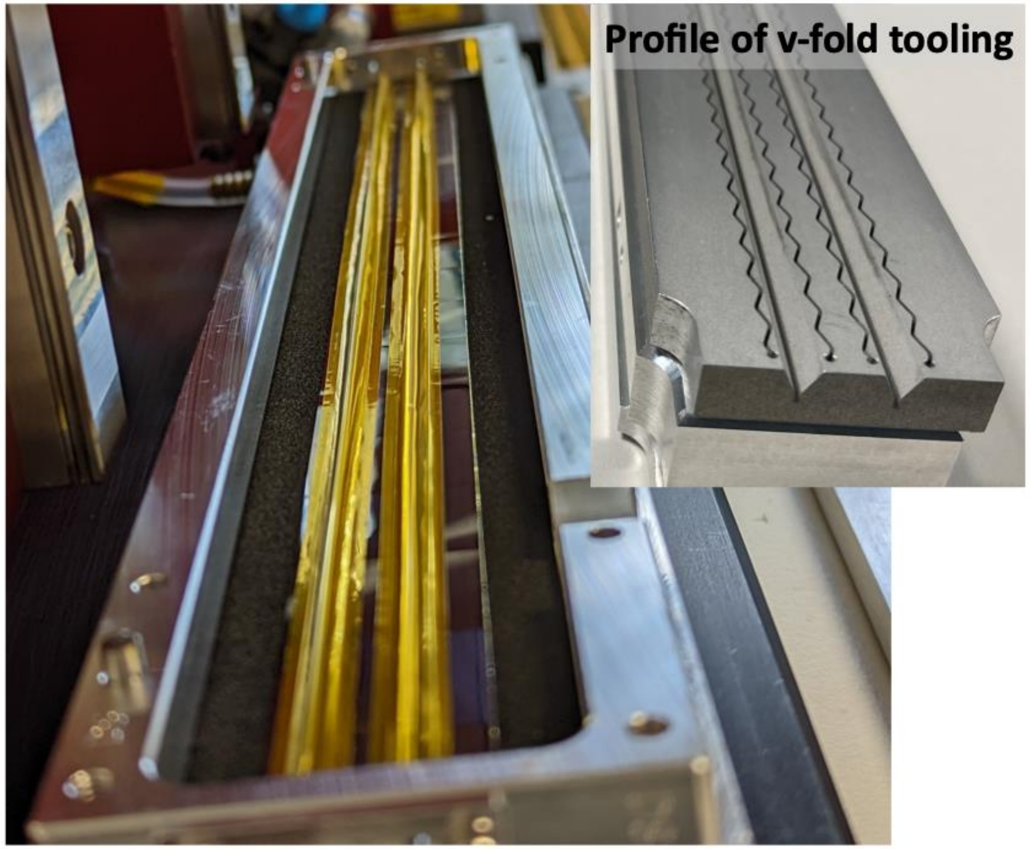


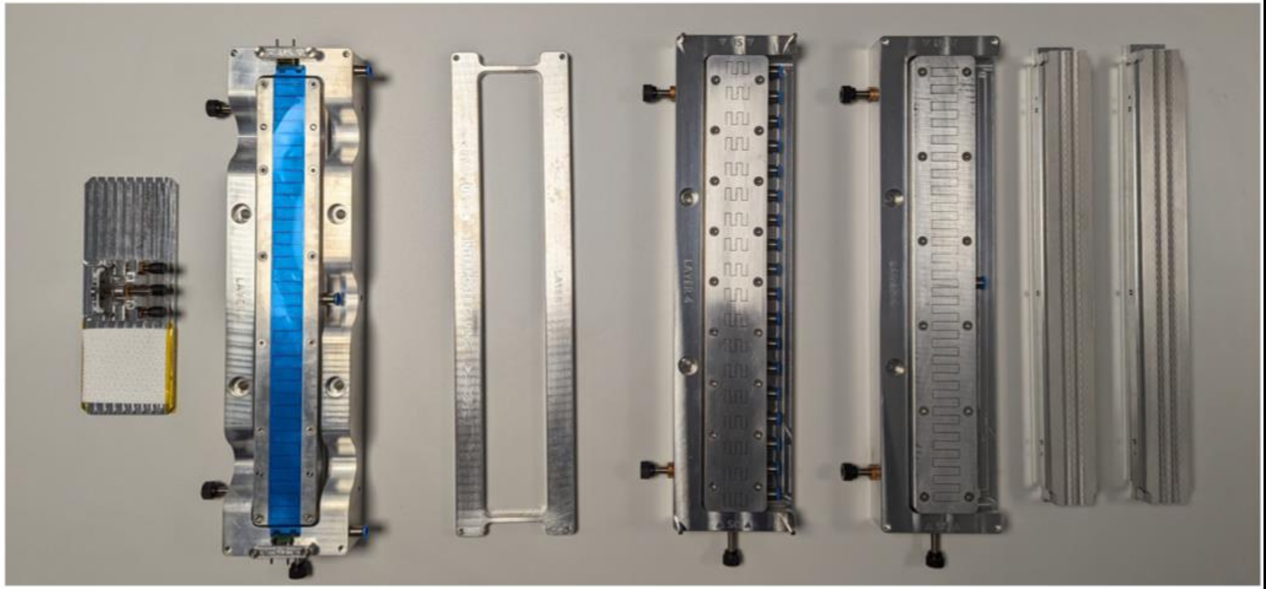
Mu3e outer layer fabrication

Production tooling for Layer 4 is almost complete, tooling for Layer 3 to commence shortly after.

- Expected production rate is $\mathcal{O}$(1.5 ladders / day), to commence March 2024

Prototype outer pixel layers have been fabricated.





Interposer flex bending tool	Align, glue, TAB bond interposer and ladder flexes	Ring frame to hold ladder during production	Chip chuck: align MuPix 11 array on robot and glue chips to ladder	Flex chuck for MuPix11 TAB binding, and V-fold gluing	V-fold and U-fold chucks

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