

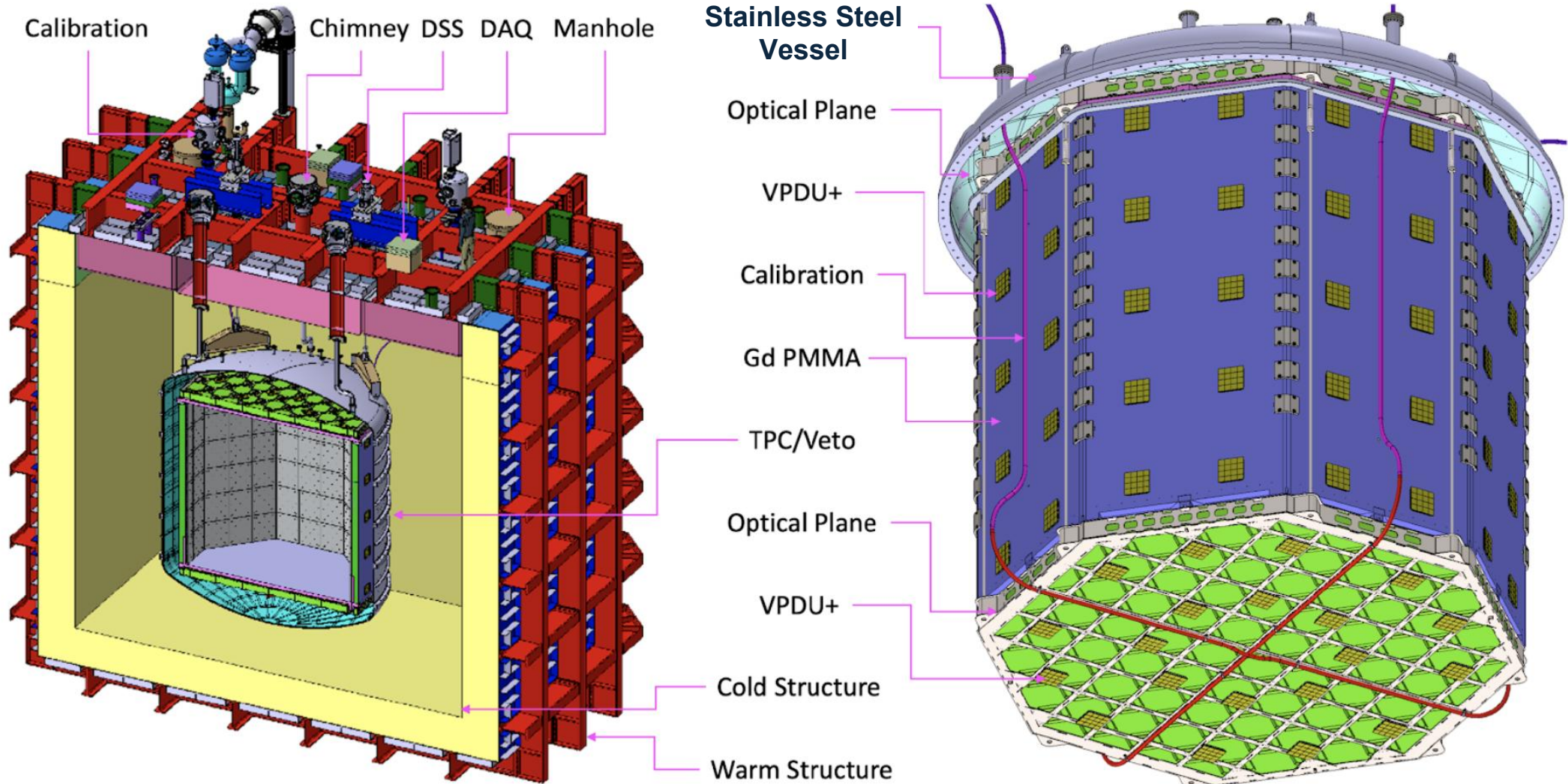
# Characterization and Integration of Large Area SiPM Arrays at the NOA Facility

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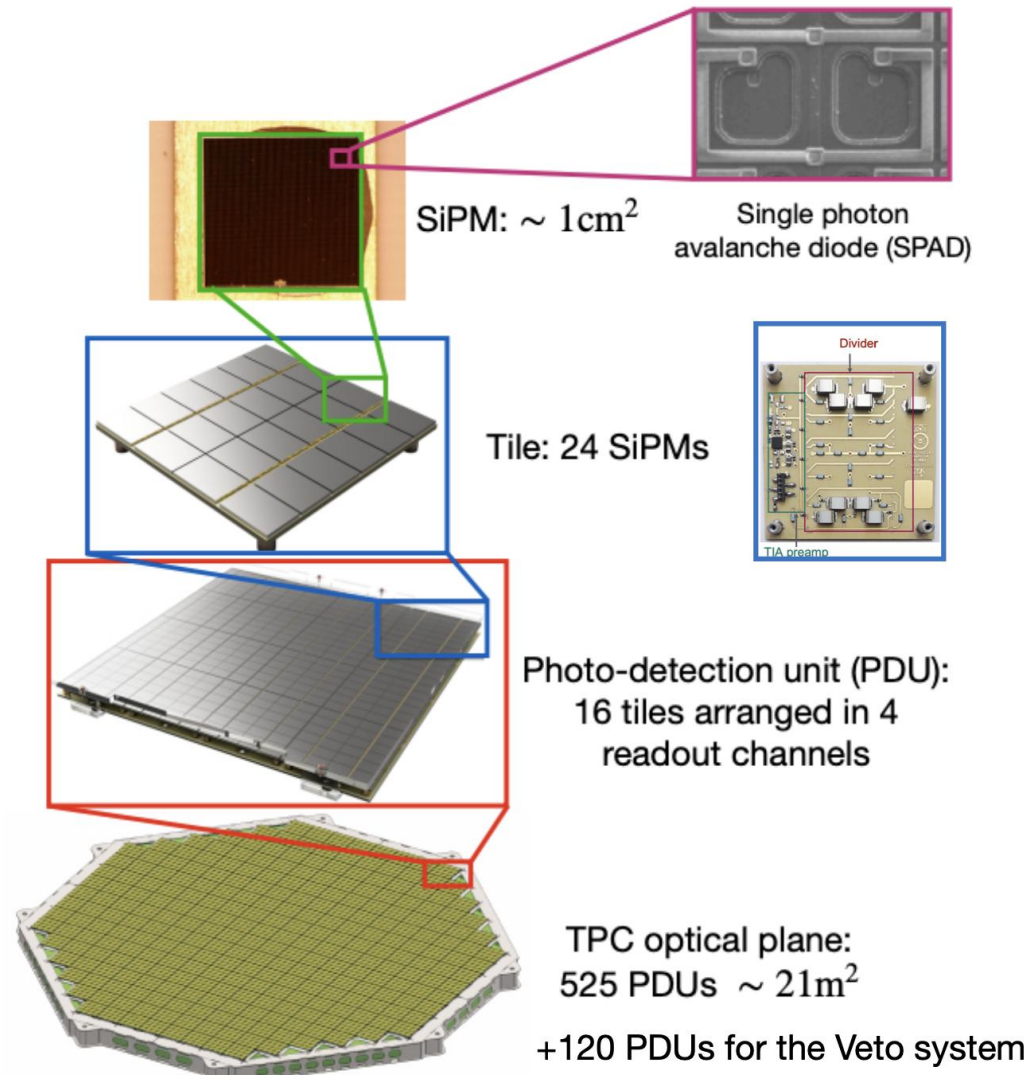


**Tutors:** Lucia Consiglio,  
Devidutta Gahan,  
Andrea Marasciulli

# DarkSide-20k experiment



# Optical planes



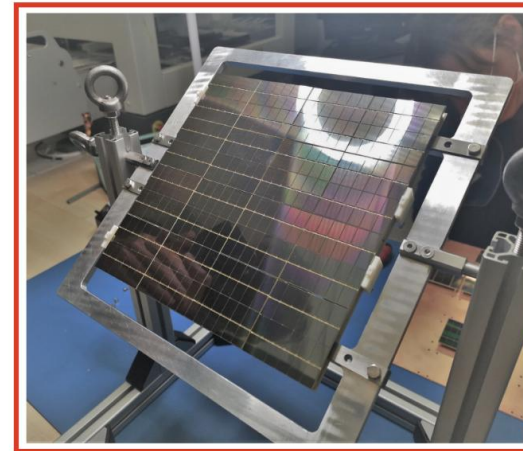
Collaboration with FBK for SPAD design

2019: 24 SiPM tile frozen

2022: refinement of the electronics

2022: full PDU!

**Late 2022 until present: mass production and assembly at NOA**



First 2 fully assembled devices are currently in N.



# The NOA facility



NOA is a clean room of ISO6 standard  
It became operational on February 2023  
NOA has two main areas:

- CR3 (350 m<sup>2</sup>) is devoted to the assembly of SiPMs, tiles, PDUs and respective tests
- CR2 (70 m<sup>2</sup>) devoted to integration of the optical planes



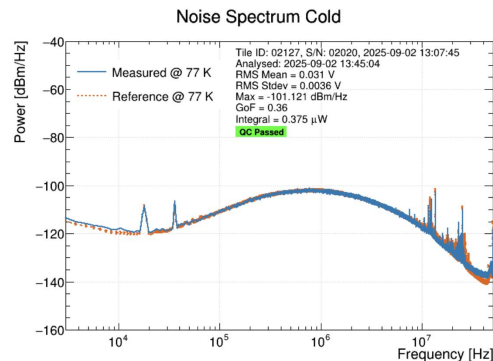
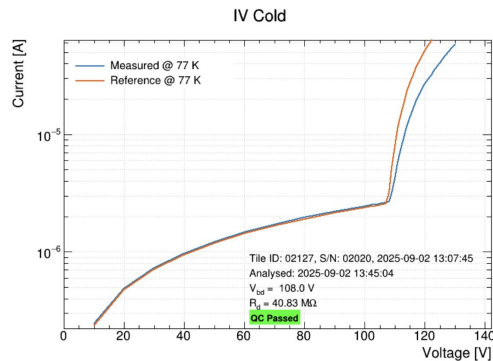
# Summarized pipeline

**Production:** wire bonding done, optical inspection...

## Tiles to be tested:

- CMOS imaging
- *DCR* (Dark Count Rate)
- *PCR* (Pulse Count Rate)
- IV curve
- Noise Spectrum
- Pulse counting
- Average single photoelectron

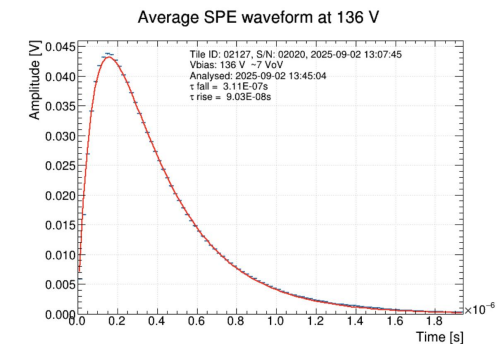
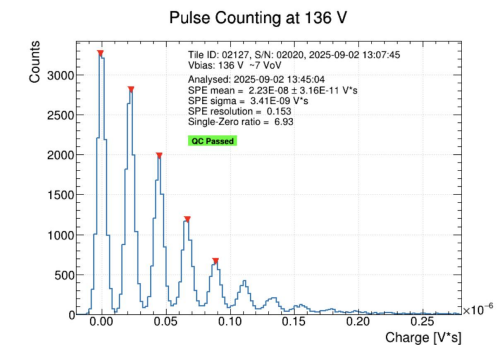
**Test passed:**  
**Waiting for PDU assembly**



## Test failed: check condition

→ Re-work

→ **Bad for sure**



# The NOA facility



# Waveform-level analysis: high-PCR tiles

## PCR events:

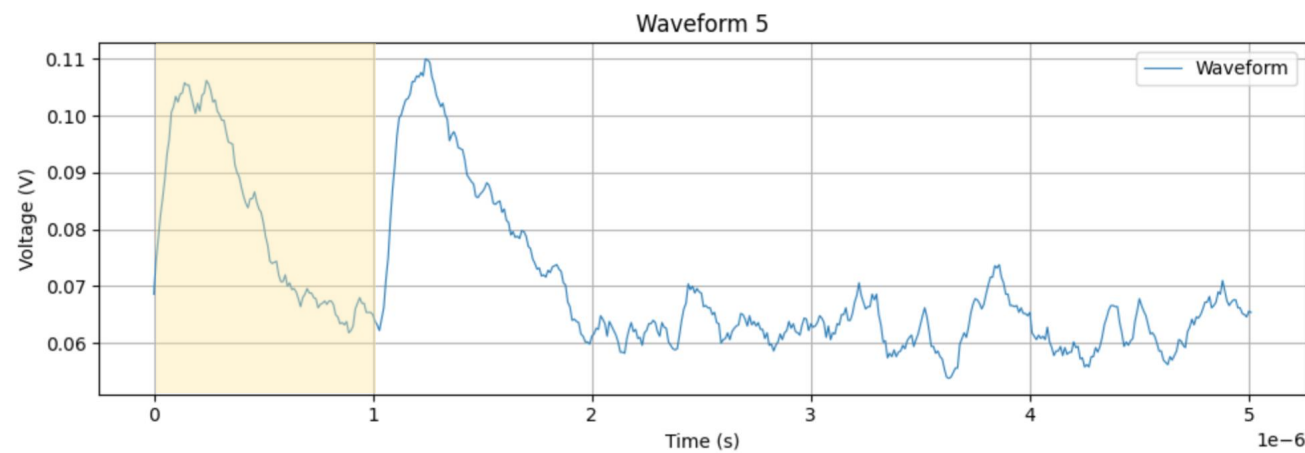
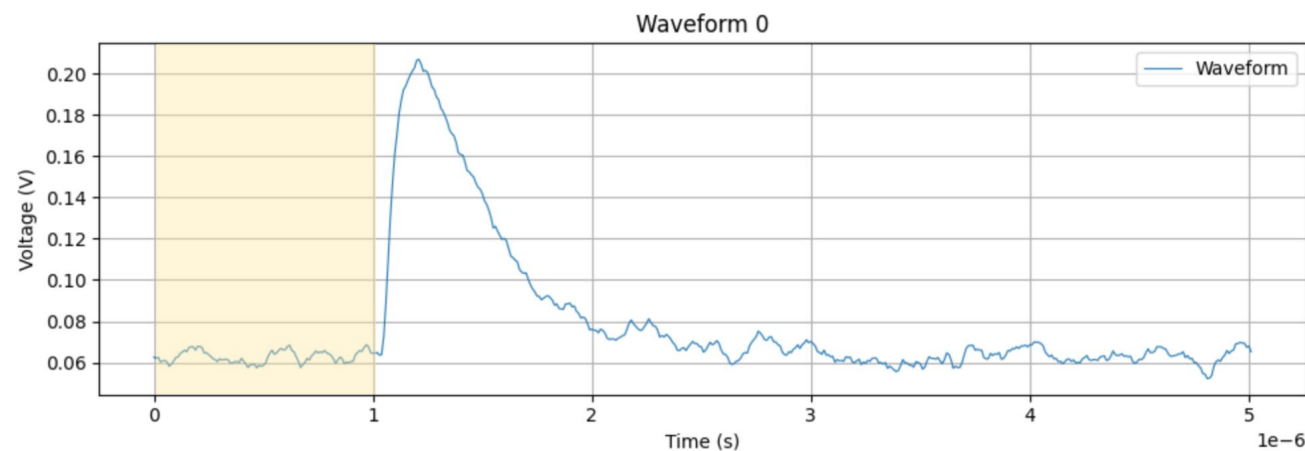
Photoelectrons in the pretrigger region (external trigger)

→ Baseline overestimated

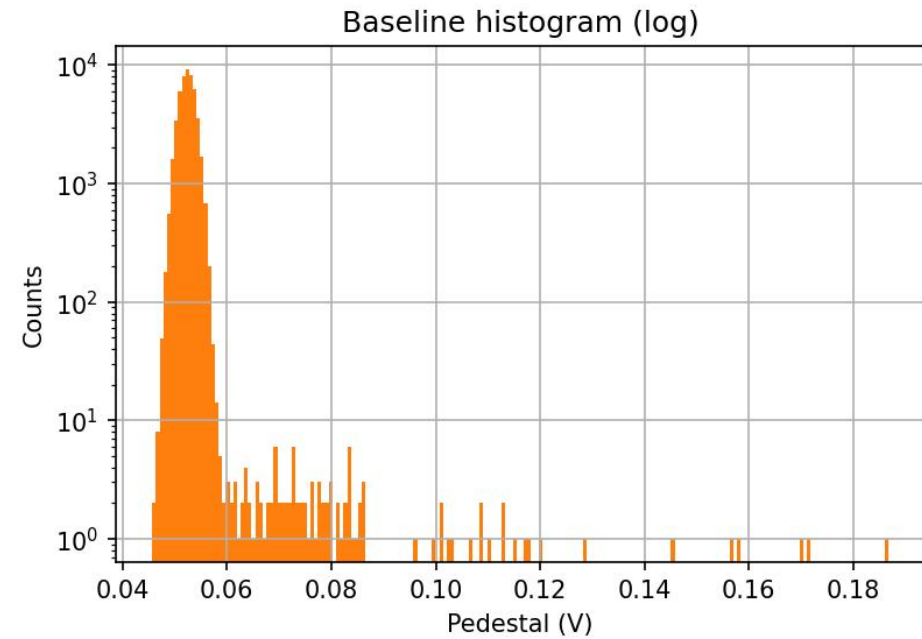
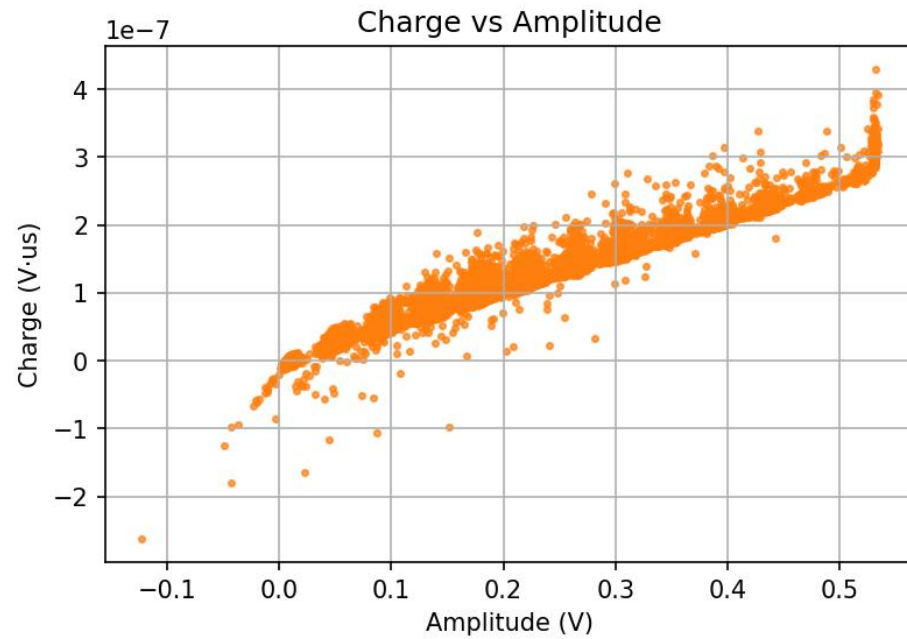
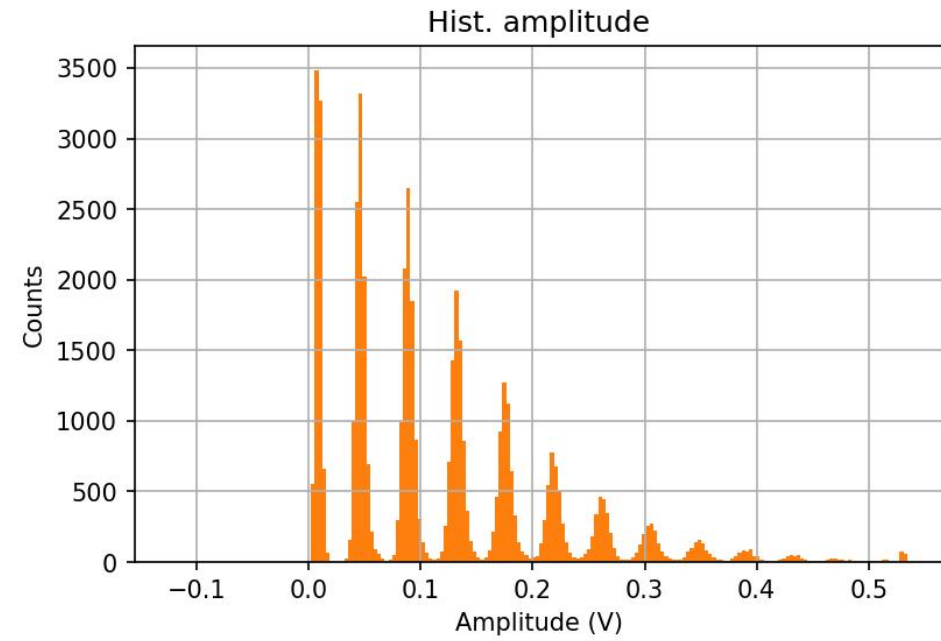
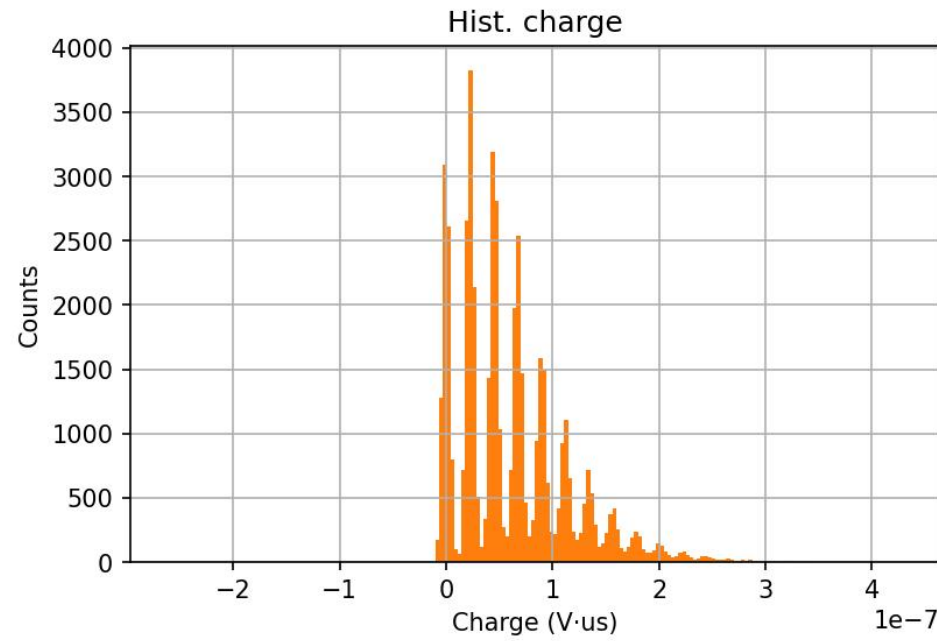
→ Integrated charge underestimated

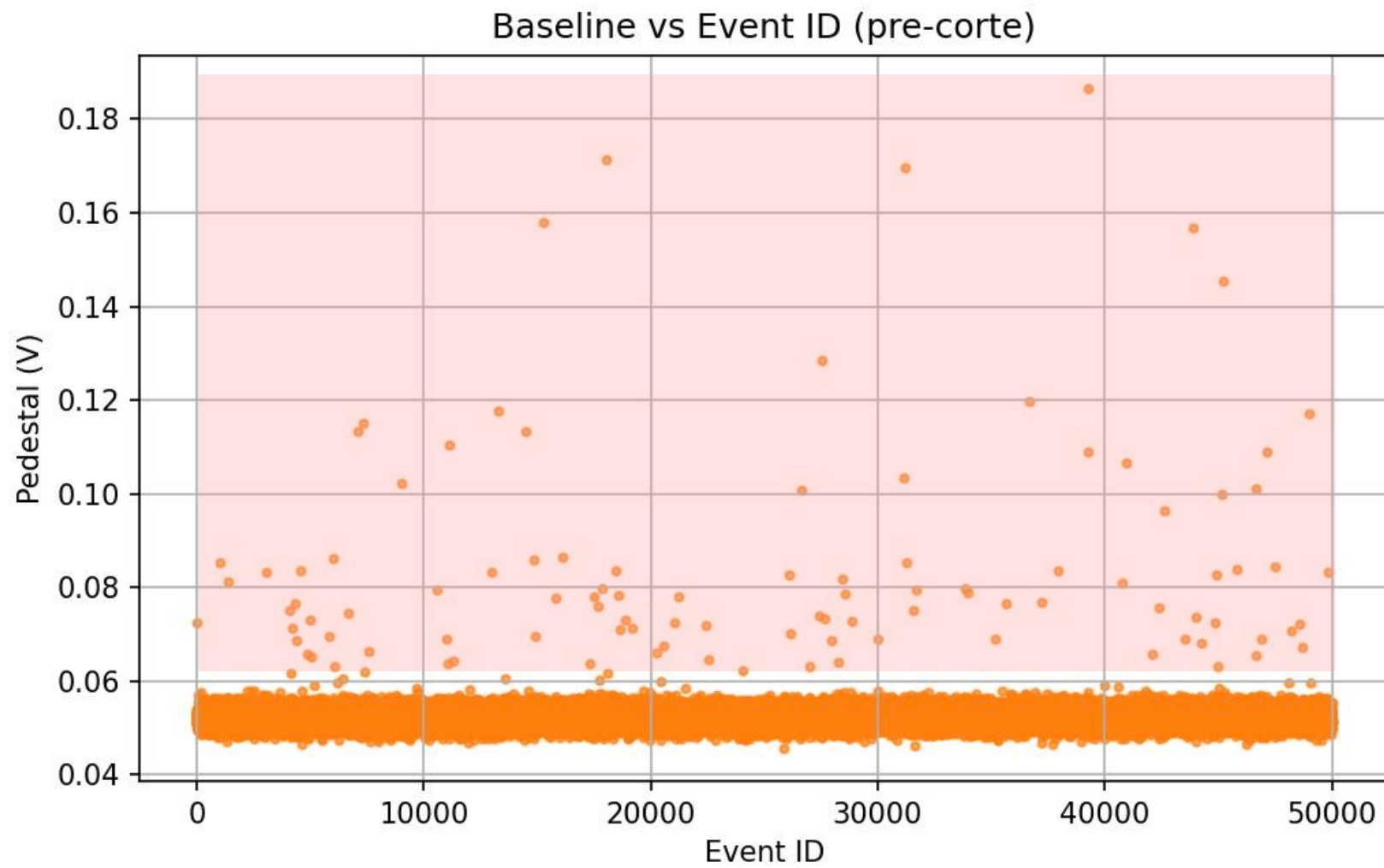
Correlation with DCR (if DCR is high, we expect PCR high too), but what about the opposite?

Python analysis to identify these events from the waveform level...

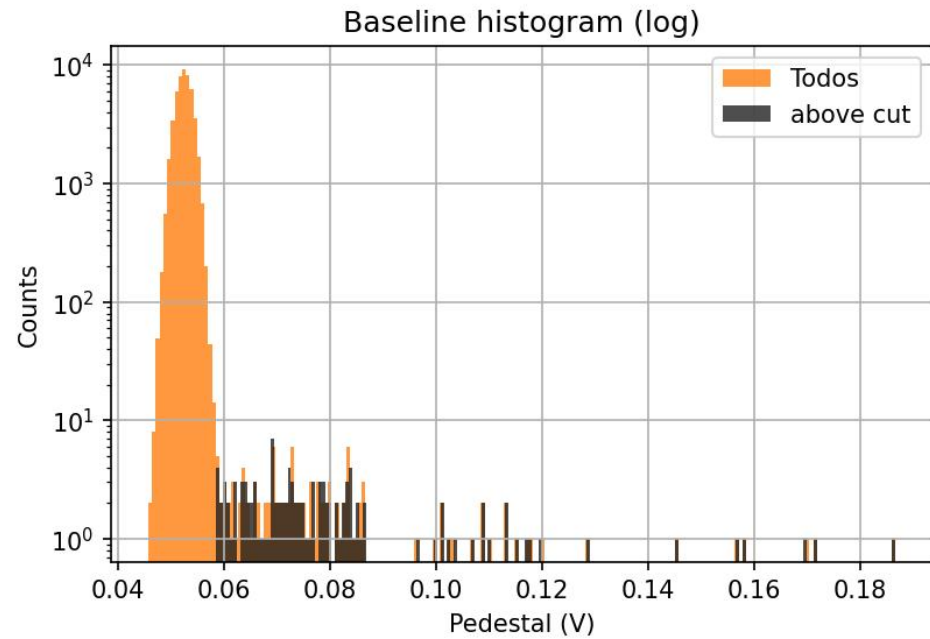
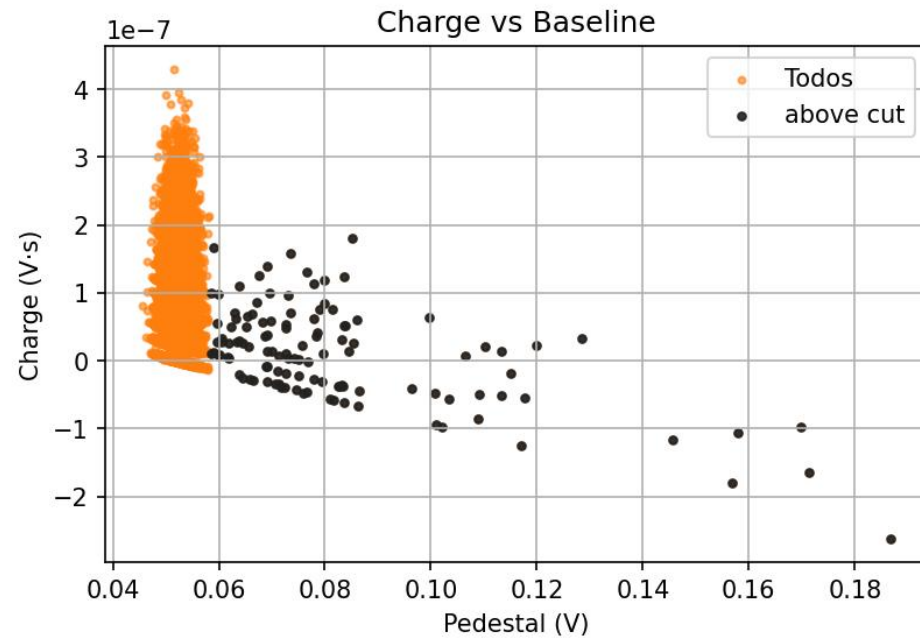
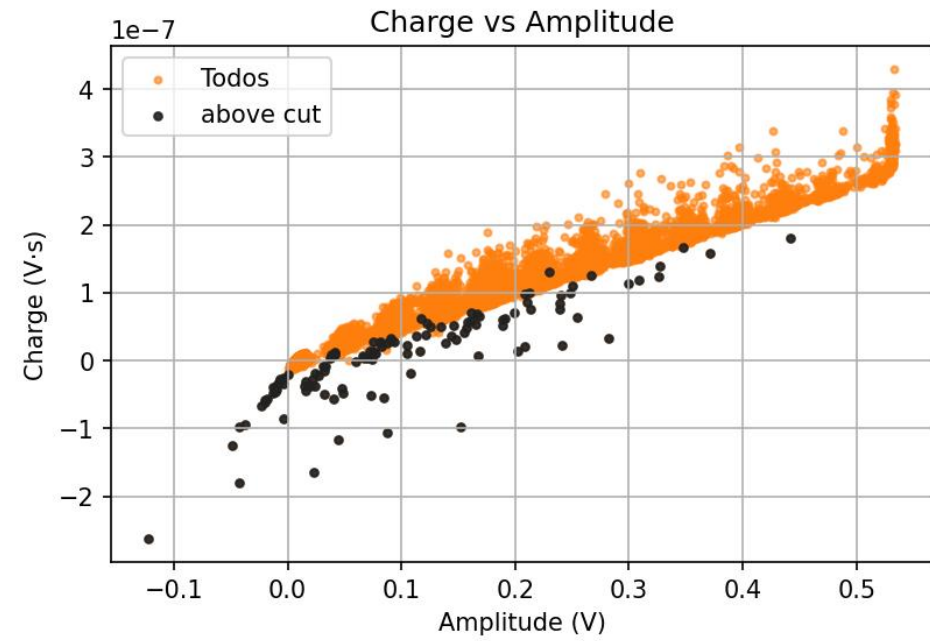
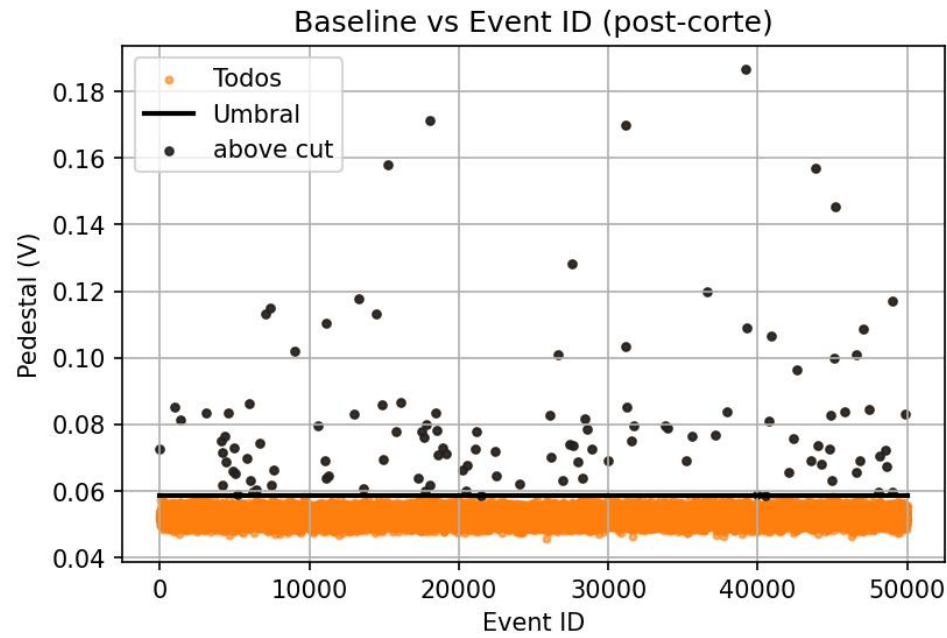






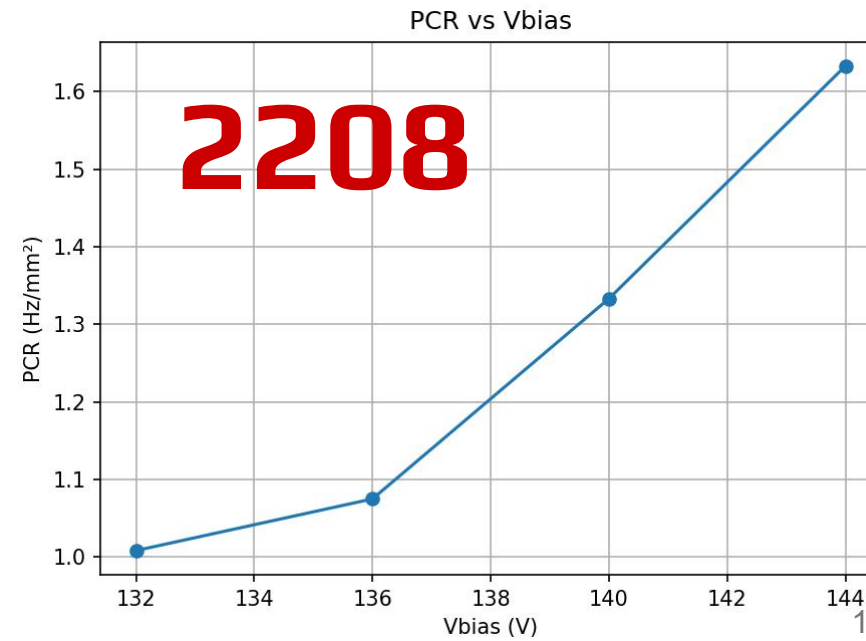
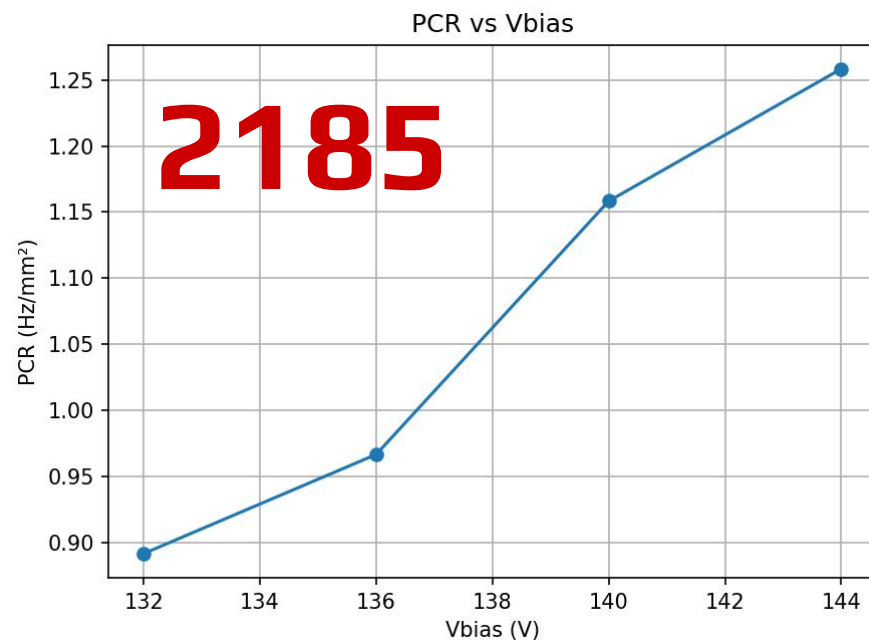
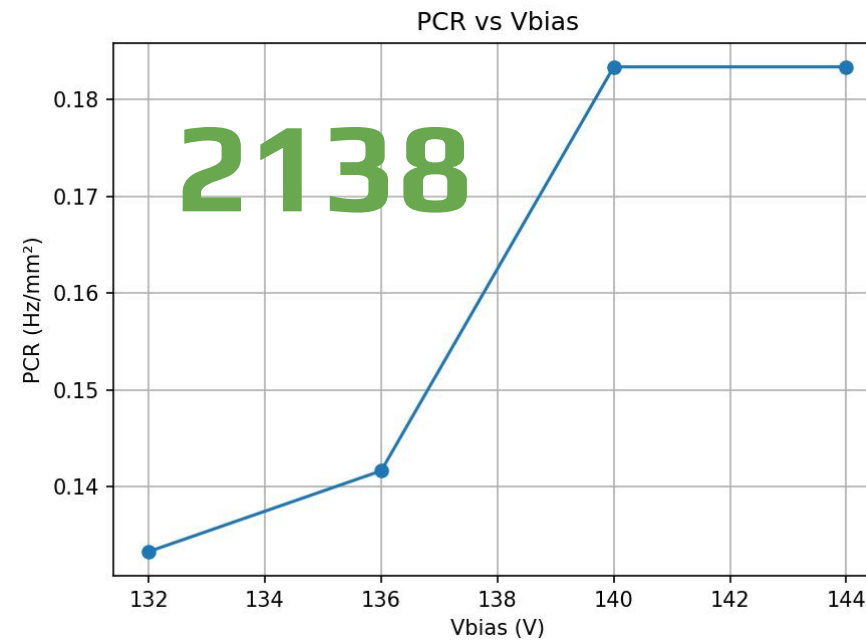
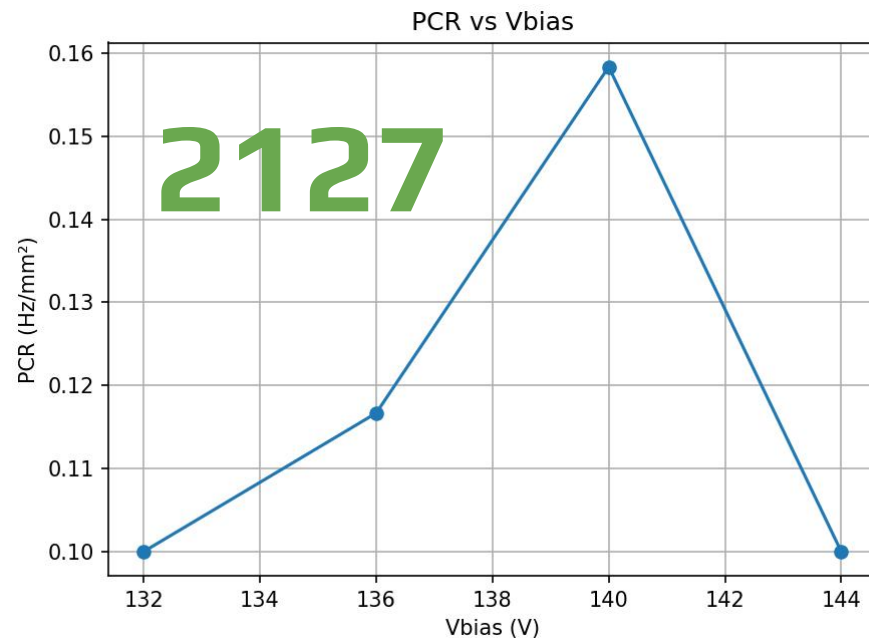


Tile02185 Cold 136V — Post-cut (k=4)

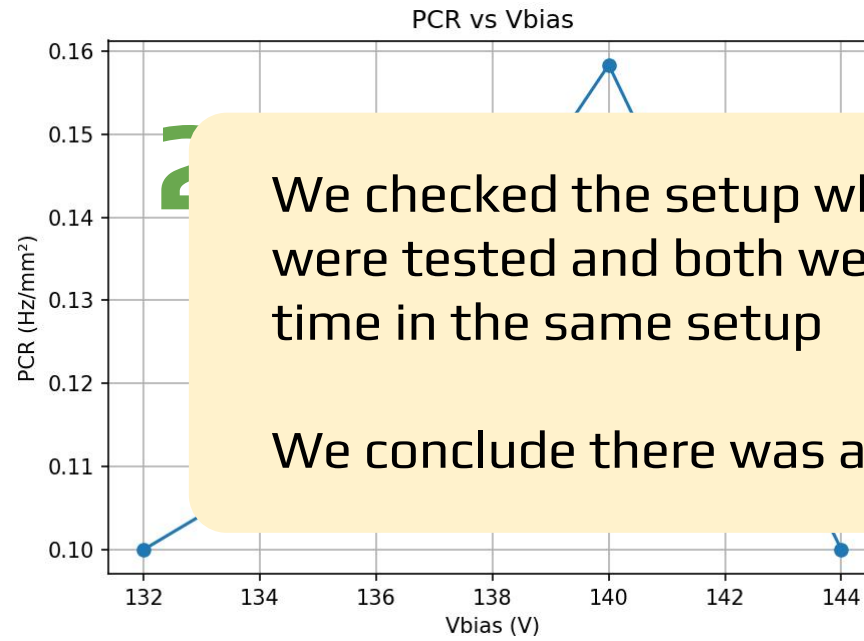




# PCR results

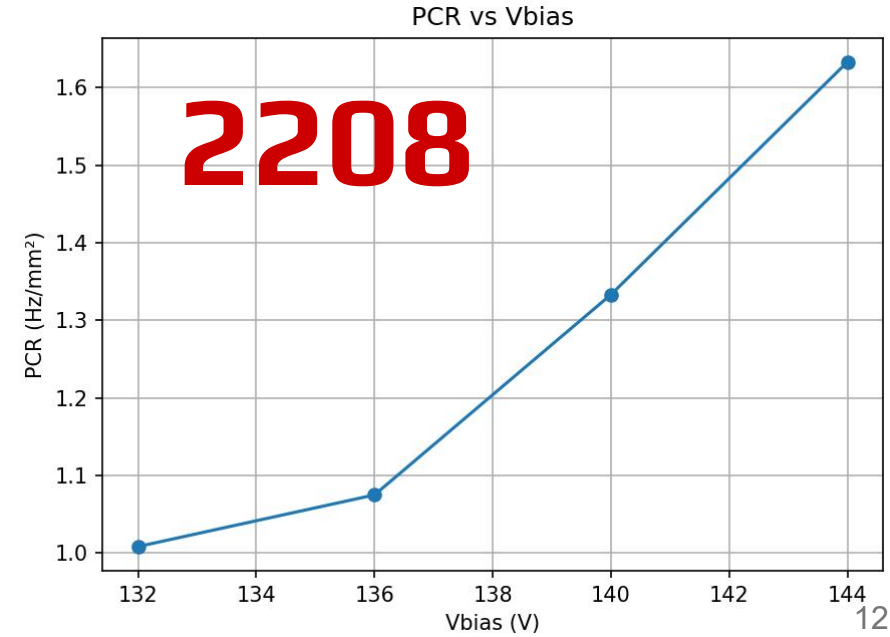
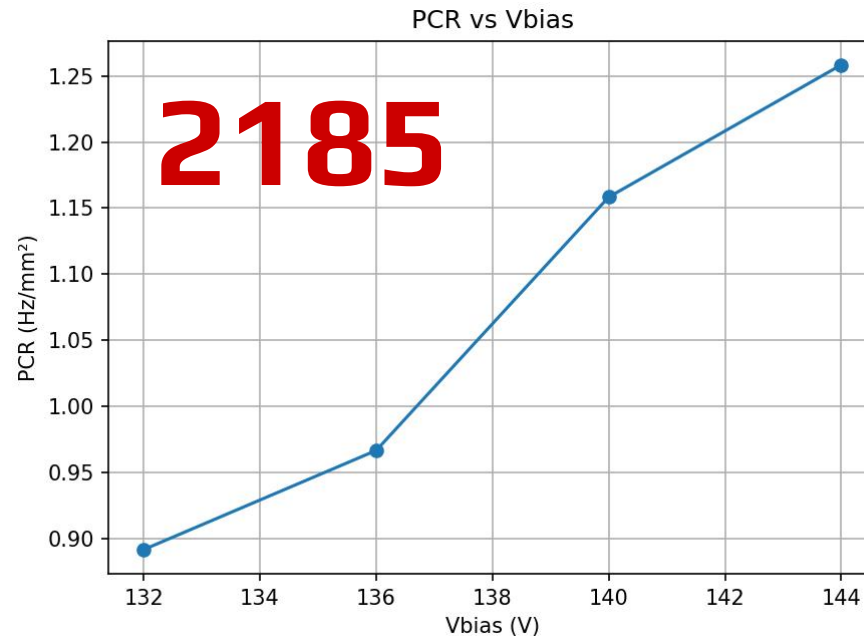
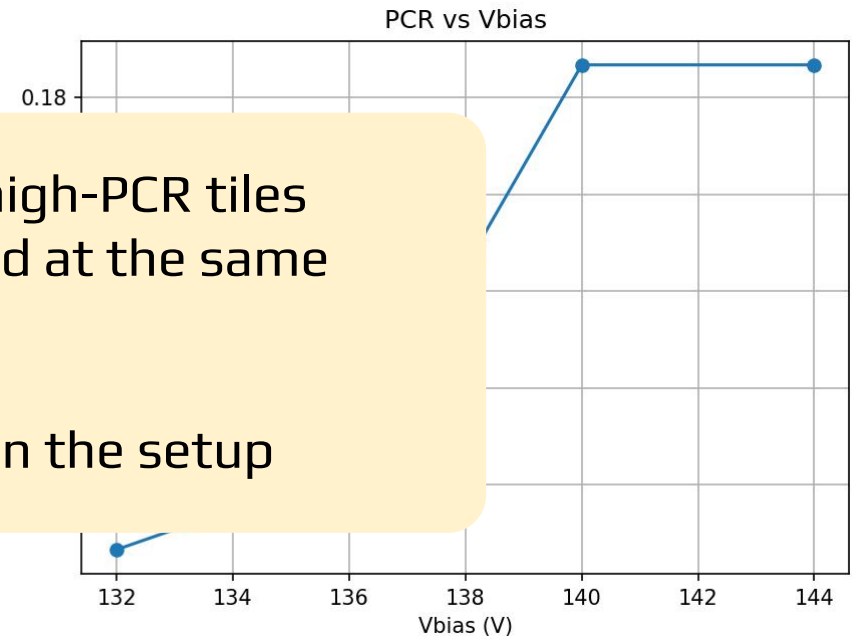


# PCR results

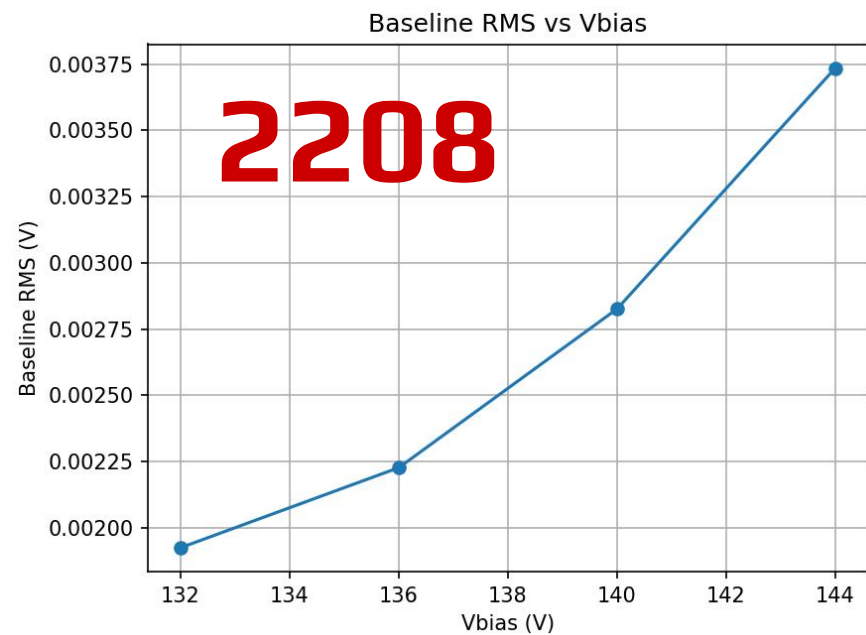
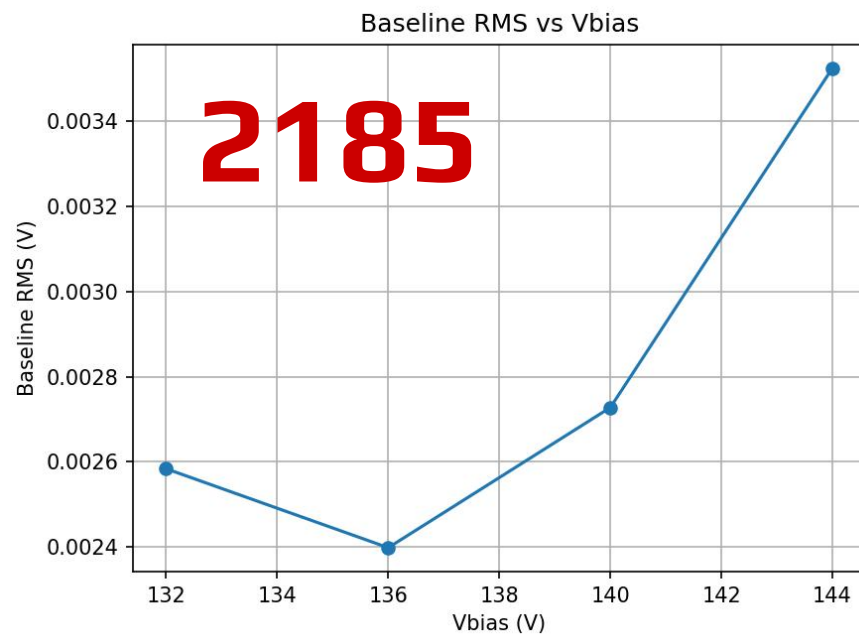
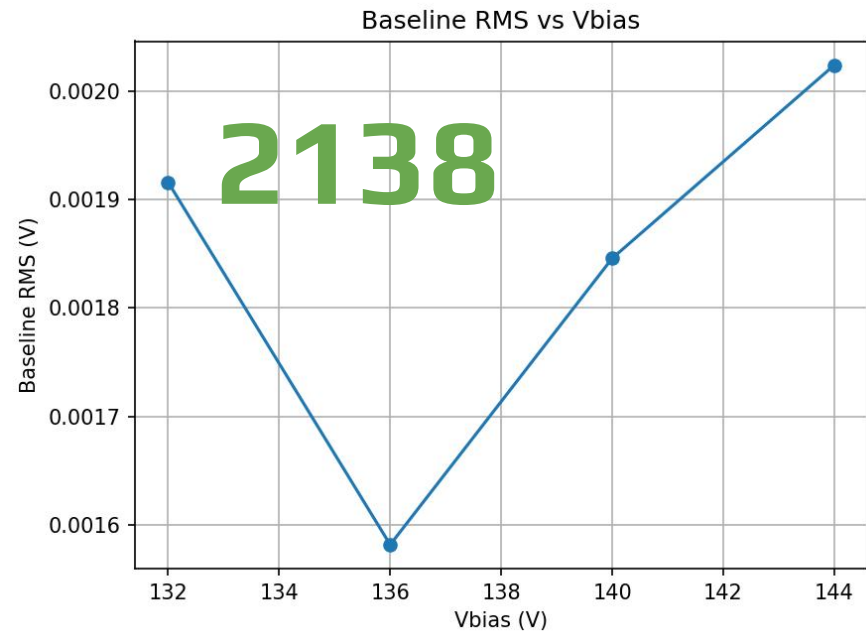
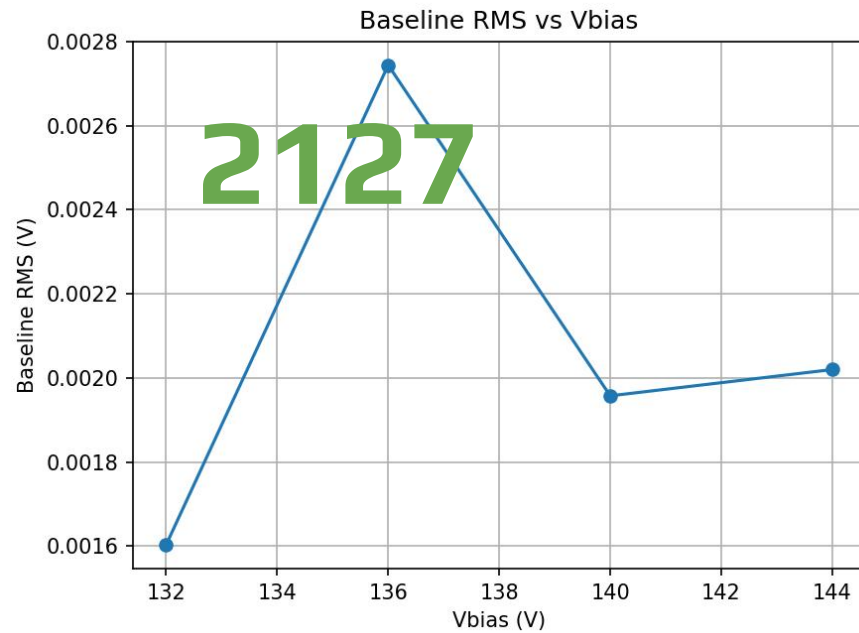


We checked the setup where the 2 high-PCR tiles were tested and both were measured at the same time in the same setup

We conclude there was a **light leak** in the setup

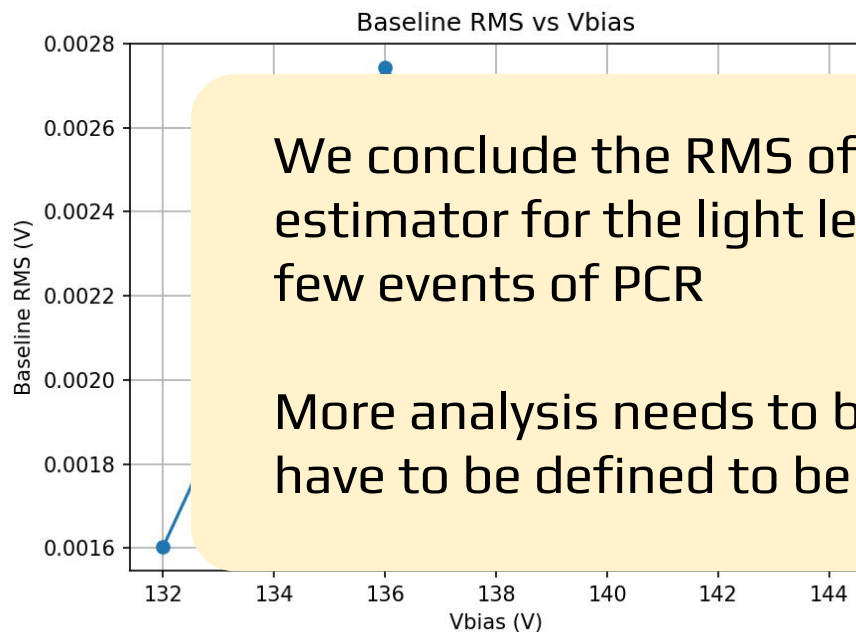


# Baseline RMS as a light leak estimator?



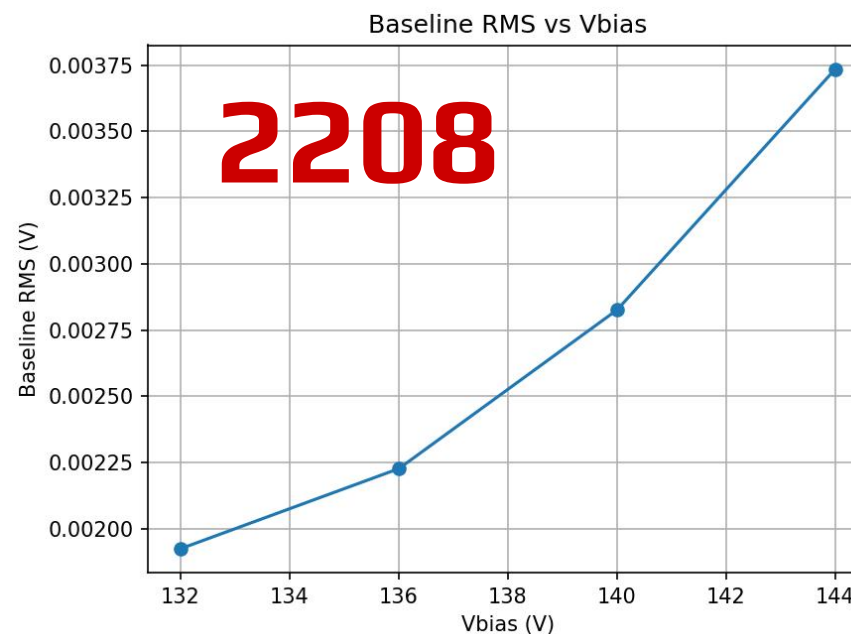
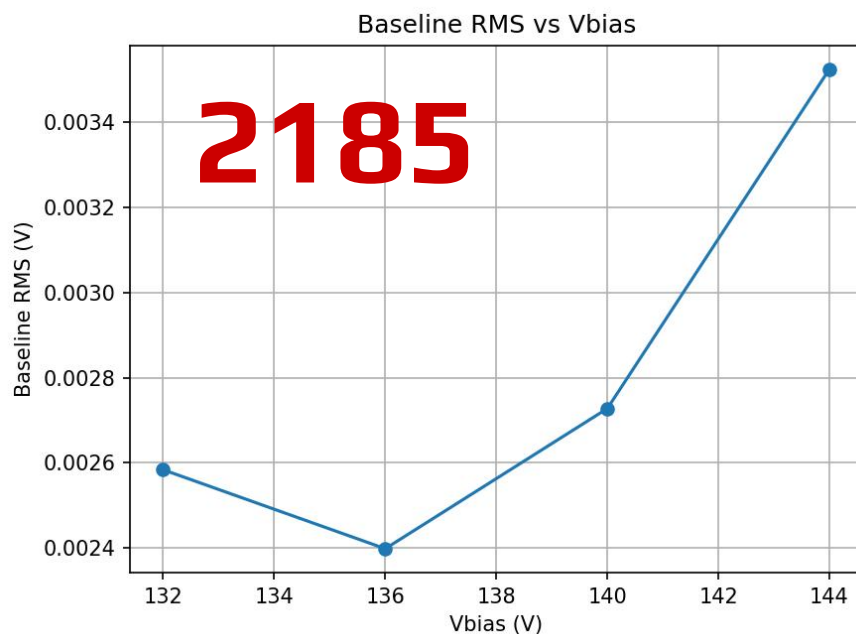
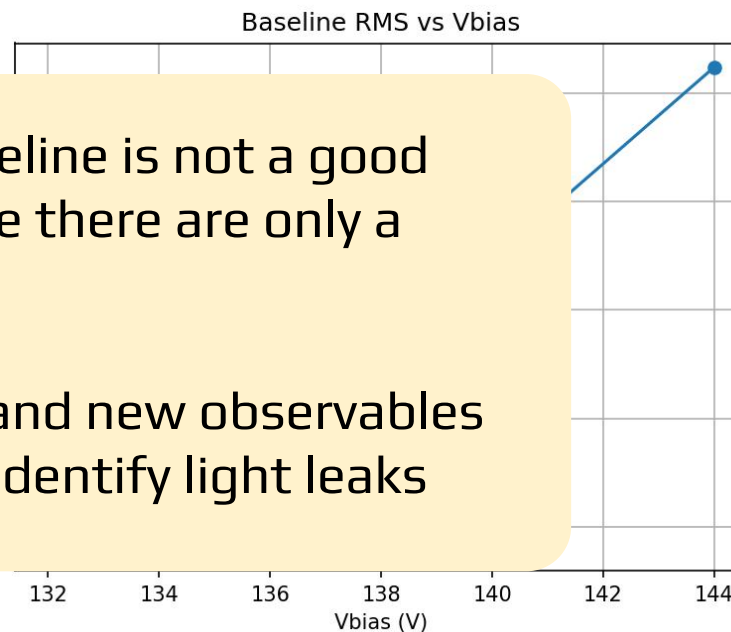


# Baseline RMS as a light leak estimator?

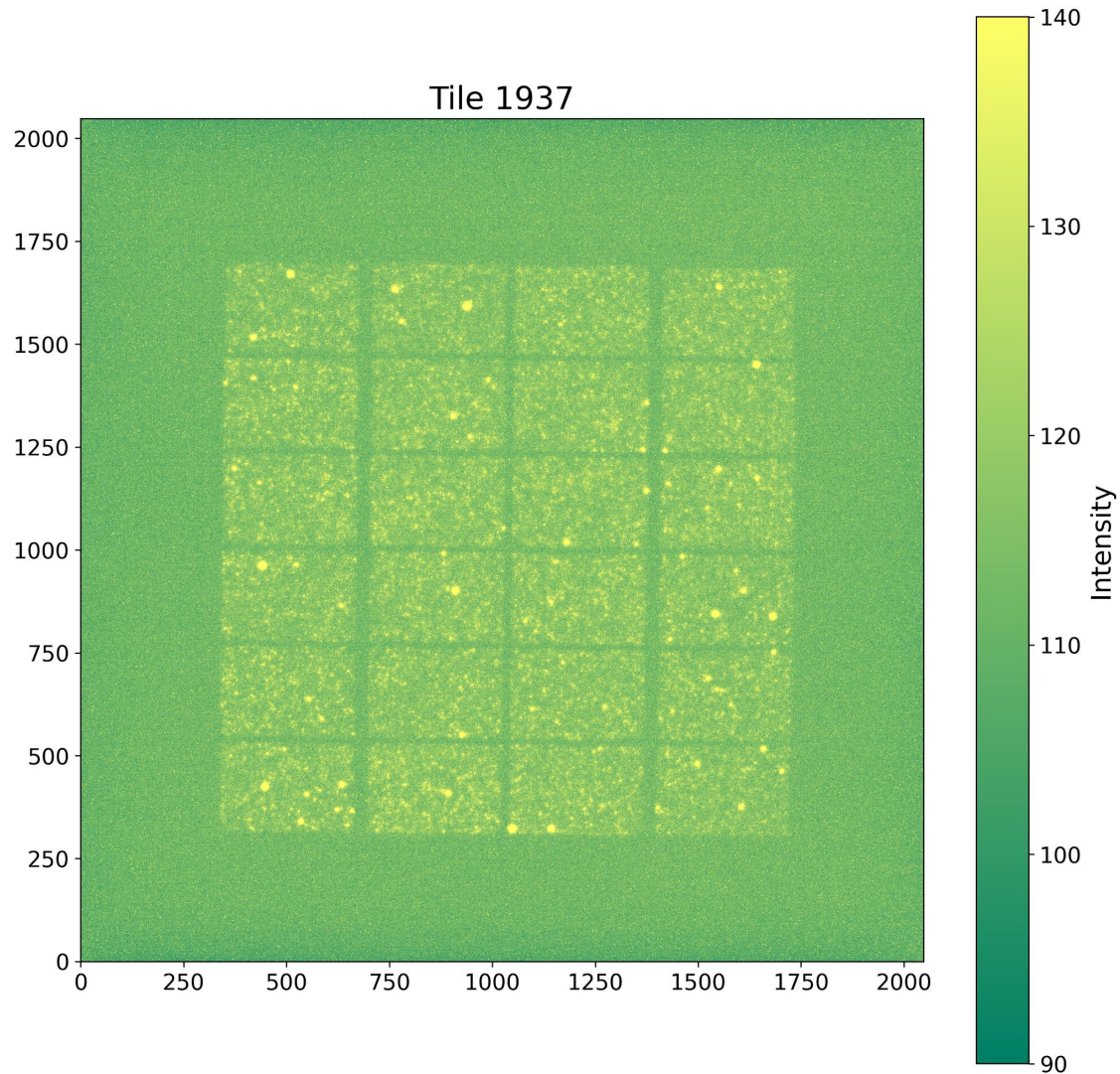


We conclude the RMS of the baseline is not a good estimator for the light leaks since there are only a few events of PCR

More analysis needs to be done and new observables have to be defined to be able to identify light leaks



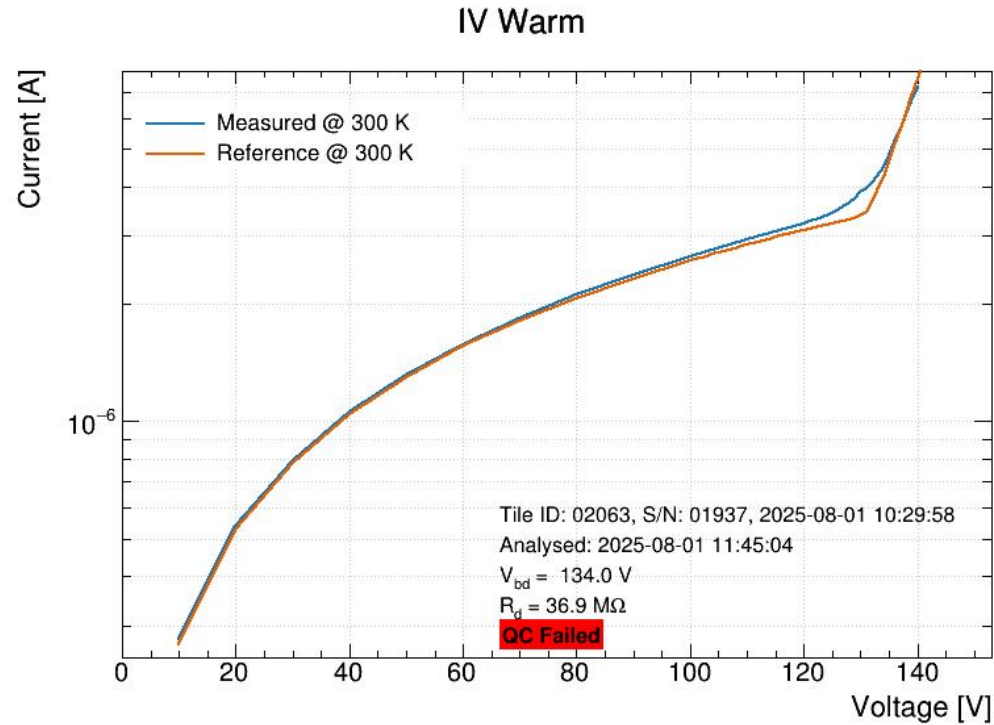
# Tile testing



## Tile #1937

- CMOS image doesn't show any damaged SiPM
- You can recognise bad SiPMs because they appear darker

# Tile testing

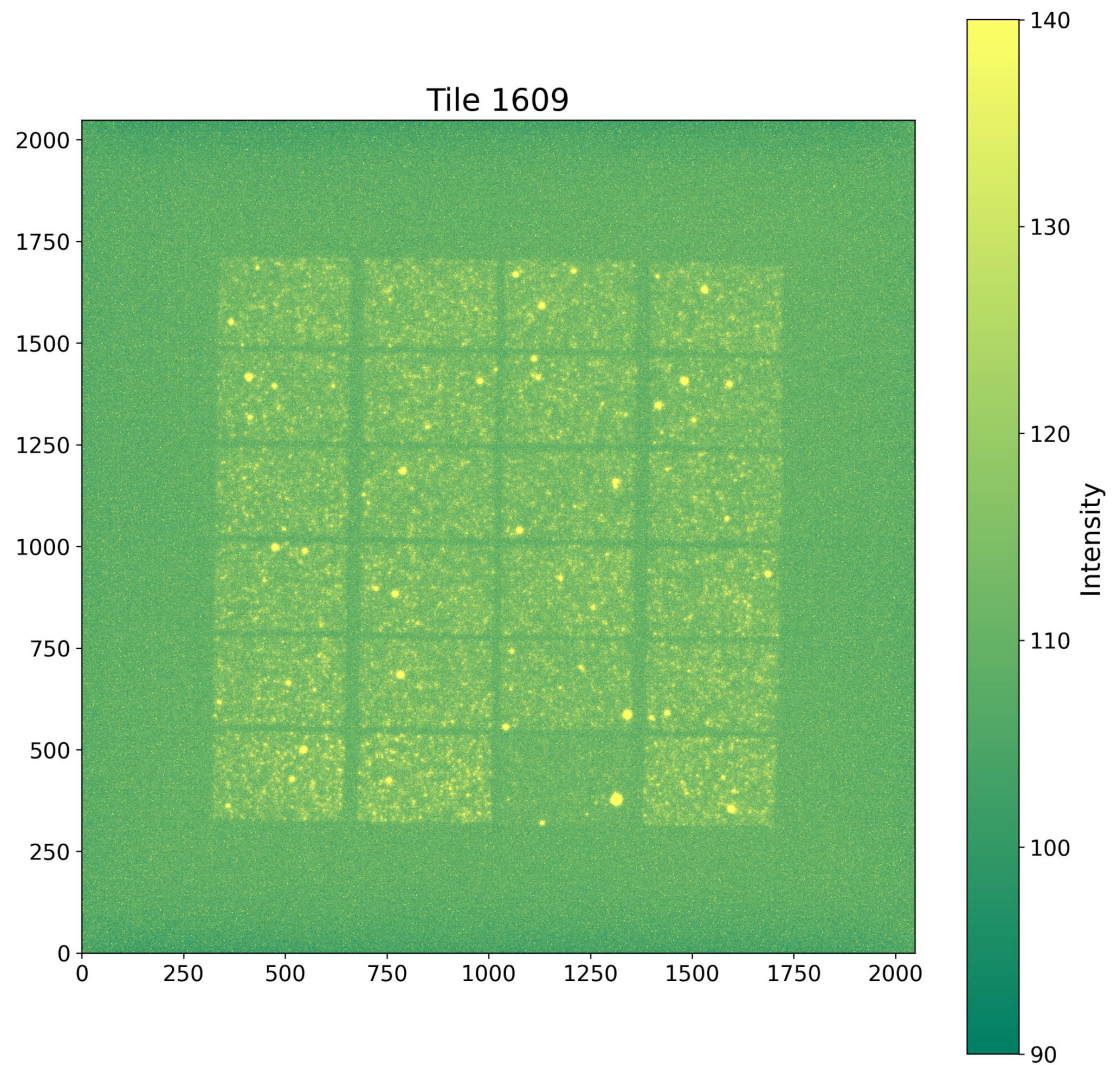


Even though from the CMOS image it seems that no SiPM is damaged, the IV Warm test failed because the measured breakdown voltage (blue line) is lower than the theoretical value (orange line, 132 V)

The other plots such as Noise Spectrum, Pulse Counting at 144V and 136V, and PCR curve are good.



# Tile testing

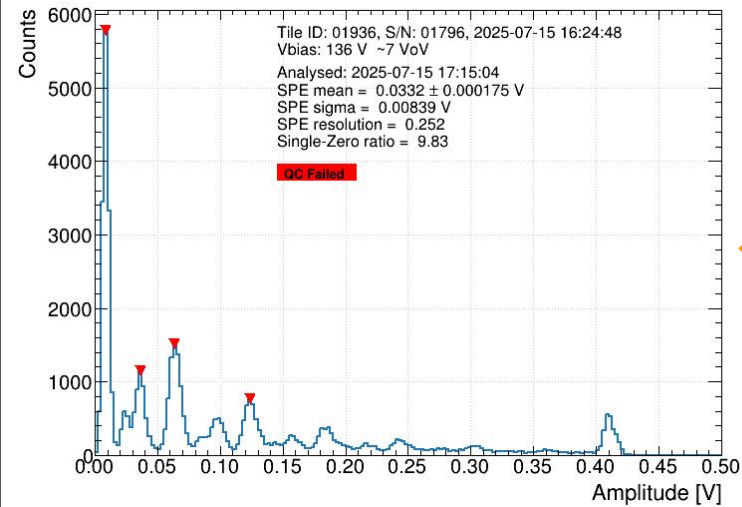


## Tile #1609

- The 3rd SiPM of the last row is darker so it is damaged

# Tile testing

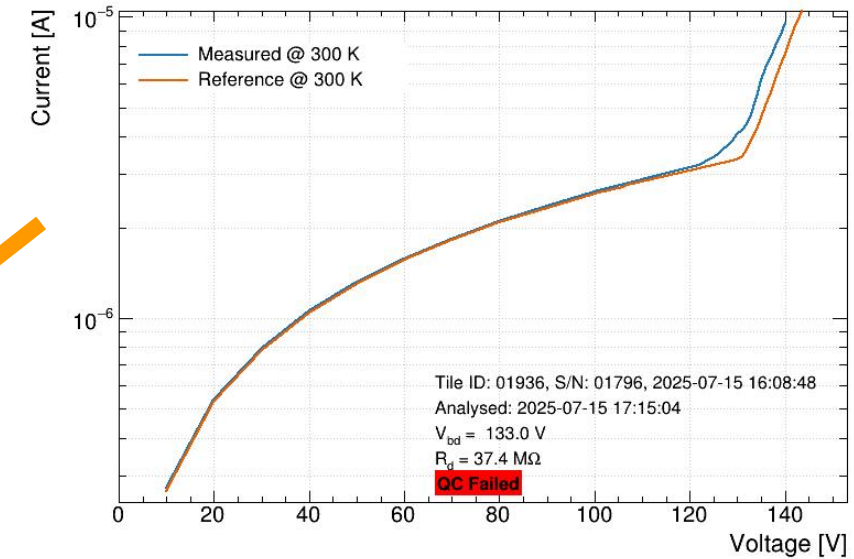
Pulse Counting at 136 V



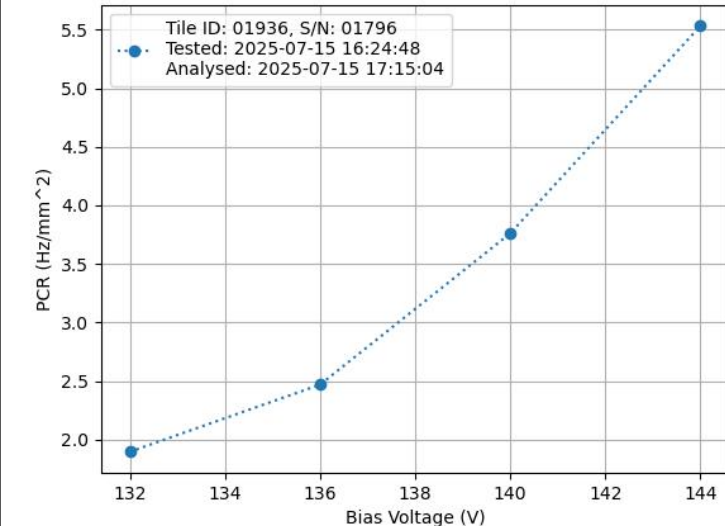
The Pulse Counting test failed because, as you can see, this is not a proper finger plot.

Regarding the IV Warm test, the measured breakdown voltage is lower than the theoretical value.

IV Warm



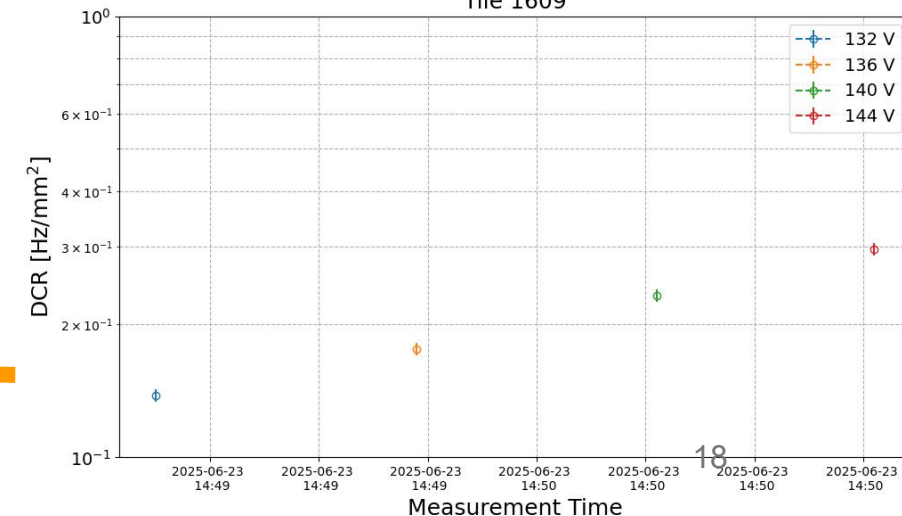
PCR vs Vbias



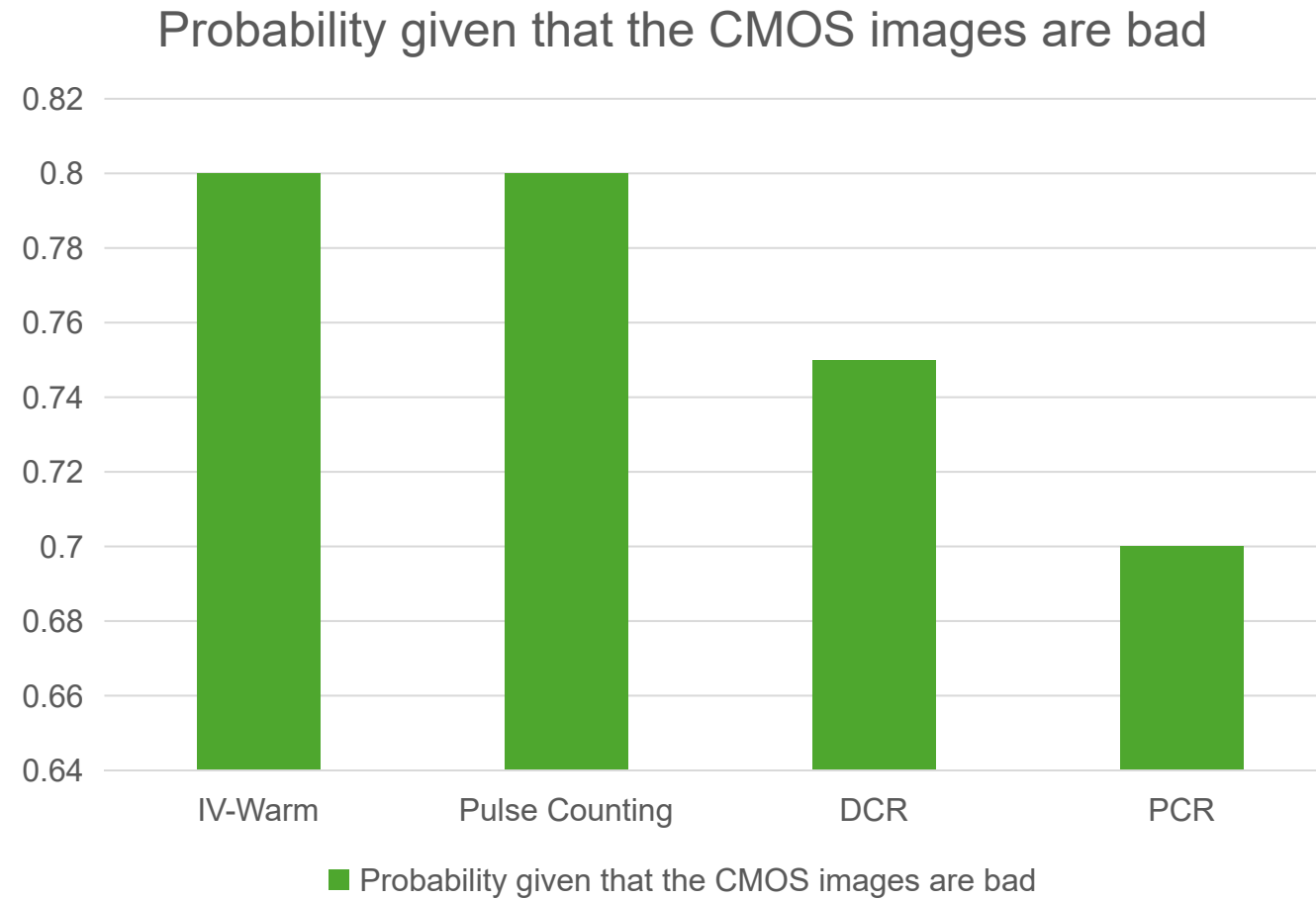
The maximum PCR value at 136V must be 0.3 while in our case it is 2.5

The maximum DCR value at 136V must be 0.1 while in our case it is 0.18

Tile 1609



# What we observed

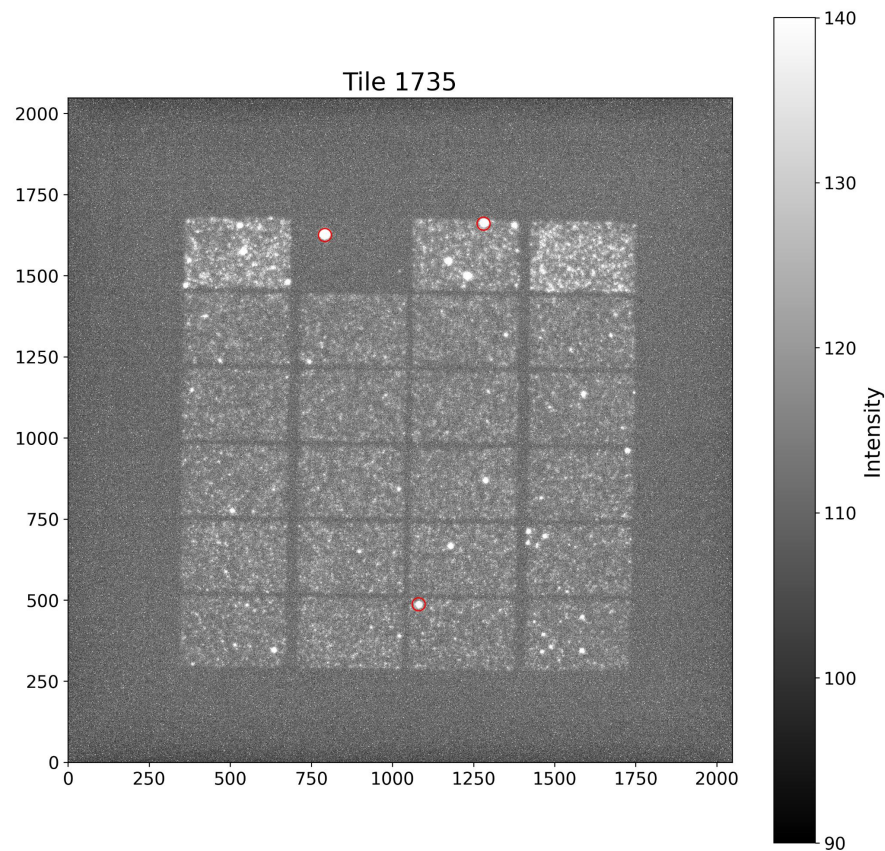


# What we found out

- Bad CMOS result is correlated with IV test failure, Pulse Counting test failure, high DCR and PCR values but this correlation is not conclusive, meaning we cannot tell which specific test failure will happen if the CMOS images show damaged SiPMs but we know that there will be at least a failure.
- In most cases the Noise Spectrum was good. Any problem with this kind of test is usually correlated to electronics.
- It is important to keep in mind that our sample space had few data points (particularly for the DCR values) so this results are not too conclusive.
- Additionally, as we observed for the tile #1937, sometimes the CMOS images are fine but the DCR and PCR values are too high or too low and the IV and Pulse Counting tests fail so we can conclude that CMOS images are not a reliable indicators of any bad results.

# CMOS pictures analysis

We also investigated the possibility of a more quantitative and systematic approach, analysing the pixel matrix of the CMOS images.

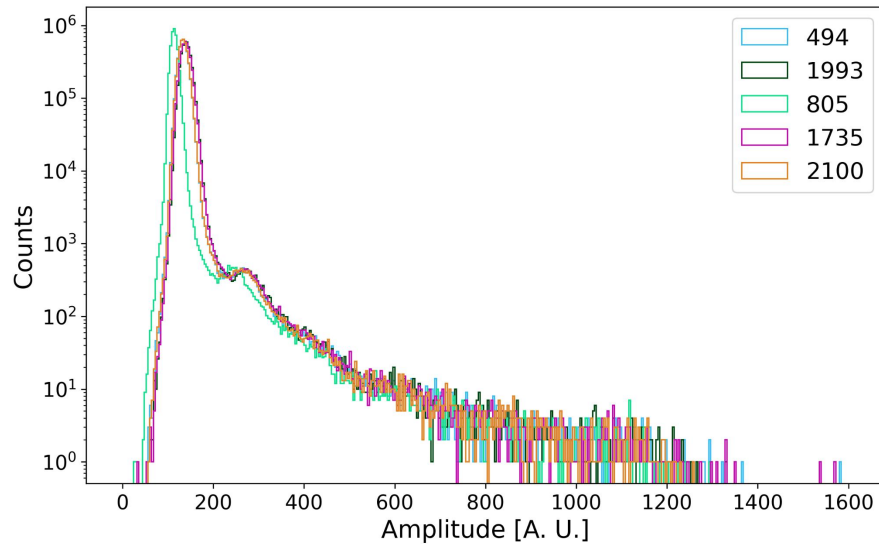


Example of peak finding algorithm applied on a damaged tile:

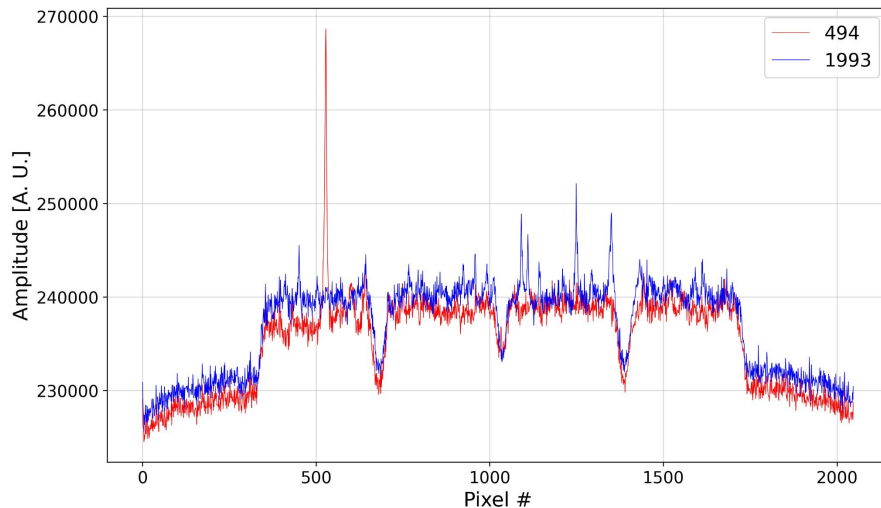
- a precise tuning would be required to obtain a reliable technique
- from rough analysis no dependence of DCR with respect to number and intensity of peaks has been found
- ML techniques could help, but training data would be required



# CMOS pictures analysis



Amplitude distributions do not provide any separation

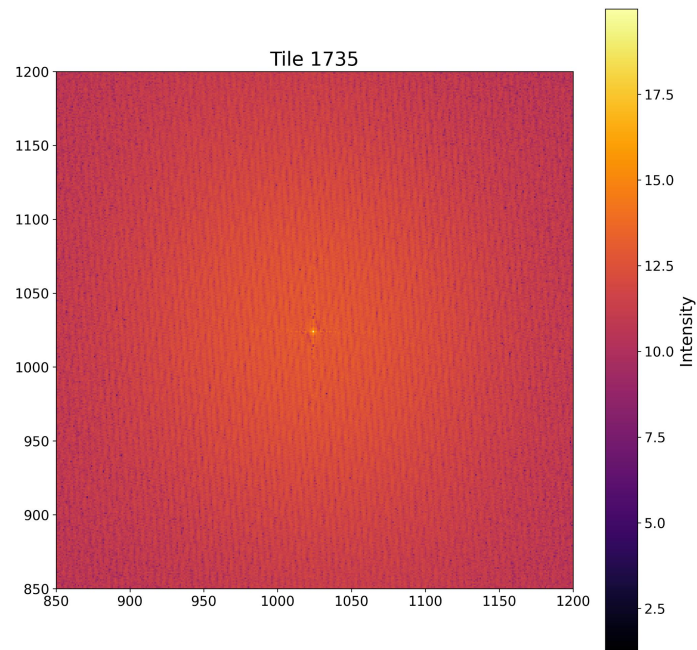


1D projections sometimes spot hidden spikes but they are not predictive on the DCR:

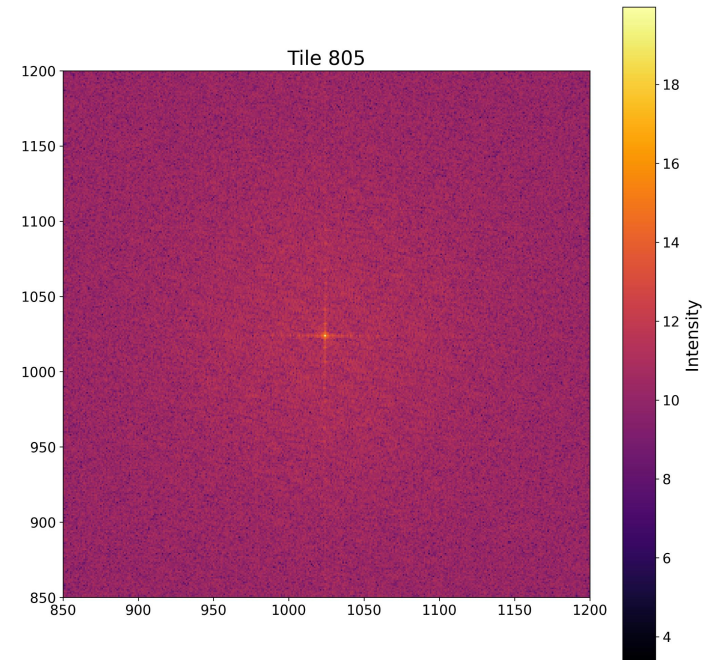
- 494 has low DCR
- 1993 has high DCR

# CMOS pictures analysis

A spatial Fourier analysis has also been attempted



low DCR tile



high DCR tile

- Some differences are visible in Fourier space
- Whether this can have an application is an open question

# Conclusions: What we have done

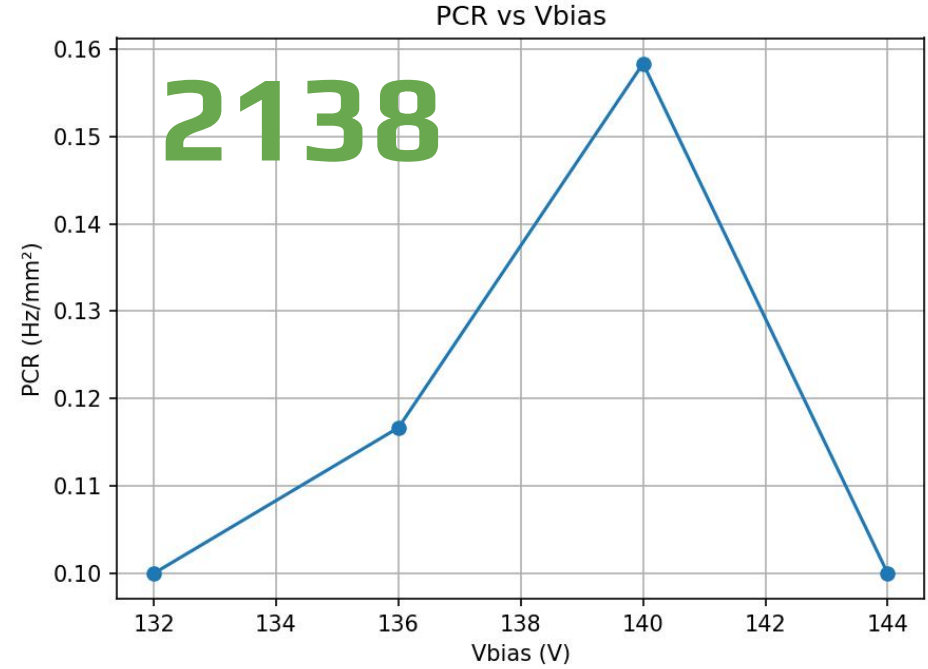
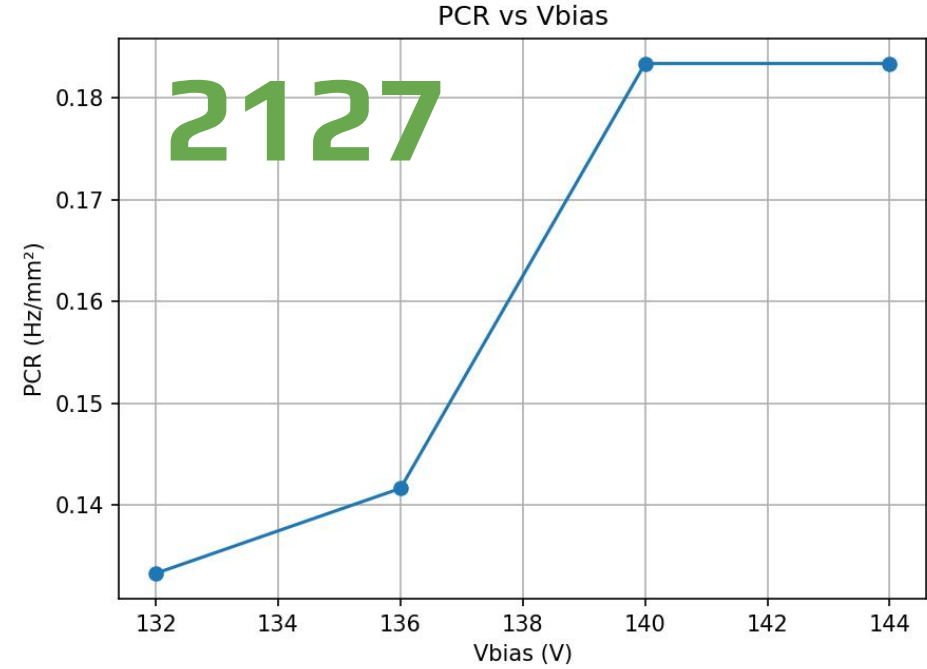
- Familiarize ourselves with procedures of tile quality testing.
- Develop a waveform-level analysis to estimate the PCR and checked different observables to identify light leaks.
- Discover if a correlation between CMOS results and other tests exists.
- Be able to predict which specific type of failure will happen based on the CMOS images.
- Find a more quantitative way to study CMOS results.

# Thanks for listening!





Good PCR tiles show values <0.3 Hz/mm<sup>2</sup>



# Tile02127 Cold 140V — Post-cut (k=4)

