Electronics, **DAQ** and signal processing techniques

Pierre-André Amaudruz

TRIUMF, Vancouver, BC, CANADA

What does DAQ mean?

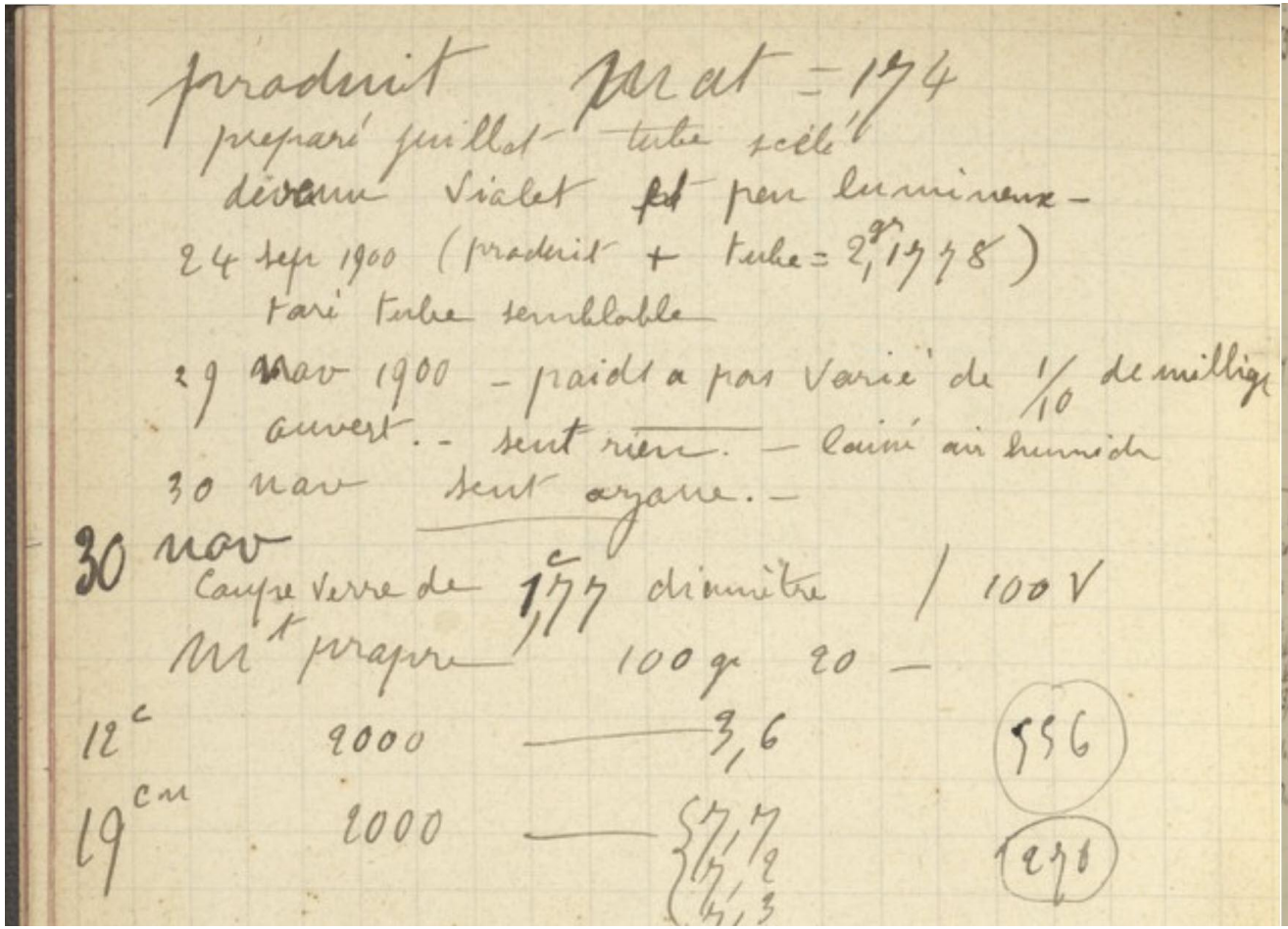
Data **Ac****Q**uisition…

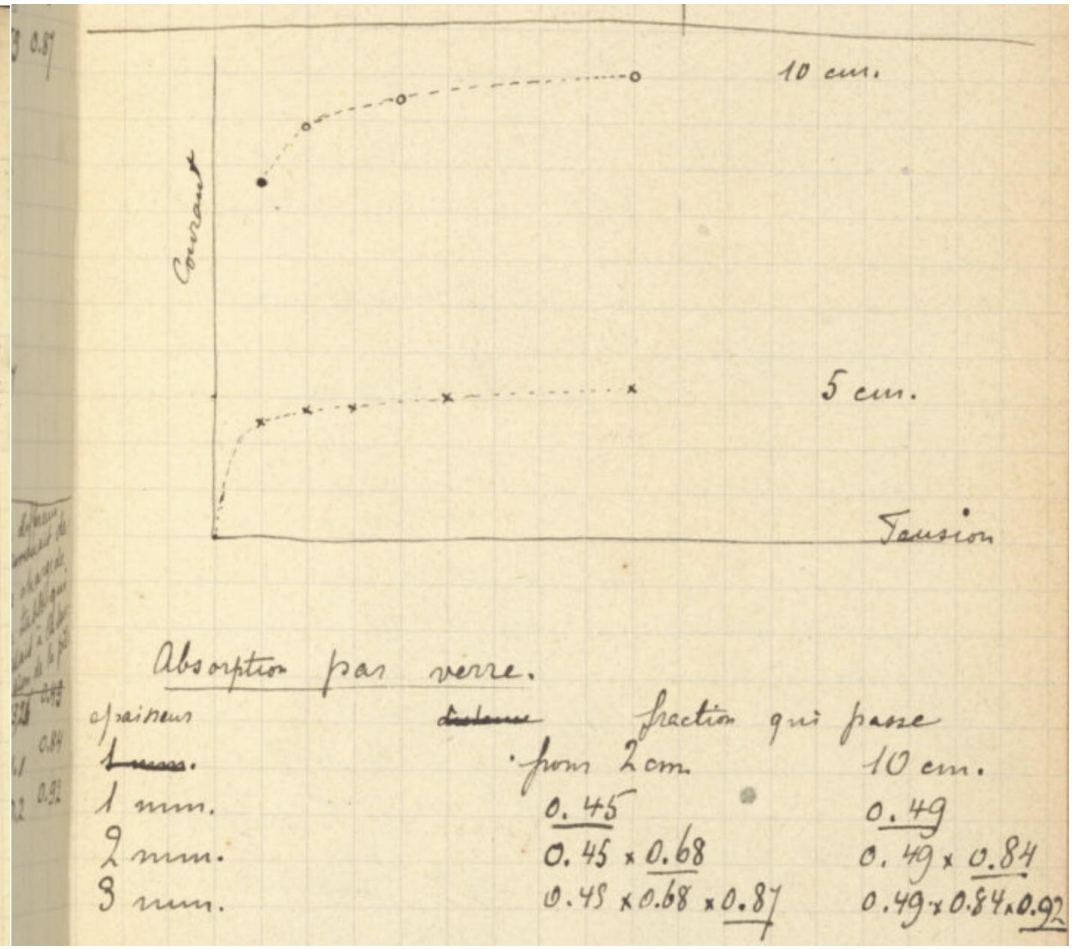
Data **information** “converted” into numbers to be able to digitally manipulate the “information”

Acquisition refers to the **Equipment** involved in the extraction, conversion and gathering of the “data”

How did we do it before our time?

Pencil, Paper and Patience (PPP)





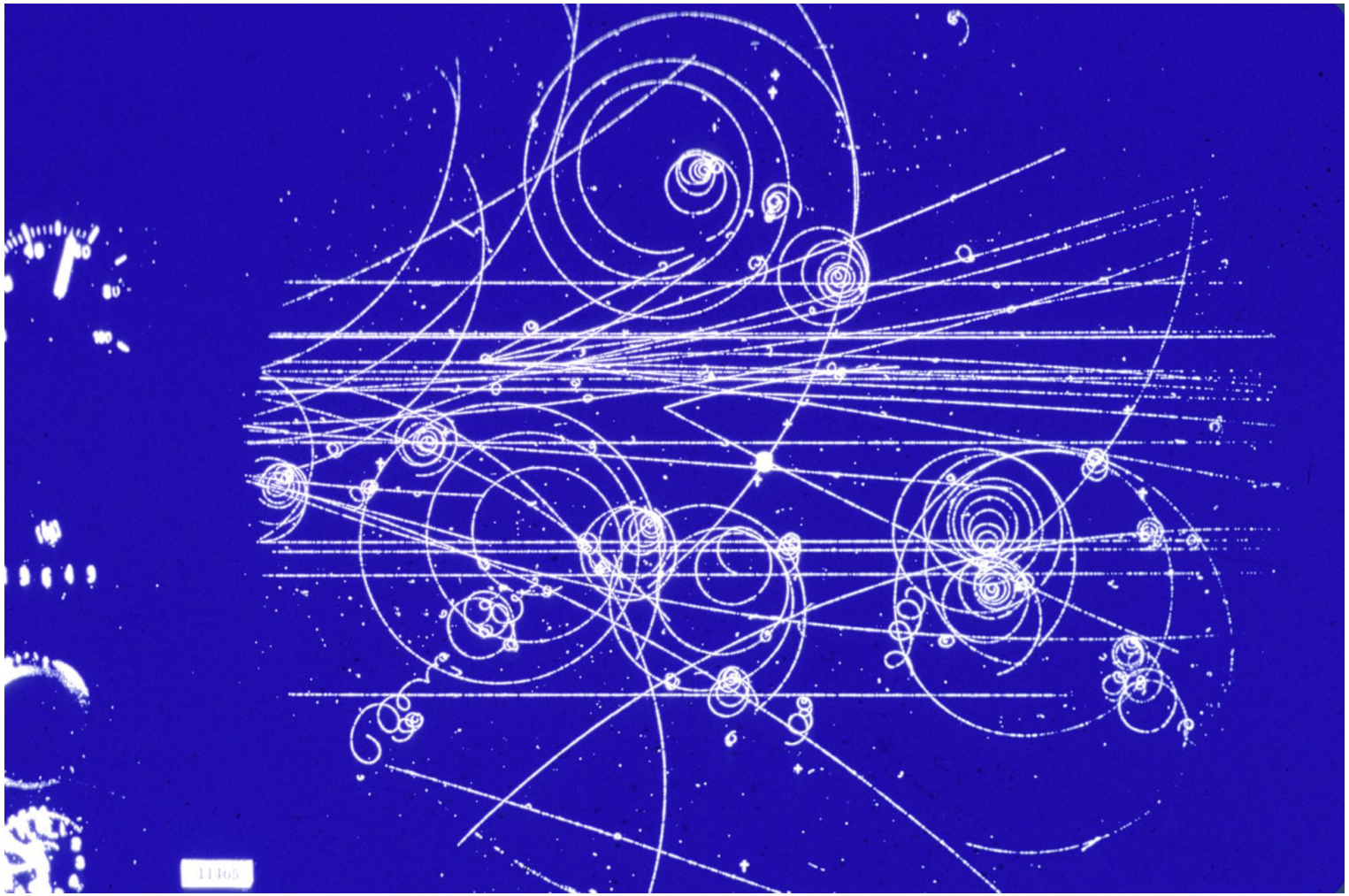
Curie, Marie, 1867-1934.

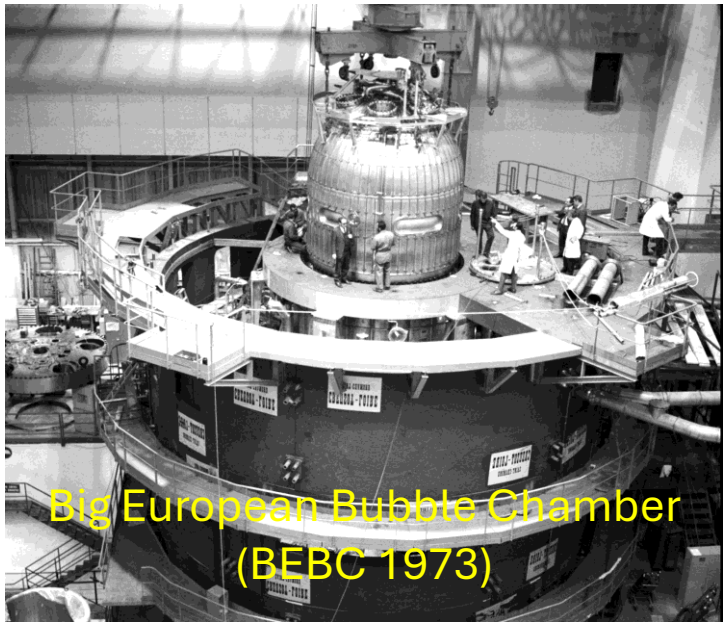
Nobel Prize 1903, Physics for her research of radiation phenomena.

Nobel Prize 1911, Chemistry for the discovery of polonium and radium.

Logbook Marie Curie ~1900

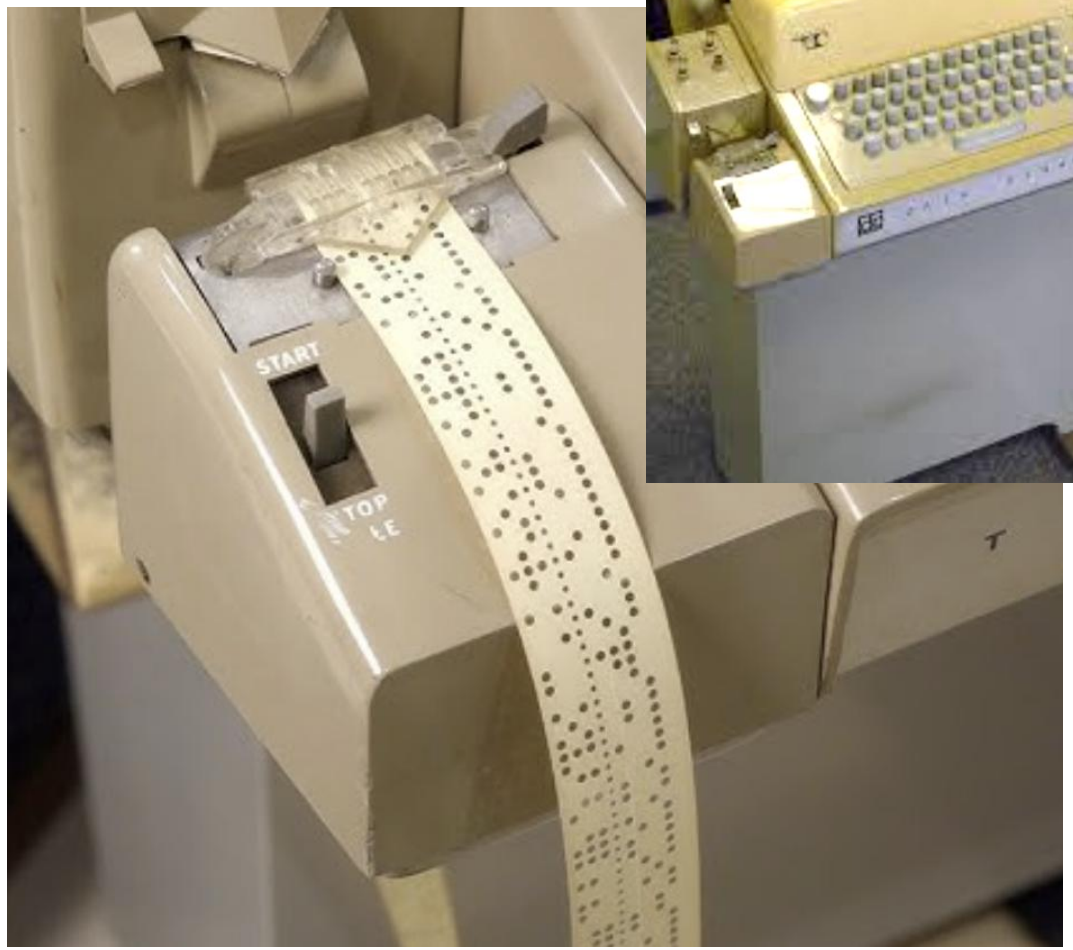
Pencil, Paper, Patience and Ruler

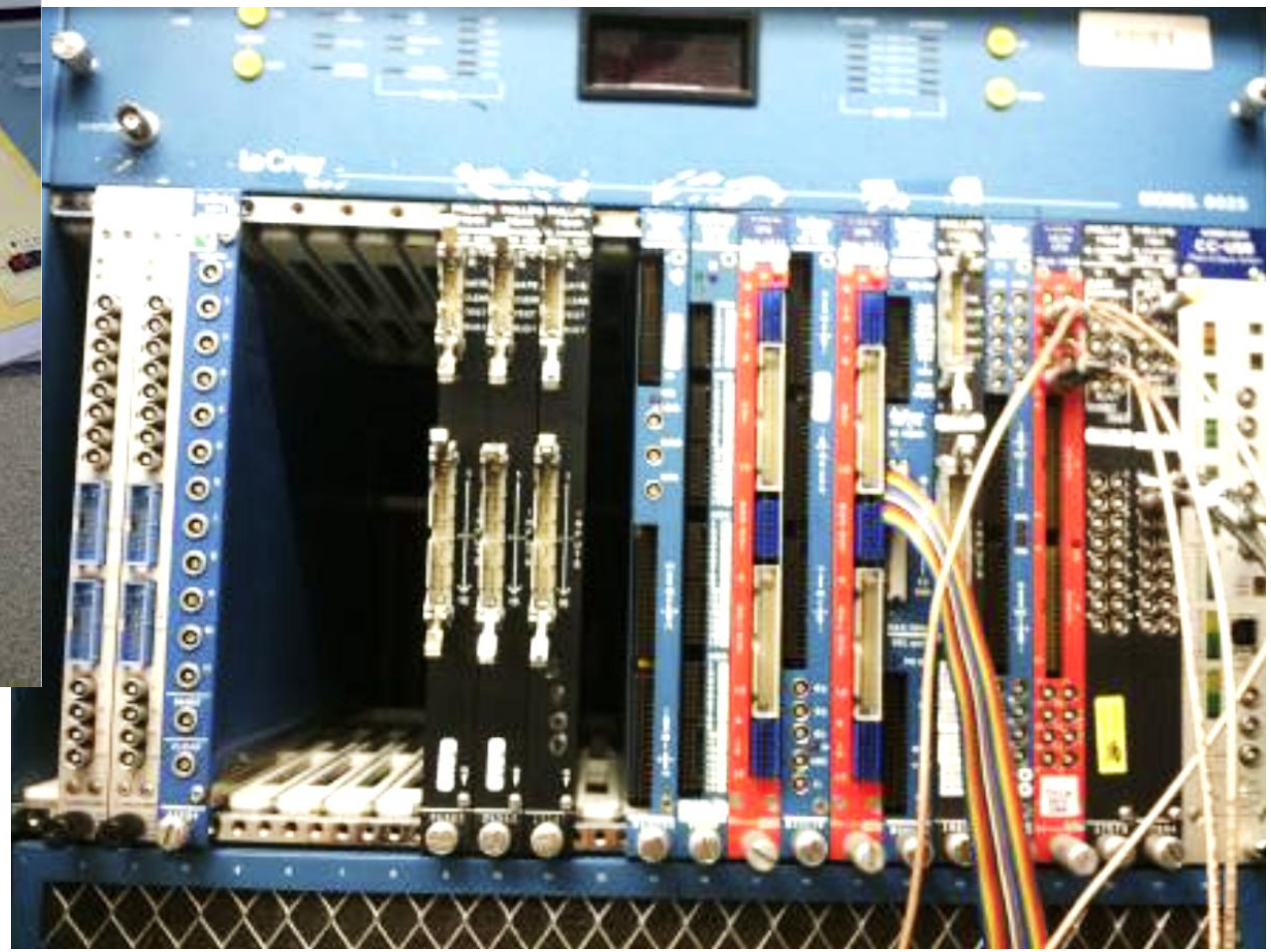




Bubble Chamber event
INFN - National Institute for Nuclear Physics (Trieste Section) - Sistema Scientifico

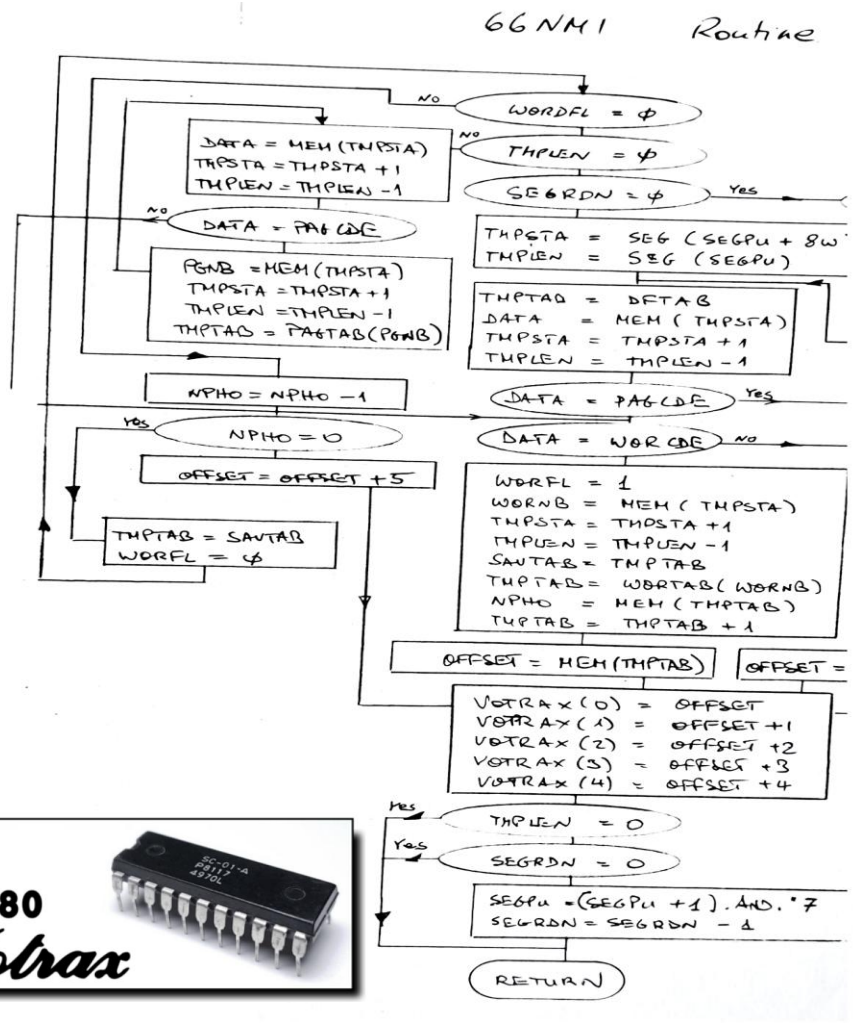
Teletypewriter





7, 8 bits paper coding for CAMAC (’70)
(**C**omputer **A**utomated **M**easurement **A**nd **C**ontrol)

Microprocessors (CPU Z80, MC6800, Intel8080)




```
_S1$DUS1:[AMAUDRUZ.LIBELLULE.BACKUP]66NMI.ASS;1    14-AUG-19

        66NMI routine
        =============

description :
This segment contains the NMI#0066 routine.
It takes care of the VOTRAX ship for speaking.
It can be addressed only by the NMI hardware request

PAGEO   : F42E          RUN     : F43C          A
SATAB   : F438                                  B
SEGRDN  : F424                                  D : tmplen
SEGO    : F426                                  H : tmpsta
SEGPU   : F42A                                  IX: tmptab
WORFL   : F432                                  IY
WORDO   : F430
SPEAK   : F440                  PAGCDE  : FD
SPKFL   : F434                  WRDCDE  : FE
NPH     : F43A
DFTAB   : F436
REGO    : 80    REG1    : 81    REG2    : 82    REG3    : 8

*****************************************************************
0060    : Start address
*****************************************************************
c
c       GETNMI should not start at 0066 to allow the call f
c
c
FFFFFF  0060
FFFFFF  0063
D9      0066            EXX             switch registers
08                      EX              switch register
0000                    NOP
000000                  NOP
00                      NOP
00                      NOP
3A32F4          begin   LD A,(WORFL)
A7                      AND A
C28A01                  JP NZ 'word'    word in progress =>
7A                      LD A,D
B3                      OR E
C24C01                  JP NZ 'nth'     check TMPLEN # 0 =>
3A24F4                  LD A,(SEGRDN)
A7                      AND A
CA7001                  JP Z 'speak'    check SEGRDN = 0 =>
**
** First path to GETNMI then prepare the work
3A2AF4                  LD A,(SEGPU)    load segment pointe
2A26F4                  LD HL,(SEGO)    load start address
85                      ADD L
3001                    JP NC 'a'
24                      INC H
6F              a       LD L,A          get segment index f
5E                      LD E,(HL)       load low byte of TM
23                      INC HL          next
56                      LD D,(HL)       load high byte of TH
3E0F                    LD A,#0F        move to the SEG(0+H
85                      ADD L
3001                    JP NC 'b'
24                      INC H
6F              b       LD L,A          get segment index f
4E                      LD C,(HL)       load low byte of sta
23                      INC HL          next
```

```
_S1$DUS1:[AMAUDRUZ.LIBELLULE.BACKUP]VOTRAX.VO5;1   14-AUG-1987

[#0000 31 FF FF 21 00 20 36 00 7C D3 90 23 7C B5 20 F6
#0010 3E D0 D3 90 CD 00 02 DB 89 FB C3 00 04

#0030 FF FF FF FF FF FF FF FF F5 C5 D5 E5 CD 00 03 DB
#0040 89 E1 D1 C1 F1 FB ED 4D

#0060 FF FF FF FF FF FF D9 08 00 00 00 00 00 00 00 3A
#0070 32 F4 A7 C2 8A 01 7A B3 C2 4C 01 3A 24 F4 A7 CA
#0080 70 01 3A 2A F4 2A 26 F4 85 30 01 24 6F 5E 23 56
#0090 3E 0F 85 30 01 24 6F 4E 23 46 60 69 DD 2A 36 F4
#00A0 7E 23 1B FE FD 20 1D 7E 23 1B E5 D5 2A 2E F4 CB
#00B0 27 30 01 24 85 30 01 24 6F 5E 23 56 ED 53 36 F4
#00C0 D1 E1 18 D8 FE FE 20 2E 3E 01 32 32 F4 7E 23 1B
#00D0 DD 22 38 F4 E5 D5 2A 30 F4 CB 27 30 01 24 85 30
#00E0 01 24 6F 5E 23 56 1A 32 3A F4 13 D5 DD E1 D1 E1
#00F0 DD E5 18 1C 3E 00 DD E5 4F 06 00 CB 27 30 02 CB
#0100 C0 CB 20 CB 27 30 02 CB C0 81 30 01 04 4F DD 09
#0110 DD 7E 04 D3 84 DD 7E 03 D3 83 DD 7E 02 D3 82 DD
#0120 7E 01 D3 81 DD 7E 00 D3 80 DD E1 7A B3 20 19 00
#0130 00 00 3A 24 F4 A7 28 10 47 3A 2A F4 3C 3C E6 0F
#0140 32 2A F4 78 3D 32 24 F4 08 D9 ED 45 7E 23 1B FE
#0150 FD C2 C4 00 7E 23 1B E5 D5 2A 2E F4 CB 27 30 01
#0160 24 85 30 01 24 6F 5E 23 56 D5 DD E1 D1 E1 18 DC
#0170 3A 34 F4 A7 28 0D DD 21 40 F4 3E 00 32 34 F4 DD
#0180 E5 18 9D 32 3C F4 08 D9 ED 45 3A 3A F4 3D 32 3A
#0190 F4 A7 28 0F DD 23 DD 23 DD 23 DD 23 DD E5
#01A0 C3 10 01 DD 2A 38 F4 3E 00 32 32 F4 C3 72 00

#0200 3E DE D3 90 21 00 F4 22 26 F4 7D C6 10 30 01 24
#0210 6F 22 48 F4 21 00 F8 22 2E F4 21 00 FA 22 30 F4
#0220 21 80 06 22 36 F4 21 00 60 22 46 F4 08 D9 3E 00
#0230 47 4F 57 5F 67 6F D9 08 2A 48 F4 3E 06 06 00 70
#0240 23 77 2A 26 F4 3E 00 06 32 70 23 77 3E 01 32 3E
#0250 F4 32 24 F4 C9

#0280 21 00 20 23 7C B5 20 FB C9

#0300 2A 4A F4 ED 5B 4C F4 ED 4B 4E F4 DB 88 D3 90 4F
#0310 3A 20 F4 A7 C2 82 03 79 FE FE 20 10 3E 01 D3 90
#0320 32 20 F4 3E 04 32 22 F4 47 C3 EC 03 FE FF 20 2A
#0330 3E 02 D3 90 32 20 F4 3A 24 F4 3C E6 F0 20 F8 2A
#0340 26 F4 3A 28 F4 85 30 01 24 C6 10 30 01 24 6F 5E
#0350 23 56 D5 E1 16 00 5A C3 EC 03 FE FD 20 04 2A 2C
#0360 F4 E9 FE FC 20 13 3E 04 32 20 F4 D3 90 3E 05 32
#0370 22 F4 47 21 40 F4 C3 EC 03 FE FB C0 3E 01 32 34
#0380 F4 C9 FE 01 20 43 78 A7 20 12 7A B3 28 08 71 23
#0390 1B 7A B3 C2 EC 03 32 20 F4 D3 90 C9 FE 04 20 08
#03A0 21 2C F4 71 05 C3 EC 03 FE 03 20 09 23 71 2A 2C
#03B0 F4 05 C3 EC 03 FE 02 20 05 59 05 C3 EC 03 51 7A
#03C0 B3 CA 8D 03 06 00 C3 EC 03 FE 02 20 06 CD 00 05
#03D0 C3 EC 03 FE 04 20 0D 71 23 05 78 A7 C2 EC 03 3E
#03E0 01 32 34 F4 3E 00 32 20 F4 D3 90 C9 ED 43 4E F4
#03F0 ED 53 4C F4 22 4A F4 C9

#0400 3A 3C F4 A7 28 0C 3A 20 F4 A7 20 F4 3E 60 D3 90
#0410 18 EE 3A 24 F4 A7 28 1C 3E 01 32 3C F4 3E E8 D3
#0420 84 3E A8 D3 82 3E 50 D3 81 3E C0 D3 80 3E 5C D3
#0430 83 C3 00 04 3A 20 F4 A7 20 04 3E 1D D3 90 DB 8A
#0440 3A 3E F4 A7 20 0A 3A 34 F4 A7 CA 00 04 C3 18 04
#0450 3E 00 32 3E F4 32 2A F4 ED 5B 46 F4 2A 48 F4 73
#0460 23 72 C3 00 04

#0500 79 FE FF 28 04 13 71 23 C9 7A B3 28 33 E5 2A 26
```

block diagram assembler downloaded code

Votrax Voice Synthesizer IC (Text to speech converter)

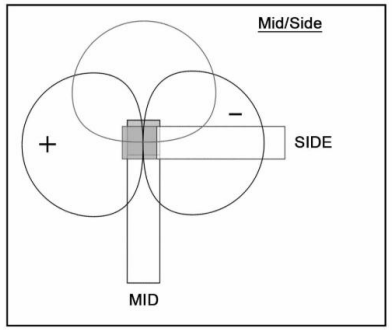
What is DAQ now-a-days?

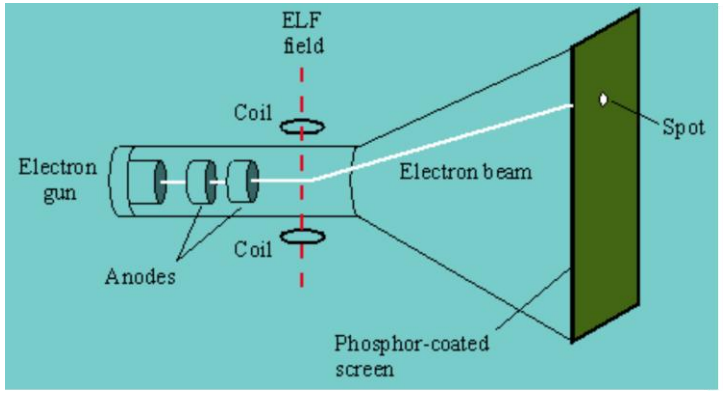
DAQ is everywhere meaning…
Where information needs to be collected and sent, the sensors information is first converted to digital/numerical format, transmitted and analyzed and eventually converted back to an analog form for human convenience (graph, text).

Examples:

- Microphone (analog) – A to D converter - Digital storage (CD, memory) – D to A convert – Speaker (analog)
- Images (films, CCDs) – A to D converter - Digital storage (CD, DVD, memory) – D to A convert – CRT (analog)

Stereo recording:
XY, ORTF, **Mid-Side** (MS), Blumlein, DIN



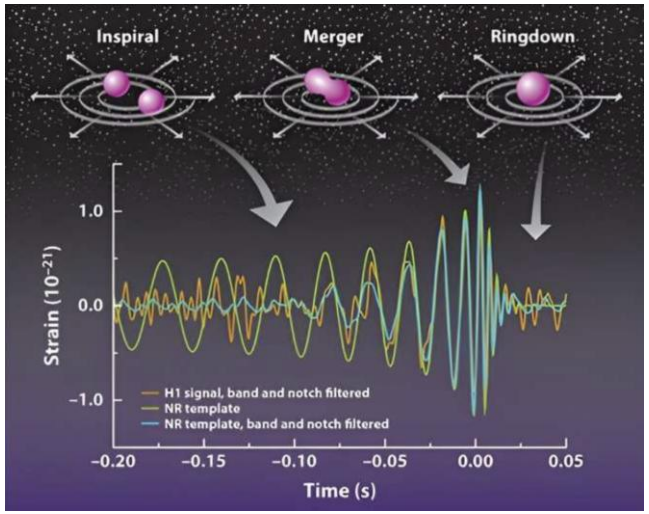


What is DAQ now-a-days?

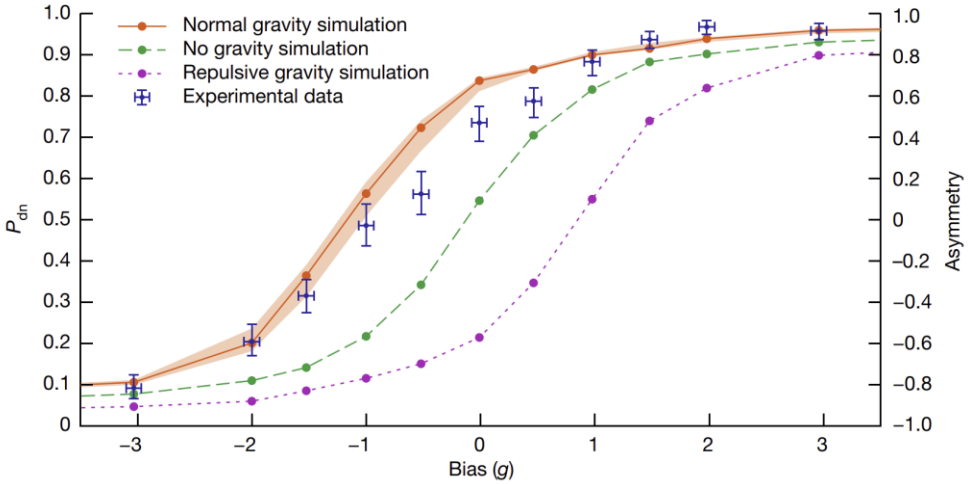
In Physics:

- What “information” can we have access to?
  - Quantitative data (position ({x, y, z}, {r, θ, z}), “event” Time, “signal” Amplitude, Charge, Magnetic Field, Temperature, Pressure conditions, … momentum, energy, …)
  - Collect data using a combination of detectors/sensors to acquire the relevant parameters.
  - Convert all in a digital form for easier processing.

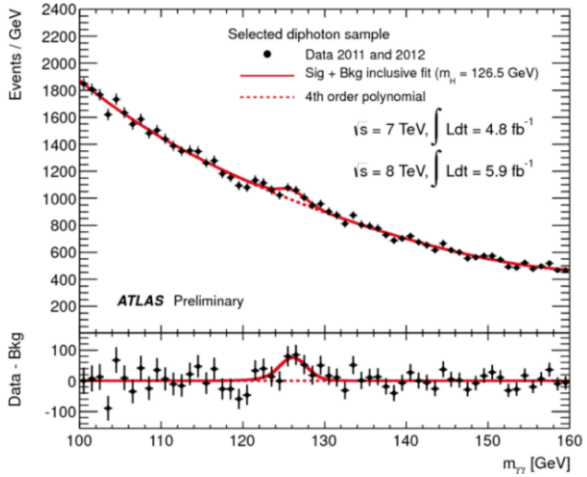
Experiments results



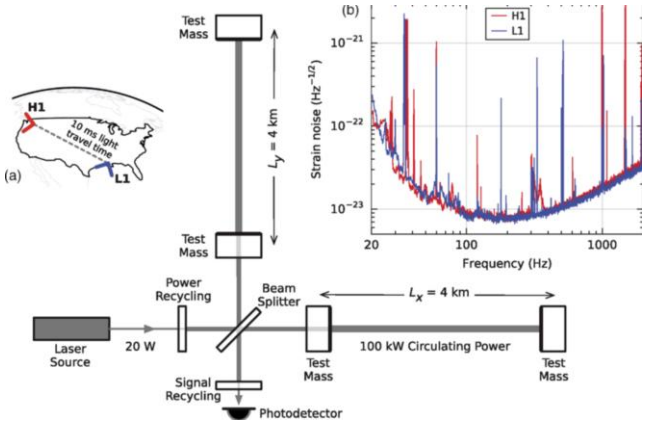
https://www.nature.com/articles/s41586-023-06527-1



https://phys.org/news/2024-07-creation-deep-algorithm-unexpected-gravitational.html



https://home.cern/resources/image/physics/higgs-collection-images-gallery

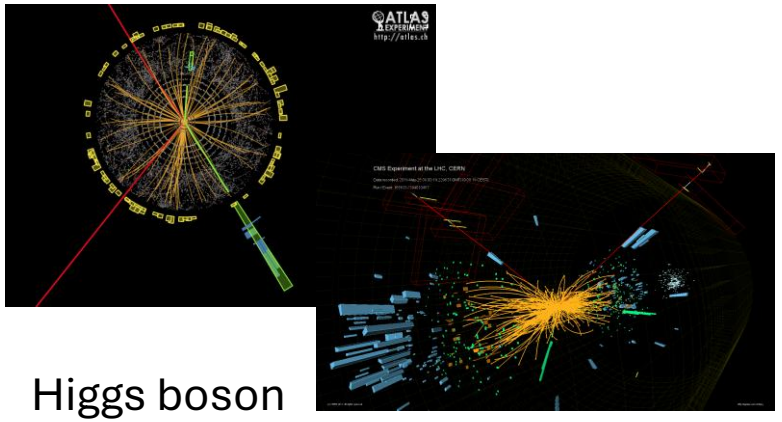


LIGO-Virgo-KAGRA (2016)

Laser Interferometer Gravitational-Wave Observatory
Nobel 2017, Rainer Weiss, Barry Barish, Kip S. Thorne

Alpha-g (2023)

Antihydrogen Laser Physics Apparatus



Higgs boson (2012)

Nobel 2013, Peter Higgs, François Englert

Data path from the detector to the publication

DAQ in Experimental physics

Dealing with equipment from the sensors (analog) …

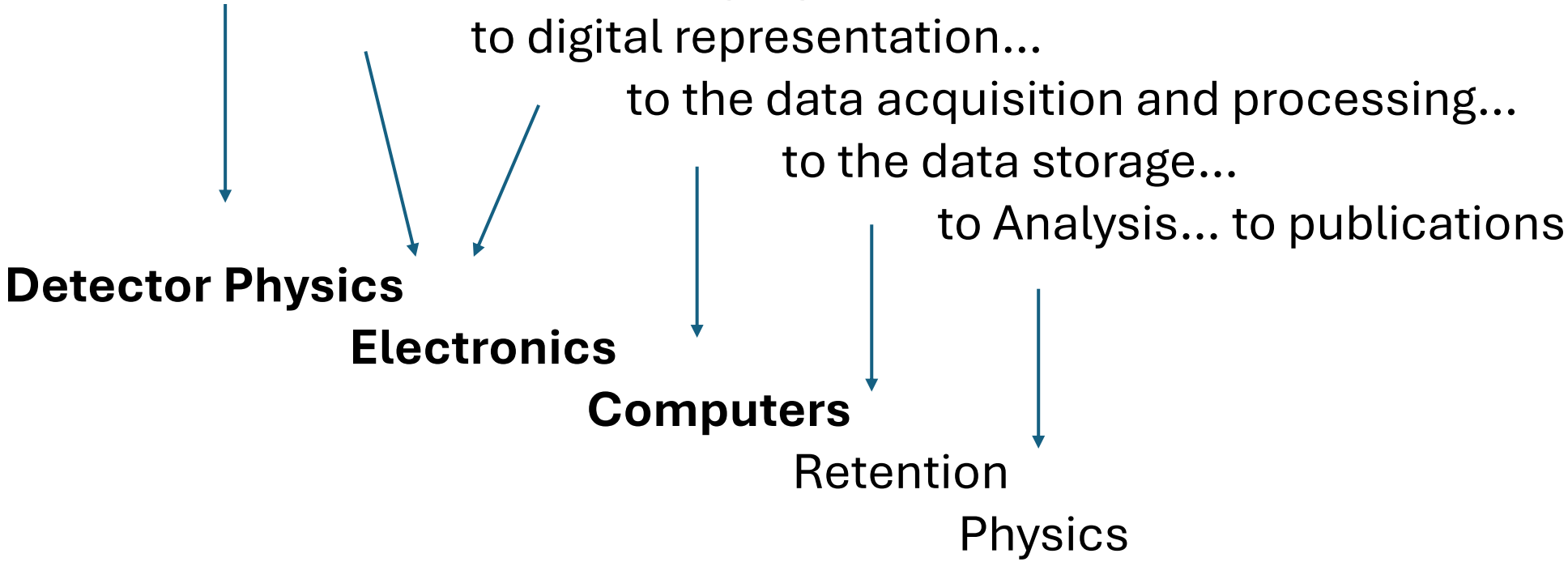
to electrical analog signals…

to digital representation…

to the data acquisition and processing…

to the data storage…

to Analysis… to publications



We need to have some good knowledge of the different elements of the DAQ chain

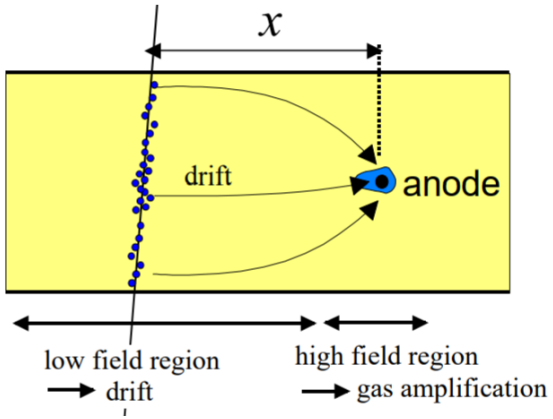
- **Detector - Sensors**
  - Gas detector (MWPC, DC, TPC, Micro-Pattern-Gas-Detector [MicroMega, Gems, μ-Rwell, etc.)
  - Silicon based detector (Si-Strip Det., **SiPM**, etc.)
  - Photon based detector (MCP, PMTs, CMOS)

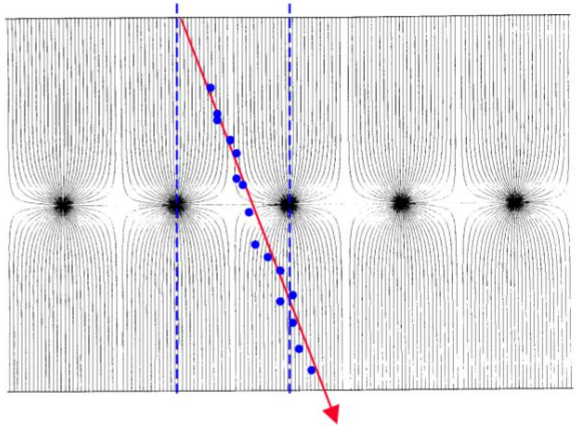
Marco Poli Lener
(Frascati, CERN)

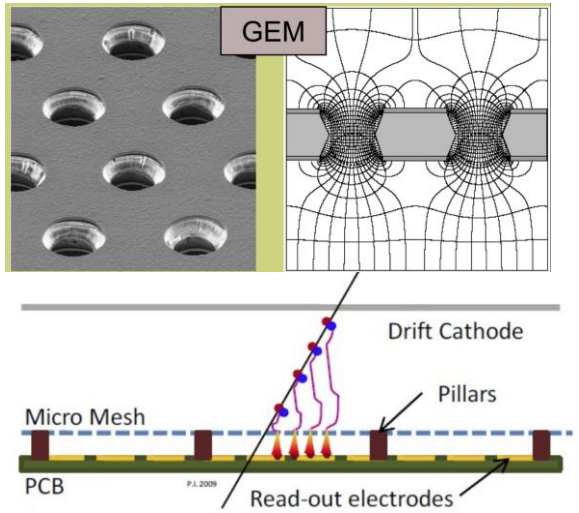
Detector Type	***Gas Gain***	***Typical Use***
Proportional Counter	10^2–10^4	X-ray/gamma spectroscopy
MWPC	10^4	Tracking
Drift Chamber	10^4	Precision tracking
TPC	10^4	3D tracking
GEM/Micromegas	10^3–10^5	High-rate physics
micro-RWELL	>10^4	High-rate physics
RPC	10^5	Trigger systems

Detector Type	***Position Sensitivity***	***Energy Resolution***	***Time Resolution***	***Typical Use***
Silicon Strip	1D / 2D	Good	Good	Tracking
Silicon Pixel	2D	Good	Good	Imaging, vertex detection
APD	No	Moderate	Excellent	Photon detection
SiPM	No	Poor	Excellent	Photon counting
CCD / CMOS	2D	Good	Poor	Astronomy, imaging

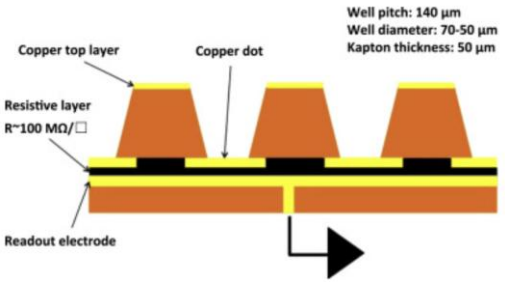
Detector - Sensors





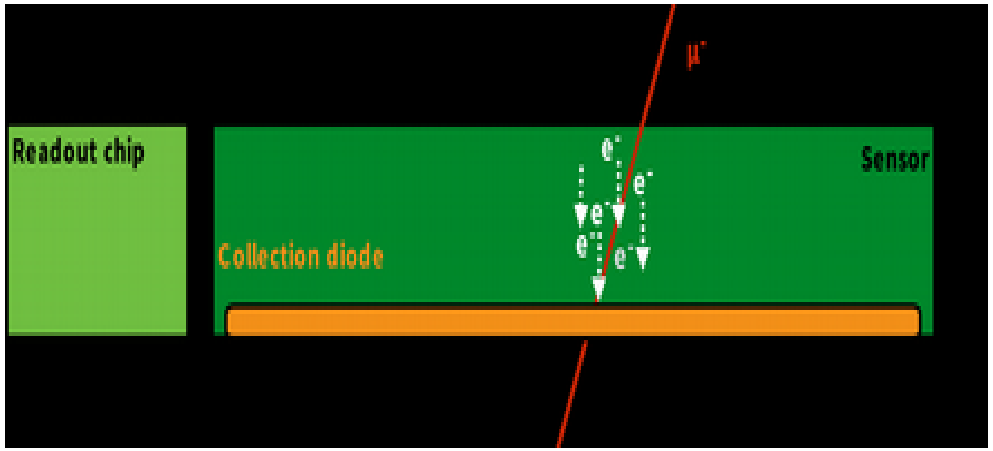


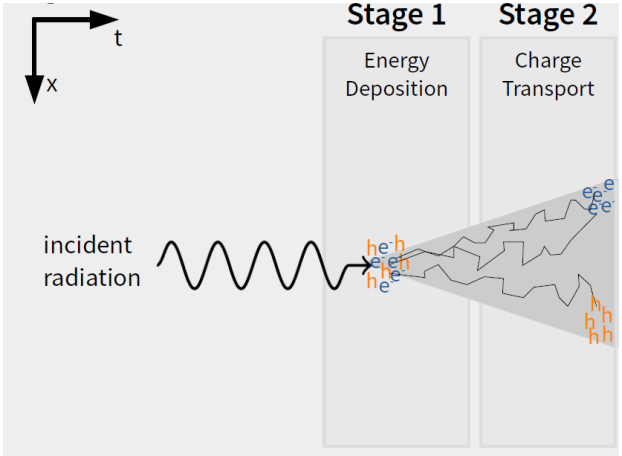
MicroMega

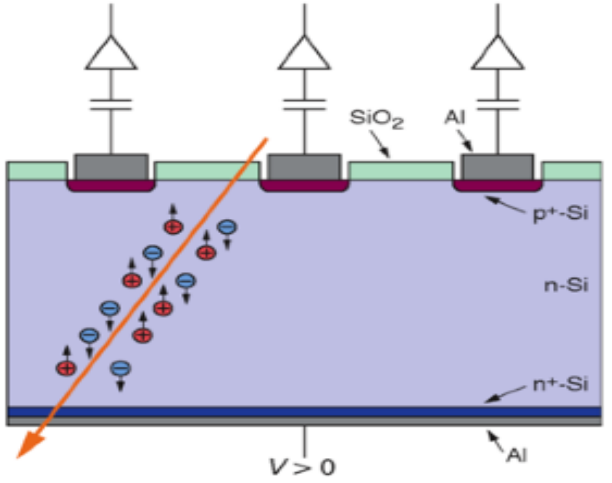


Micro RWELL

$100e^- * 1E^6$ (gain) @ 1µs @ 50Ω ~ 0.8 mV





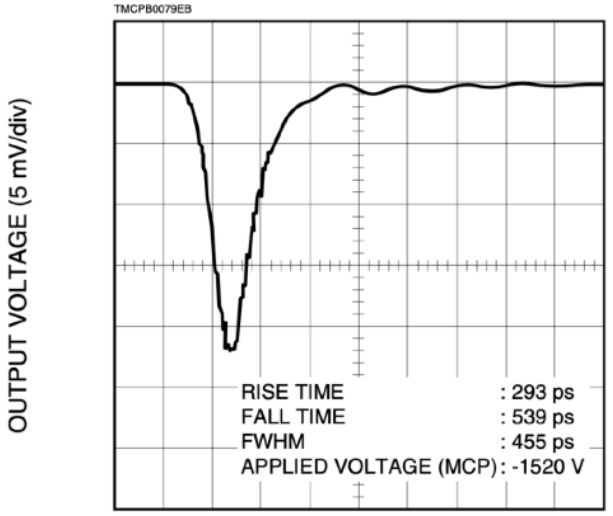


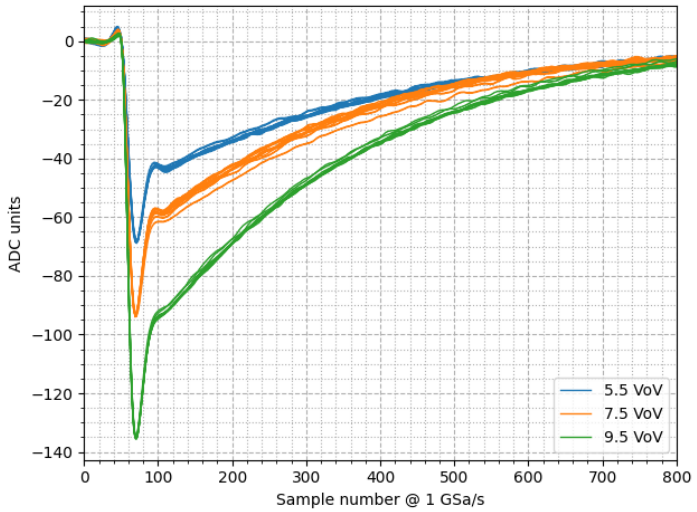
We need to have some knowledge of the different elements of the DAQ chain

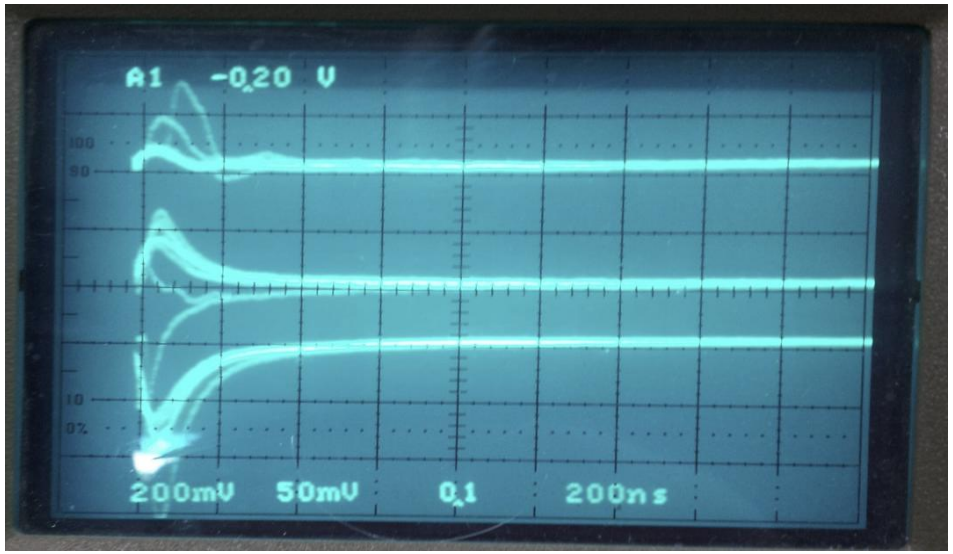
Electronics

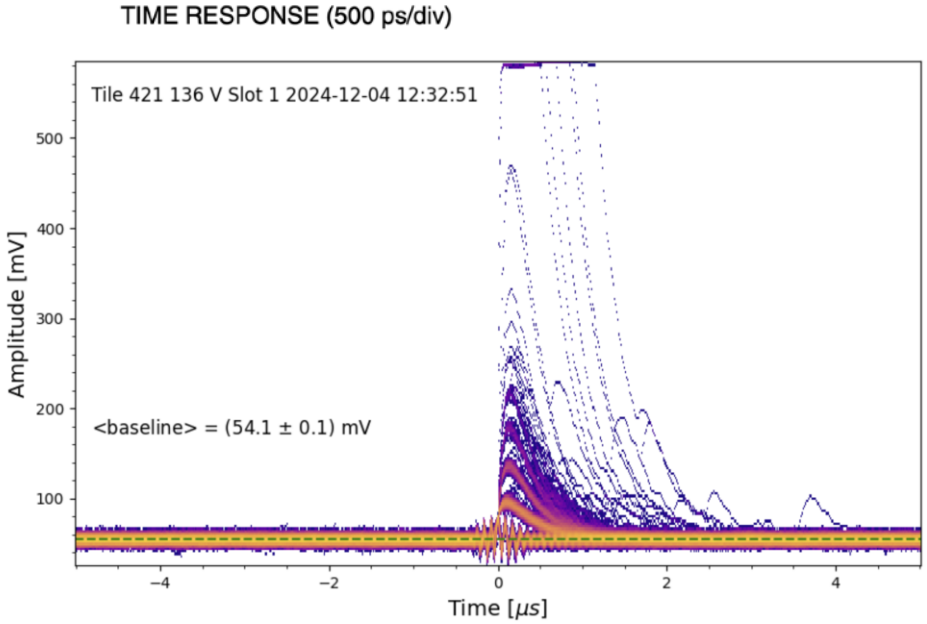
- Electrical Signal (pulse)
- Amplification – Filtering – Shaping
- Threshold – Logic Signal
- Pulse conversion from analog to digital
  - Counting
  - Time, Amplitude, charge measurements
- Electronics instrumentation
- Clock, Trigger

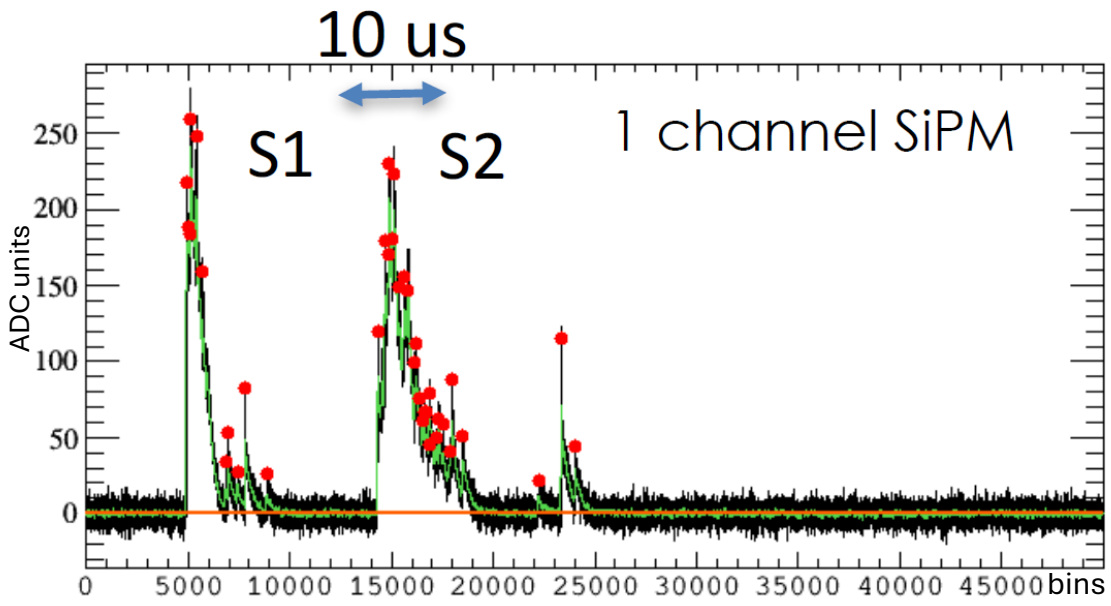
Electrical Signal (pulse)





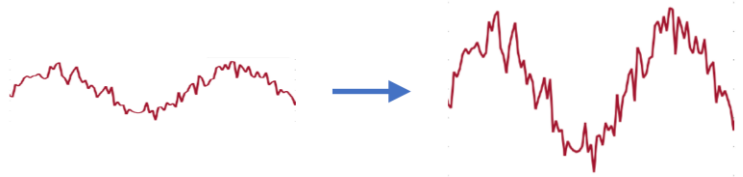






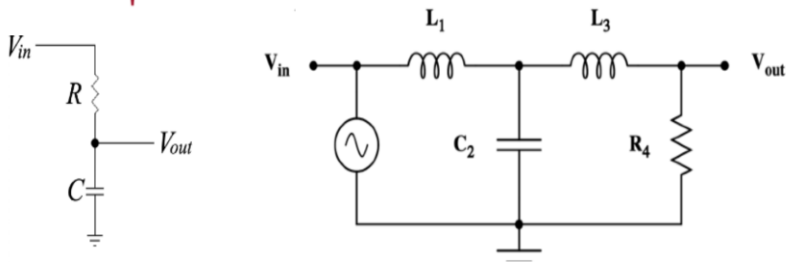
Amplification - Filtering – Shaping

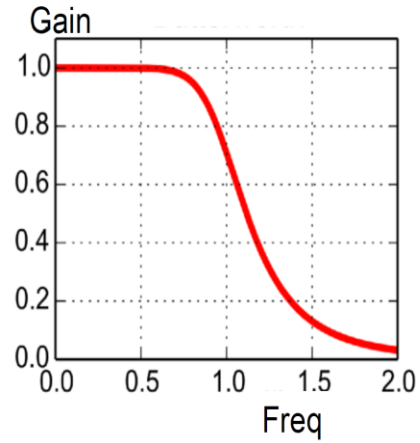
Signal from the detectors may need to be boosted for transmission to next stage of signal processing (10mV..100mV).
Noise is also amplified!



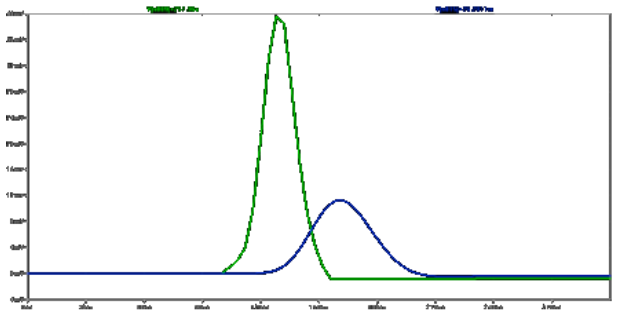
Noise are mainly high-frequency that can be reduced by signal filtering

RC circuitry such as Butterworth, Low pass filter, High pass filter, Pass band filter, ...

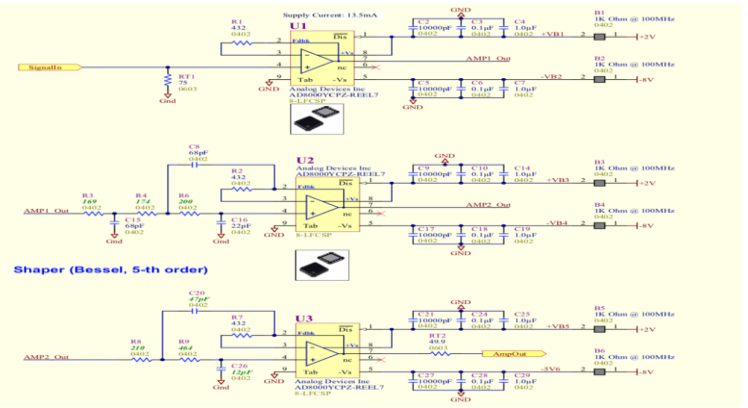




Signal shaping act as filtering, but allows change of shape (timing, and amplitude)



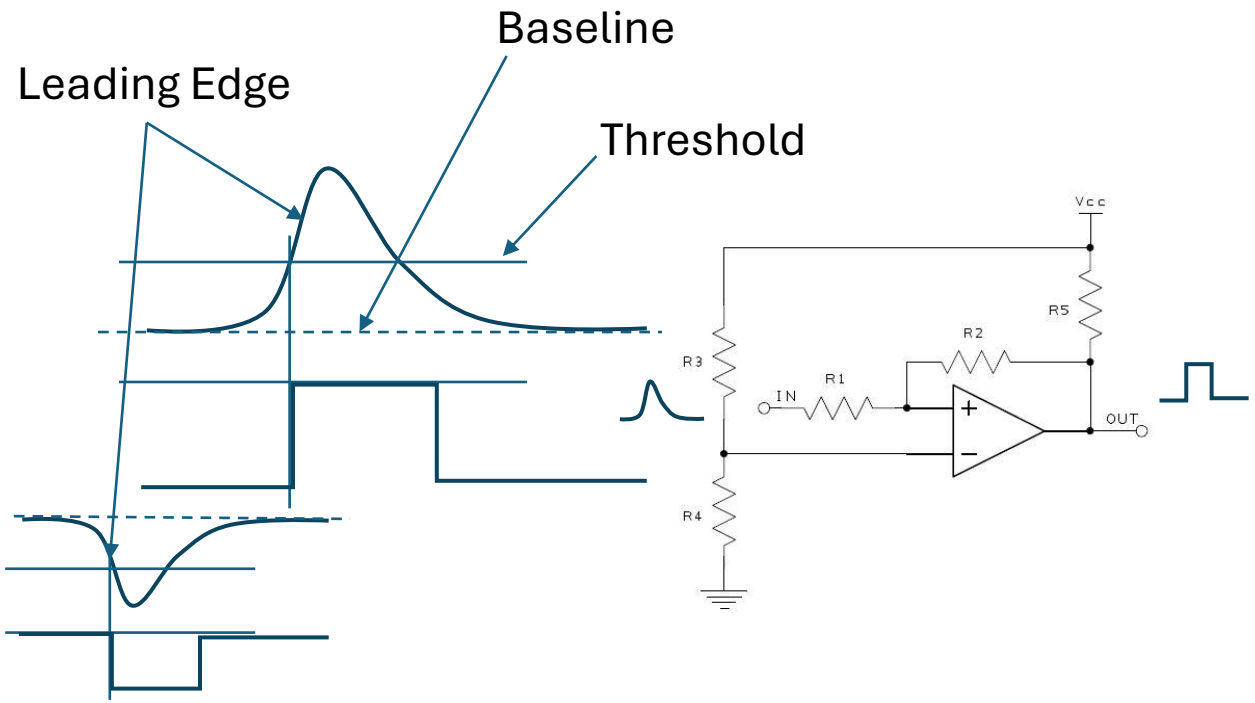
Use to match digitizer characteristics (Nyquist–Shannon sampling theorem, bandwidth)

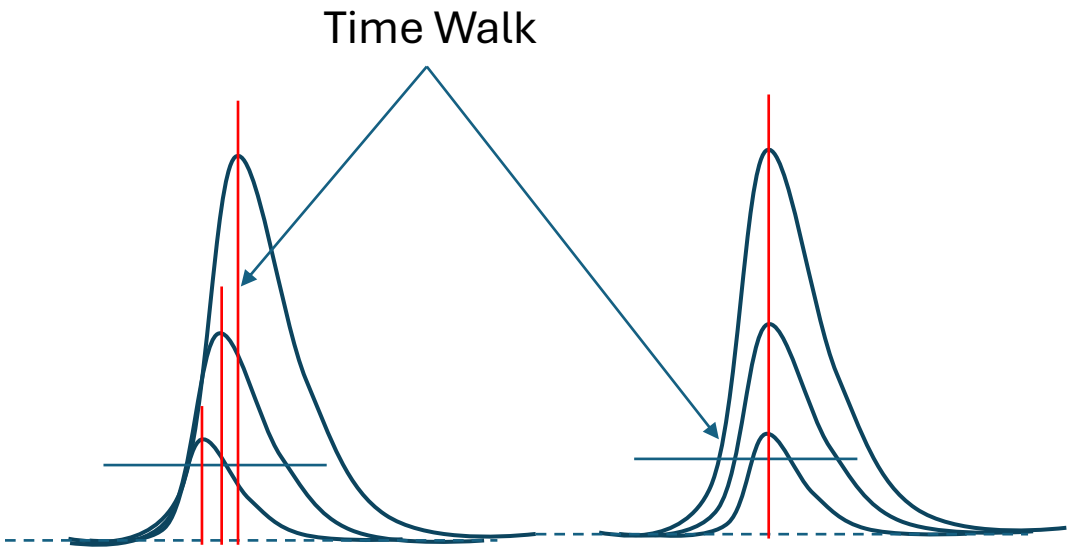


Electronics – Signal manipulation (conversion)

Threshold – Logic Signal

- Produce a new binary signal out of an Analog signal for presence detection or timing purpose
  - **Leading Edge detection [LE]**



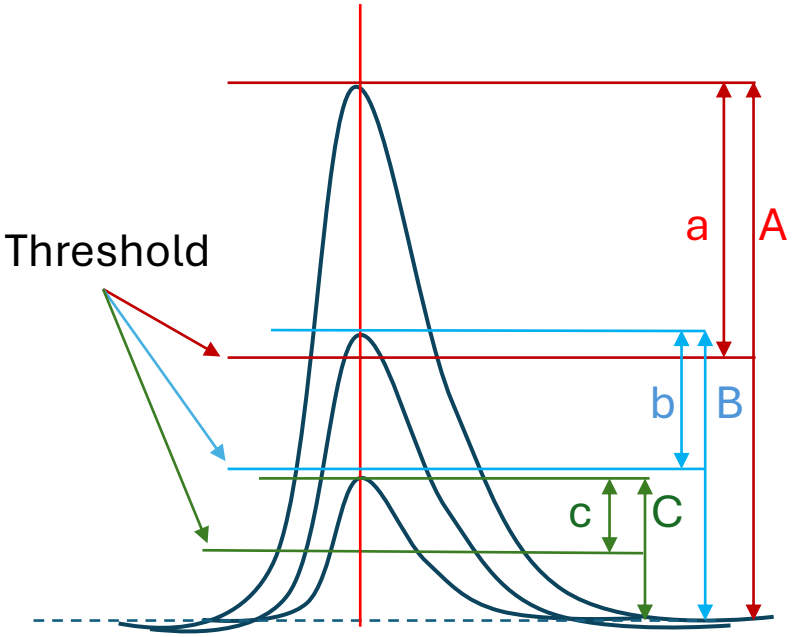


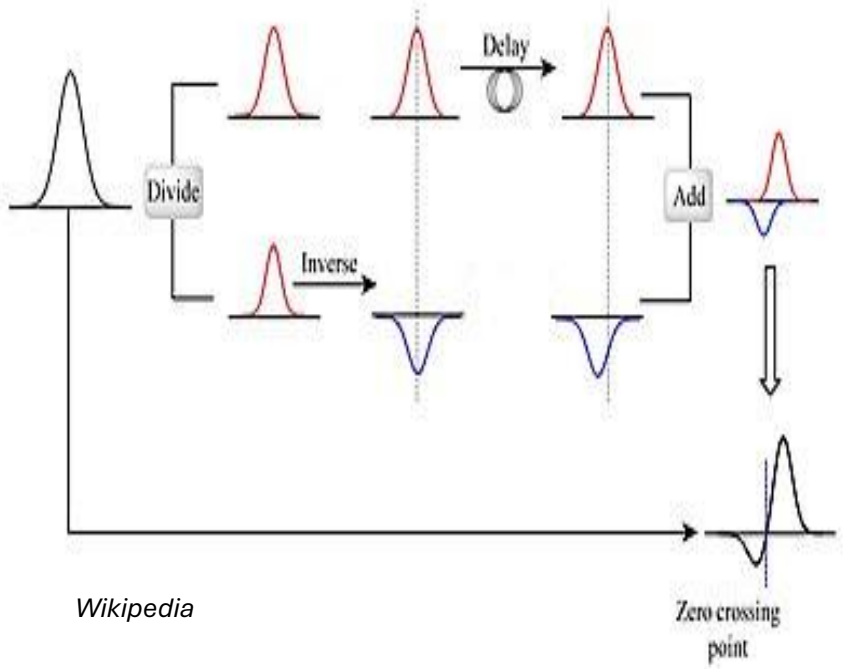
Electronics – Signal manipulation (conversion)

Threshold – Logic Signal

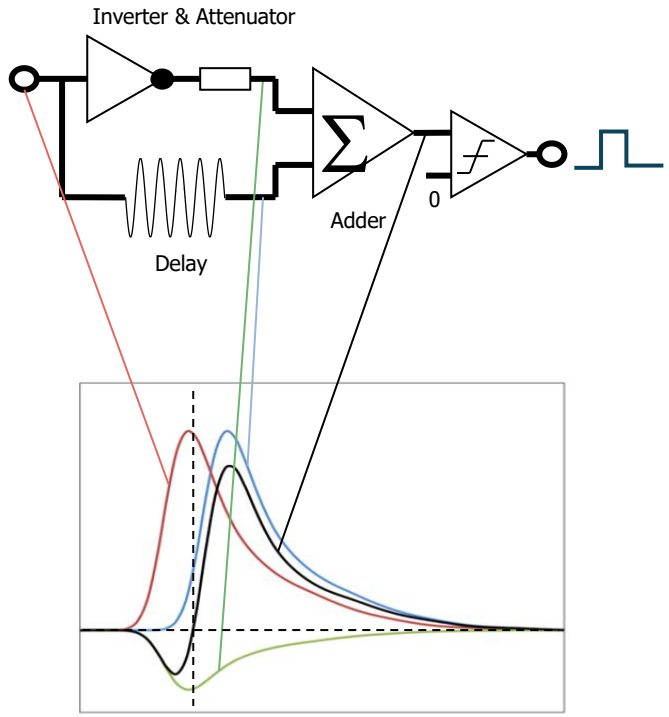
- Produce a new binary signal out of an Analog signal for presence detection or timing purpose
  - **Constant Fraction Discriminator [CFD] – dynamic threshold setting based on the signal amplitude**

$$\frac{a}{A} = \frac{b}{B} = \frac{c}{C} = \text{Constant}$$





Wikipedia

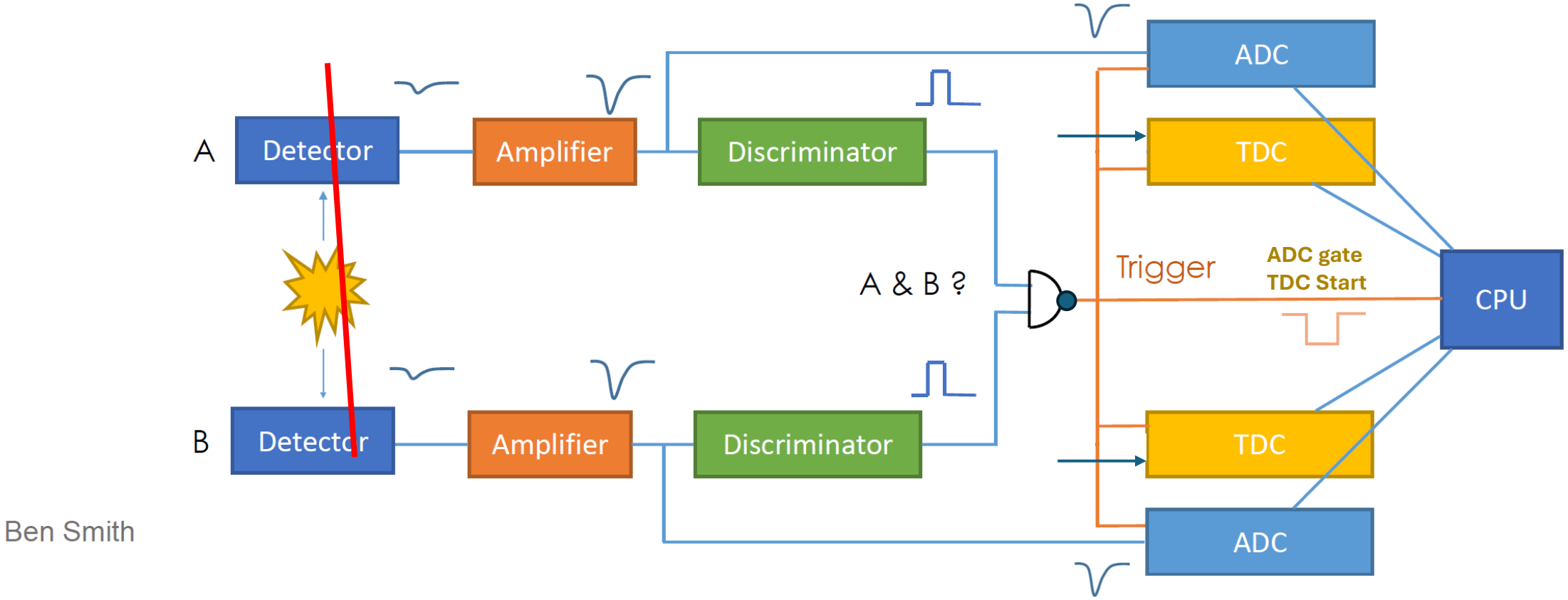


Stefan Ritt

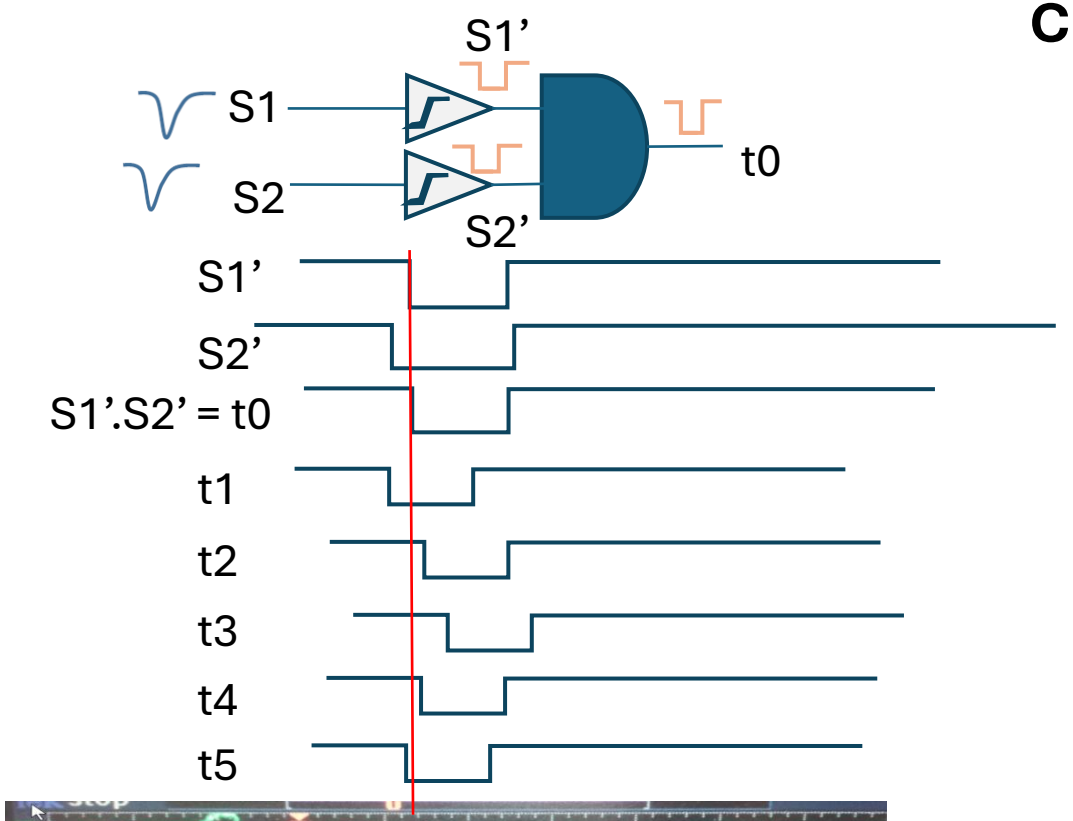
Coincidence

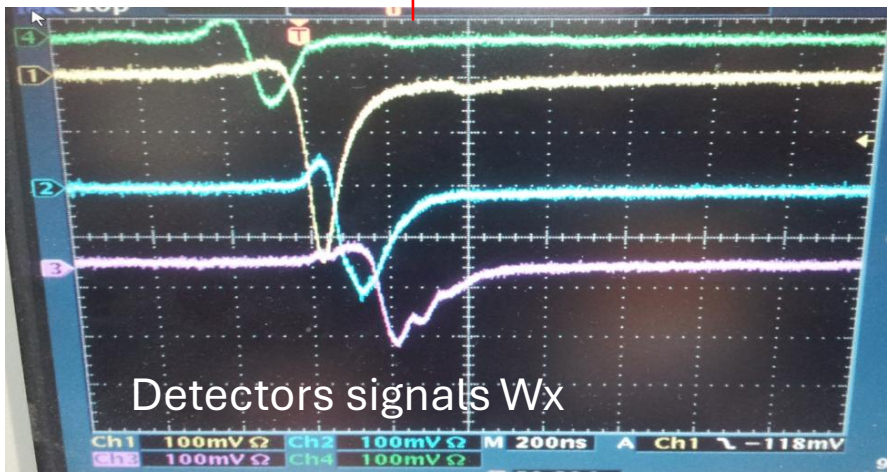
Logical Signal for Coincidence

Signal from different sensors may define the “event” of interest (EOI) by coincidence
Generate a trigger that will initial the “event” recording
The same logic signal can be used as gate to the ADC and/or TDC (start conversion)

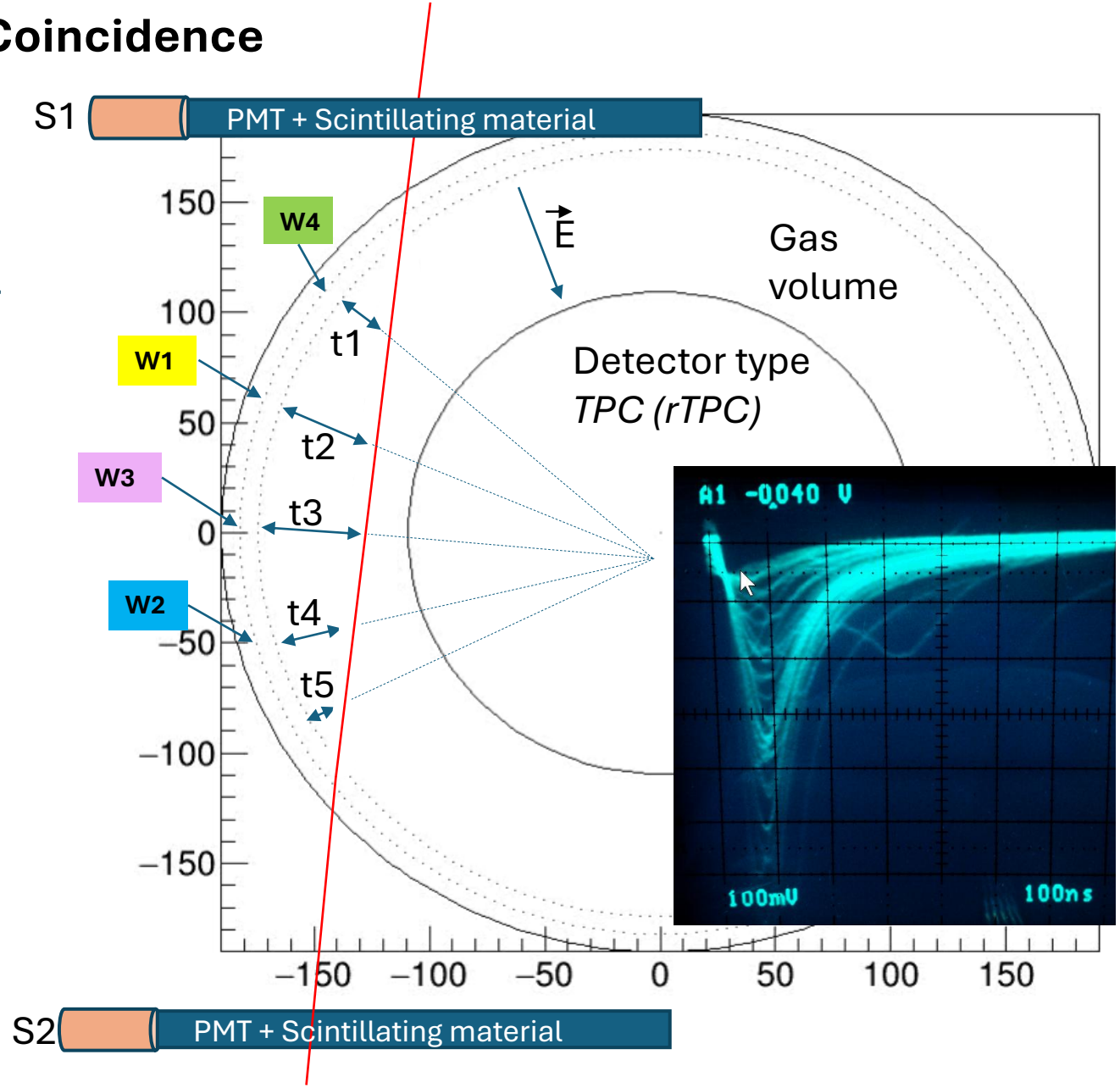


Ben Smith

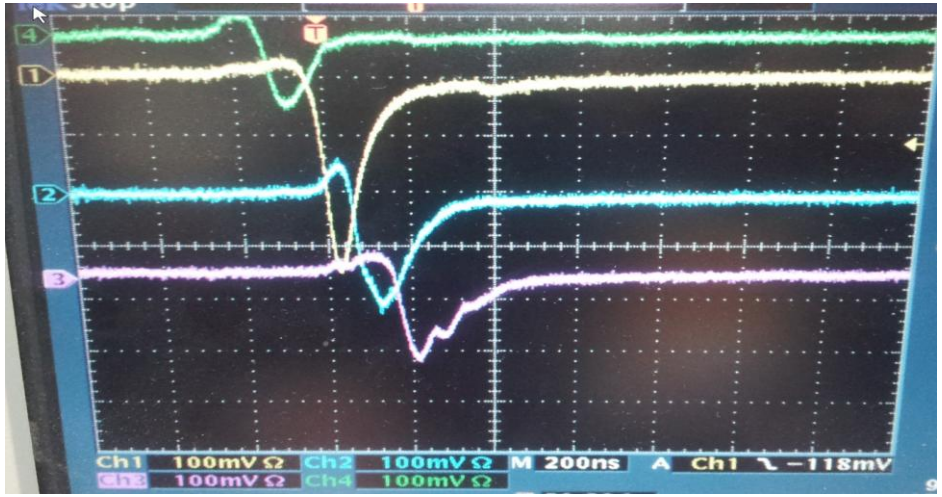




Coincidence



Electronics – signal conversion from analog to digital



b00 1011 0101 1001
b00 1000 0101 1001
b00 1001 0001 1111
b00 1001 0101 1000

@ Time T_x

- Signal — Levels, Transmission
- Counter — Just count the pulses (Freq, Multichannel Scalers)
- ADCs — measure amplitude / prominence, charge…
- TDCs — measure relative time…

Electronics - Digital signal levels

- Different type of digital and analog signals evolved based on:
  - Logic Family
  - Need for Speed
  - Reduce current consumption
  - Improve immunity to interference

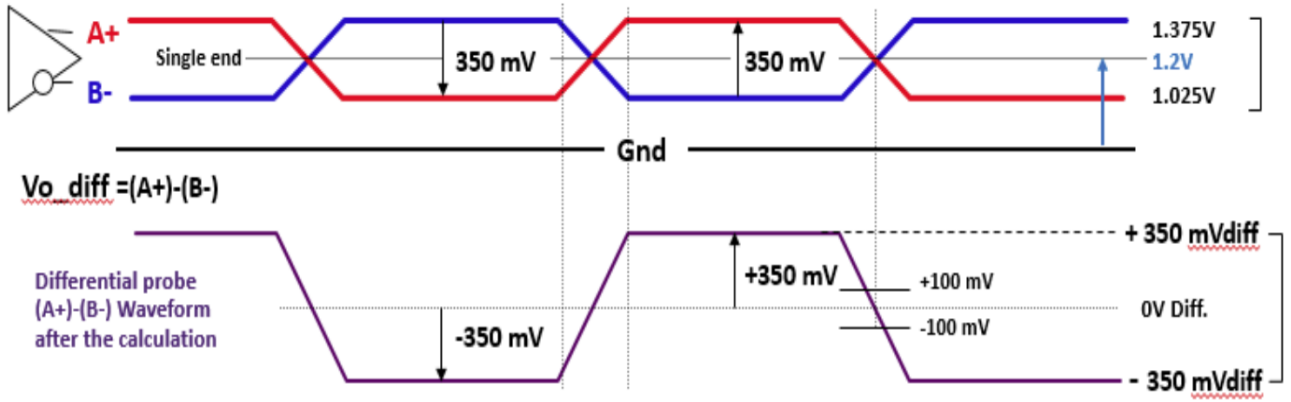
BNC-RG59

LEMO00-RG174

MCX connectors and other Coaxial types (SMA, SMB, etc)

TTL (CMOS-TTL) VOL= [0.0:0.4]V , VOH= [2.4:5]V
NIM VOL=0V , VOH=-0.8V, IOH=[-14:-18]mA, IOL=[-1:+1]mA @50Ω
Differential LVDS VOL=1V , VOH=1.4V, VCM=1.2V, (400mV swing) @100Ω

- For analog signal transmission, same type of cable



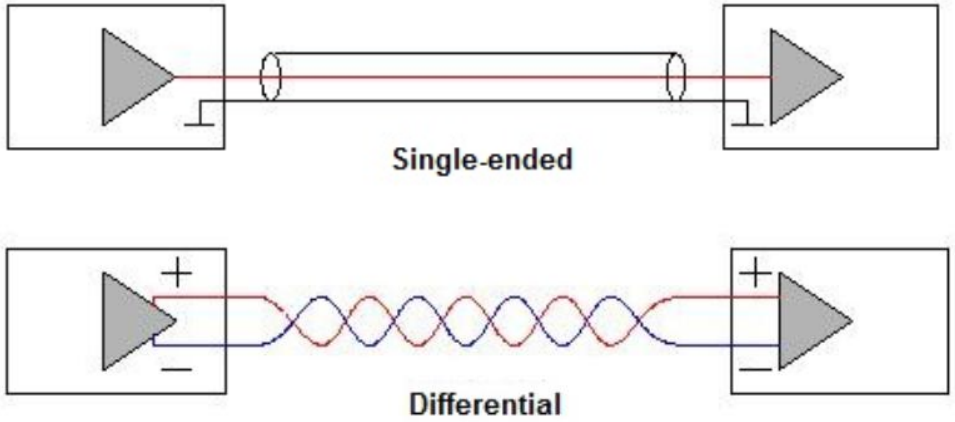
Pair of pins per signal
Flat, Twisted pair cable

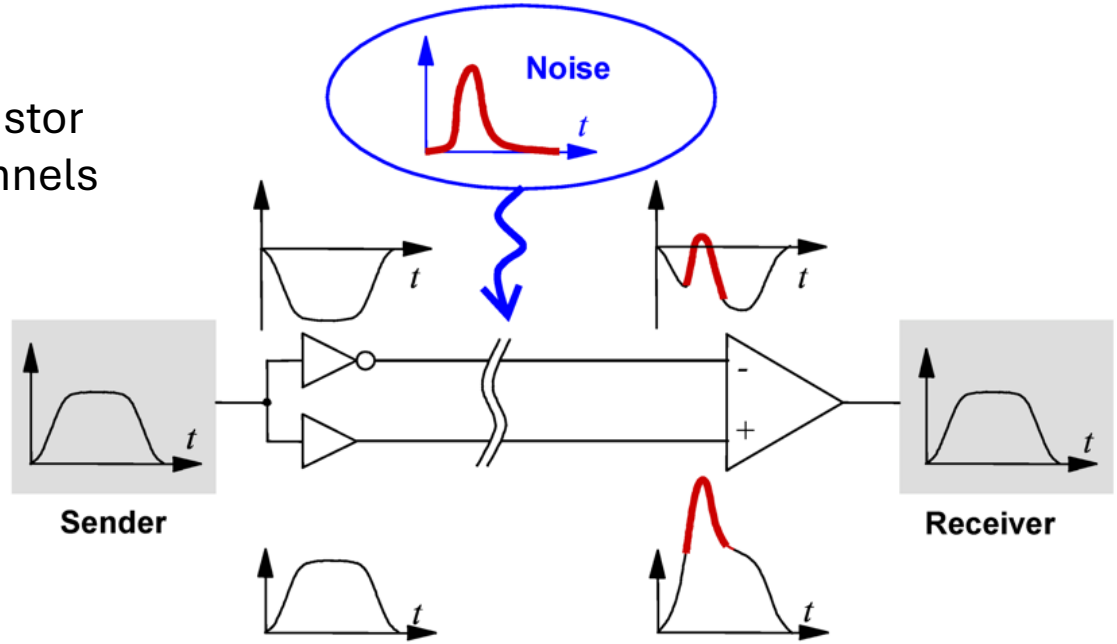
types	V_{ee}	V_{bas}	V_{haut}	V_{diff}	V_{cc}	V_{cm}
ECL	–5,2 V	–1,75 V	–0,9 V	–0,85 V	GND	
PECL	GND	3,4 V	4,2 V	0,8 V	5,0 V	
LVPECL	GND	1,6 V	2,4 V	0,8 V	3,3 V	2,0 V

Electronics - Signal transmission

Signal disturbance

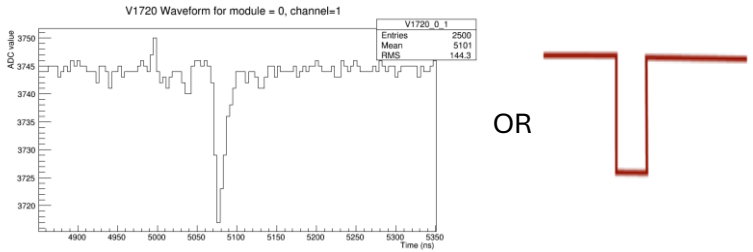
- Electromagnetic Interference (EMI) - surrounding equipment, power supply
- Ground Loop - signal return path (IEEE Std: two point intended to be at the same potential are in fact at a different electrical potential)
- Signal shielding - cable bundle extra shielding
- Media transmission (electric cable coax, twisted pair, optical)
  - Transmission path - signal degradation
  - Attenuation - signal loss
  - Impedance – reflection, matching Z, termination resistor
  - Cross-talk - interference between neighbouring channels



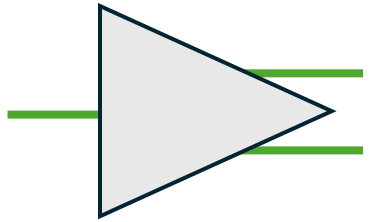


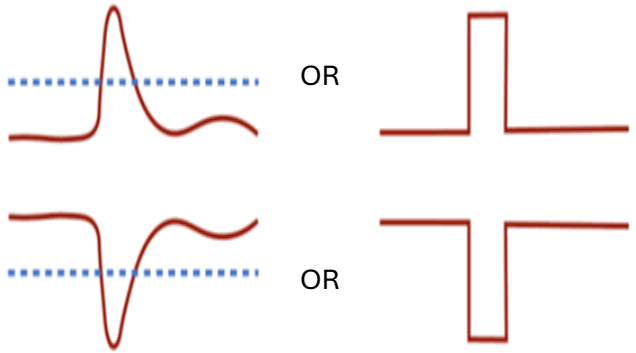
Electronics - Signal transmission (Cables)

Single Ended versus Differential



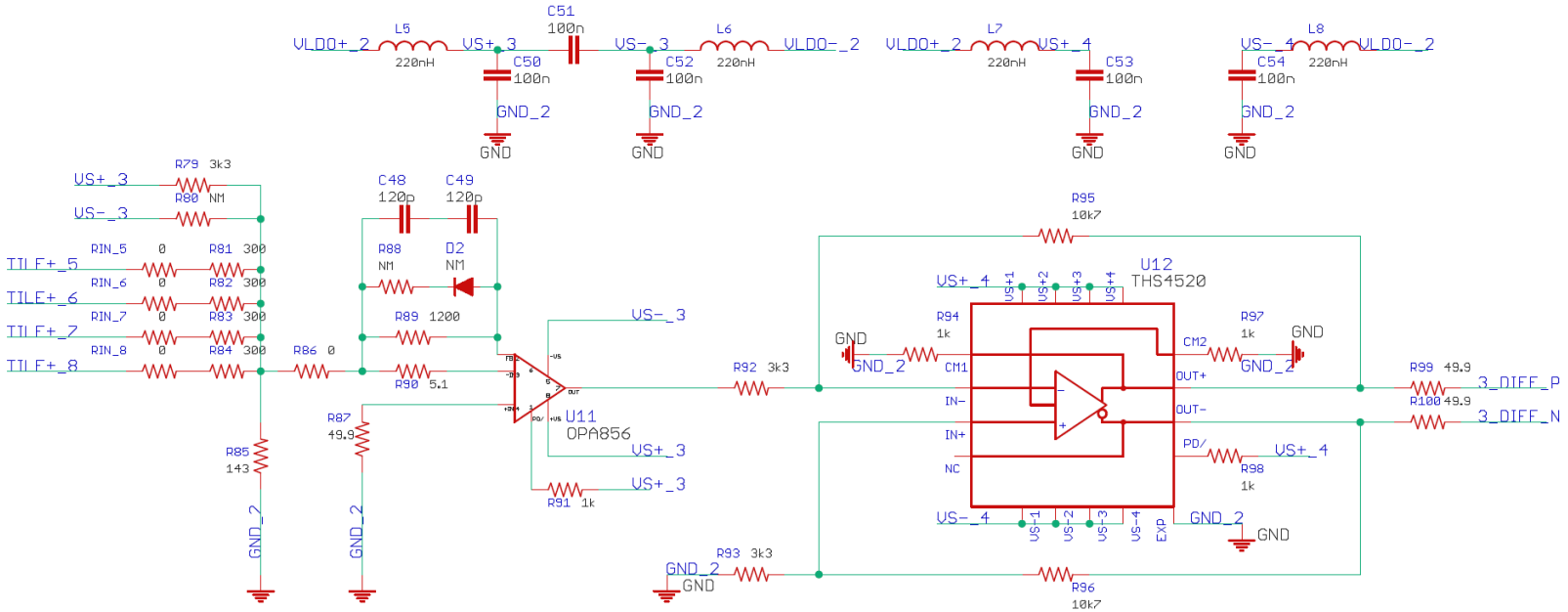
OR



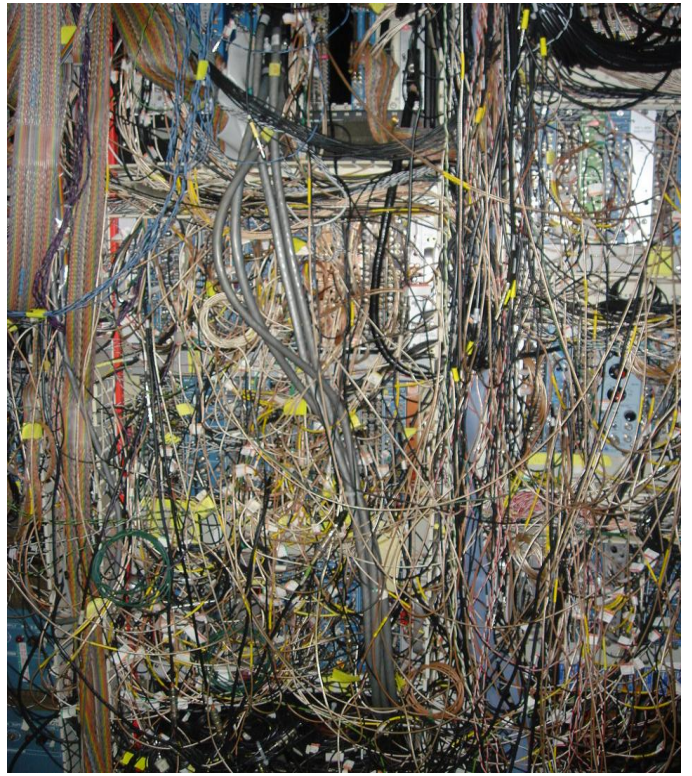


OR

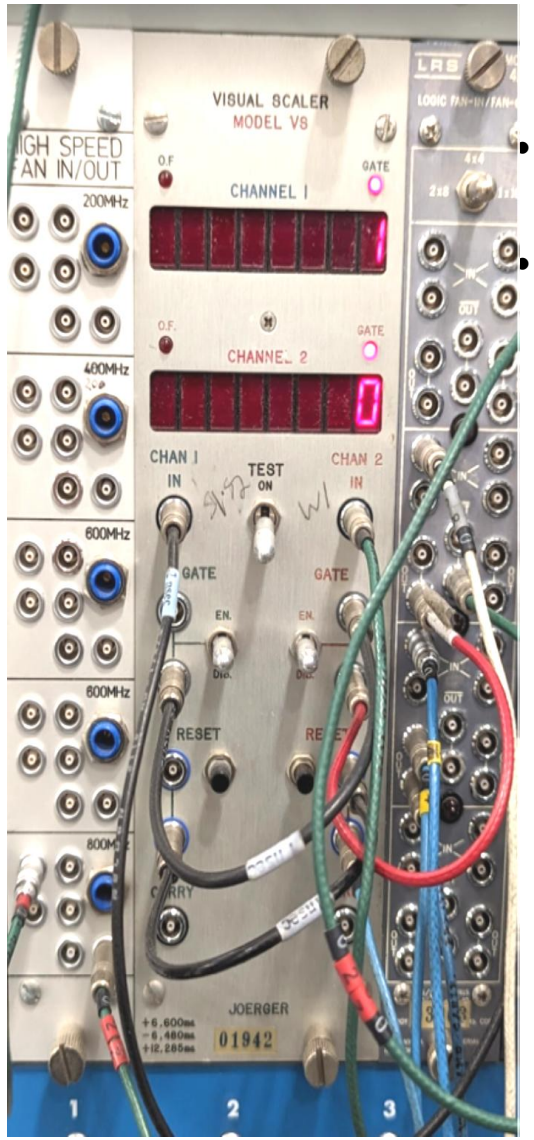
OR



DarkSide-20K PDU signal SE to Differential conversion (analog)



Electronics – Counter

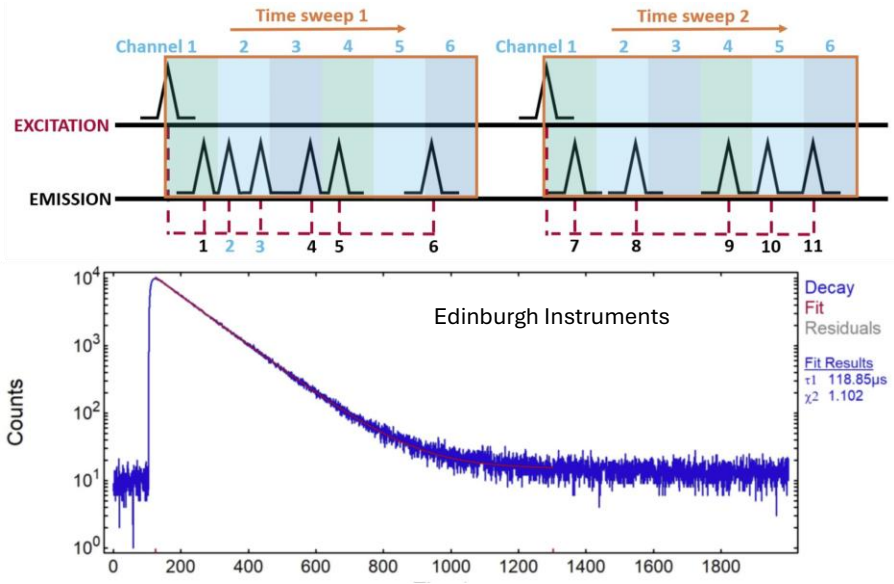


- Simplest thing you can do with digital signals - count!
- Visual / blind versions available

Move to next bin

Things to count

- Multi-channel scaler (MCS) “histogramming scaler”
- Counts pulses in each time bin (dwell time)

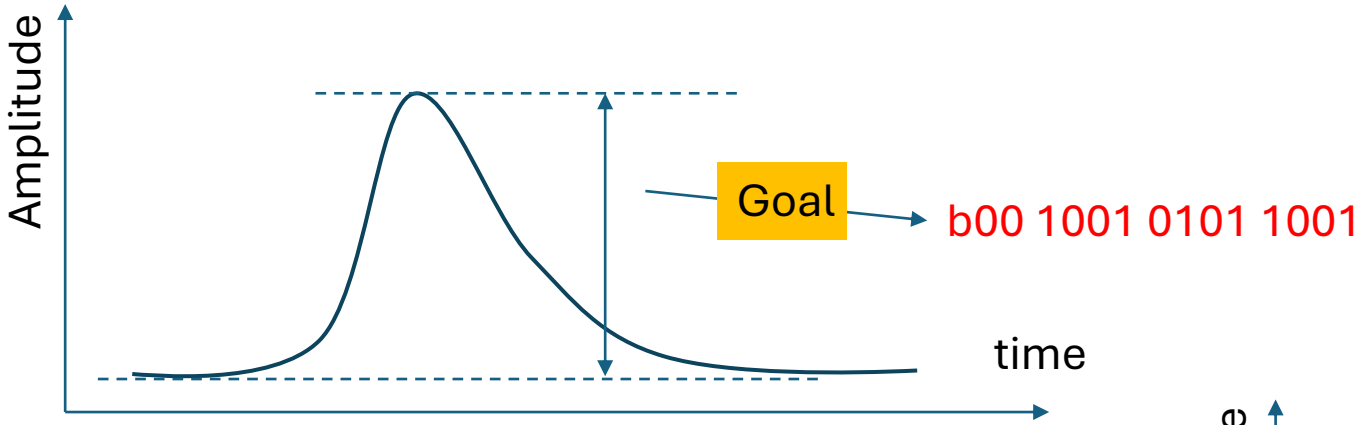


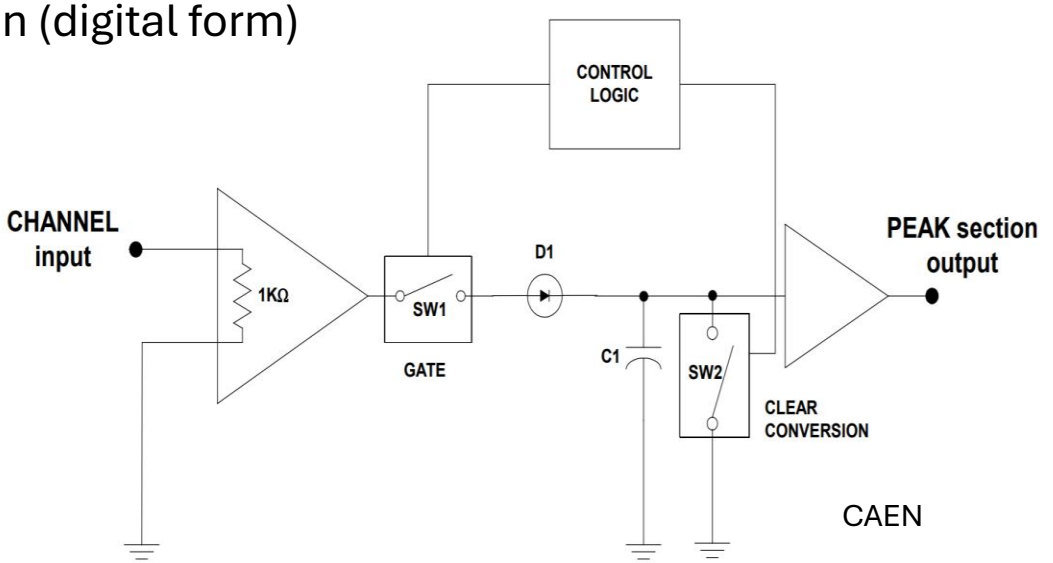
Struck SIS3820:

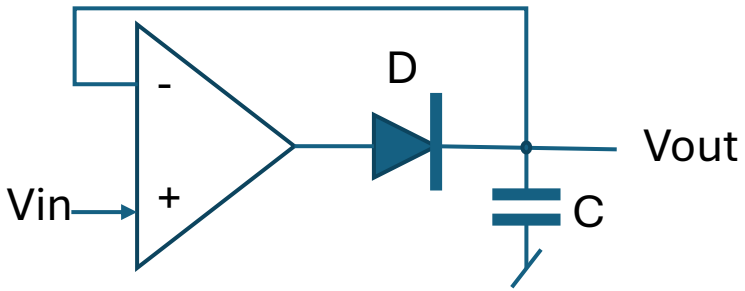
- 24/32-bit channel depth
- 250 MHz (ECL inputs) / 50 MHz (SE)
- ECL/TTL/LVDS or NIM inputs
- Flat cable/LEMO mixed input
- configurations

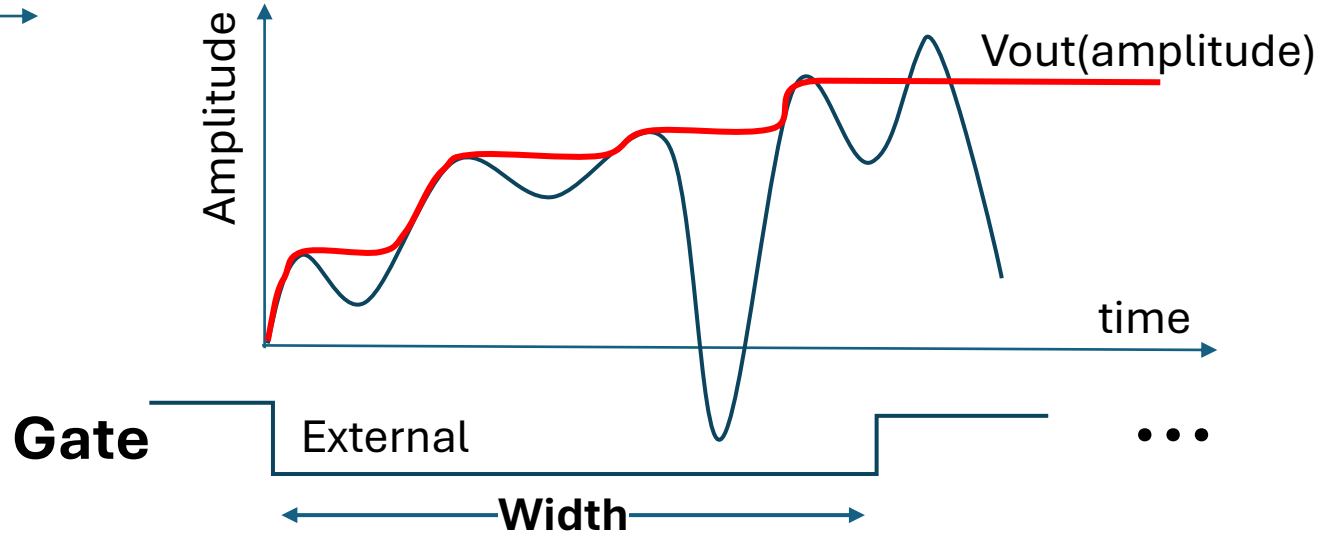
Signal feature conversion

- Convert one of the Analog signal feature to its binary representation (digital form)
  - **Amplitude to Digital Converter [Peak sensing ADC]**



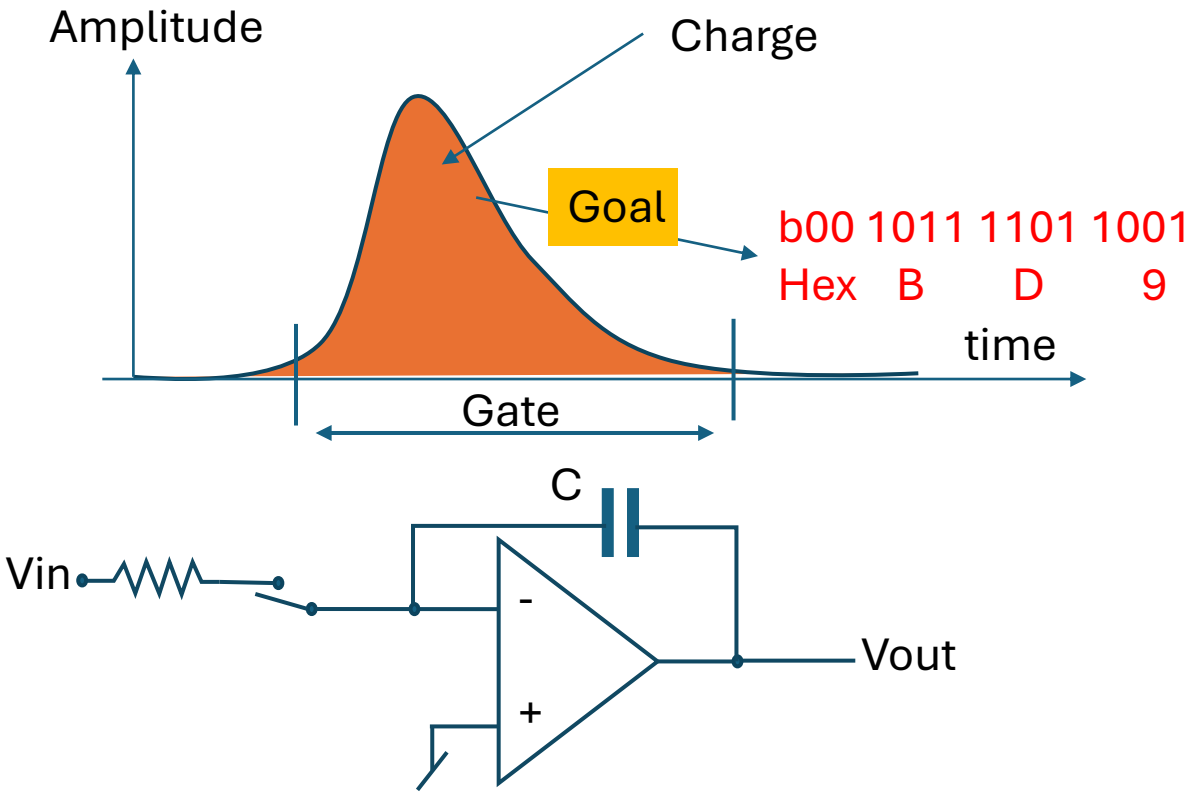


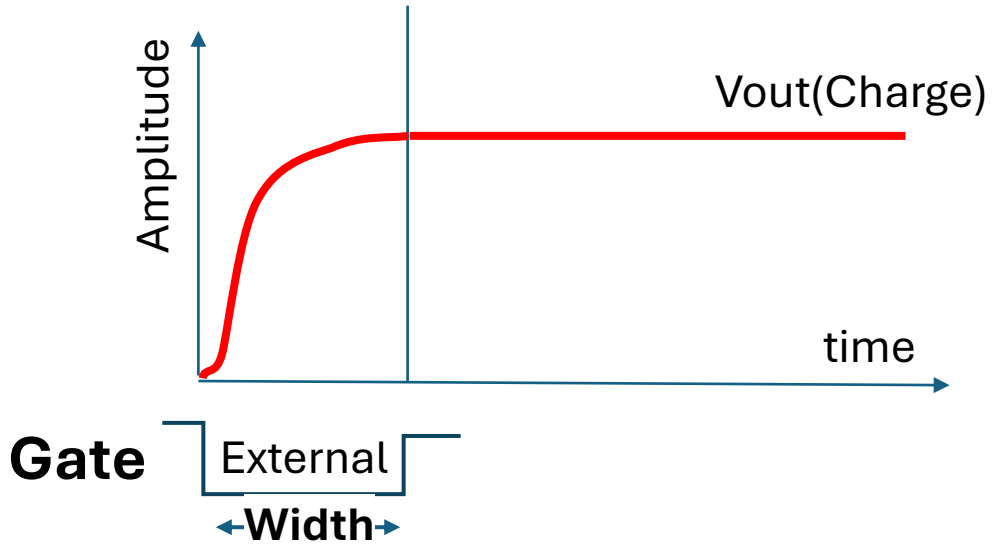




Signal feature conversion

- Convert one of the Analog signal feature to its binary representation
  - **Charge to Digital Converter [QDC, or ADC (A to D)]**

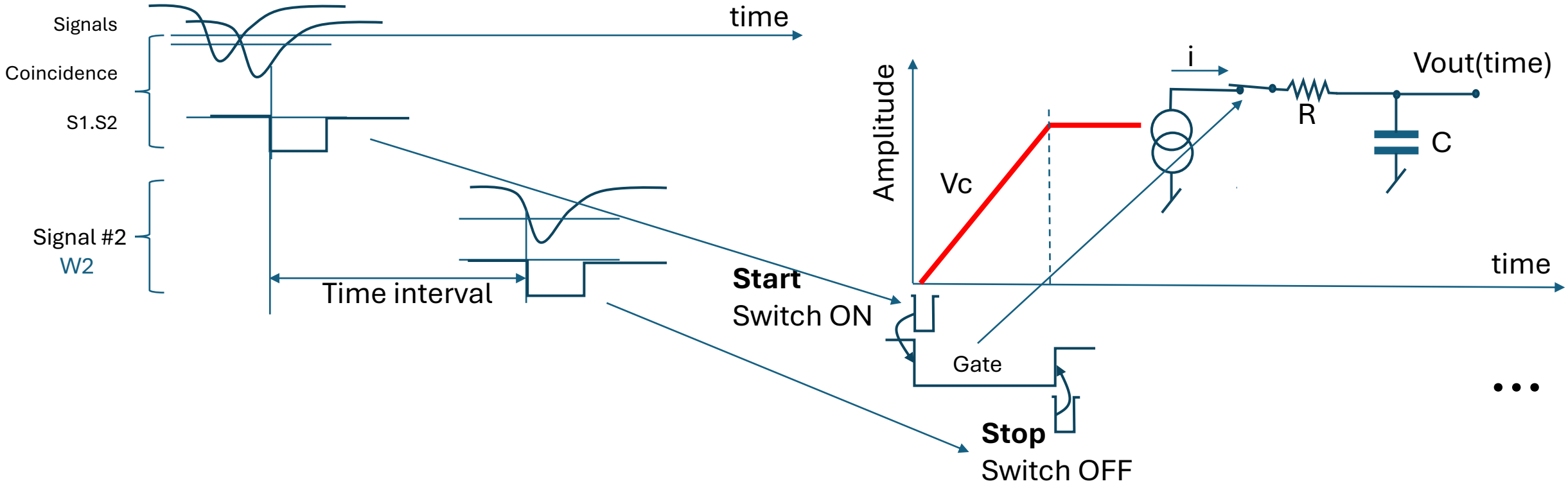




• • •

Signal feature conversion

- Convert one of the Analog signal feature to its binary representation
  - **Time to Digital Converter [TDC]**



Electronics – Analog to Digital Converter

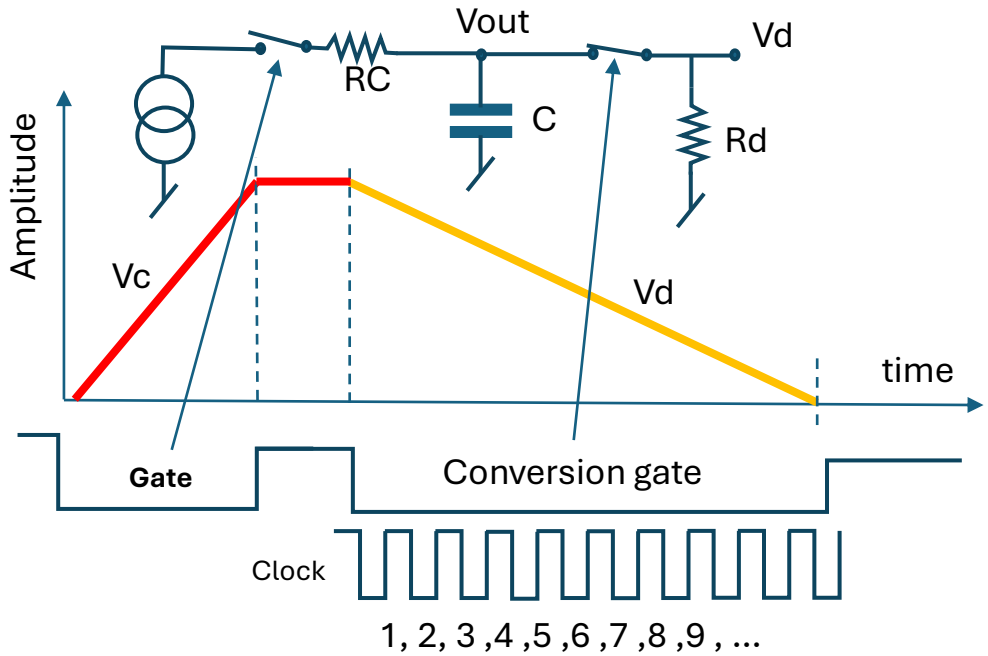
- ADC translate the analog signal amplitude to its digital representation

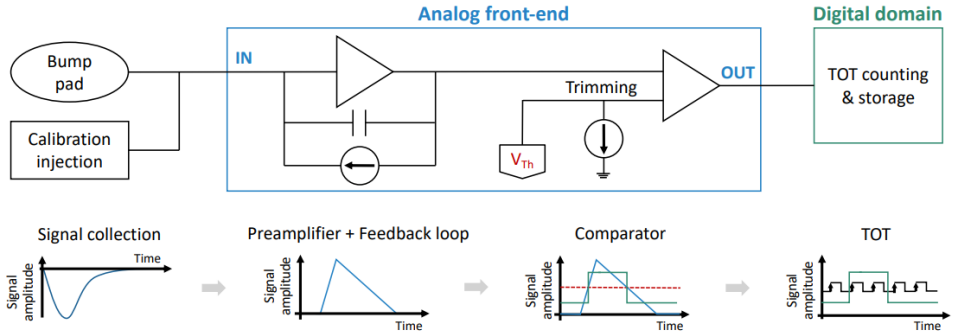
- How fast can I convert a voltage level to its binary representation?

- Different methods
  - Wilkinson ADC, dual-slope, etc.

  Time of discharge proportional to Vout
  Time measured in number clock period
  Time over Threshold (TOT)

  Limited by the clock rate for Hi-Resolution
  Conversion time dependent on the amplitude range
  Excellent linearity
  Tradeoff : Speed versus Precision





The Tracker Group of the CMS Collaboration et al 2021 JINST 16 P12014

Electronics – AD Converter

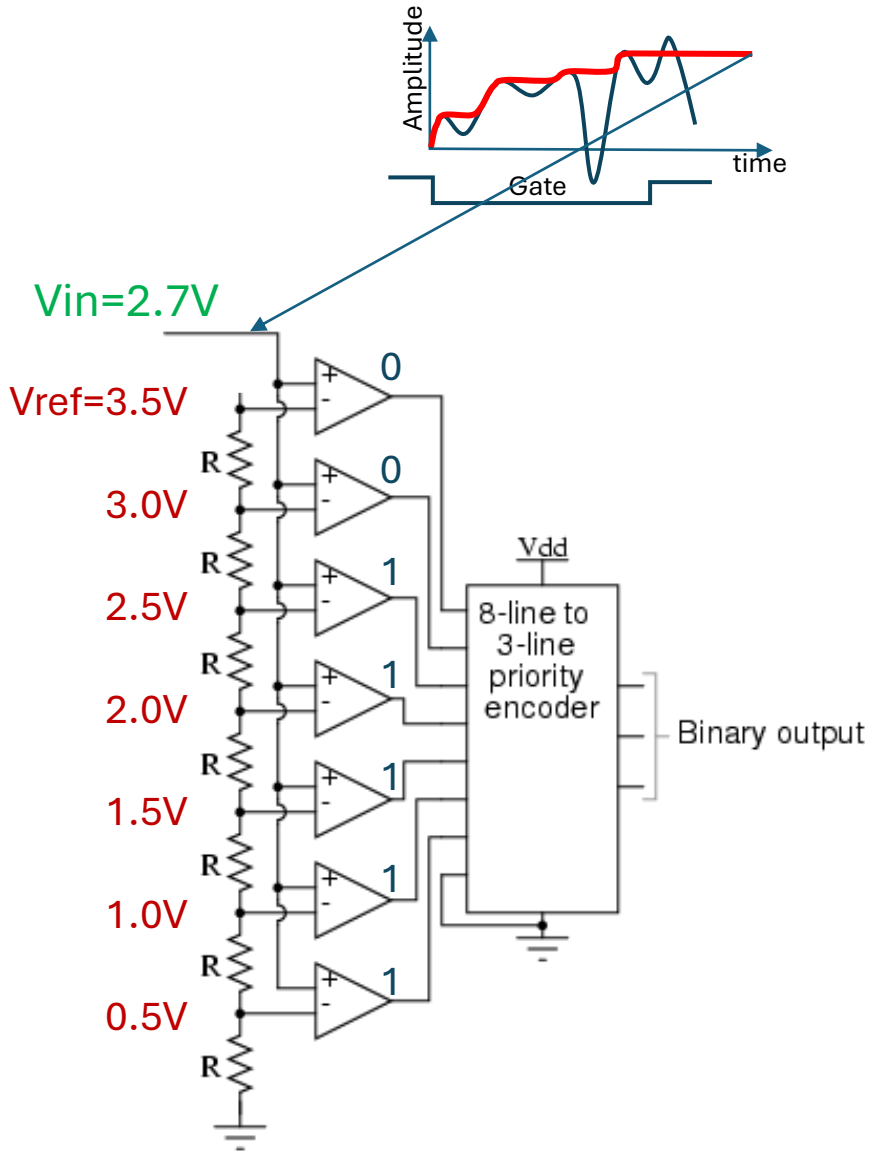
- ADC translate the analog signal to its digital representation

- Different methods
  - 1, 2, n-bit Flash ADC (thermometer code)

  Requires 2^n Comparators for n output bits!

  Requires calibrated “resistor chain”

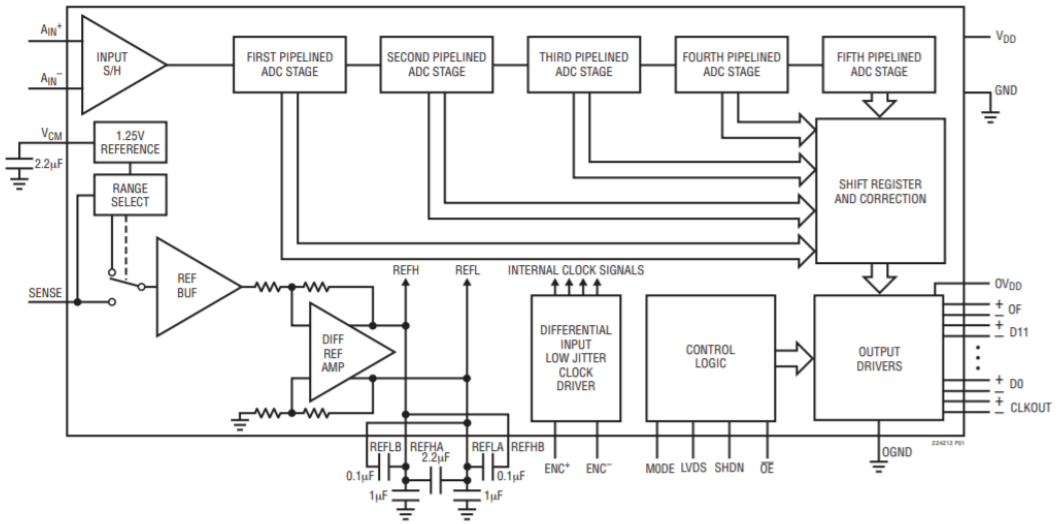
  Fastest conversion time – for small number of bits –
    - ➢ Possible to keep converting the input signal

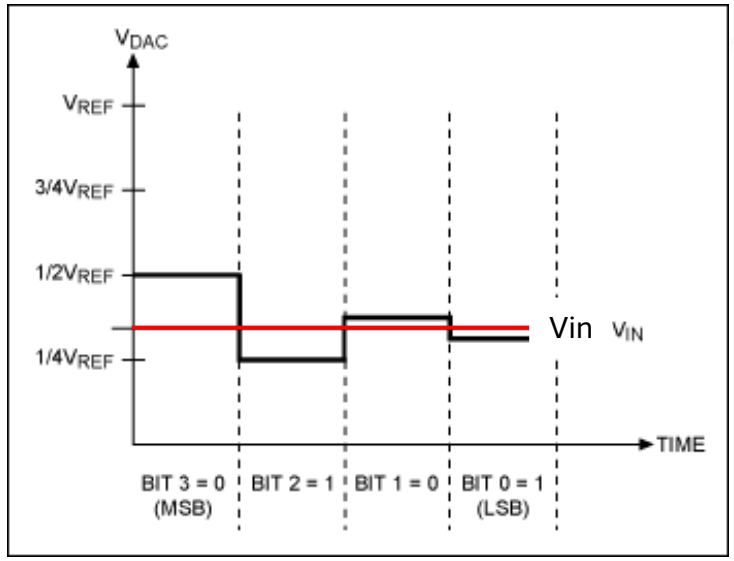


Electronics – AD Converter

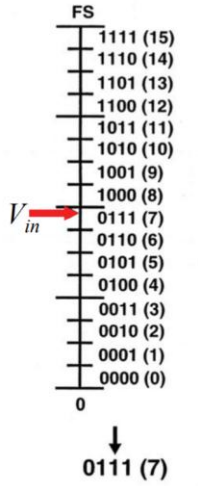
- ADC translate the analog signal to its digital representation
- Different methods
  - Successive Approximation (SAR), Pipeline, Combination of **SAR and Flash**.

LTC2242 12bits@250Msps

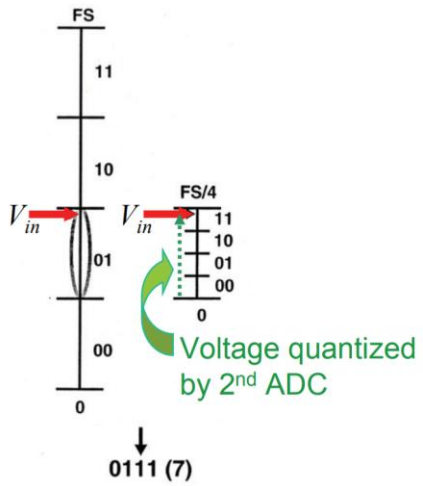


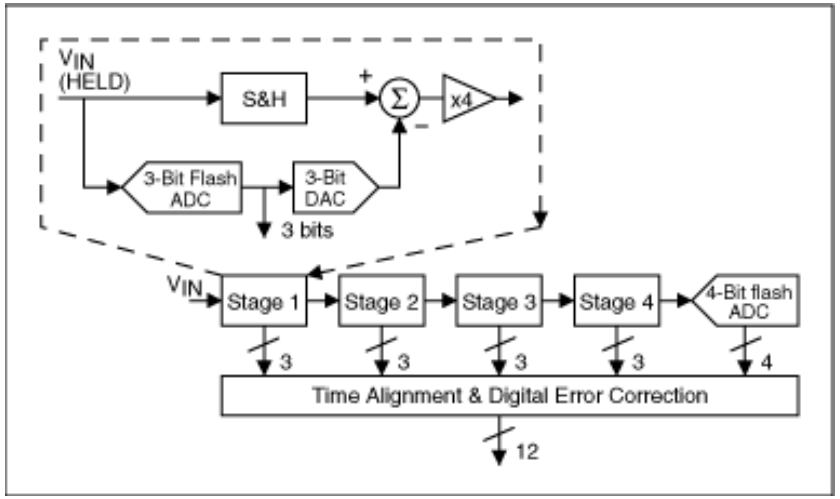


4-bit Straight Flash ADC



Ideal 2-step Flash ADC

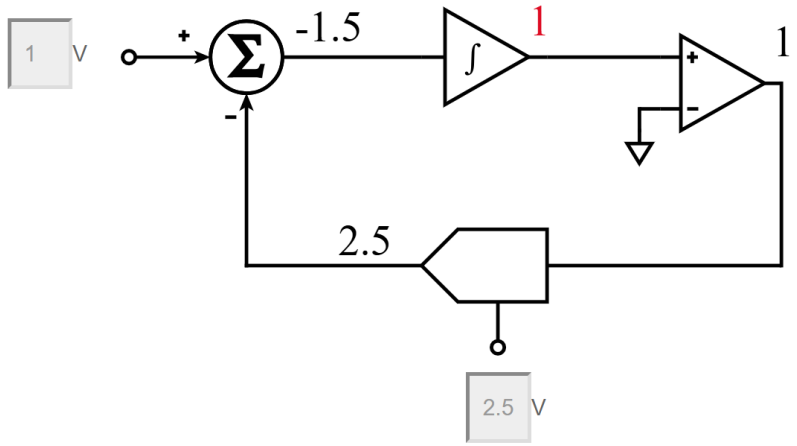




Electronics – AD Converter

- ADC translate the analog signal to its digital representation

- Different methods
  - **Sigma-Delta** ADC (oversampling, slow converter, high resolution)



Analog.com

Bit Stream: 1 0 1 1 1 0 1 1 0 1 1 0 1 1 1 0 1 1 0 1 1 0 1 1 1 0 1 1 0 1

Mean Output: 1

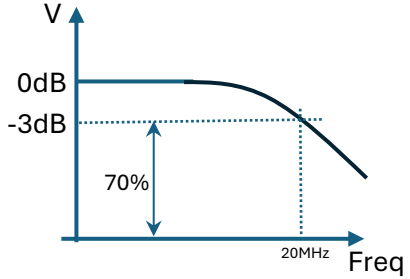
The integrator (sigma) output becomes 1V.

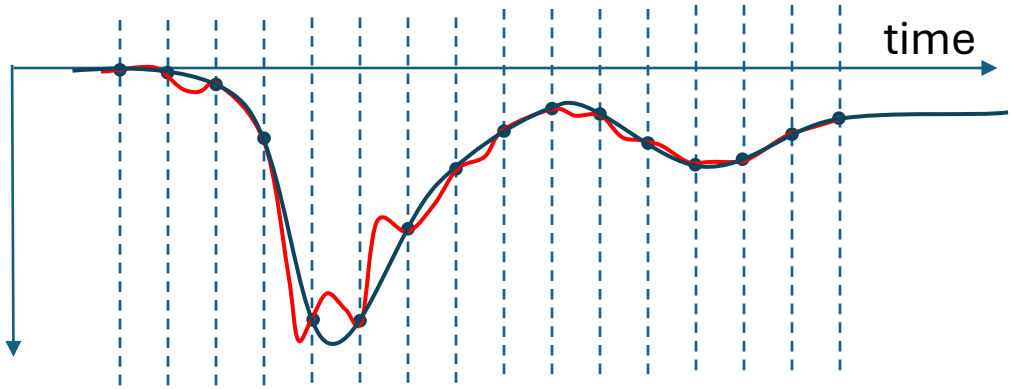
Digitization

- Digitize the signal waveform
  - But does this WF shape fits the real signal?
    - Are you sampling the signal fast enough?
    - What is the bandwidth of the incoming signal?

V1740 : 12 bit 62.5 MS/s ADC
V2740 : 16 bits 125MHz/s ADC

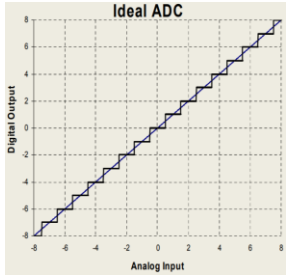
VX2745 : bandwidth of 20 MHz (-3dB)
VX2740 : bandwidth of 50 MHz (-3dB)

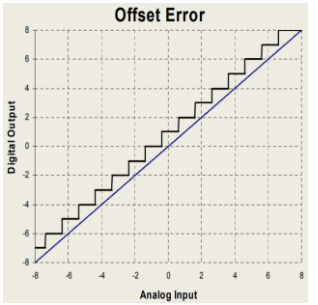




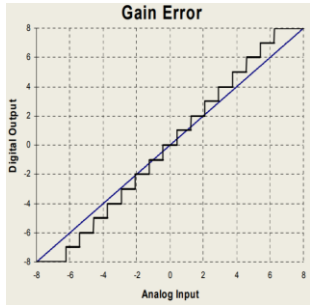
- Signal features can be extracted/improved in the digital world (DSP) only if the digital representation is faithful -> High sampling, good conversion characteristics

Amplitude, Charge, timing measurement errors!

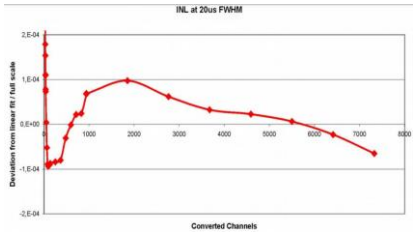




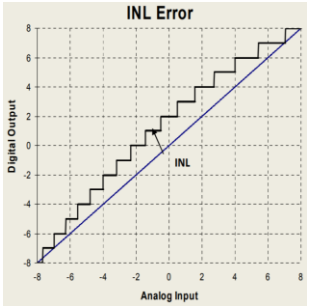
Can be corrected using a reference voltage



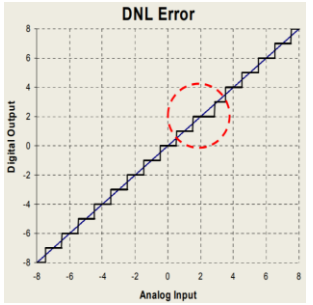
Slope issue, can be corrected using a second point reference voltage



Example of INL (0.01%) Mesytec



Cannot be corrected, due to ADC architecture

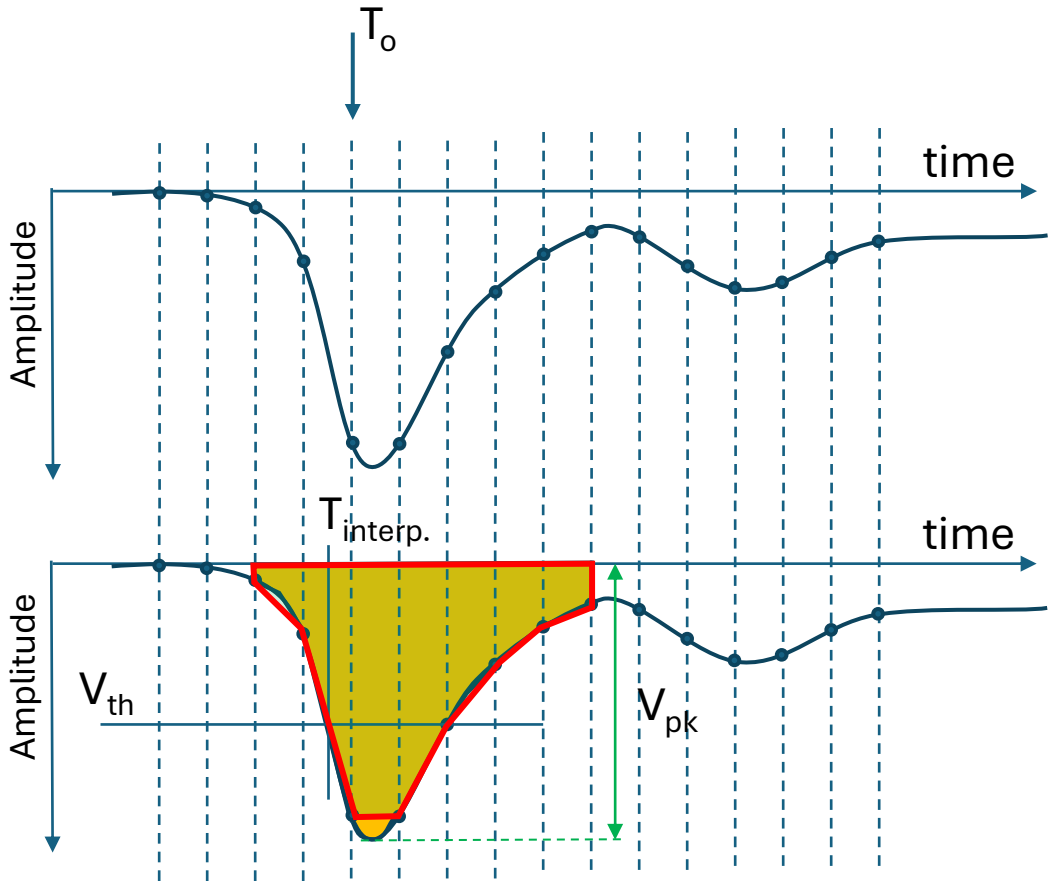


Cannot be corrected, due to ADC architecture

Cypress

Digitization

- Digitize the signal waveform, **WaveForm Digitizer (WFD)**
  - Collect amplitude values at fix time interval in “real time”
  - Extract signal features within the digital world, Digital Signal Processing (DSP)…
  - Good representation of the WF out of the collected data (Q, V_{pk}, Time)



Type of ADC	Resolution (max. bits)	Conversion rate (max.)
Dual slope	12-20	100 samples/s
Successive approximation	8-18	10 Msamples/s
Flash	4-12	10 Gsamples/s
Pipeline	8-16	1 Gsample/s
Delta-sigma	8-32	1 Msample/s

Electronicdesign

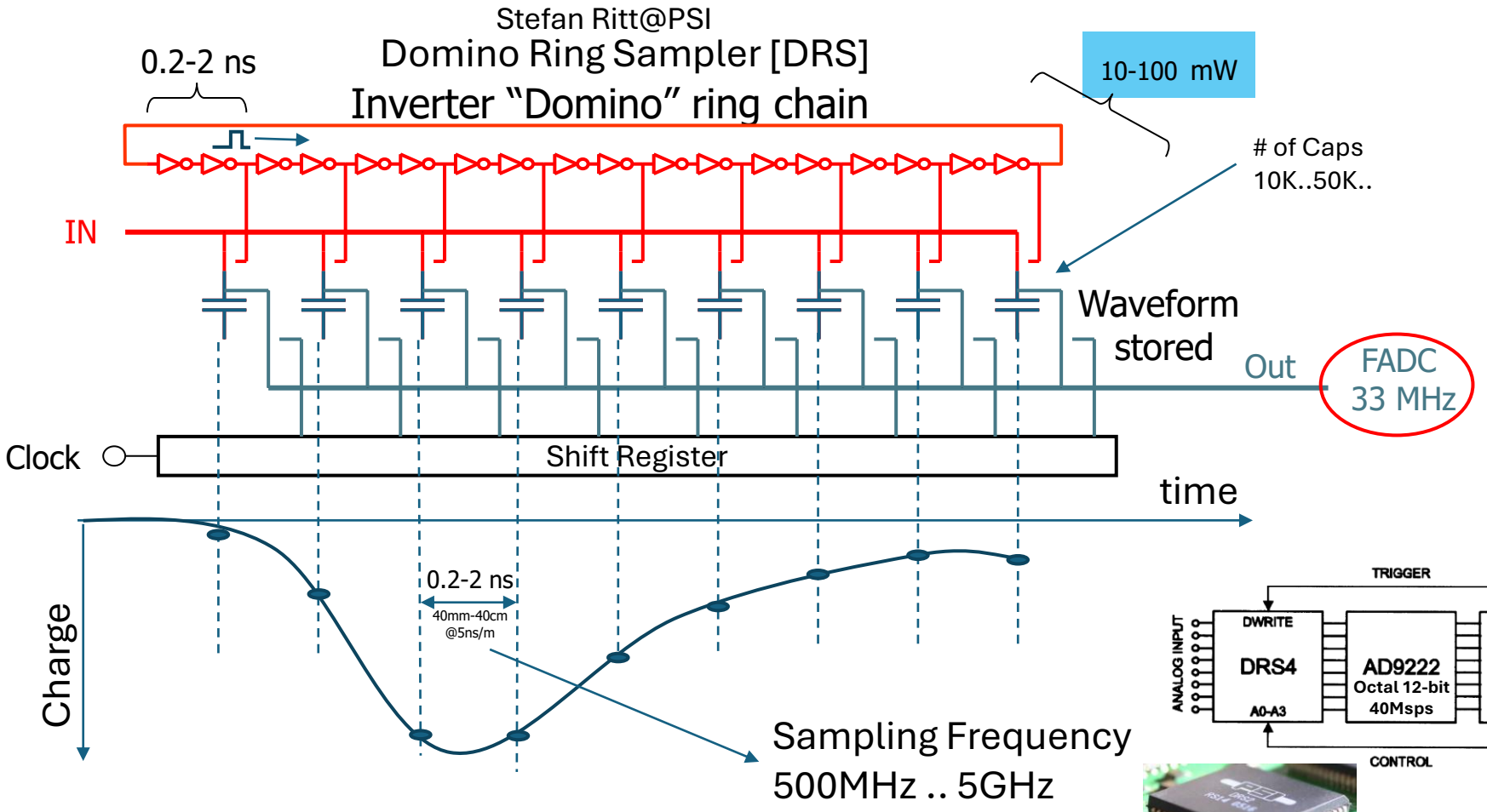
8 channels Flash ADC 14-bit @ 500Msps (2ns) CAEN
Meaning every 2ns, 14-bit data can be recorded.
No deadtime!

AD9653 (AD, 4ch., 16-bit, 125MS/s, $2V_{p2p}$, Pwr 0.7W, ~USD0.5K).
ADC12DJ5200RF (TI, 2ch., 10-bit, 5.2 GS/s, 0.825 V_{p2p} , Pwr 4W, USD3K)
AD9208 (AD, 2ch., 14-bit, 3 GS/s, $1.7V_{p2p}$,Pwr 1.7W, ~USD1.4K).

Digitization

ASIC (Application Specific Integrated Circuit) – FIXED function - WFD chip

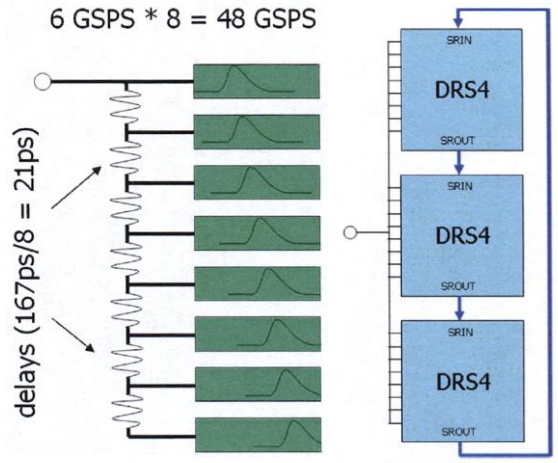
- Yet another Waveform Digitizer architecture : **Switched-Capacitor Array [SCA],** an Ultra-Fast ADC ASIC



DRS4 (PSI, 9ch., 0.7-5 GS/s, ~1V_{p2p} ,Pwr 0.14W@2Gs/s, ~USD60@1K in 2015).

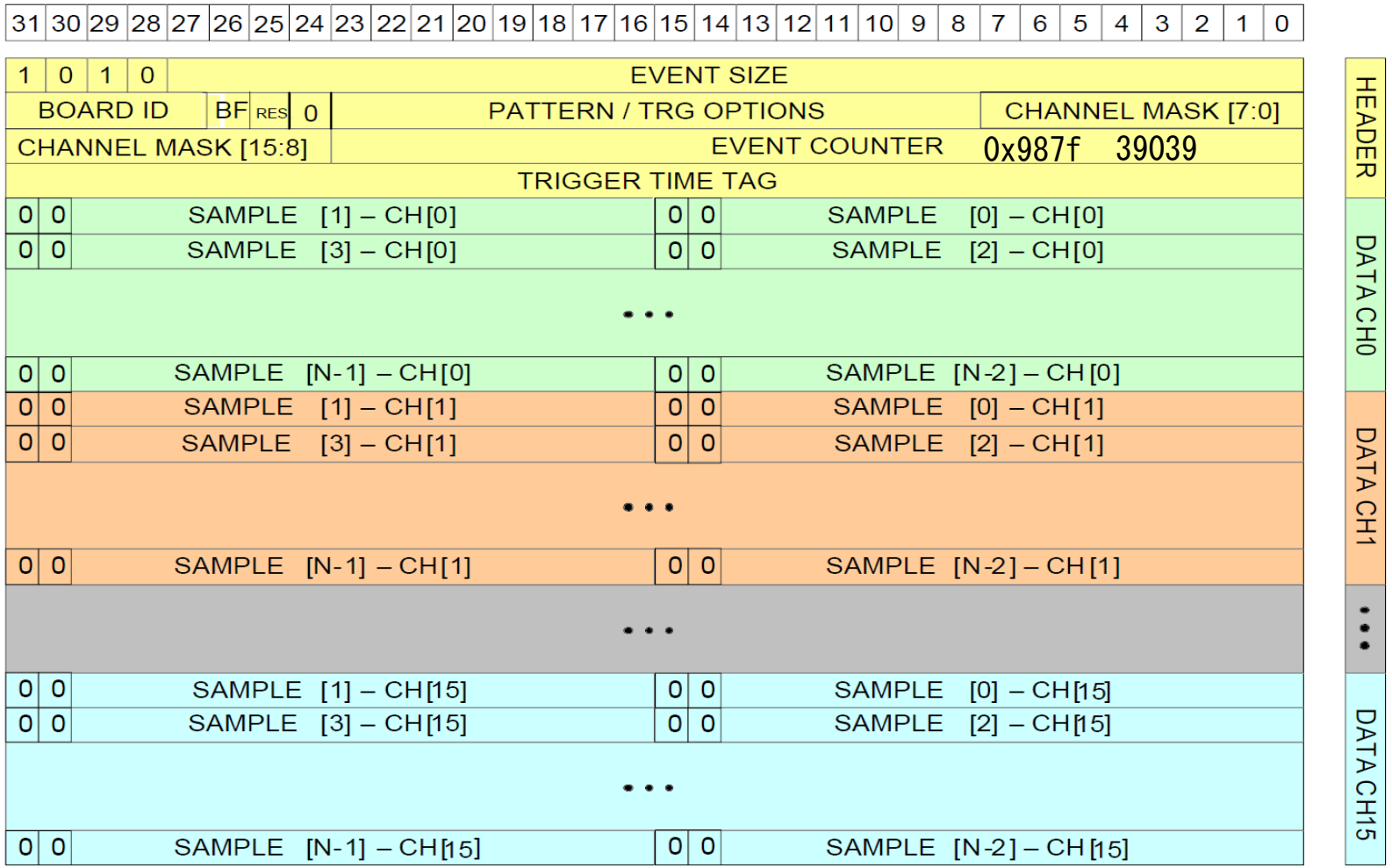
- ! individual cells are readout through a standard ADC at relatively low speed
- Need calibration in charge and time. All quantization errors apply to this architecture.
- Number of cell per chip is limited!

- But neat trick can be played!



Data Format

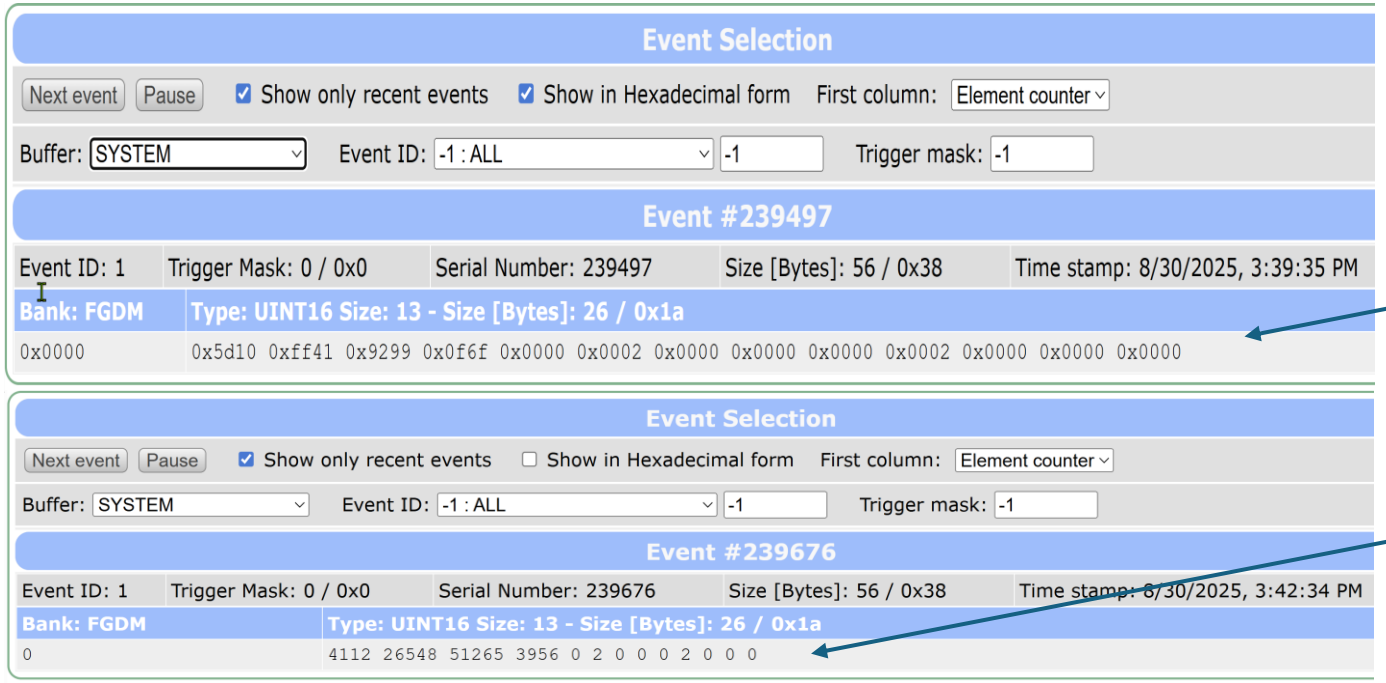
Digitizer binary output data block (CAEN)



Binary format:
0000 0010 1101 0111
≡
Hex format:
0x02D7

```
0xa0007d14    Header[0]
0x000002ff    Header[1]
0xff00987f    Header[2]
0x13a291b7    Header[3]
0x3c173c19    Data[n+1, n]
0x3c1a3c1a    Data[n+3, n+2]
0x3c183c1b    Data[n+5, n+4]
```

Data Format



GDM data block

Hexadecimal representation

Decimal representation

CAEN V1725 : 14-bit@250Msps (Time bin = 4ns)

What about those data?
In Decimal format they make no sense!

```
...
  1-> 0xa0007d14 0x000002ff 0xff00987f 0x13a291b7 0x3c1807d1 0x3c183c1c 0x3c1a3c19 0x3c1b3c18
  9-> 0x3c1c3c16 0x3c193c12 0x3c1a3c19 0x3c163c18 0x3c183c1a 0x3c163c17 0x3c1f3c17 0x3c193c18
 17-> 0x3c183c19 0x3c183c1a 0x3c193c1b 0x3c173c19 0x3c193c14 0x3c1b3c18 0x3c183c16 0x3c183c18
 25-> 0x3c173c19 0x3c1a3c19 0x3c183c19 0x3c183c12 0x3c183c1a 0x3c193c19 0x3c1c3c14 0x3c173c19
 33-> 0x3c193c14 0x3c193c16 0x3c153c1a 0x3c1b3c15 0x3c183c16 0x3c163c19 0x3c193c17 0x3c1c3c19
 41-> 0x3c1a3c18 0x3c193c17 0x3c193c15 0x3c173c1b 0x3c183c17 0x3c163c18 0x3c173c15 0x3c163c1a
 49-> 0x3c1c3c14 0x3c173c1c 0x3c193c16 0x3c183c19 0x3c193c16 0x3c173c1a 0x3c173c17 0x3c1b3c18
 57-> 0x3c163c13 0x3c193c17 0x3c163c19 0x3c1d3c15 0x3c1b3c18 0x3c163c19 0x3c1b3c1a 0x3c153c1c
 65-> 0x3c183c1b 0x3c1c3c16 0x3c193c17 0x3c193c18 0x3c183c1a 0x3c193c1a 0x3c173c18 0x3c173c1d
 73-> 0x3c173c17 0x3c1b3c1b 0x3c173c17 0x3c163c19 0x3c183c18 0x3c1c3c17 0x3c1c3c17 0x3c173c1b
 81-> 0x3c173c18 0x3c183c19 0x3c1a3c19 0x3c193c1b 0x3c193c1b 0x3c1b3c19 0x3c173c16 0x3c1b3c18
 89-> 0x3c1b3c15 0x3c193c1b 0x3c173c1a 0x3c163c1a 0x3c173c19 0x3c153c19 0x3c153c15 0x3c1c3c1c
 97-> 0x3c183c14 0x3c1a3c17 0x3c183c1b 0x3c183c1d 0x3c183c15 0x3c183c16 0x3c1a3c16 0x3c1b3c1b
105-> 0x3c163c1b 0x3c163c18 0x3c193c15 0x3c193c14 0x3c163c1c 0x3c153c17 0x3c193c18 0x3c173c16
...
```

Data Format R/W

Offset	R/W	Mode	Function/Register
0x0	R/W	D32	Control/Status register
0x4	R	D32	Module Id. and firmware revision register
0x8	R/W	D32	Interrupt configuration register
0xC	R/W	D32	Interrupt control/status register
0x10	R/W	D32	Acquisition preset register
0x14	R	D32	Acquisition count register
0x18	R/W	D32	LNE prescale factor register
0x20	R/W	D32	Preset value register counter group 1 (1 to 16)
0x24	R/W	D32	Preset value register counter group 2 (17 to 32)
0x28	R/W	D32	Preset enable and hit register
0x100	R/W	D32	(Acquisition) Operation mode register
0x104	R/W	D32	Copy disable register
0x108	R/W	D32	LNE channel select register (1 of 32)
0x10C	R/W	D32	PRESET channel select register (2 times 1 out of 16)
0x110	R/W	D32	MUX_OUT channel select register (firmware 01 0B, 1 of 32, note 2)
0x200	R/W	D32	Inhibit/count disable register
0x204	W	D32	Counter Clear register
0x208	R/W	D32	Counter Overflow read and clear register
0x210	R	D32	Channel 1/17 Bits 33-48
0x214	R/W	D32	Veto external count inhibit register (firmware 01 09, note 2)
0x218	R/W	D32	Test pulse mask register (firmware 01 0A, note 2)

VME Multichannel Scaler SIS 3820

From base address (32 bits address)

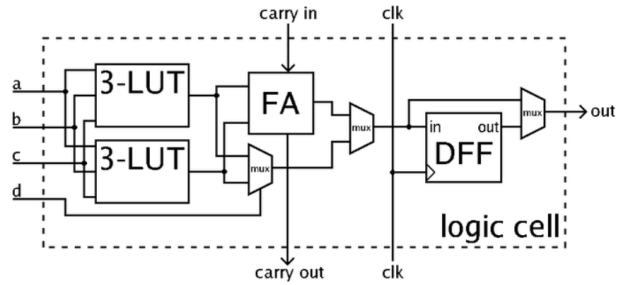
Address offsets list for R//W functions

Offset: 0x10c

Bit	Function
31	no function, read as 0
...	...
20	no function, read as 0
19	bit 3 of PRESET channel select group2
18	...
17	...
16	bit 0 of PRESET channel select group2
15	no function, read as 0
...	...
4	no function, read as 0
3	bit 3 of PRESET channel select group1
2	...
1	...
0	bit 0 of PRESET channel select group1

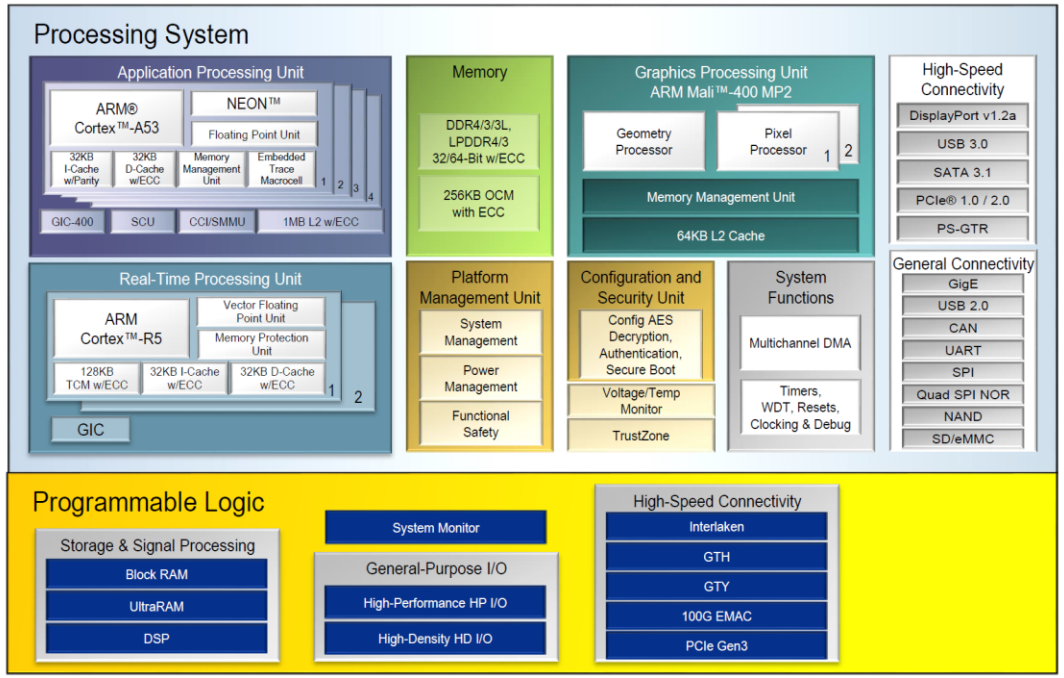
Field Programmable Gate Array (FPGA)

Integrated circuit that can be configured for a specific purpose by a customer. It is a matrix of configurable logic blocks connected by programmable interconnects and therefore it is reprogrammable.



Logic cell

Zynq® UltraScale+™ MPSoCs: EG Block Diagram



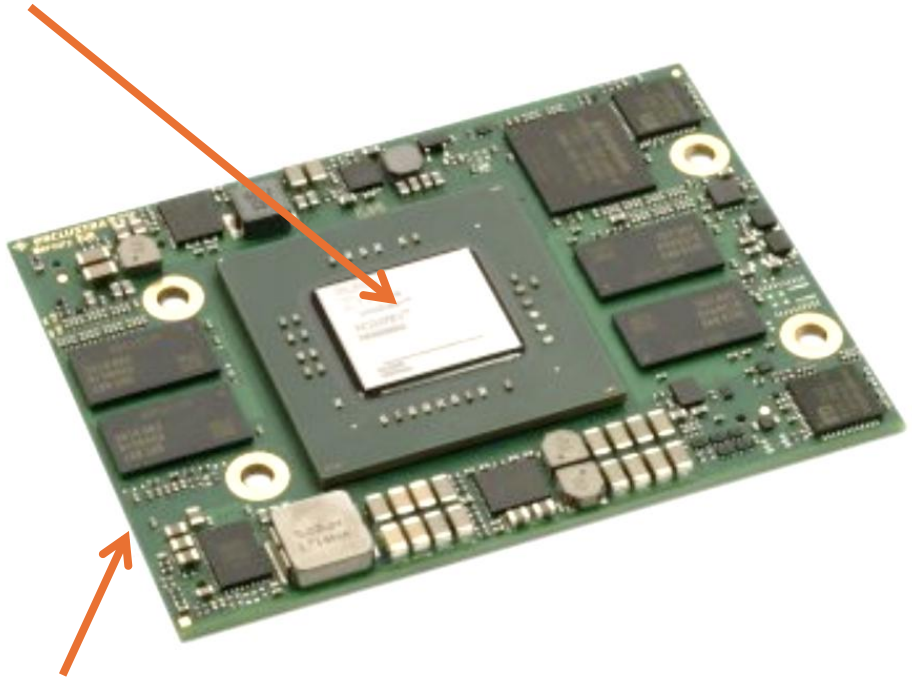
Zynq® UltraScale+™ MPSoCs: EG Devices

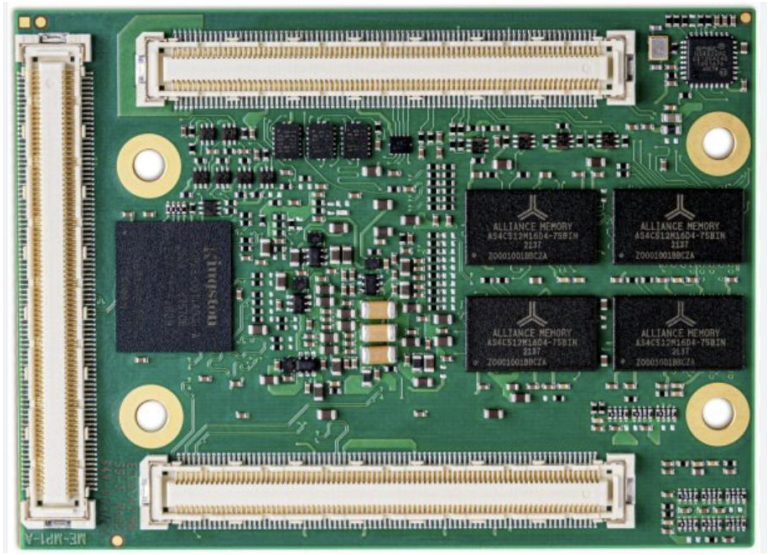
	Device Name[1]	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.5GHz									
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB									
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore™ up to 600MHz									
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core									
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz									
		Memory	L2 Cache 64KB									
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC									
		Static Memory Interfaces	NAND, 2x Quad-SPI									
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet									
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains									
		Security	RSA, AES, and SHA									
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor									
PS to PL Interface		12 x 32/64/128b AXI Ports										
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256	469	504	600	653	747	926	1,143
		CLB Flip-Flops (K)	94	141	176	234	429	461	548	597	682	847	1,045
		CLB LUTs (K)	47	71	88	117	215	230	274	299	341	423	523
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
		UltraRAM (Mb)	-	-	13.5	18.0	-	27.0	-	22.5	31.5	28.7	36.0
	Clocking	Clock Management Tiles (CMTs)	3	3	4	4	4	8	4	8	4	11	11
	Integrated IP	DSP Slices	240	360	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
		PCI Express® Gen 3x16	-	-	2	2	-	2	-	4	-	4	5
		150G Interlaken	-	-	-	-	-	-	-	1	-	2	4
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	2	-	2	4
		AMS - System Monitor	1	1	1	1	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	16	16	24	24	24	32	24	44	44
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-	16	-	28	28
	Speed Grades	Extended[2]	-1 -2 -2L			-1 -2 -2L -3				-1 -2 -2L -3			
		Industrial	-1 -1L -2										

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

FPGA, SoC, SoM

SoC chip (System on a Chip) is an integrated circuit that consolidates all or most of the essential electronic components of a device onto a single chip

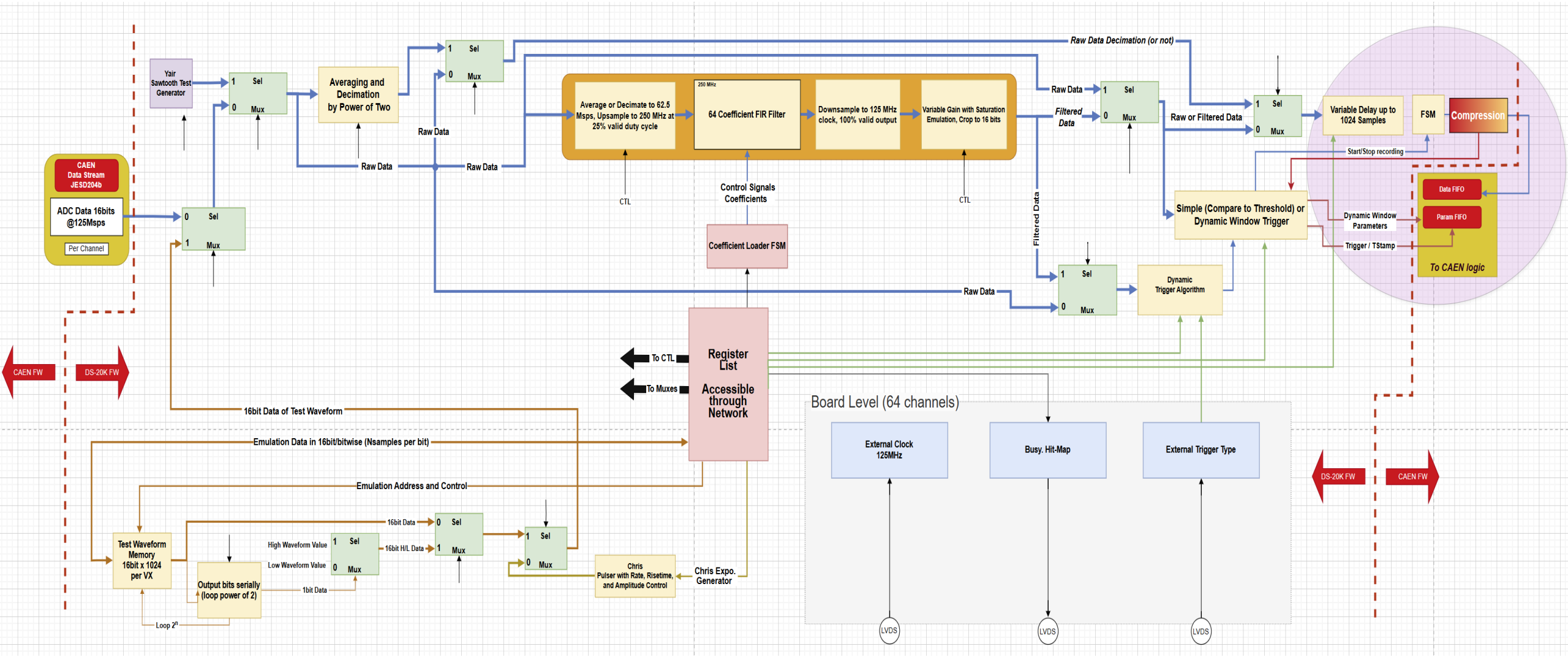




A **system on a module** (**SoM**) is a board-level circuit that integrates a system function in a single module. It may integrate digital and analog functions on a single board.

Data Processing in FPGA

DRAWIO
https://www.drawio.com/
Great drawing tool



Languages for Data Processing in FPGA

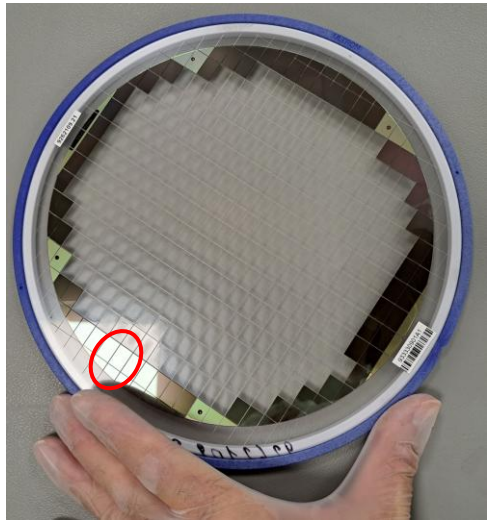
```
152 always@(posedge int_rst, posedge clk_wr) begin
153         if(int_rst) begin
154                 r_trigger                               <= 1'b0;
155                 delay_cnt                               <= {SZ_DELAY{1'b0}};
156                 trig_accepted_cnt       <= {32{1'b0}};
157                 trig_dropped_cnt                <= {32{1'b0}};
158                 ts_start                                <= {SZ_TIME{1'b0}};
159                 ts_trig                                         <= {SZ_TIME{1'b0}};
160         end else begin
161                 ts_start                                <= ts_start;
162                 ts_trig                                 <= ts_trig;
163                 trig_accepted_cnt               <= trig_accepted_cnt;
164                 trig_dropped_cnt                <= trig_dropped_cnt;
165                 r_trigger                               <= 1'b0;
166                 // Don't touch timestamp on run start, a packet may still be being finished assembling
167                 if(run_os) begin
168                         r_trigger                               <= 1'b0;
169                         delay_cnt                               <= {SZ_DELAY{1'b0}};
170                         trig_accepted_cnt       <= {32{1'b0}};
171                         trig_dropped_cnt                <= {32{1'b0}};
172                         ts_start                                <= {SZ_TIME{1'b0}};
173                         ts_trig                                         <= {SZ_TIME{1'b0}};
174                 end else begin
175                         if(trig_in && run) begin
176                                 if(!triggered) begin
```

Hardware **D**escription **L**anguages (HDLs) VHDL and **Verilog**
... but now you can find:

High-Level Languages: C, C++, OpenCL, Python (via MyHDL, Migen, PyRTL, etc.), Scala (Chisel), Haskell (Clash), MATLAB

Data Acquisition – Computers, Chips (CPU, GPU, AI, …)

- Motorola 6800 microprocessor (introduced in 1974)
  - Die size 16.5 mm^2
  - Transistor count **4,100 transistors**.
  - **250** transistors per mm^2
  - Clock 1 MHz, 8-bit data bus, 16-bit address bus
- Intel Core i9-13900k (2022)
  - Die area 257mm^2
  - Transistor count 20 billions ($20x10^{9)}$
  - 75 millions transistors per mm^2
- AMD Ryzen 7 7700x (2022)
  - The Core Complex Die (CCD) + I/O Die (IOD)
  - 6.5 billion transistors for **70** mm^2 + 3.4 billion transistors for 122 mm^2.
  - 4.5-5.4 GHz, 64-bit data bus, 52-bit address bus
  - 50 millions transistors per mm^2
- Cerebras WSE-3 (Wafer Scale Engine) FULL WAFER!
  - Die size 220mm x 220 mm (46225 $mm^{2)}$
  - 900K cores, 4 trillion transistors ($4x10^{12}$) on a single chip.
  - 86 millions transistors per mm^2



DarkSide-20K 8” wafer
SiPM size: 8mm x 12mm
area: 96 mm^2

	Cerebras WSE-3
Chip size	46,225 mm²
Cores	900,000
On-chip memory	44 Gigabytes
Memory bandwidth	21 Petabytes/sec
Fabric bandwidth	214 Petabits/sec

Cerebras WSE-3
4 Trillion Transistors
46,225 mm^2 Silicon
~22cmx22cm

Wafer Scale Engine-3 © Cerebras

Electronics instrumentation

Where all this electronics plugs in?

Electronics Bus standards

NIM (1968): Nuclear Instrument Module

- Still in use for standard logic for workbench tests

CAMAC (1972): Computer Automated Measurement and Control, use TTL parallel bus

- Still in use in older system (Triumf Cyclotron Control).

VME (1981): Vesa Module Europcard

- Very much in use, as VME modules are still commercially available (parallel backplane bus).

~~FastBus (1984): To replace CAMAC with ECL parallel bus~~

- Already dead

VXI (2004): **V**ME e**X**tensions for **I**nstrumentation

- Was an extension to fit a transition…

VXS (2006): VMEBus Switched Serial

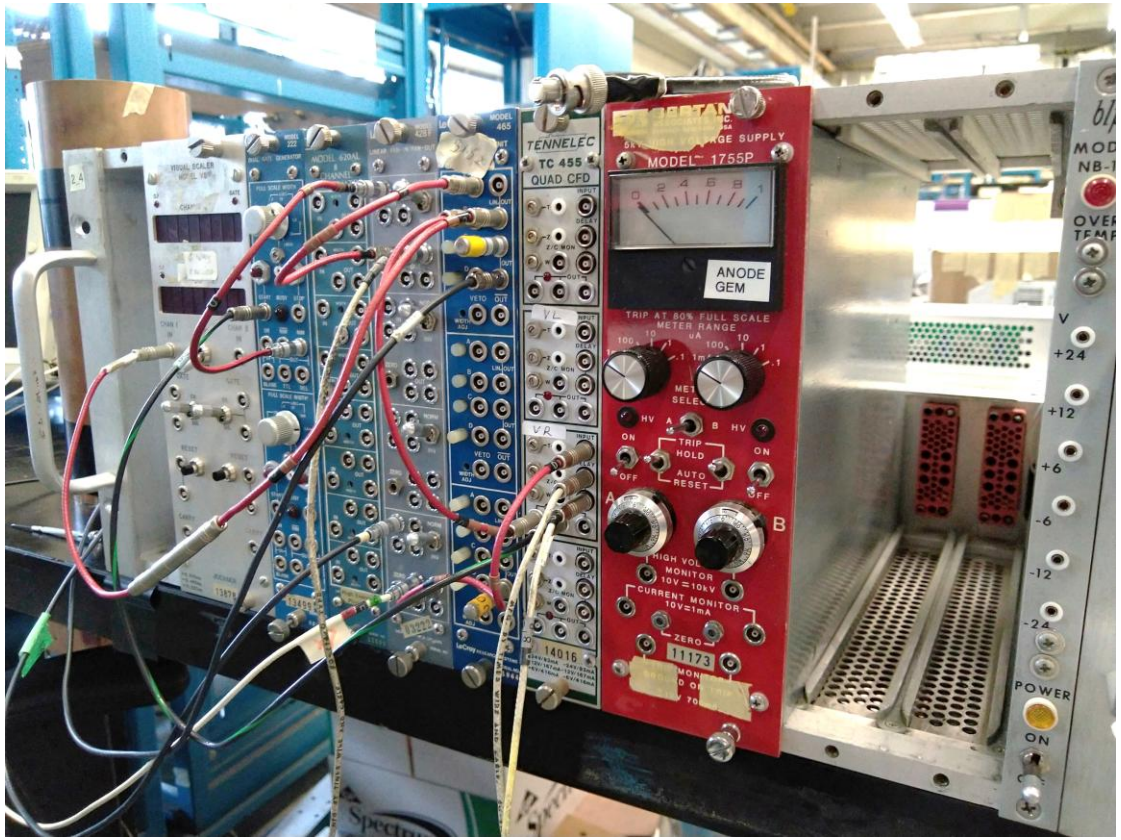
- In use due to its serial bus backplane and slot configuration (Full mesh, Dual star). Redundant

ATCA (uTCA) (2002): Advanced Telecommunications Computing Architecture

- PCI Industrial Computer Manufacturers Group (PICMG)
- New trend for Physics applications, combines VXS, self-managed crate, Single -48V, fully differential connections.

Electronics instrumentation

NIM (1968) : Nuclear Instrument Module (still in use)



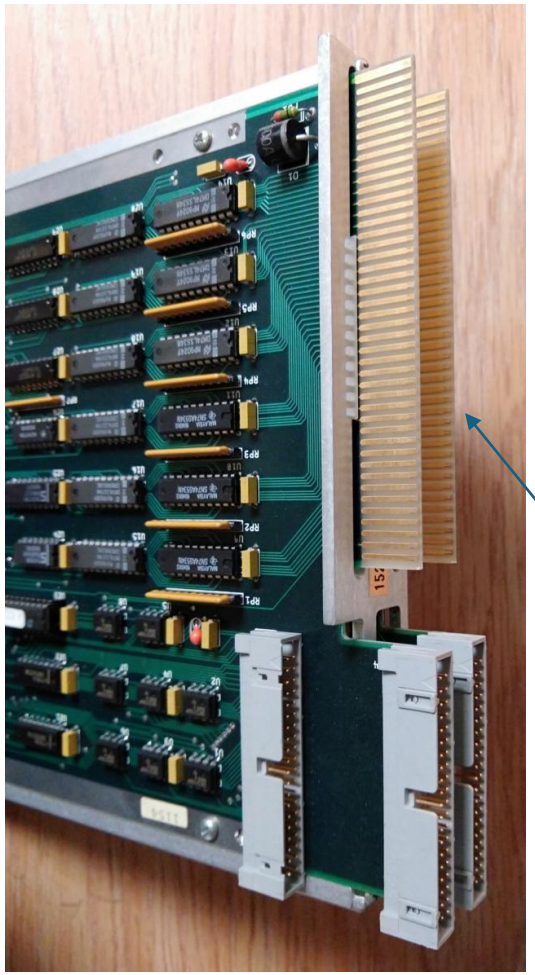
Basic Analog elements:
Delay
Splitter
Discriminator
Attenuator
Pre-Amplifier

Basic Logic elements
Inverter AND, OR
Latch, Timer, Scaler

For Power
+/- 6V
+/- 12V
+/-24V

Electronics instrumentation

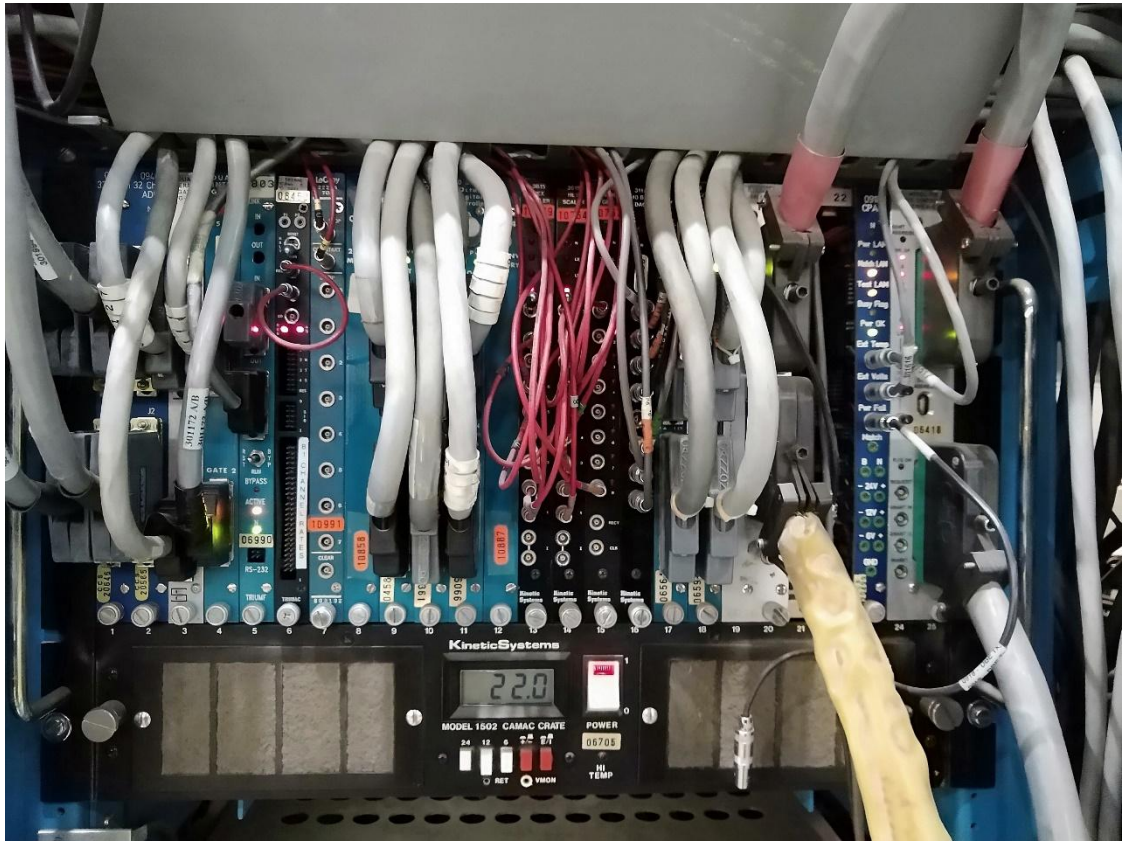
CAMAC (1972) : Computer Automated Measurement and Control (found in older working systems)



Analog to Digital converter
Programmable…
Delays, Discriminators,
Attenuators, I/Os, etc…
ADC, TDC, Scalers…

For Power:
+/- 6V, +/- 12V, +/-24V
AC117V

For Communication:
Slot Address N5
Module Add A4
Function bus F5
Data bus R24/W24



Electronics instrumentation

VME (1981) : Vesa Module Europcard (currently used in most physics labs)

FPGAs for Logic

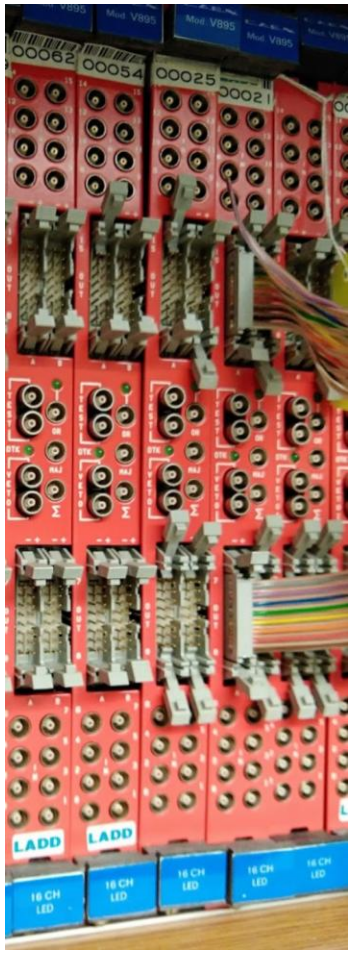
VMEIO - 2009

CAEN V1720 8ch, 12bits@250Msps

Analog to Digital converter
Programmable…
Delays, Discriminators,
Attenuators, I/Os, etc…
ADC, TDC, Scalers…

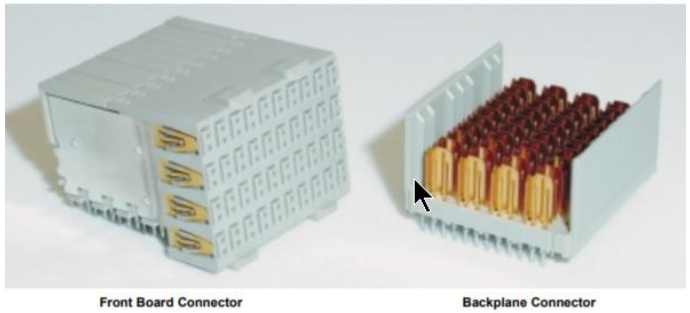
For Power:
+/- 5V, +/- 12V, +3.3V

For Communication
Address Bus: A32
Data Bus: D32
Control bus: IRQ, AM5, AS, DS0/1, +…

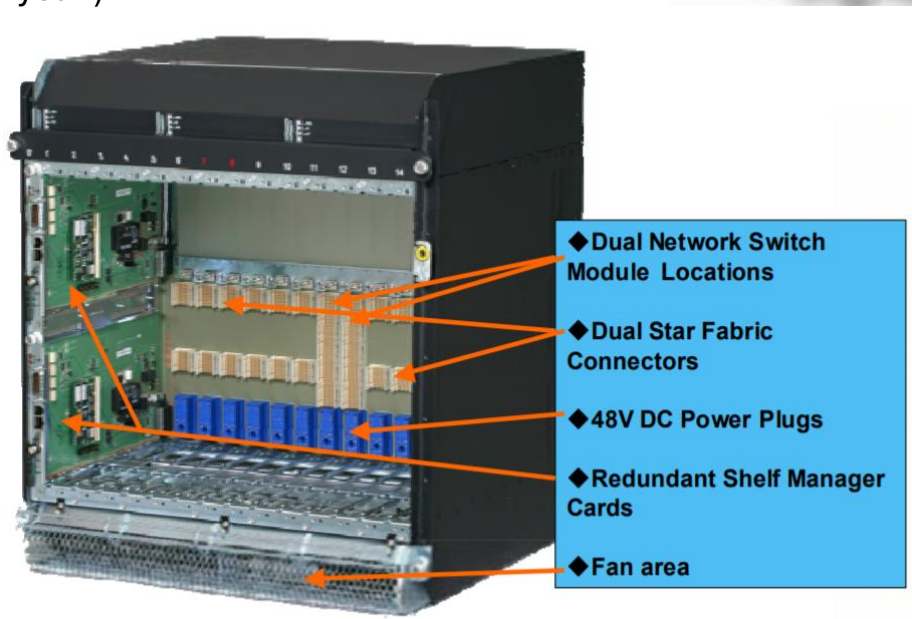


Electronics instrumentation

ATCA (uTCA): Advanced Telecommunications Computing Architecture (New large system choice)

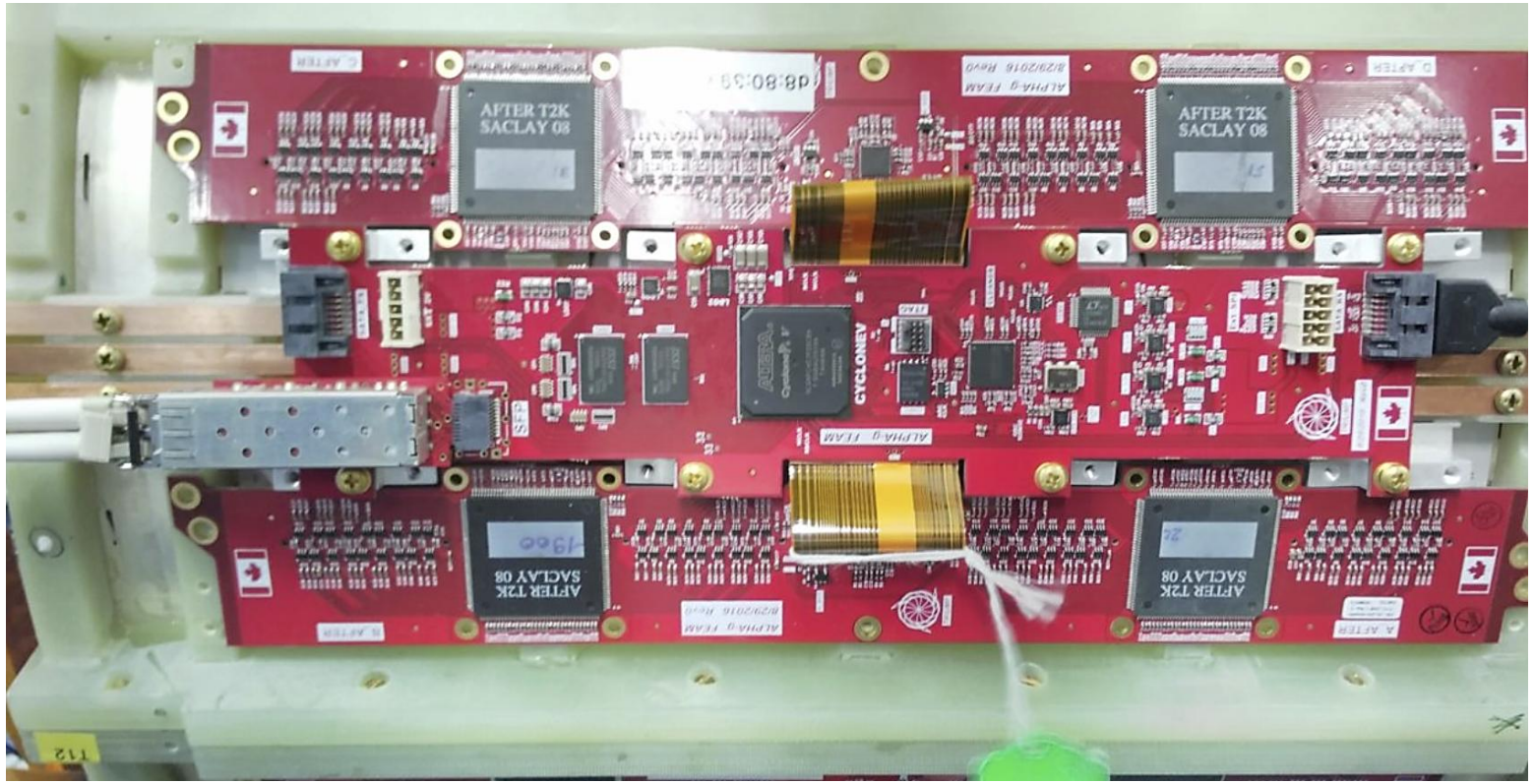


Five nines means "99.999%", High availability of services system (five-9 / max down time of 5.26 minutes per year.)



Electronics instrumentation

Custom Electronics boards



Alpha-g (custom card)
288 cathode strips readout board
4 AFTER ASICs, 1 Cyclone-V FPGA

DarkSide-20K (VME board)
Clock distribution board16 x 2.5Gbps links
1 SoM Enclustra XU8

Data Storage

- **Tapes** not used at the DAQ level anymore (Exabyte 8mm)
- **Hard Disk Drive** used for DAQ due to high storage capacity
- **Solid-State Drive** used for OS and user applications
- **Tape drive robots** in use for data backup and long-term data retention (LTO tape)
- **Cloud storage** (private) in use for data processing

LTO-4:0.8TB
LTO-10:12TB

CERN Cray X-MP/48 (1988)
64-bit@80MHz, RAM 8.39MB

Data Acquisition – A few more points!

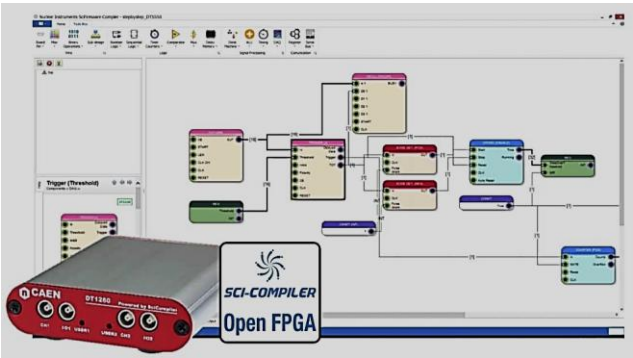
- Today's Acquisition module architecture
- Time reference, Clock, Clock distribution
- Trigger or Triggerless

Data Acquisition – Acquisition module architecture

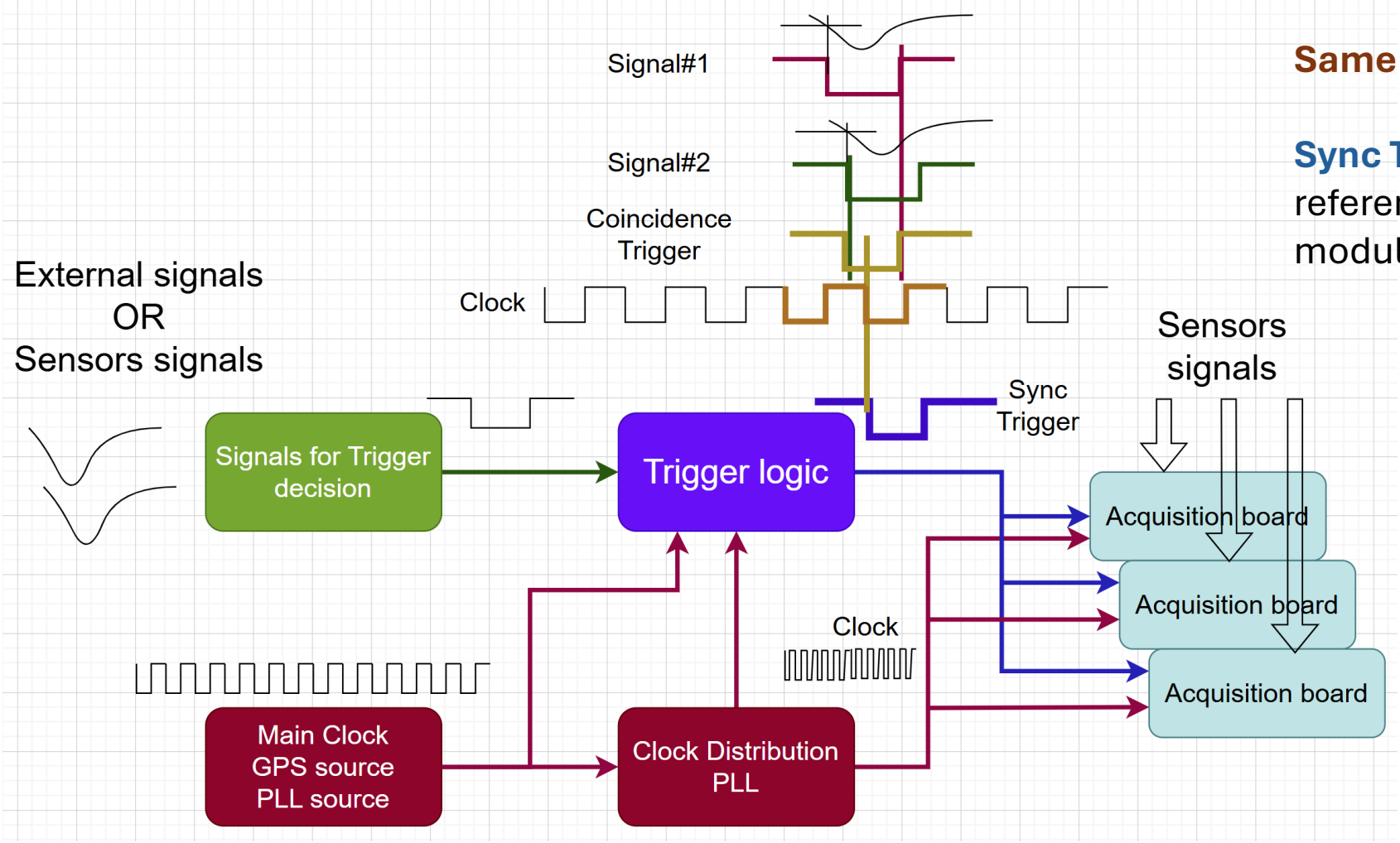
CAEN Commercial WFD (ex:VX274x) *Open FPGA*

I. **Allow user to integrates its own FW block into the commercial module.**

II. **Use CAEN SCI-Compiler**



Data Acquisition - Time reference, Clock, Clock distribution



Same clock across all Acq modules

Sync Trigger needed for same time reference across all the acquisition modules

Triggered Acquisition

Main clock GPS (1pps, 10MHz)
Clock distribution (10MHz to sampling Freq.)

Data Acquisition - Trigger or Triggerless?

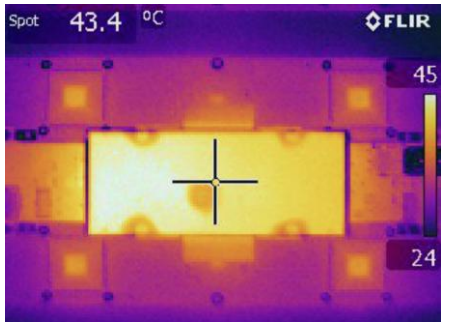
- In case of large number of channels to build a trigger *or* too many logic required to make a coincidence trigger *or* coincidence timing not acceptable for the acquisition modules.

Triggerless or self-trigger

- Each channel operates with its own trigger method.
- Individual acquisitions are self-triggered by the input signal (requires a threshold).
- Capture and read out every “hit”, “pulse” (data rate can reach multiple GB/s).
- Events are reconstructed on a server farm, or a “Level 2 trigger” filters data to determine what to store (reducing the rate to a few MB/s).

Couple of more DAQ things to consider…

- “**Slow Control**” **is** part of the Data Acquisition System
  - Environment parameters, equipment monitoring, calibration system have to be included.
  - As the DAQ-SC manage the whole electronic chain, consider to separate the power for slow control from the main acquisition data path. Maintain control of the equipment status (under UPS).



- Don’t underestimate thermal effect on the electronics equipment
  - Heat dissipation, necessity of a cooling system (air, water)
  - High current through contacts (power connectors current rating!)

- Cable path organization facilitate channel recognition, module extraction (cable tray, please use GOOD label material!)

Data Acquisition - Software development tips

- Write code that is readable!
  "Always code as if the guy who ends up maintaining your code will be a violent psychopath who knows where you live."
- Give your functions sensible names
- Document the *why* not the *what!*

Test any code you write!
Just because your code compiles doesn't mean it's correct...
Strongly consider testing frameworks:
unittest module for Python
Catch2/GoogleTest for C++
May want to write a dummy/mock device so you can run tests without talking to real hardware devices

- ChatGPT / CoPilot / Claude / Cursor / Chat.PublicAI can generate code
- *May* generate working code quickly
  - For smaller tasks, okay
    - E.g. how to add a label to a plot in matplotlib / ROOT
    - Harder to maintain or to explain
    - ...

Ben Smith (Triumf DAQ group)

Data Acquisition – Program Coding (Midas)

Function Templates

```
/********************************************************************\
            Callback routines for system transitions

  These routines are called whenever a system transition like start/
  stop of a run occurs. The routines are called on the following
  occasions:

  frontend_init:  When the frontend program is started. This routine
                  should initialize the hardware.

  frontend_exit:  When the frontend program is shut down. Can be used
                  to release any locked resources like memory,
                  communications ports etc.

  begin_of_run:   When a new run is started. Clear scalers, open
                  run gates, etc.

  end_of_run:     Called on a request to stop a run. Can send
                  end-of-run event and close run gates.

  pause_run:      When a run is paused. Should disable trigger events.

  resume_run:     When a run is resumed. Should enable trigger events.
\********************************************************************/
```

Programming Languages

Assembler
Basic
Modula-2
Pascal
COBOL
FORTRAN
Java
Erlang
Tcl
Go
C
C++
Rust
Python
R
JavaScript
Grafana
…

Data Acquisition – Program Code structure (Midas)

```
EQUIPMENT equipment[] = {

   {"Trigger",                  /* equipment name */
      {1, 0,                    /* event ID, trigger mask */
       "SYSTEM",                /* event buffer */
       EQ_POLLED,               /* equipment type */
       0,                       /* event source */
       "MIDAS",                 /* format */
       TRUE,                    /* enabled */
       RO_RUNNING |             /* read only when running */
       RO_ODB,                  /* and update ODB */
       100,                     /* poll for 100ms */
       0,                       /* stop run after this event limit */
       0,                       /* number of sub events */
       0,                       /* don't log history */
       "", "", "",},
      read_trigger_event,       /* readout routine */
   },

   {"Periodic",                 /* equipment name */
      {2, 0,                    /* event ID, trigger mask */
       "SYSTEM",                /* event buffer */
       EQ_PERIODIC,             /* equipment type */
       0,                       /* event source */
       "MIDAS",                 /* format */
       TRUE,                    /* enabled */
       RO_RUNNING | RO_TRANSITIONS |   /* read when running and on transitions */
       RO_ODB,                  /* and update ODB */
       1000,                    /* read every sec */
       0,                       /* stop run after this event limit */
       0,                       /* number of sub events */
       TRUE,                    /* log history */
       "", "", "",},
      read_periodic_event,      /* readout routine */
   },

   {""}
};
```

Equipment

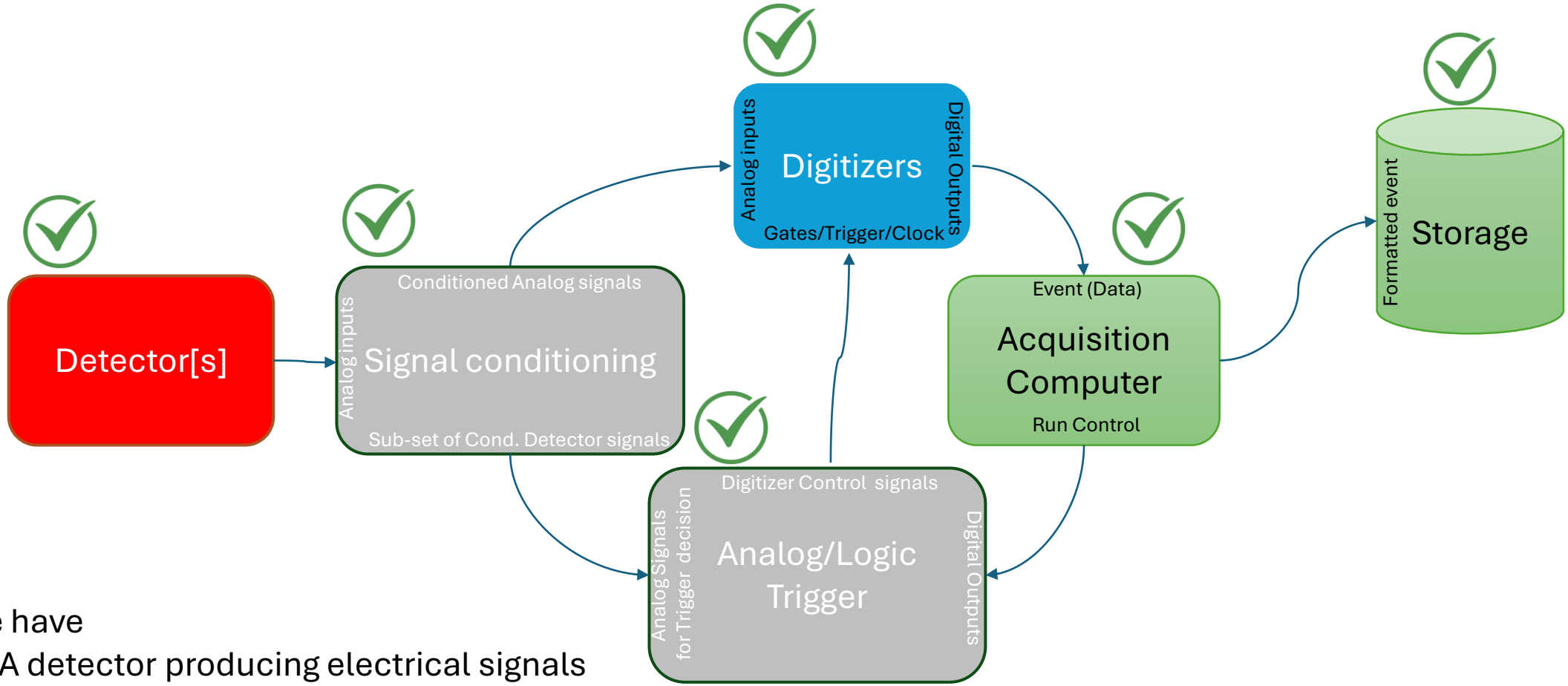
"Object" dealing with the acquisition of a block of data composing the final event

Readout Function

```
///------------------------------
/* create structured ADC2 bank */
bk_create(pevent, "ADC2", TID_DWORD, &pdata);
/* Read Event */
v792_EventRead(myvme, VADC2_BASE, pdata, &nentry);
pdata += nentry;
bk_close(pevent, pdata);
```

Specific software driver to acquire the data from the hardware module.
VME, Ethernet, GPIB, RS-232
I2C, SPI, CANBus, etc...

Data Acquisition – Data path

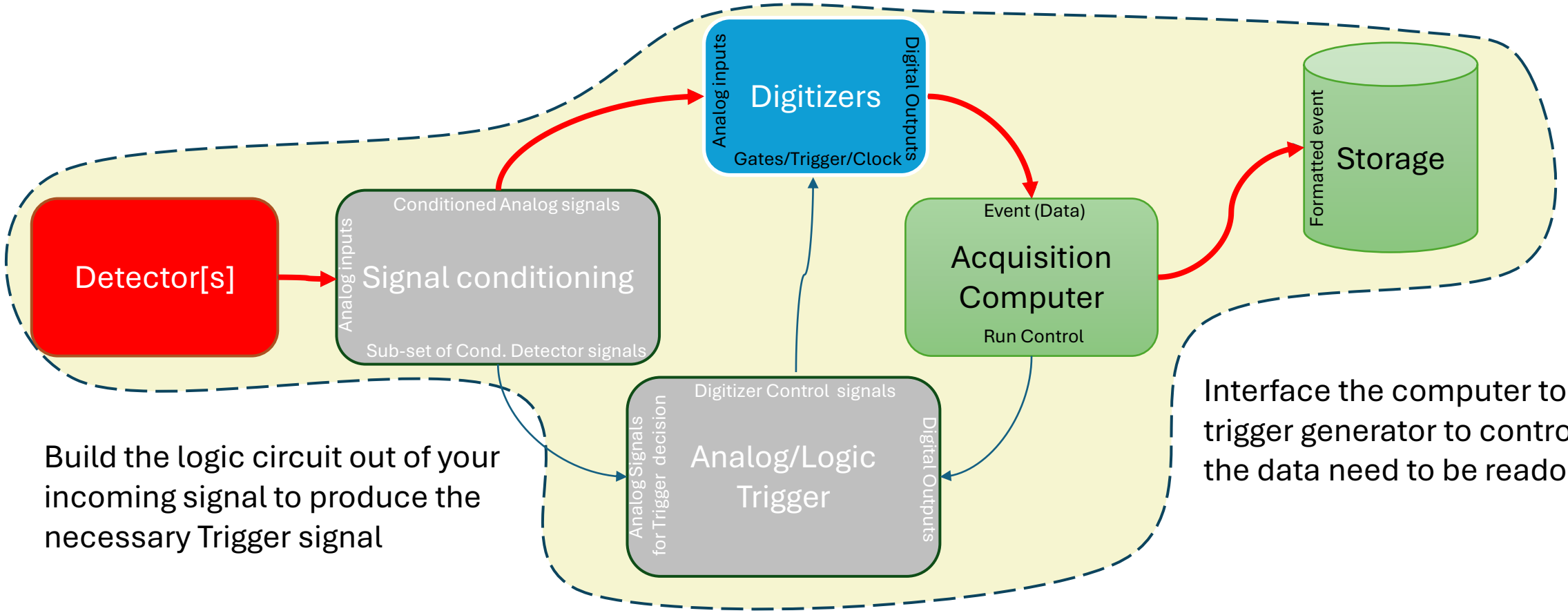


We have

- A detector producing electrical signals
- Analog electronic circuitry to condition/shape the signal for the digitizers
- Trigger circuit for event selection
- Digitizers for Amplitude, Charge, Time conversion, etc…

Data Acquisition – Physics Data path

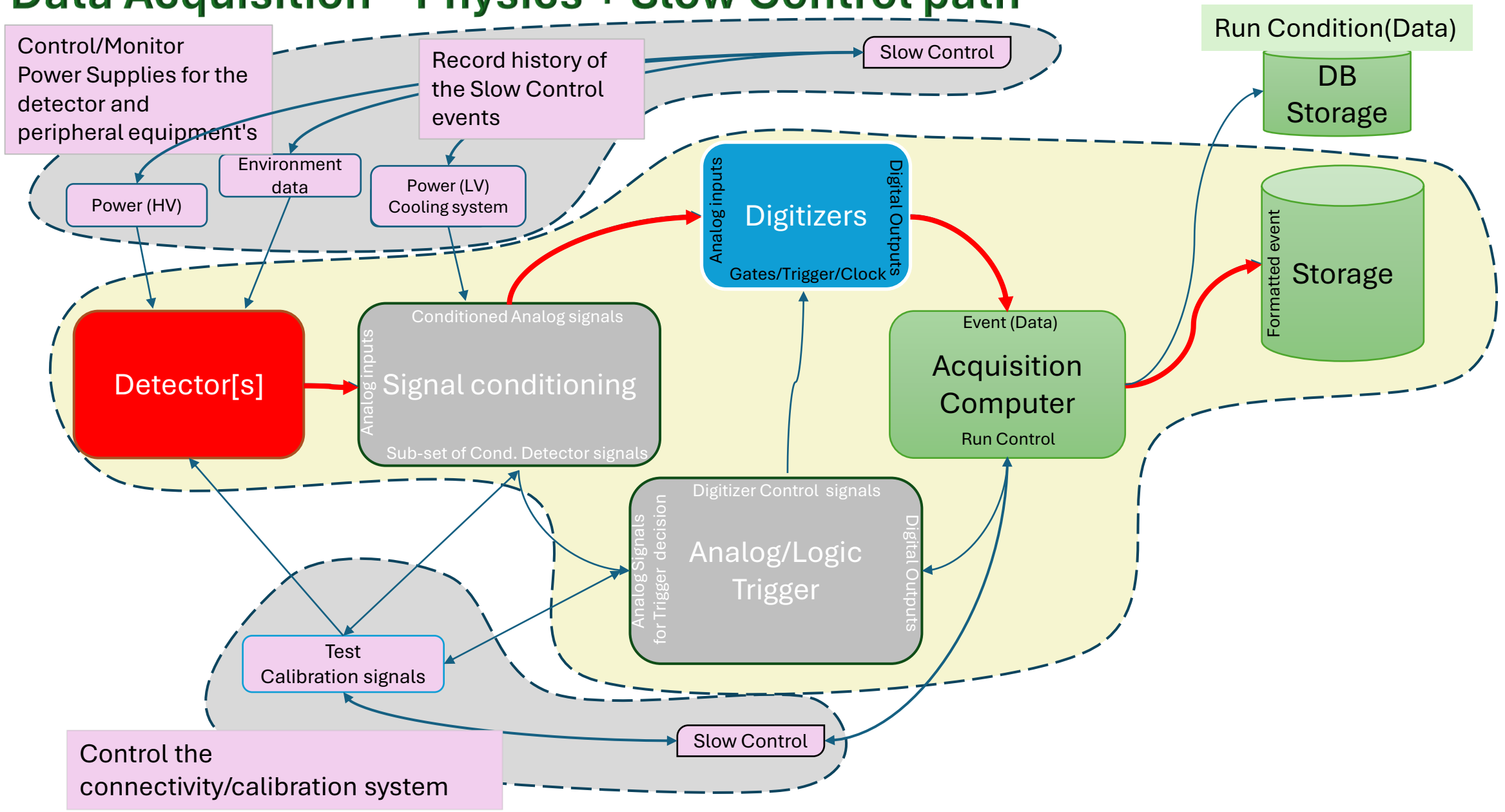
Define the type of “event” that you need to record. “event” is a collection of data tagged to a specific run condition



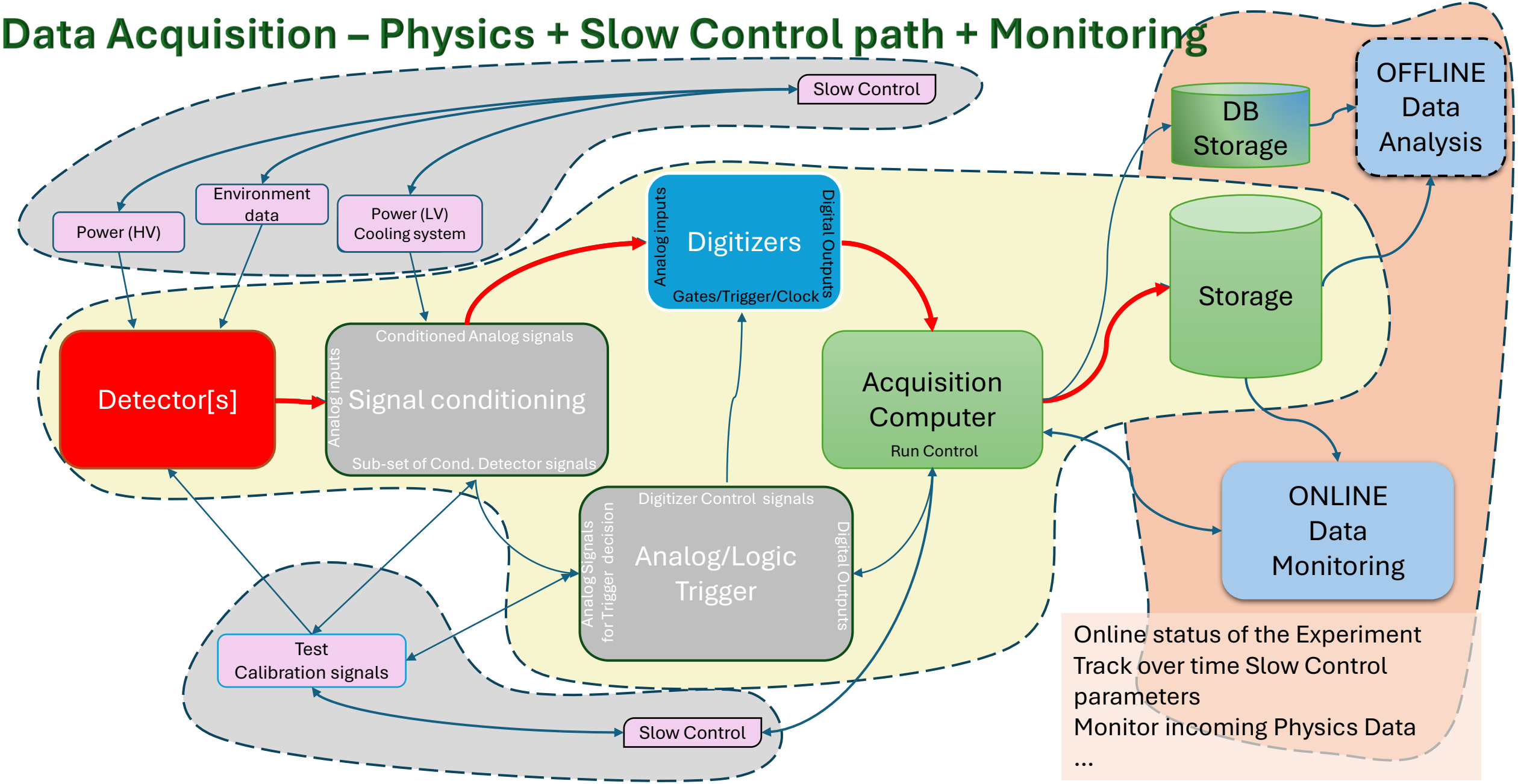
Build the logic circuit out of your incoming signal to produce the necessary Trigger signal

Interface the computer to the trigger generator to control when the data need to be readout

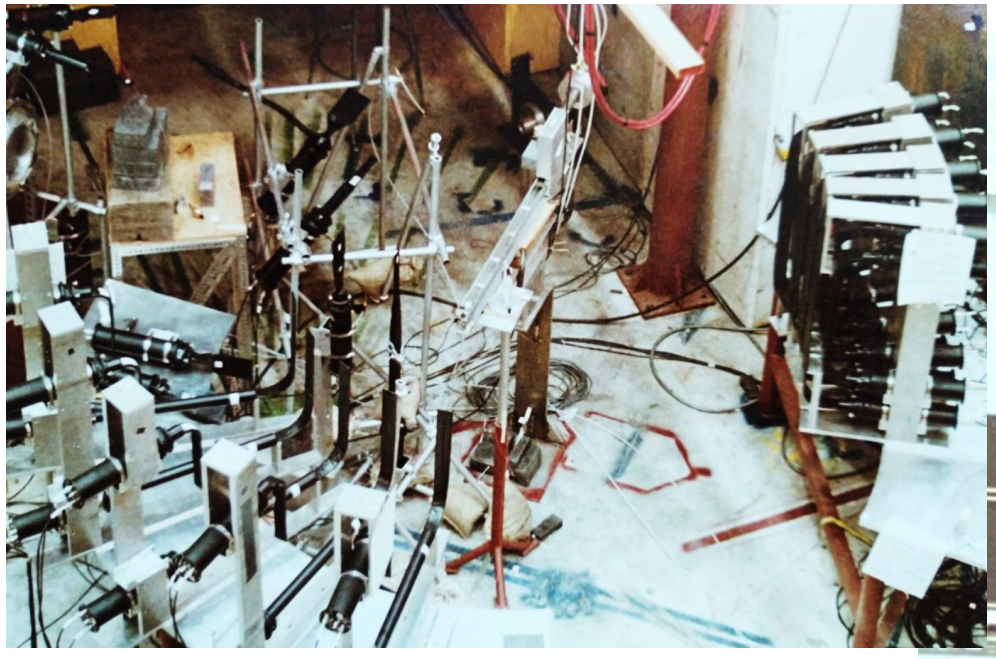
Data Acquisition – Physics + Slow Control path

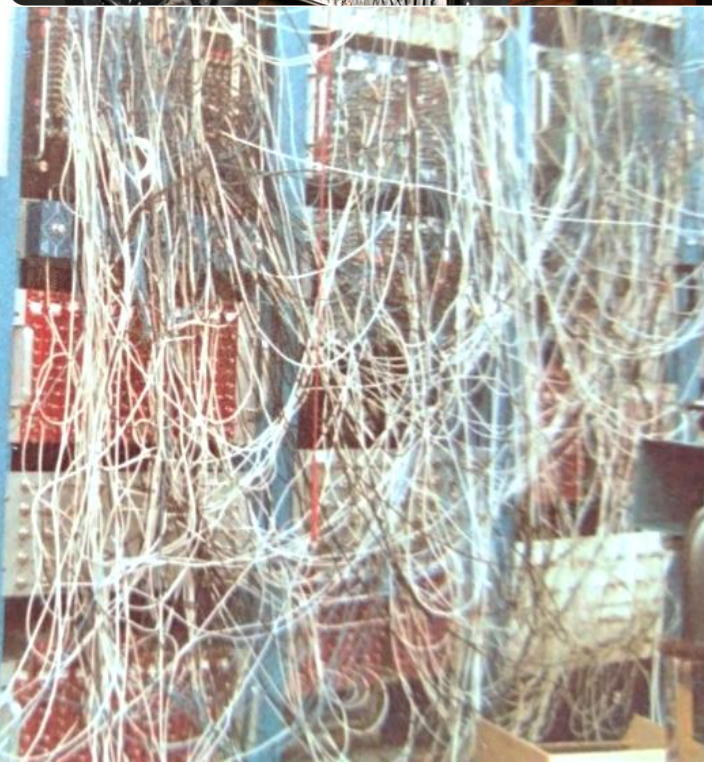


Data Acquisition – Physics + Slow Control path + Monitoring



Experiment - examples - π-scat

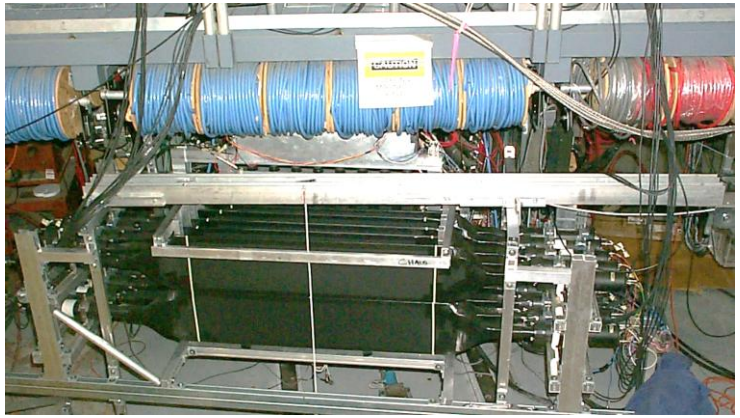


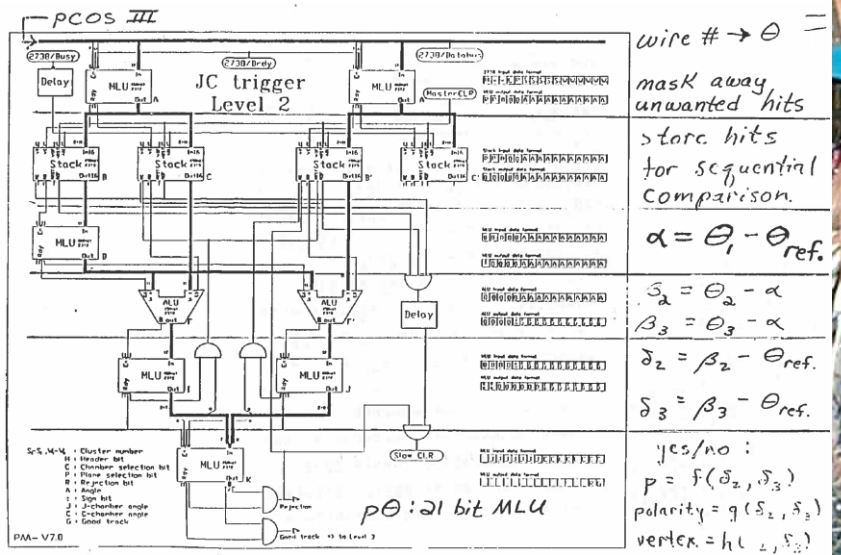


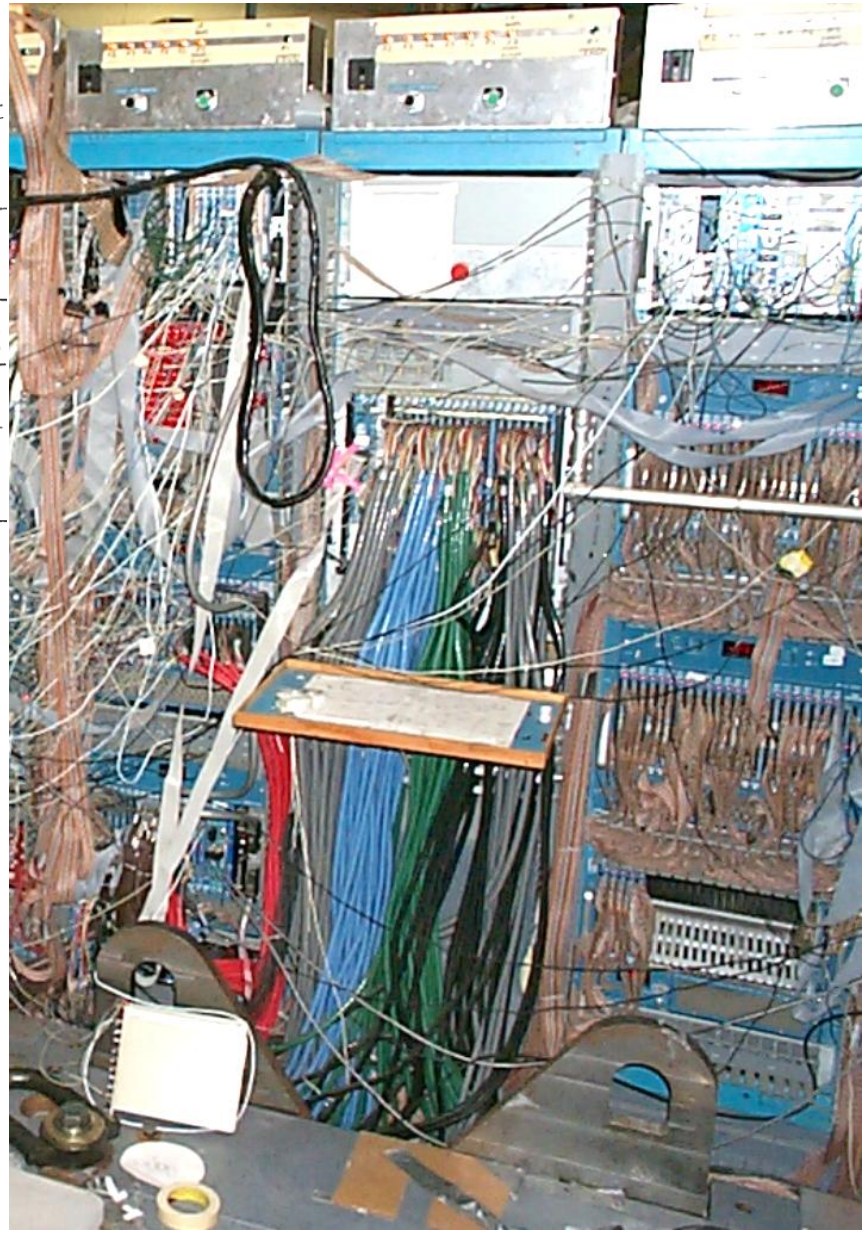
Period: < 1985
Channel Count: <100
DAQ Hardware: NIM, CAMAC [ADCs, TDCs, Scalers]
Computer: Digital PDP 11/34
Rates: 100evt/s
Programming Language: FORTRAN
Storage: Memorex MRX-V ½”x 10-¾”

Experiment - examples - CHAOS

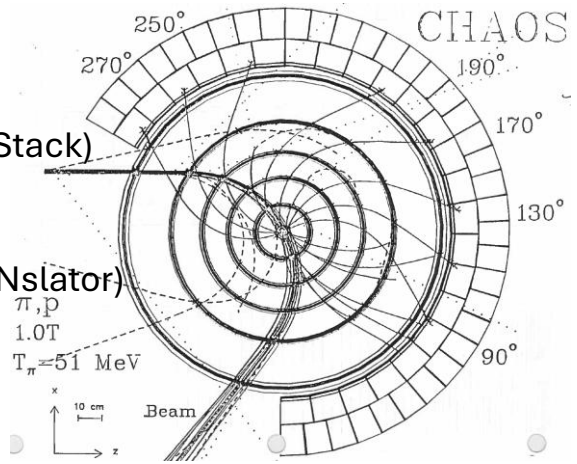
Delay Lines (~20m) for ~2000 channels



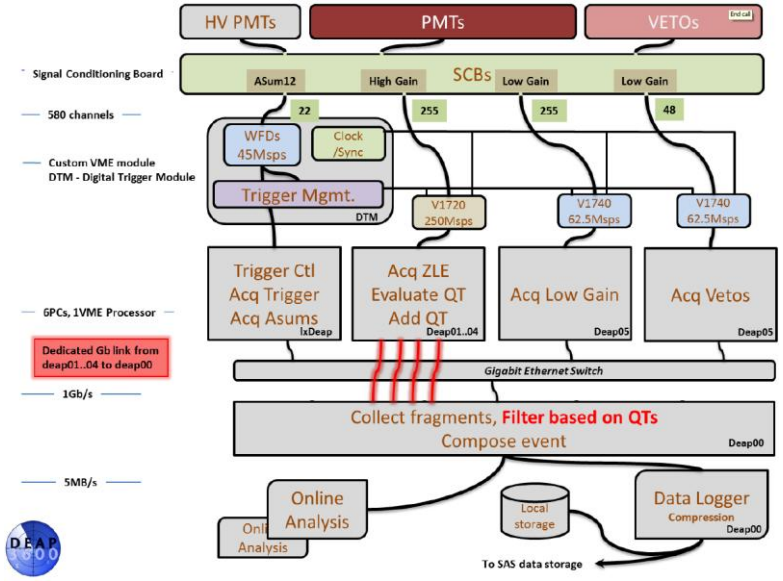


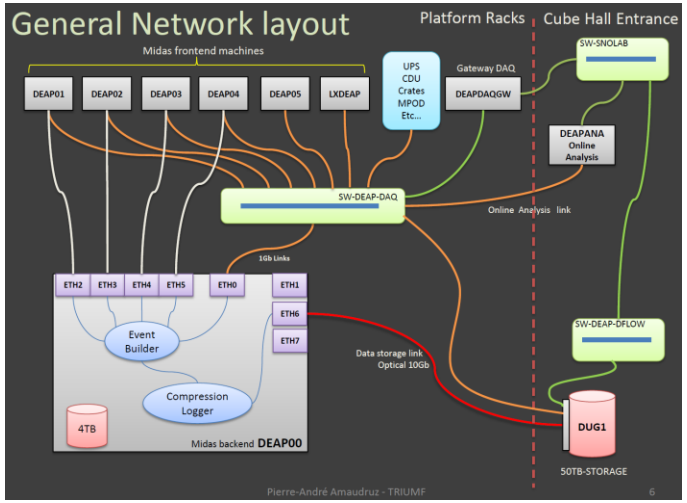


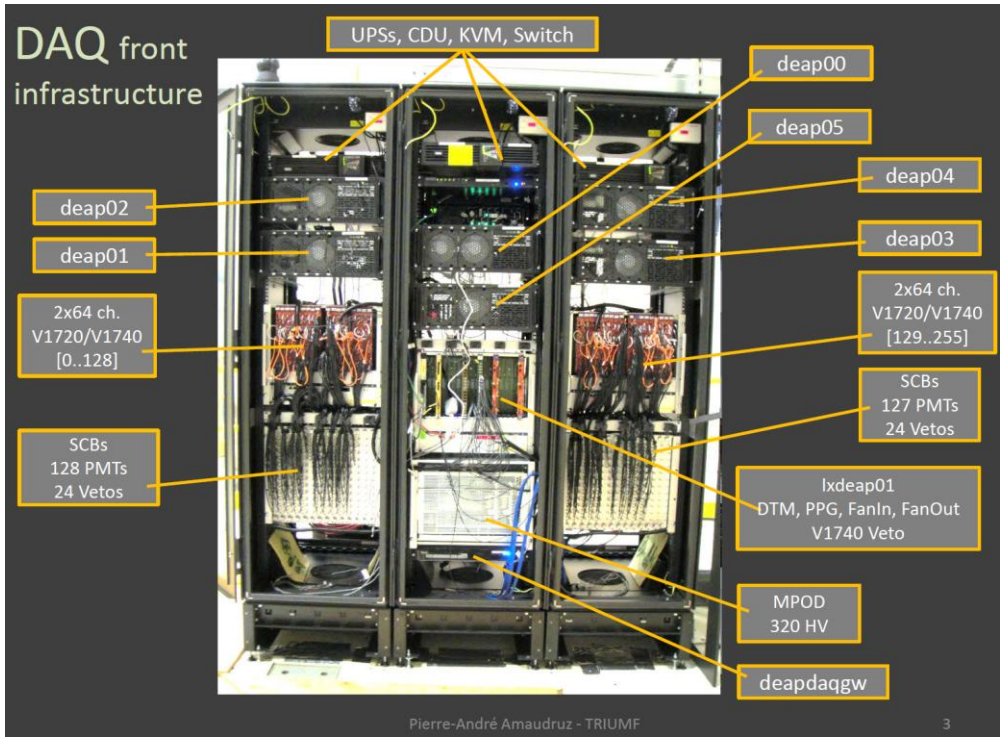
Period: 1990 - 2000
Channel Count: ~2500
DAQ Hardware: NIM, CAMAC, VME, FastBus
L2-Trigger **FPGA Precursor** in ECL-logic (CAMAC: ALU, MLU, Stack)
Computer: Digital µVax-3400
Rates: few hundred events per second
Programming Language: FORTRAN (IBM 1957, FORmula TRANslator)
Storage: Sony QG112M 2.5/5GB 8mm D8 Data Cartridge
DLTape IV 80GB (compressed)



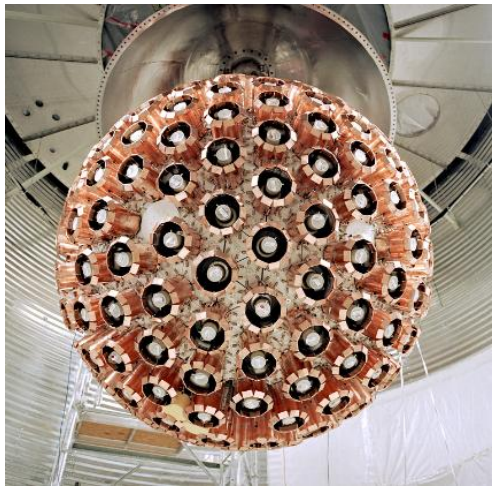
Experiment - examples - DEAP





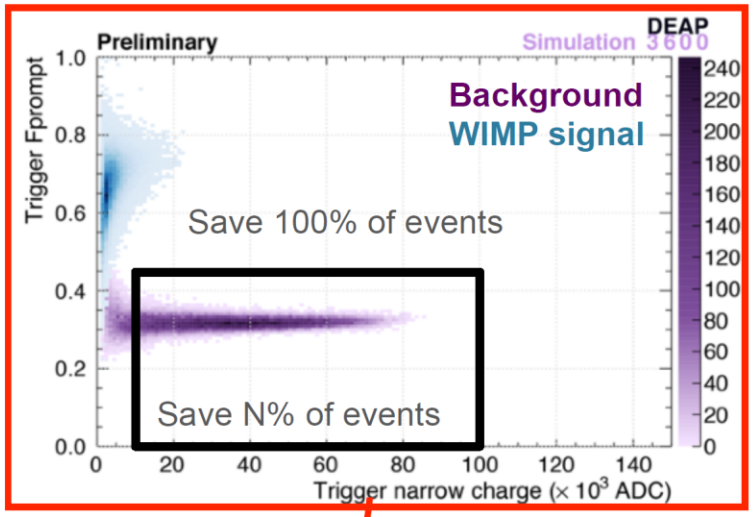


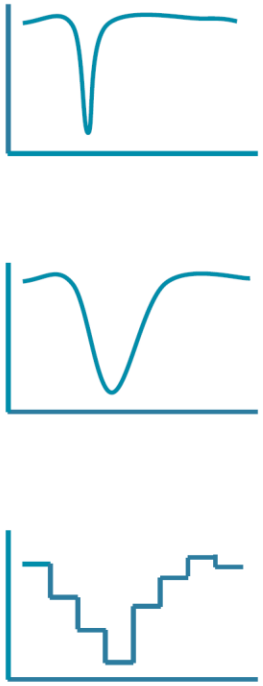
Period: 2010 -
Channel Count: ~600
DAQ Hardware: VME, PCIe Optical interface
L1 Trigger FPGA-based
Computer: PCs
Rates: ~3KEvt/s, ~12MB/s
Programming Language: C, C++, Web tools
Storage: Local HDD, Cloud



Experiment - examples - DEAP

Example 1 - DEAP-3600





255 LAr PMTs

22 signal conditioning boards (slow down the fast PMT pulses)

SUM

Trigger signals

Trigger (DTM)

32 250MHz digitizers

4 62.5MHz digitizers

4 readout PCs

Event builder PC

Custom hardware

Commercial hardware

Custom software/ firmware

Ben Smith

Experiment - examples - DEAP

What features a DAQ system must provide?

- **Run Control**

  Define the data acquisition sequence – Run concept (cycle) –

  Run: Data set collected with a defined experimental condition

- **Record the selected Data to storage device**

  Multiple storage media, event type, etc. (Logger)

- **Hardware configuration**

  Based on pre-selected configuration

- **Online status of the Experiment**

  Real time messages with permanent record (log)

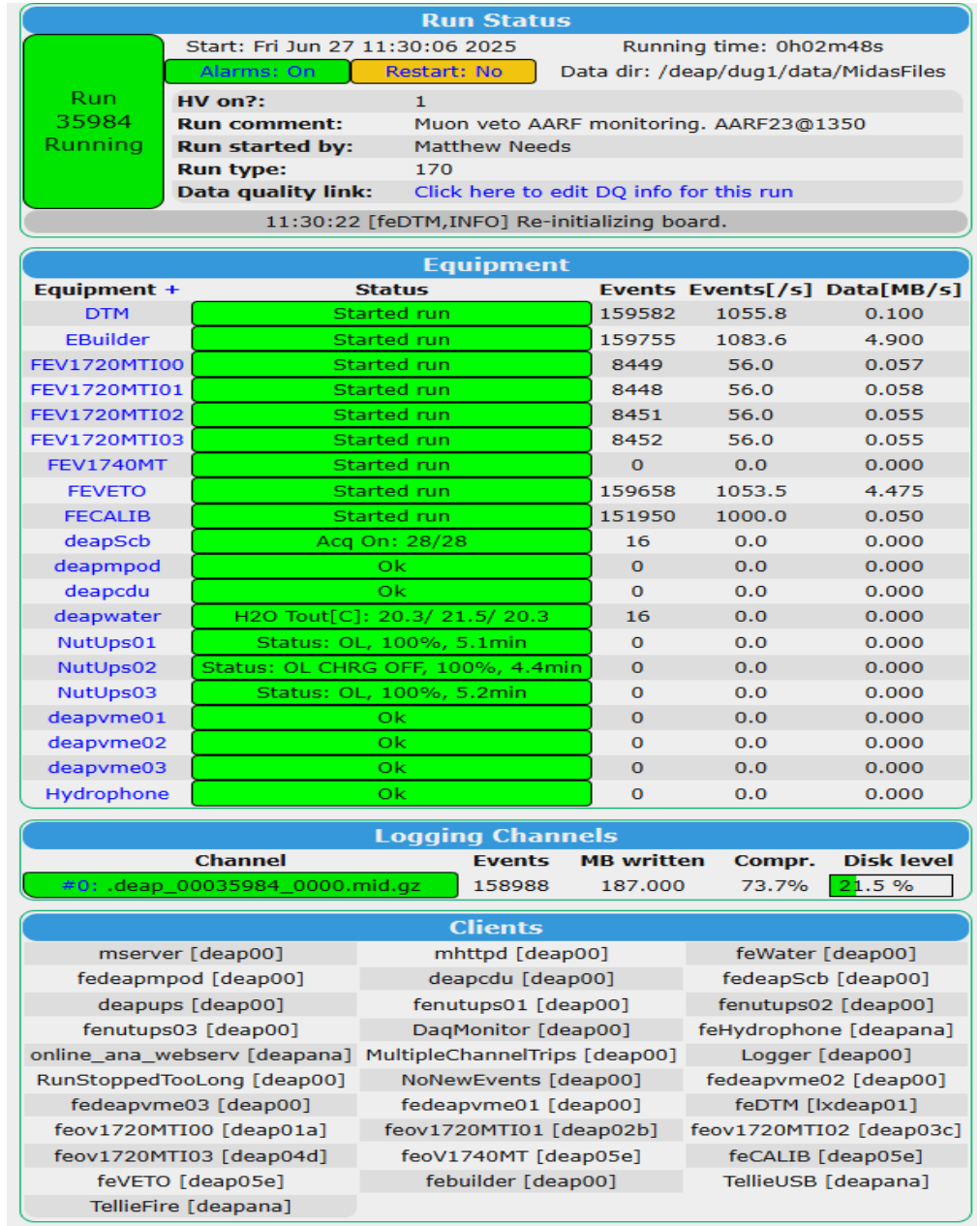
- **Track over time experimental condition parameters**

  Chart plot of any experimental variable (History)

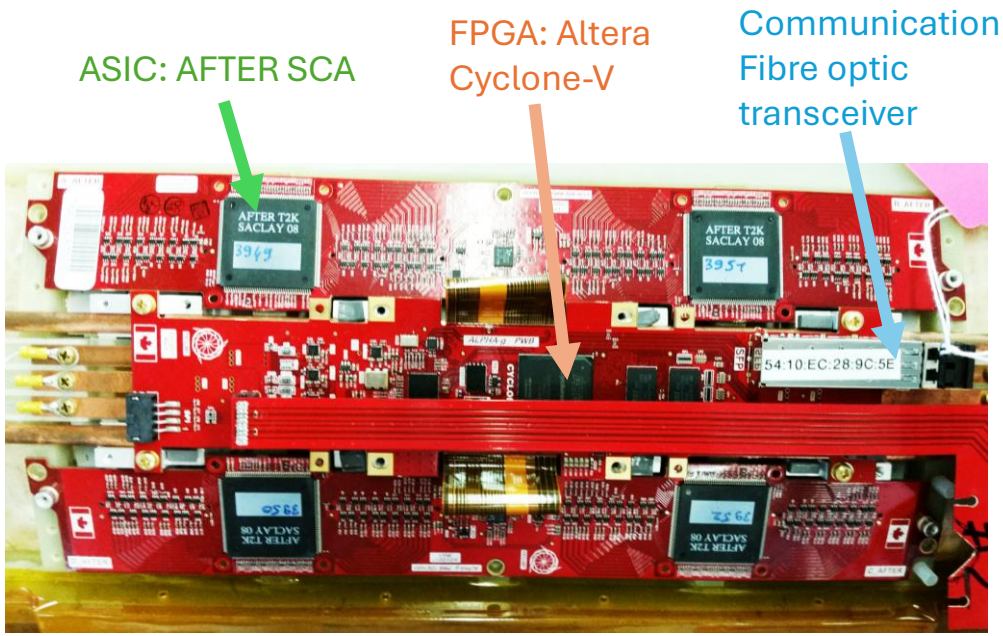
- **Monitor incoming Physics Data**

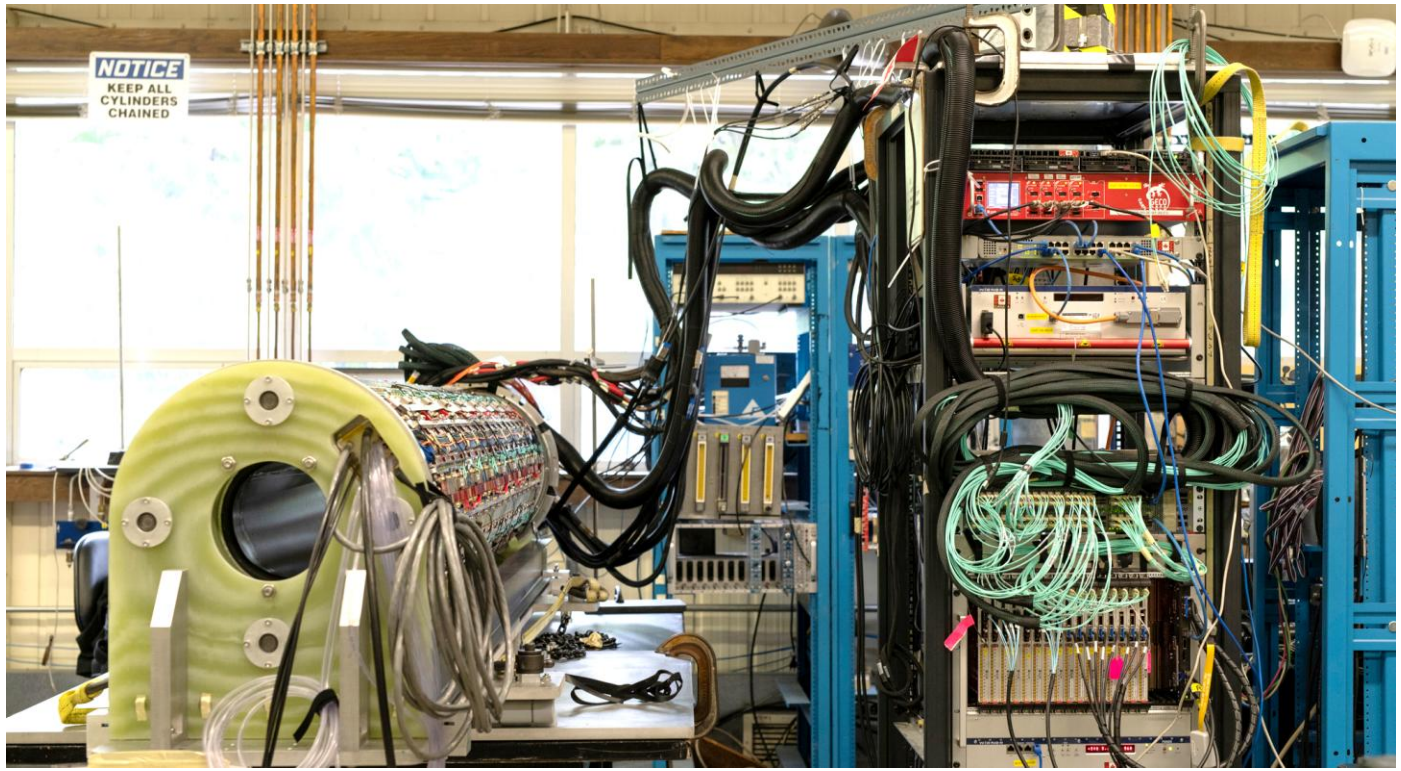
  Online Data Analysis mechanism with data display (Rootana)

- **Custom User Parameters/Data display (Custom Web page, script)**
- **Custom alarm and custom action based on Alarm condition (Alarms)**
- And more…



Experiment - examples - Alpha-g

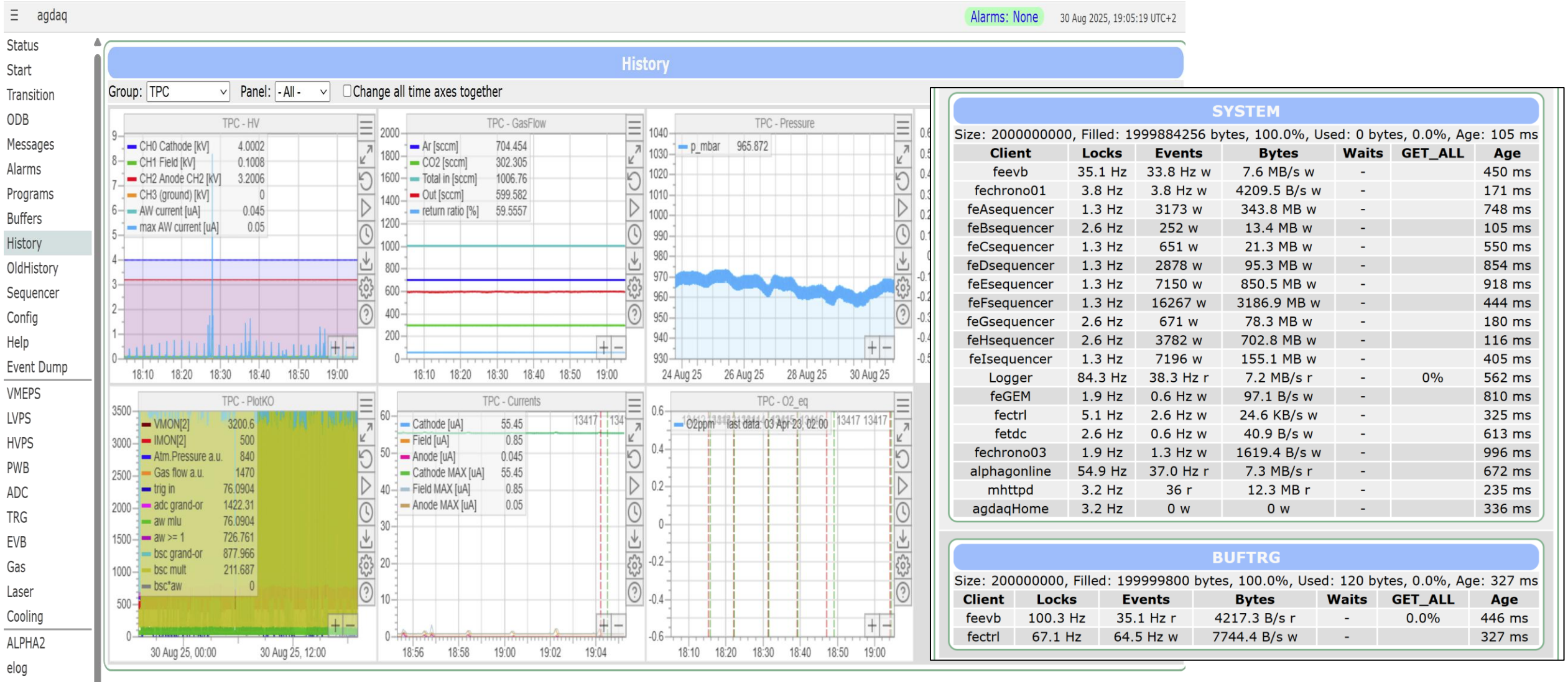




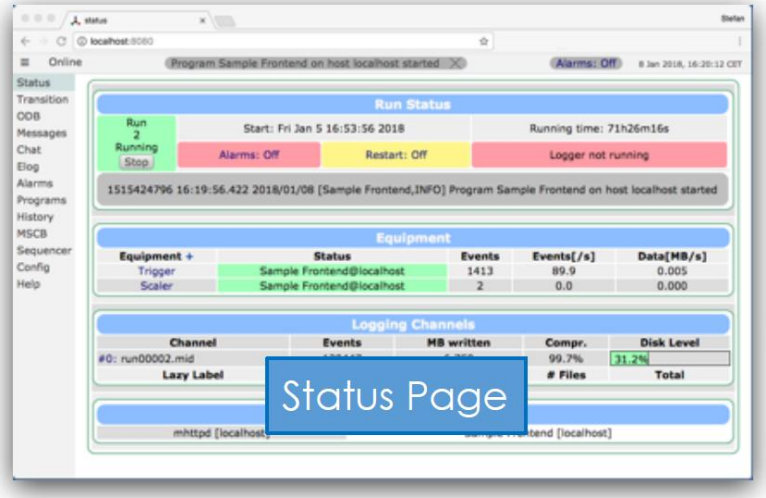
Period: 2016 -
Channel Count: ~19’000! … (18’000 of SCAs)
DAQ Hardware: VME (for power only), Ethernet Optical Links
Custom Build Hardware with FPGAs : WFDs, TDCs, Logic
ASICs, SCA AFTER chip (Saclay France)
Computer: PCs
Rates: ~1KEvt/s, ~200MB/s
Programming Language: C, C++, Web tools
Storage: Local HDD, Cloud

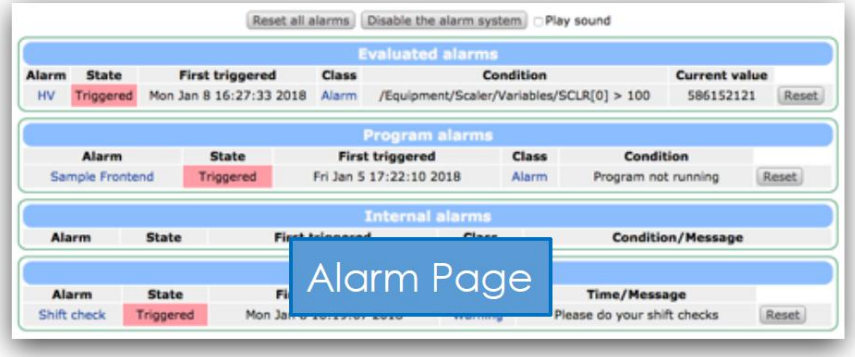
Large portion of the frontend electronics including the waveform digitizers reside on the detector (256 ASICs)

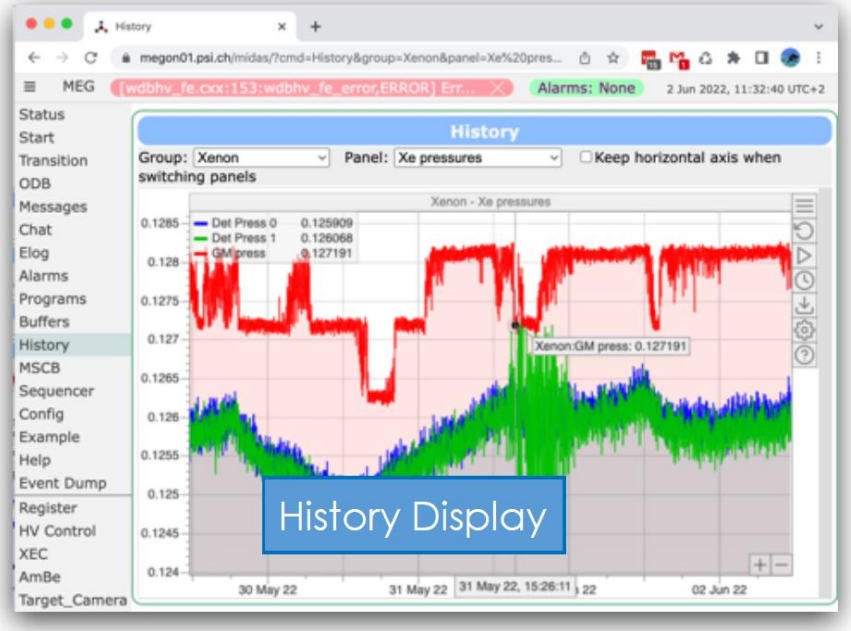
Experiment - examples - Alpha-g

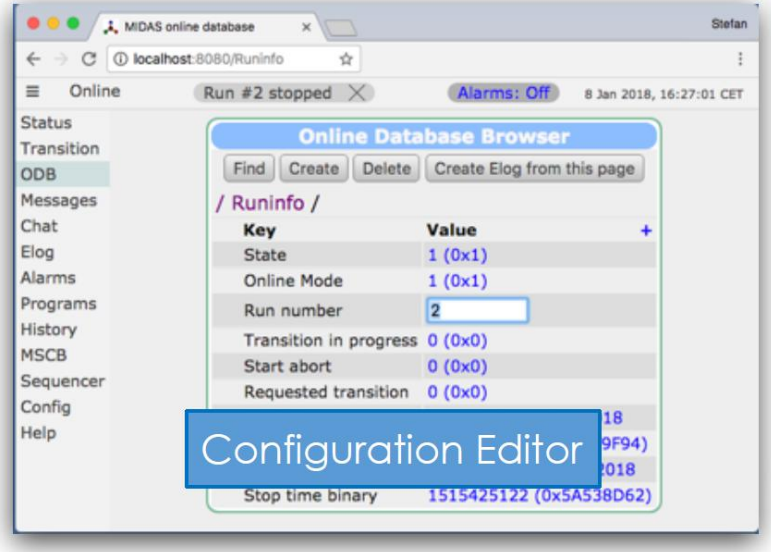


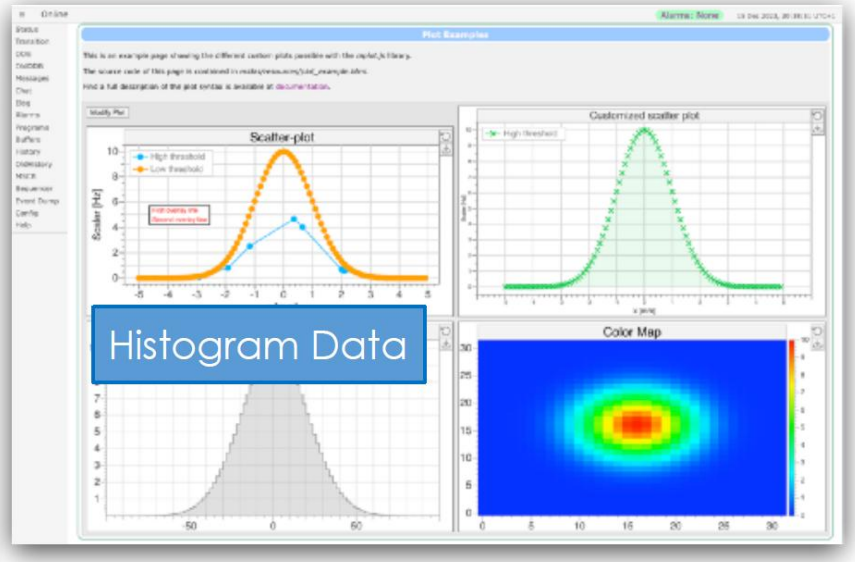
Experiment - examples - MEG

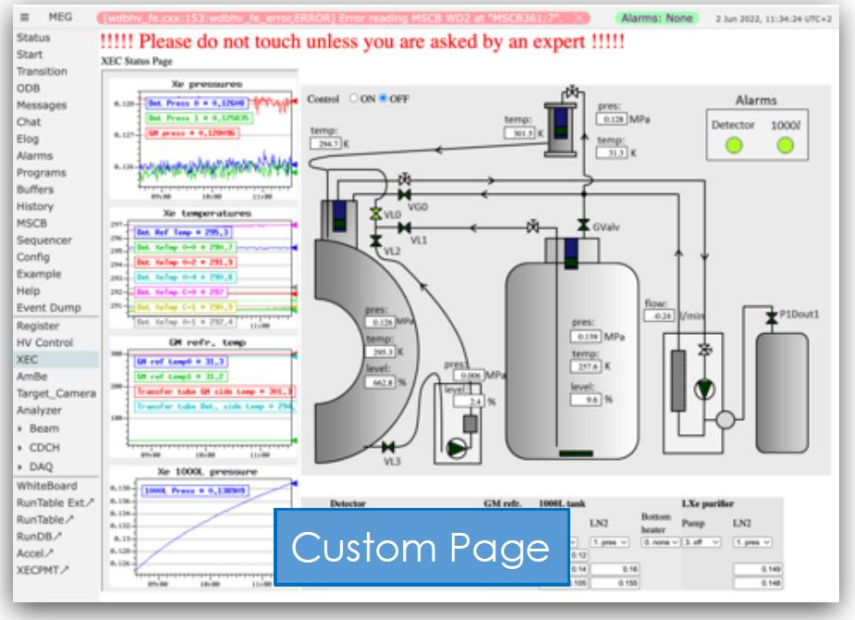






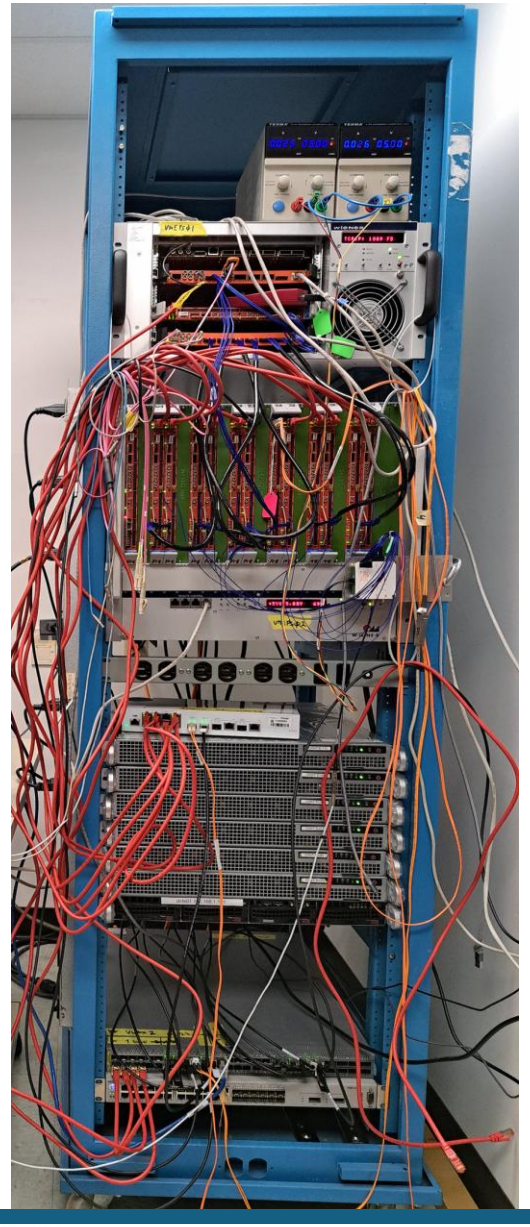


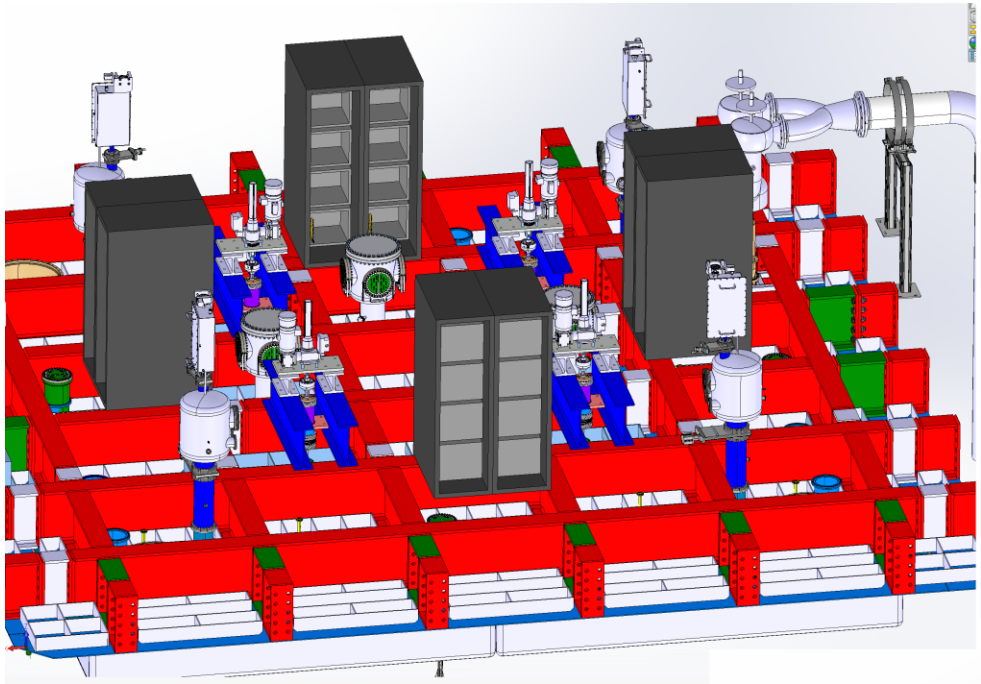


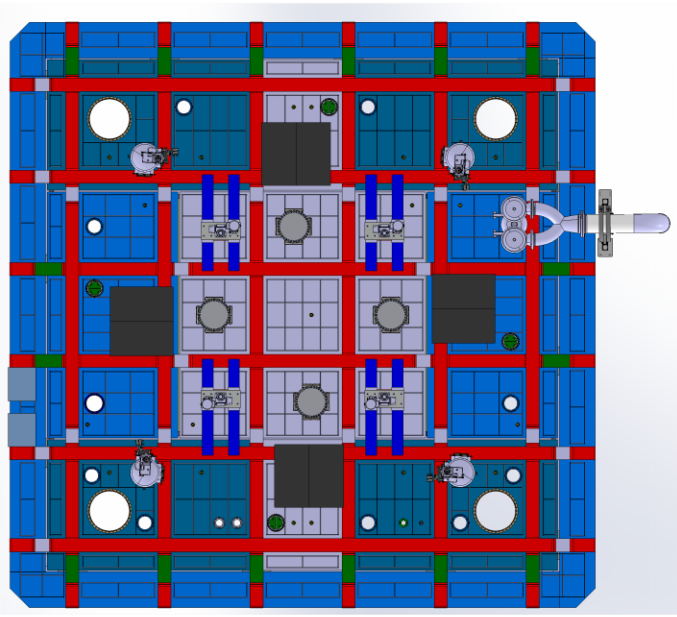


Ben Smith

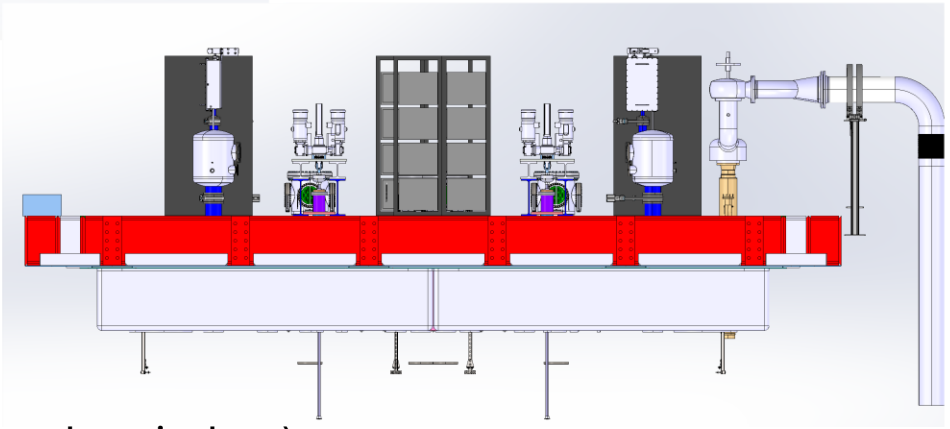
Experiment - examples – DarkSide-20K





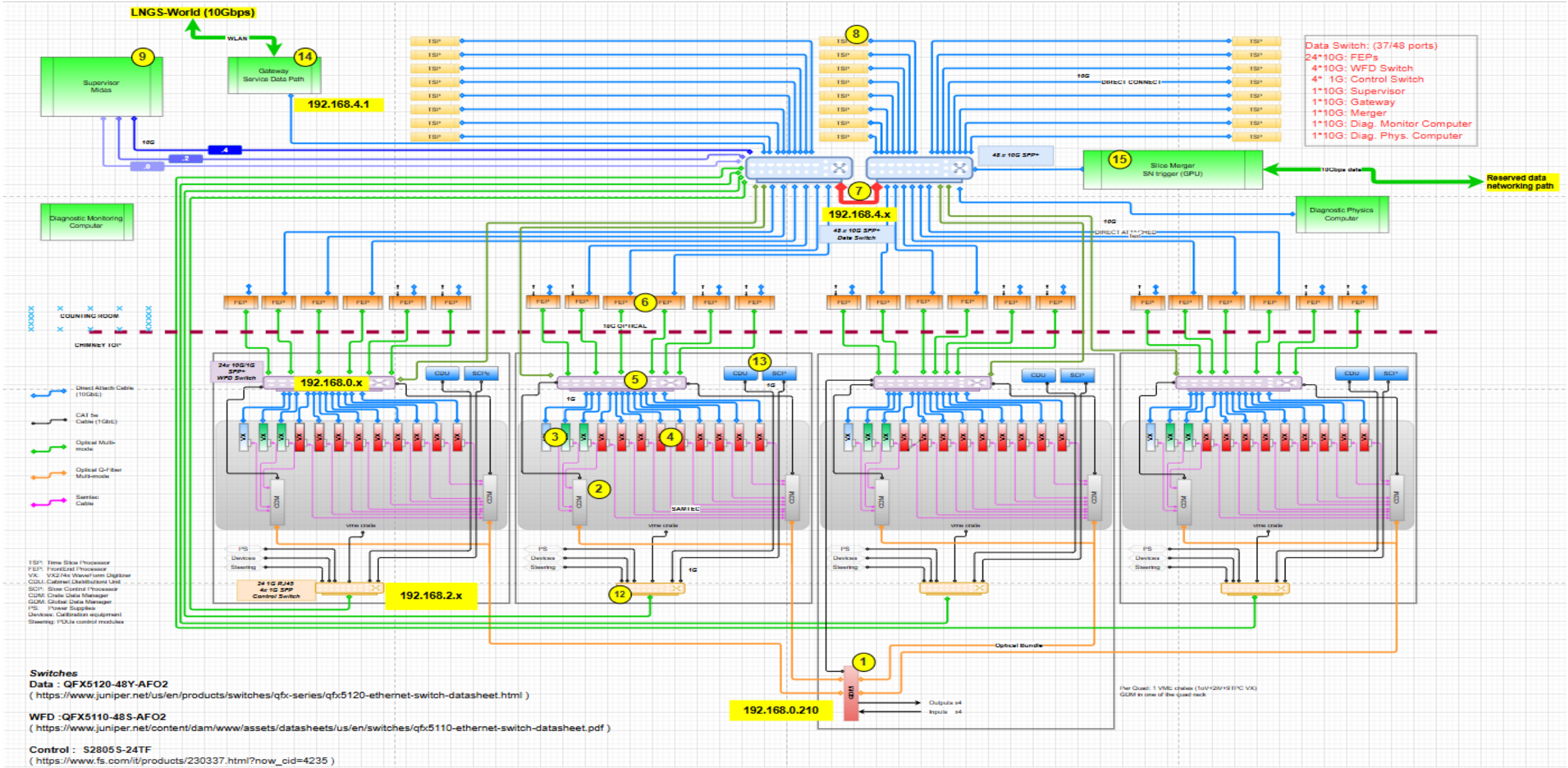


DarkSide-20K
Rooftop with 4 double DAQ racks
#1 DAQ + Network + Slow Control
#2 sensors (PDUs) Power+Control



DarkSide-20K
“Quadrant” DAQ rack (12 WFD, 6 PCs, 3 Network switches)

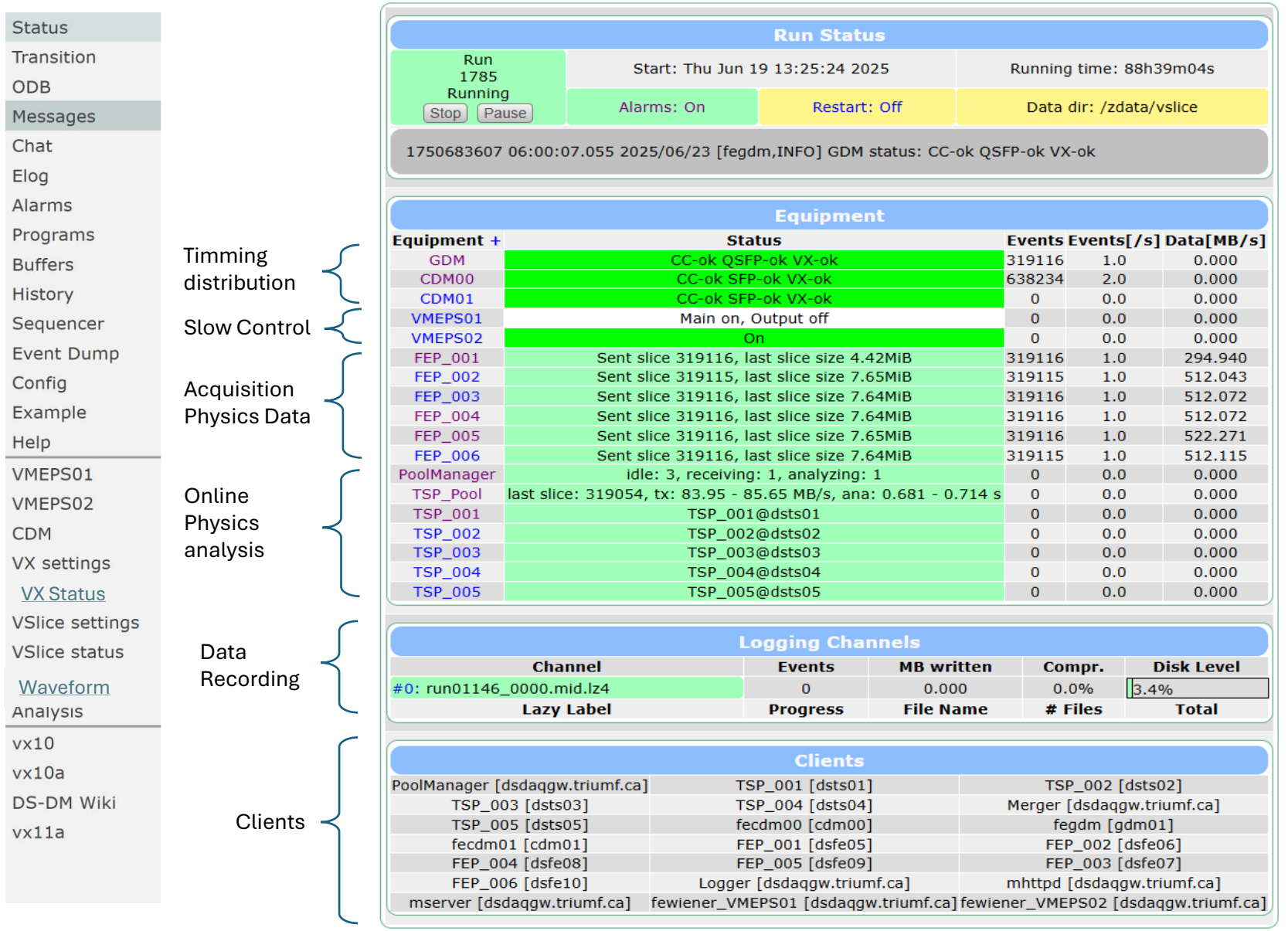
Experiment - examples – DarkSide-20K



Experiment - examples – DarkSide-20K

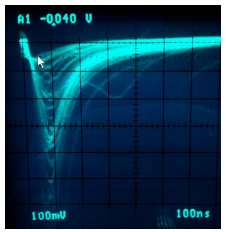
DarkSide-20K Quadrant

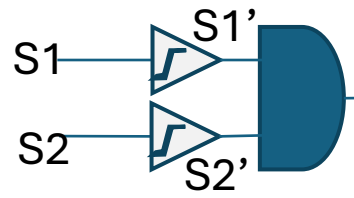
Run Status & Control

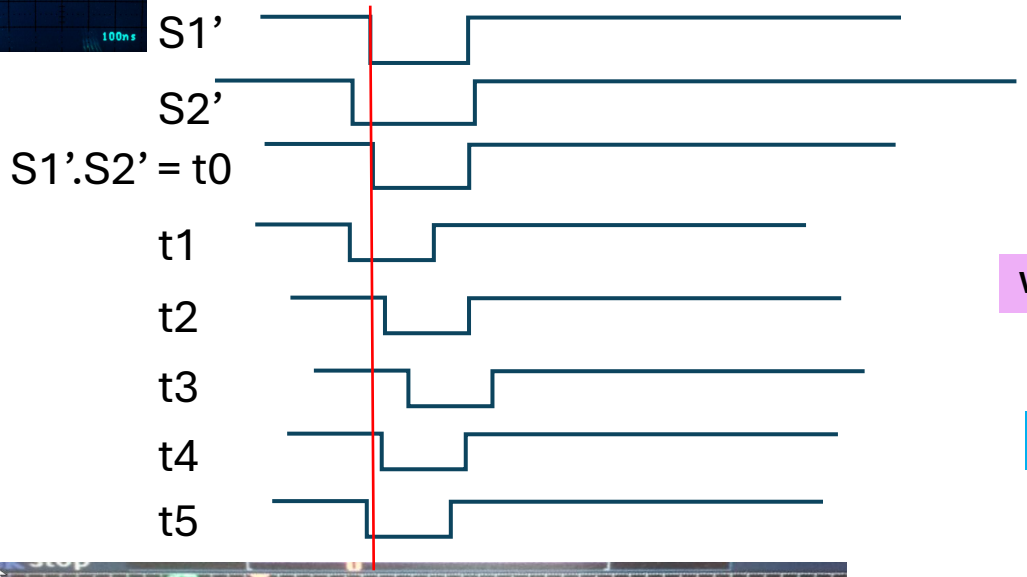


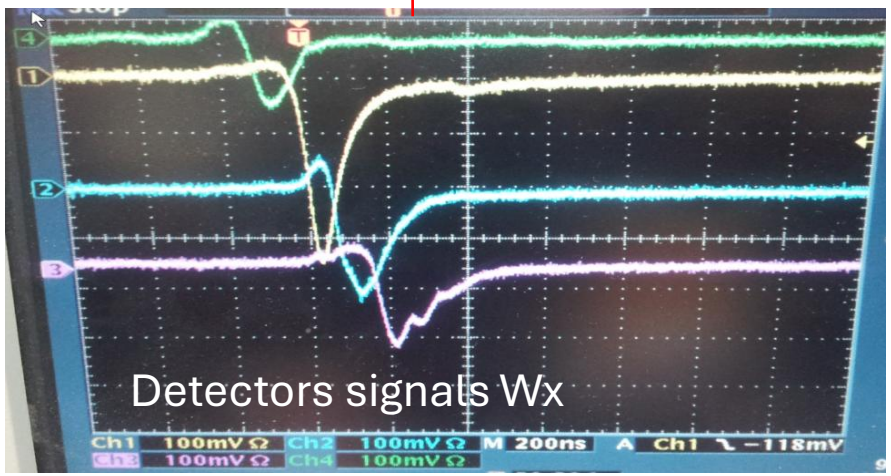
There are other DAQ software packages?

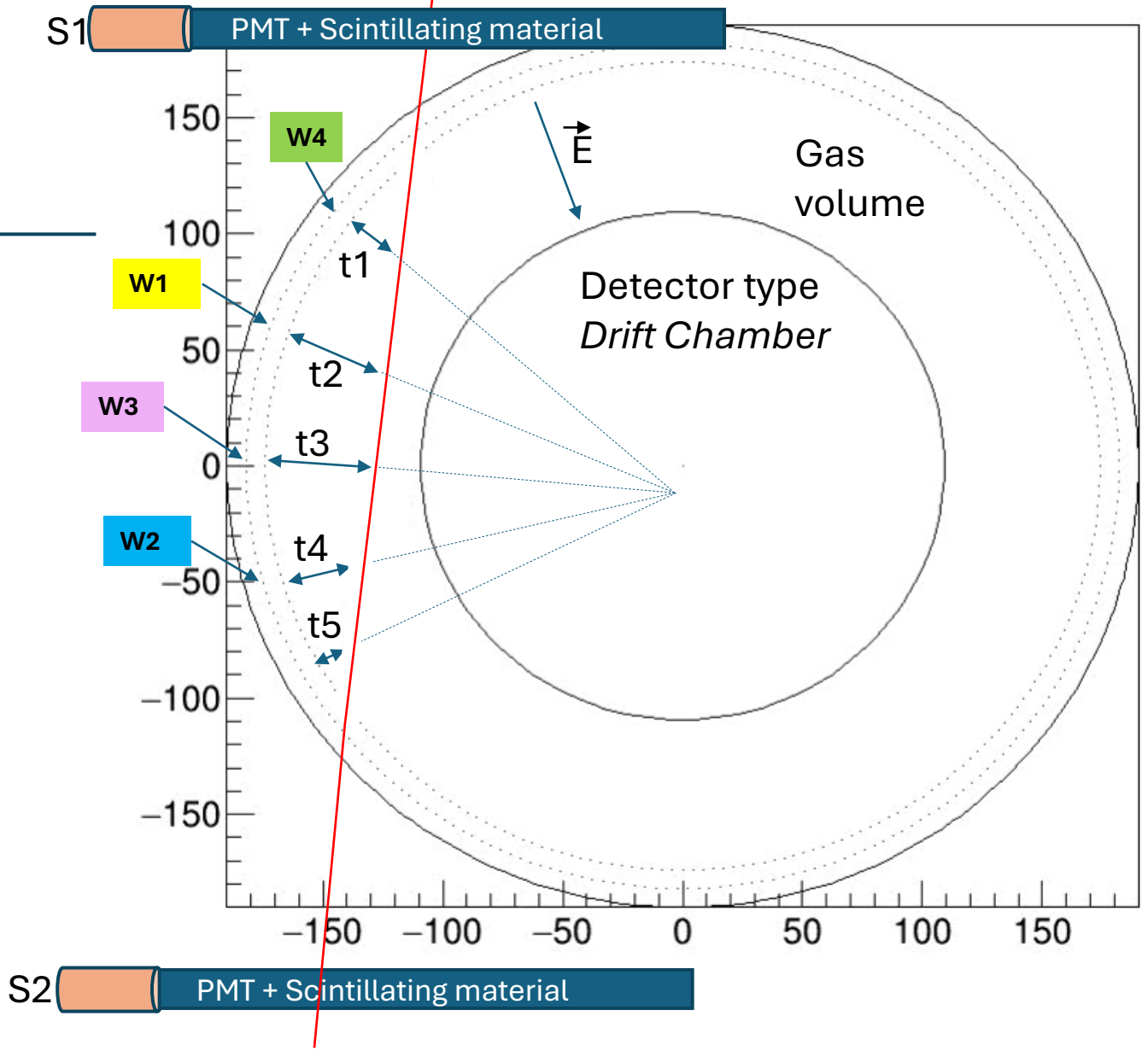
- Most of the Physics Labs have their own DAQ system and experts.
- **Labview**: works well for many small setups
  - Labview drivers provided for many commercial devices.
  - Getting generic device drivers for linux can be tricky.
- **ORCA**: developed by group at University of North Carolina
  - Runs on MacOS
  - Experiments: KATRIN, MAJORANA, SNO+
- **Artdaq**: developed by FNAL
  - Based on art offline analysis framework (originally from CMS)
  - Experiments: LARiAT, Darkside-50, Mu2E
- **Midas-UK**: **M**ulti **I**nstance **D**ata **A**cquisition **S**ystem (Rutherford - STFC)
- **CODA** : Jefferson Laboratory (formerly **C**EBAF **O**nline **D**ata **A**cquisition)
- And many more…

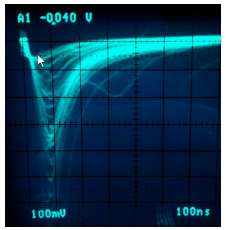


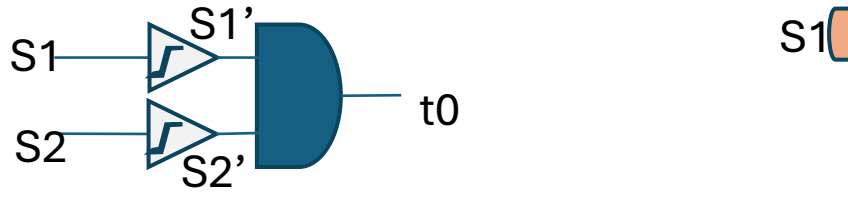

S1
S2
S1'
S2'
t0

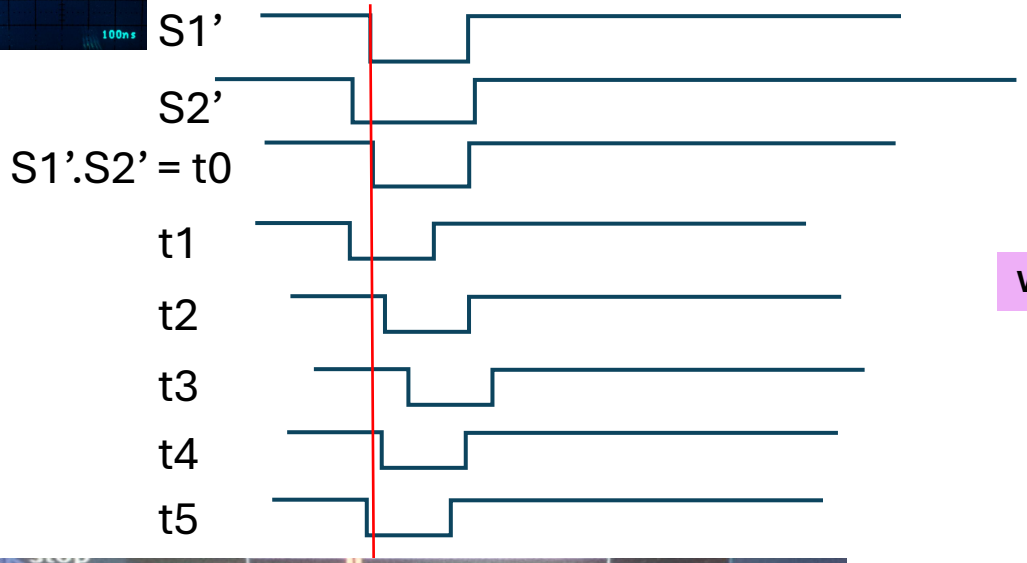

S1'
S2'
S1'.S2' = t0
t1
t2
t3
t4
t5

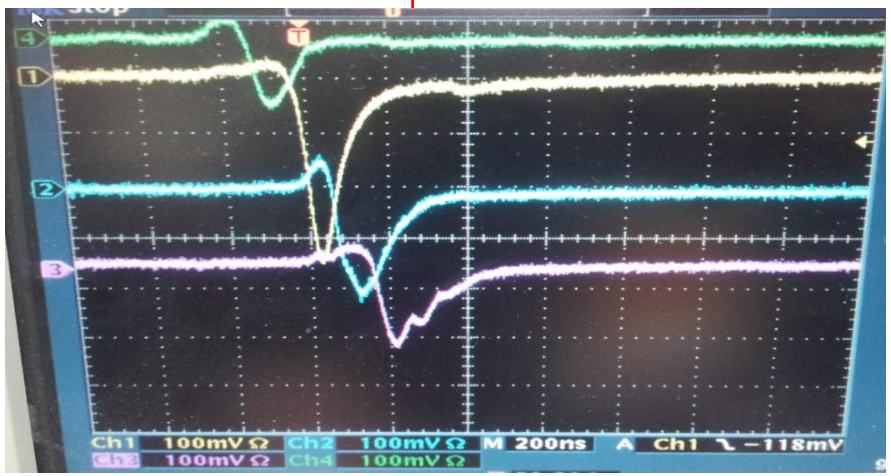

Detectors signals Wx
Ch1 100mV Ω Ch2 100mV Ω M 200ns A Ch1 ∿ -118mV
Ch3 100mV Ω Ch4 100mV Ω

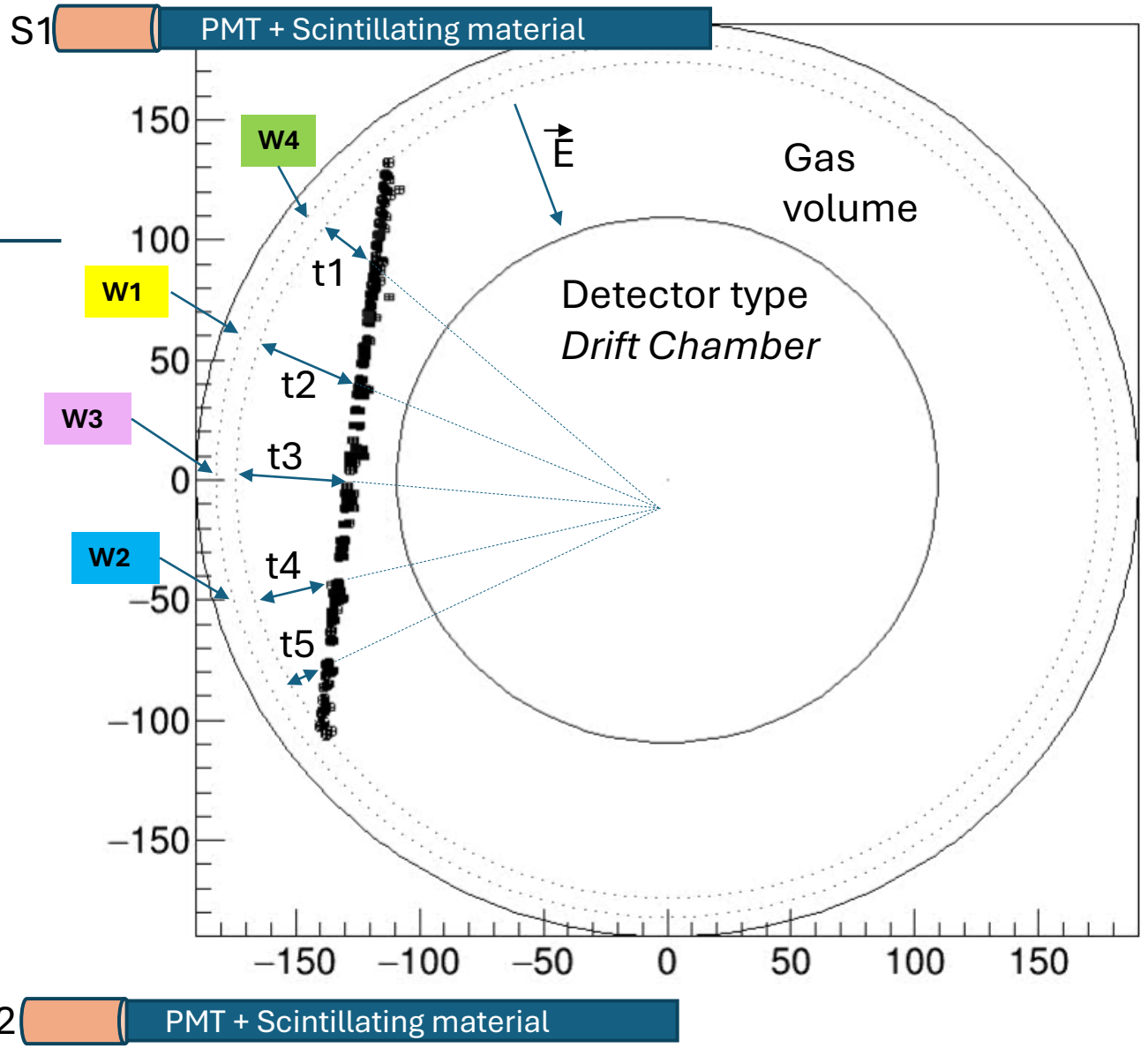

S1
PMT + Scintillating material
W4
W1
W3
W2
E
Gas volume
Detector type
Drift Chamber
t1
t2
t3
t4
t5
150
100
50
0
−50
−100
−150
−150 −100 −50 0 50 100 150
S2
PMT + Scintillating material



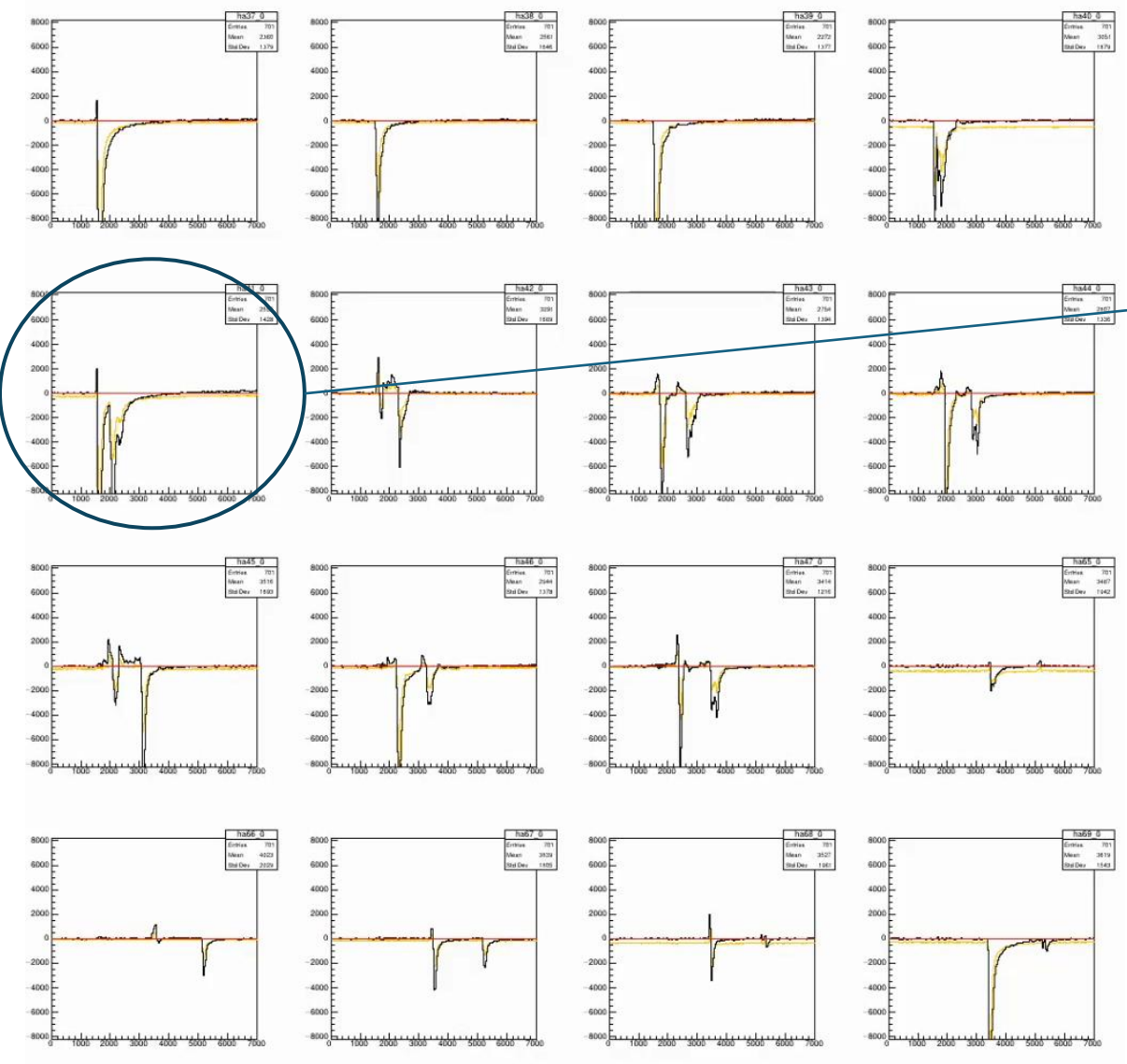

S1
S1'
S2
S2'
t0


S1'
S2'
S1'.S2' = t0
t1
t2
t3
t4
t5


Ch1 100mV Ω
Ch2 100mV Ω
M 200ns
A Ch1 ∿ −118mV
Ch3 100mV Ω
Ch4 100mV Ω

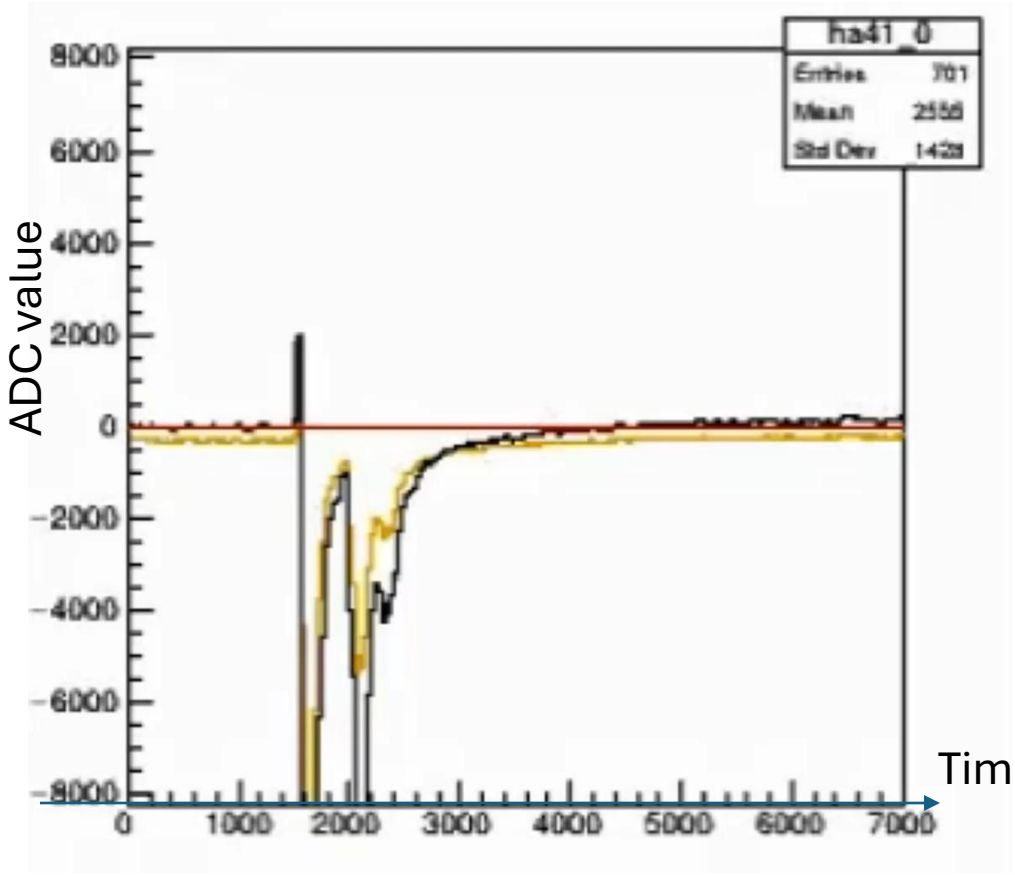

S1
PMT + Scintillating material
W4
W1
W3
W2
t1
t2
t3
t4
t5
E
Gas volume
Detector type
Drift Chamber
150
100
50
0
−50
−100
−150
−150
−100
−50
0
50
100
150
S2
PMT + Scintillating material

Data Analysis - Deconvolution



- Match single avalanche response to signal
- Subtract induction responses from neighbors

Yellow : Original signal
Red : Signal evolution during the deconvolution
Black : Residual signal



References...

Gas Detector Effects: Electric field, Diffusion, Lorentz effect
Detectors types: MWPC, TGC, RPC, DCs, Gas, µMega, GEM, Silicon detectors

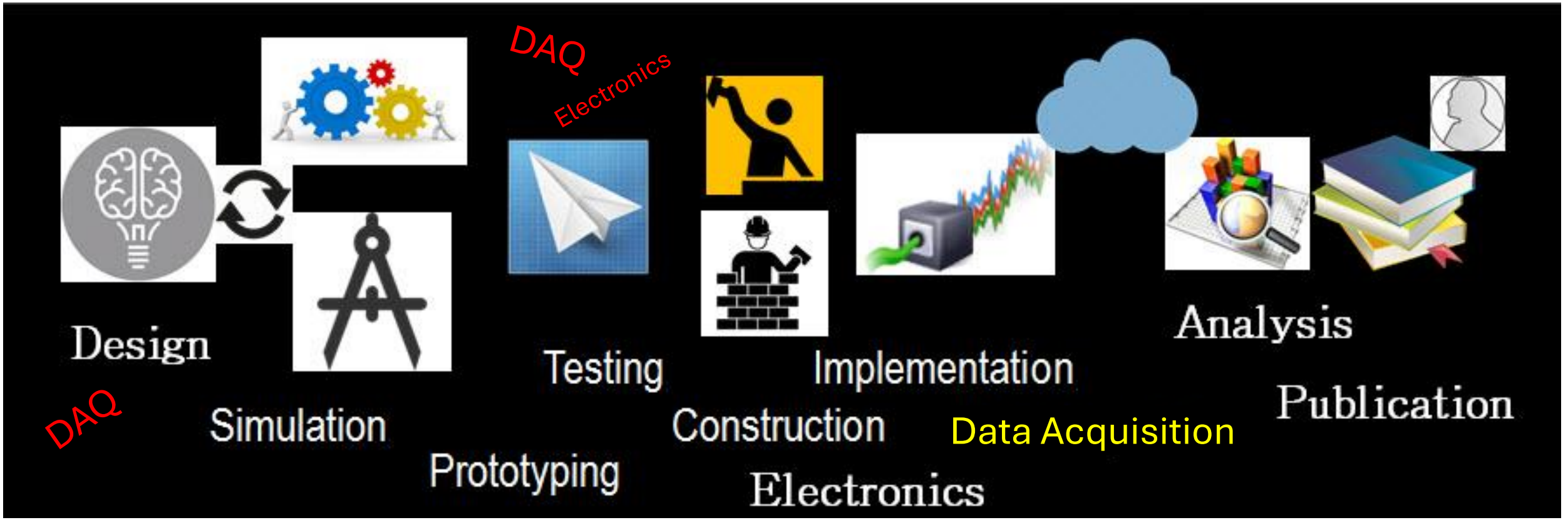
Fabio Sauli (CERN)
Gaseous Radiation Detectors Fundamental and Applications (2014)

Y. Assran, Archana Sharma
Transport Properties of operational gas mixtures used at LHC

Archana Sharma
Sciencedirect_articles_22Oct2015_04-43-06.230 (collection of NIM-A papers)
...

https://www.analog.com/en/analog-dialogue/articles/understanding-and-eliminating-1-f-noise.html
https://www.electronics-tutorial.net/analog-integrated-circuits/data-converters/dual-slope-type-adc/
https://www.electronicdesign.com/adc/what-s-difference-between-sar-and-delta-sigma-adcs
https://www.analog.com/en/design-center/interactive-design-tools/sigma-delta-adc-tutorial.html
Pipelined ADC: https://www.maximintegrated.com/en/app-notes/index.mvp/id/1023

Data Acquisition



Additional DAQ information

- MIDAS DAQ package
- DAQ Midas Workshop 2025 22–23 Sept 2025
- ISOTDAQ School, CERN

- ***IEEE***: Institute of Electrical and Electronics Engineers
  - NPSS: **Nuclear & Plasma Sciences Society**

    IEEE NPSS International Schools
    - CANPS: Computer Applications in Nuclear and Plasma Sciences

      25th Real Time conference 2026, Elba Italy 25–29 May 2026

CANPS Real Time Conferences

IEEE NPSS NUCLEAR & PLASMA SCIENCES SOCIETY

IEEE

NPSS is …

Nuclear & Plasma Sciences Society

- The Technical Society that covers
  - Fusion
  - Nuclear Medical and Imaging Sciences
  - Particle Accelerator Science and Technology
  - Pulsed Power Systems
  - Radiation Effects
  - Radiation Instrumentation
  - Plasma Sciences and Applications
  - Standard for Nuclear Instruments and Detectors
  - **Computer Applications in Nuclear and Plasma Science**

IEEE NPSS NUCLEAR & PLASMA SCIENCES SOCIETY

IEEE

Have fun during the hands-on lab projects!

Enough for today!

END

IEEE is …

Institute of Electrical and Electronics Engineers

- The largest technical/scientific professional organization
- The most prolific technical publisher
- International with activities in all regions of the world
- Organizes the greatest number of technical meetings and has the highest aggregate attendance
- The professional organization with the broadest technical scope with 38 Technical Societies

IEEE NPSS NUCLEAR & PLASMA SCIENCES SOCIETY

IEEE

NPSS is …

- Organizes and supports many symposia, conferences and workshops each year
- Publishes 4 Transactions (peer reviewed journals)
- Publishes Newsletter to all members
- Presents awards each year to recognize major contributions to the field
- Provides access to publications on-line (IEEE Xplore)
- Members save on conference registration
- Members keep in touch via the Newsletter
- Supports the growth of the profession
- Members can get involved with NPSS and help direct and further promote our profession
- Excellent network!

IEEE NPSS NUCLEAR & PLASMA SCIENCES SOCIETY

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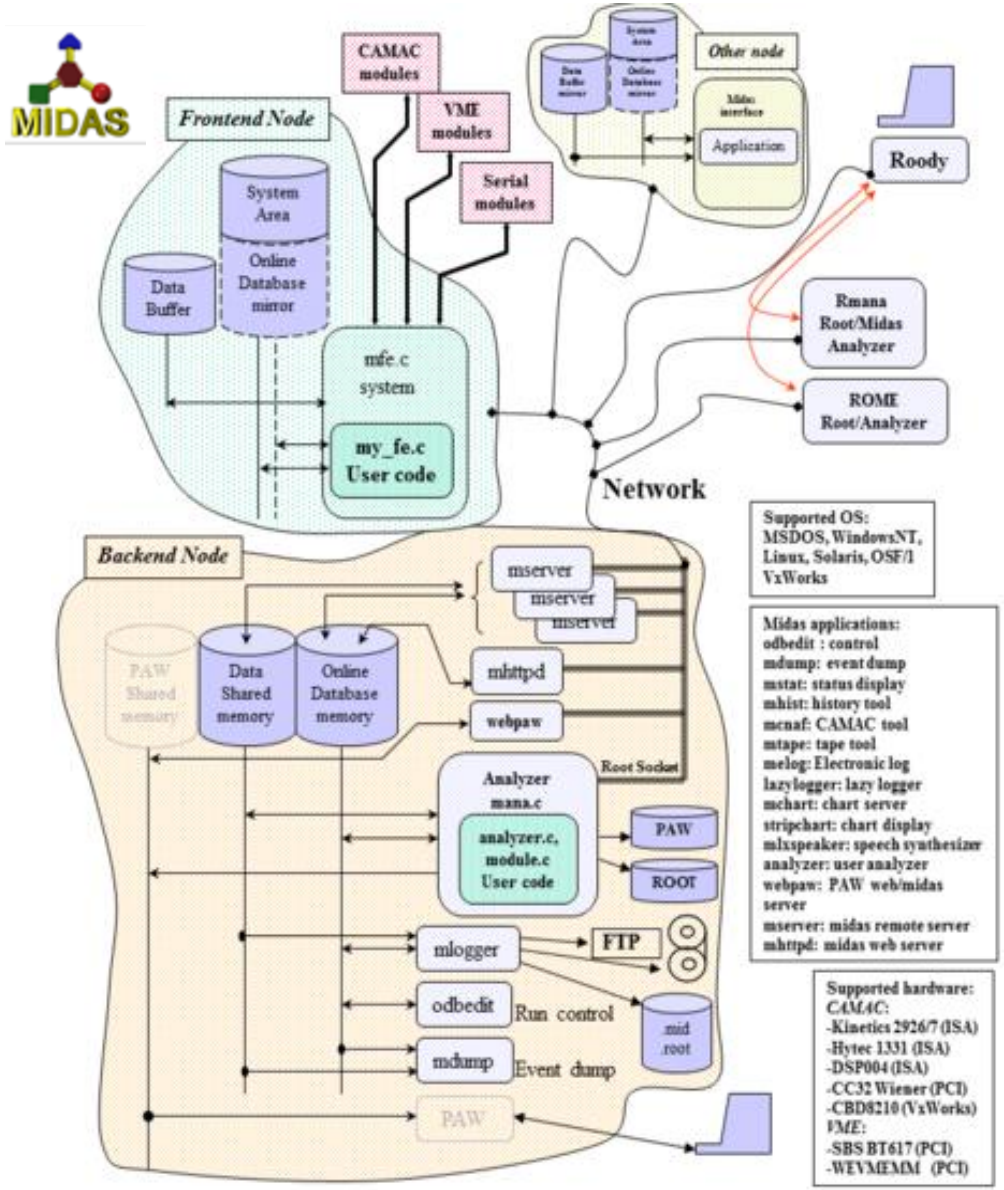
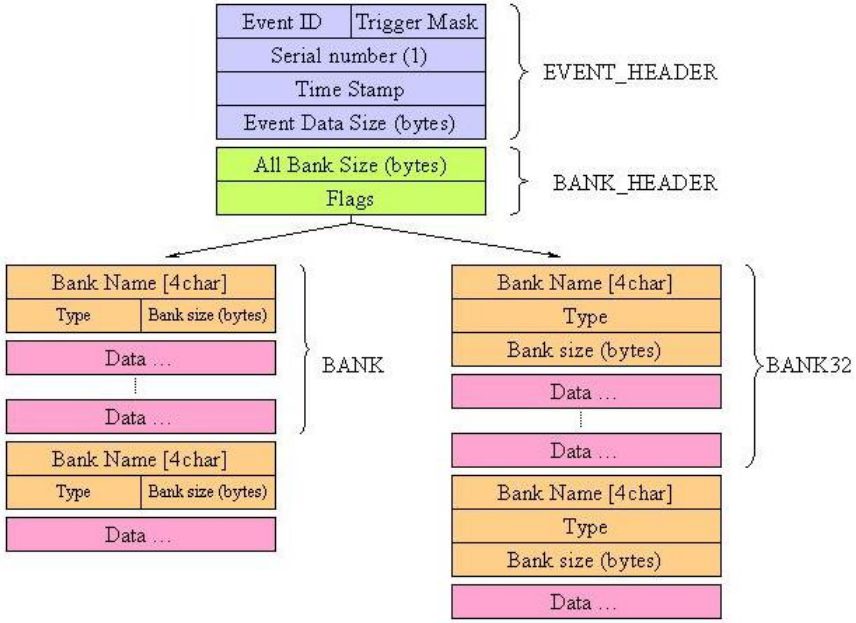
Data Acquisition – Software Architecture



Midas Data Structure

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#banks:4 - Bank list:-W200W201W202W203-

Bank:W200 Length: 128080(I*1)/32020(I*4)/32020(Type) Type:Unsigned Integer*4
   1-> 0xa0007d14 0x000002ff 0xff00987c 0x1bc43d3d 0x3aa707d1 0x3aa33aa6 0x3aa63aa4 0x3aa53aa7
   9-> 0x3aa73aa9 0x3aa63aab 0x3aac3aa2 0x3aa63aa7 0x3aa73aa2 0x3aa43aa4 0x3aa73aa9 0x3aa93aa7
  17-> 0x3aa63aa1 0x3aab3aa5 0x3aa33aa4 0x3aa83aa5 0x3aab3aa7 0x3aa83aa3 0x3aa53aa6 0x3aa73aa5
  25-> 0x3aaa3aa4 0x3aa83aa2 0x3aa63aa5 0x3aa83aa9 0x3aab3aa6 0x3aaa3aa9 0x3aaa3aa2 0x3aa73aa3
  33-> 0x3aaa3aa7 0x3aa53aa6 0x3aab3aa6 0x3aa53aa6 0x3aa63aa2 0x3aa53aa5 0x3aa93aa1 0x3aa93aa5
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```