dRICH (Back-End) DAQ

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Giornate Nazionali ePIC Italia 2025 - Padova
June 17h 2025

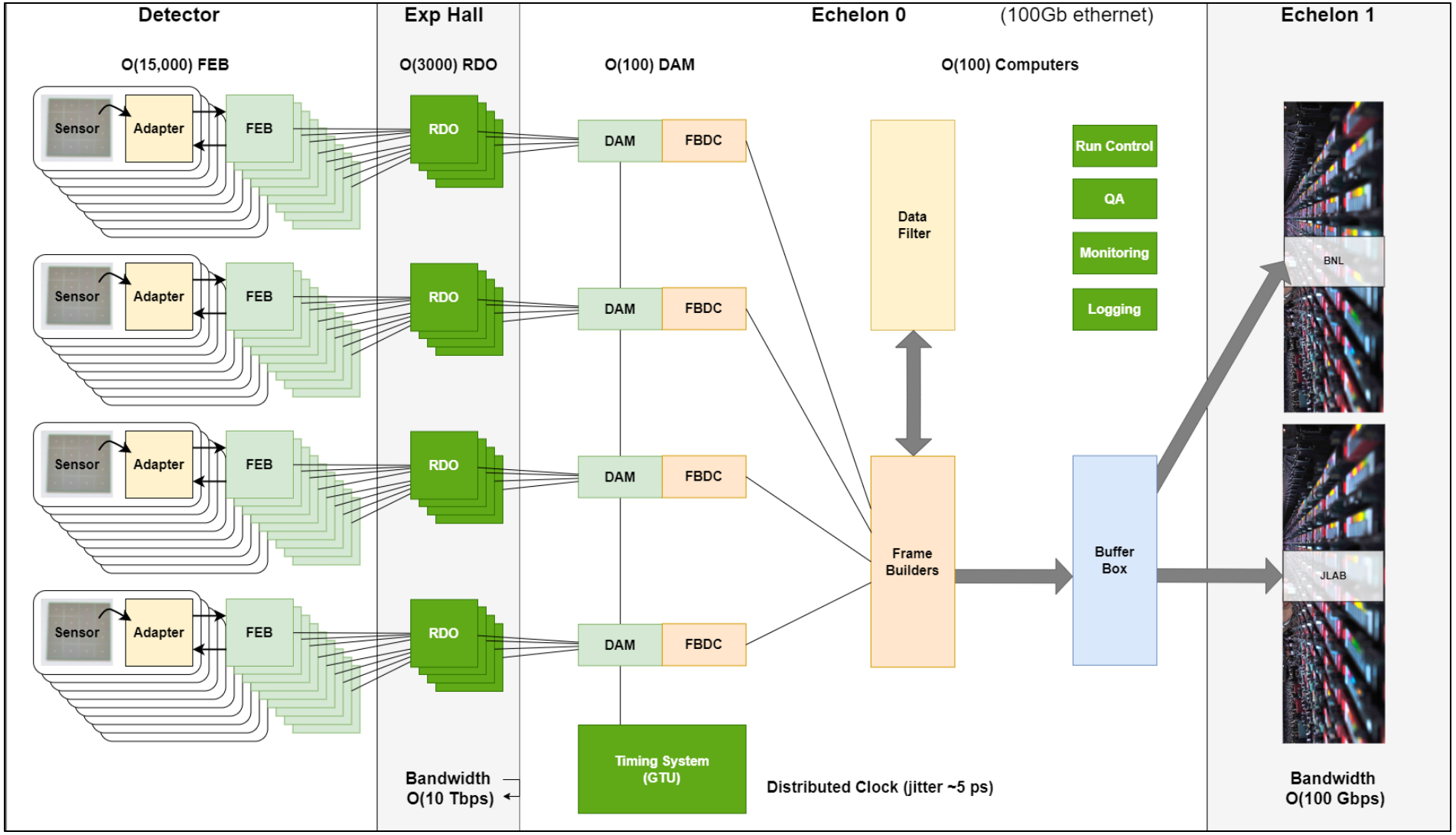
EIC Streaming DAQ/Computing Architecture

Collider Characteristics

- 1260 Bunches arriving at 98.5Mhz (10.15ns bunch separation)
- 1.015us abort gaps (100 bunches)
- $\sqrt{s} \Rightarrow$ 20 – 141 GeV
- $\mathcal{L}_{max} \Rightarrow 10^{34}$ cm^{-2} s^{-1}
- Electron, proton, and light nuclei beams can be polarized
- Each bunch can have different polarization states
  - DAQ must tag data to specific bunch crossings
  - Need to track luminosity for each bunch crossing

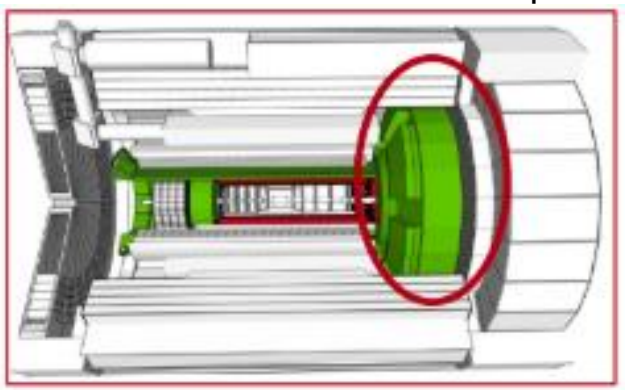
Physics Performance

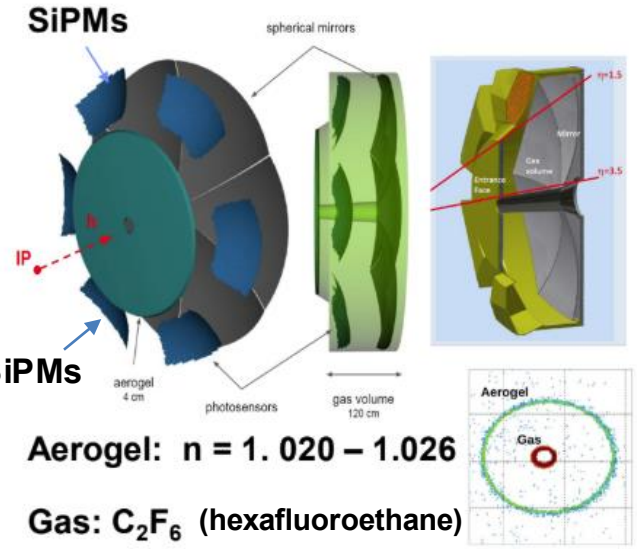
- Maximum DIS rate ~500kHz
- Large number of Channels
- Low occupancy



Dual Radiator RICH (dRICH)

Forward cap





PDU

- 1 photodetector unit PDU: 4x64 SiPM array device (256 channels), 4 FEBs, 1 RDO
- 1248 PDUs for full dRICH readout
- 319488 readout channels divided in six sectors

FELIX

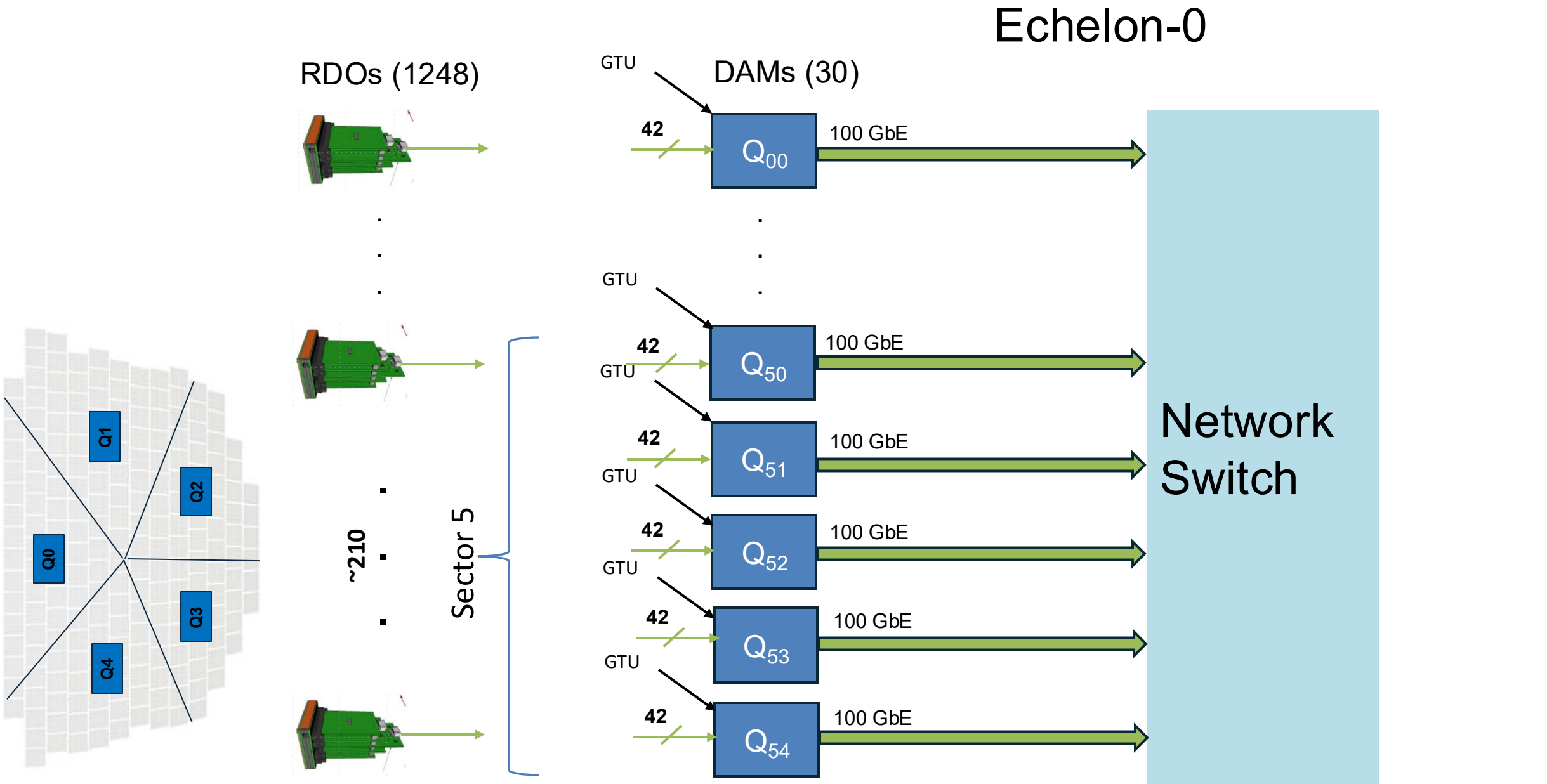
DAM
Data Aggregation Module

SERVER

- 42 links from PDUs to Felix-155 board
- 30 Felix-155 boards in total

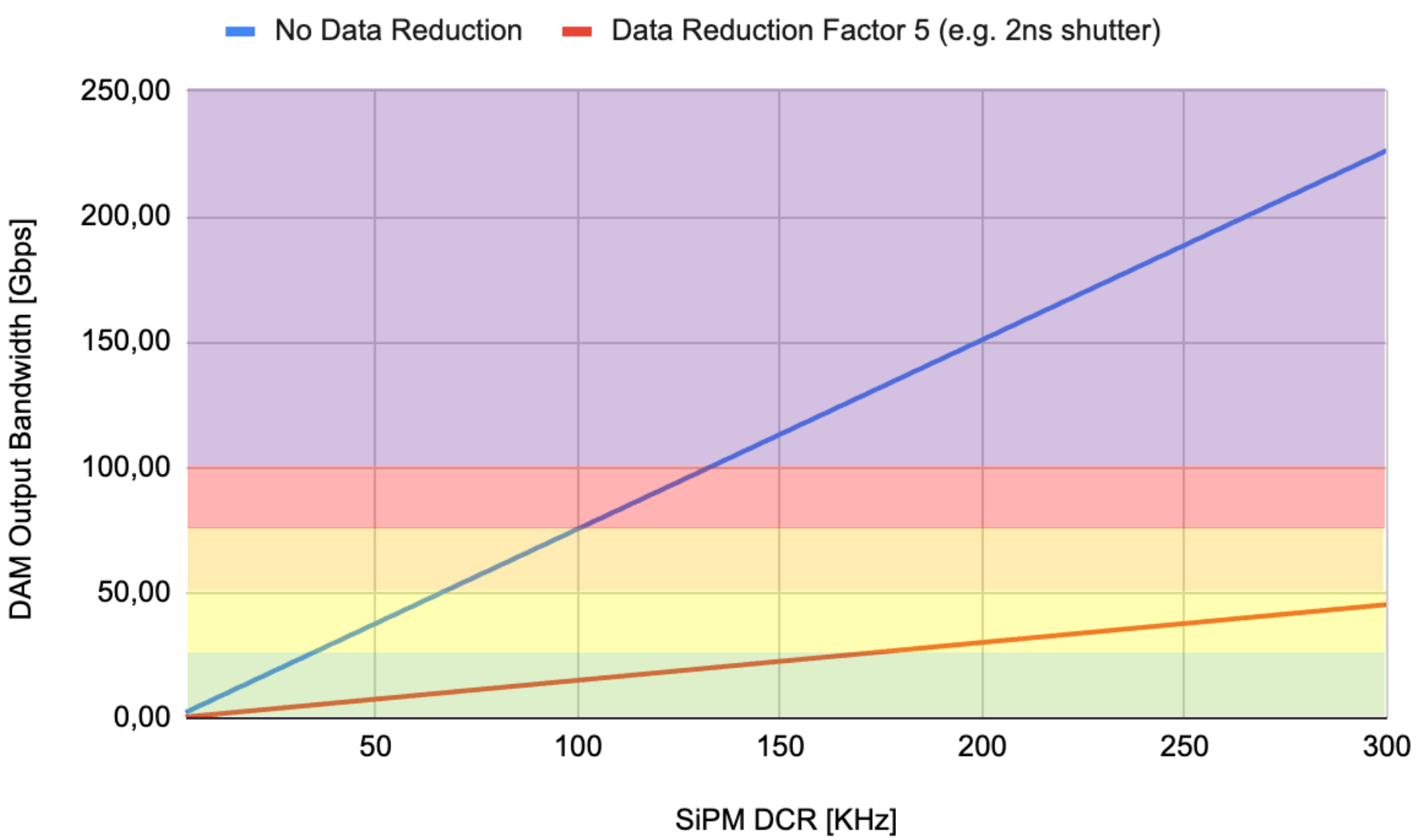
ePIC processing and storage system

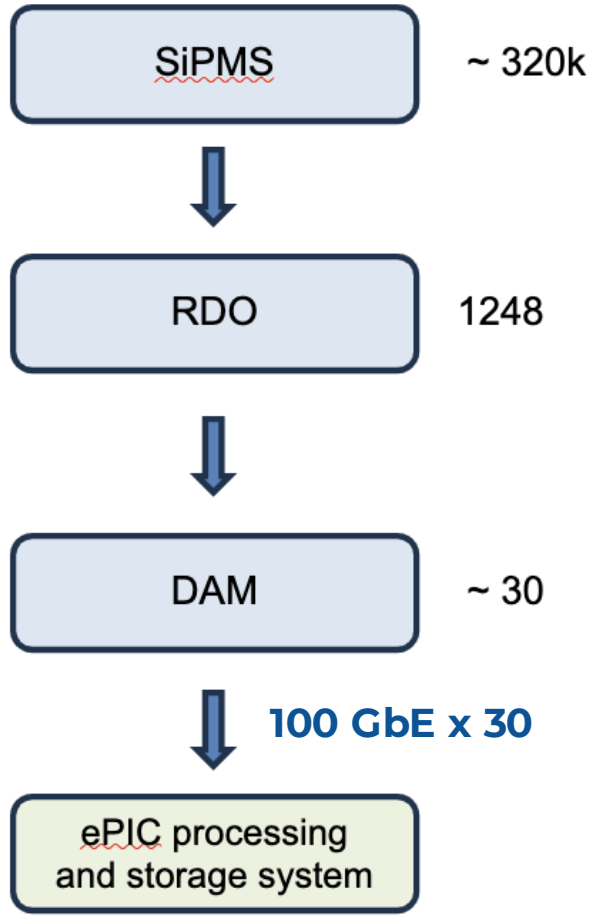
dRICH DAQ


Echelon-0
RDOs (1248)
DAMs (30)
GTU
42
100 GbE
Q_{00}
Q_{50}
Q_{51}
Q_{52}
Q_{53}
Q_{54}
~210
Sector 5
Q0
Q1
Q2
Q3
Q4
Network Switch

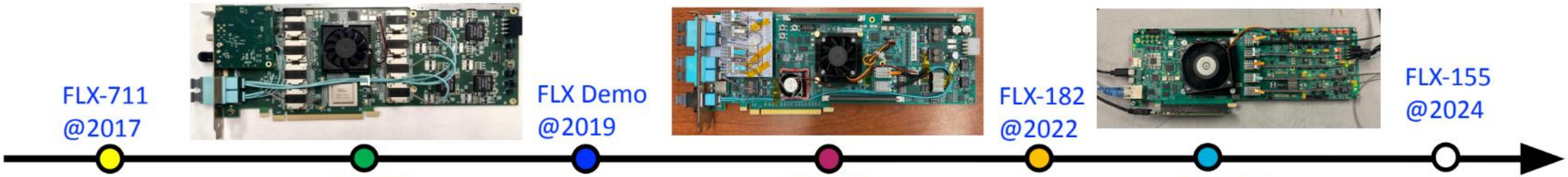
Analysis of dRICH Output Bandwidth

Net payload BW < ¼ Max	< Net payload BW < 1/2 Max	< Net payload BW < 3/4 Max	< Net payload BW < Max





FELIX Hardware Development at BNL



FLX-711 @2017

PCIe Gen3 x16
48x 10 Gb/s
DDR3

FLX-712 @2018

PCIe Gen3 x16
48x 10 Gb/s

FLX Demo @2019

PCIe Gen3 x16
25 Gb/s with various optical modules

FLX-181 @2021

PCIe Gen4 x16
FMC+ 16x 25 Gb/s
12x 16 Gb/s
SoC / DDR4

FLX-182 @2022

PCIe Gen4 x16
28x 10/25 Gb/s
100 GbE
SoC / DDR4

FLX-182B @2023

FLX-155 @2024

PCIe Gen5 x16
48x 10/25 Gb/s
100/400 GbE
SoC / DDR4

FLX-182B Hardware

Assembled FLX-182B

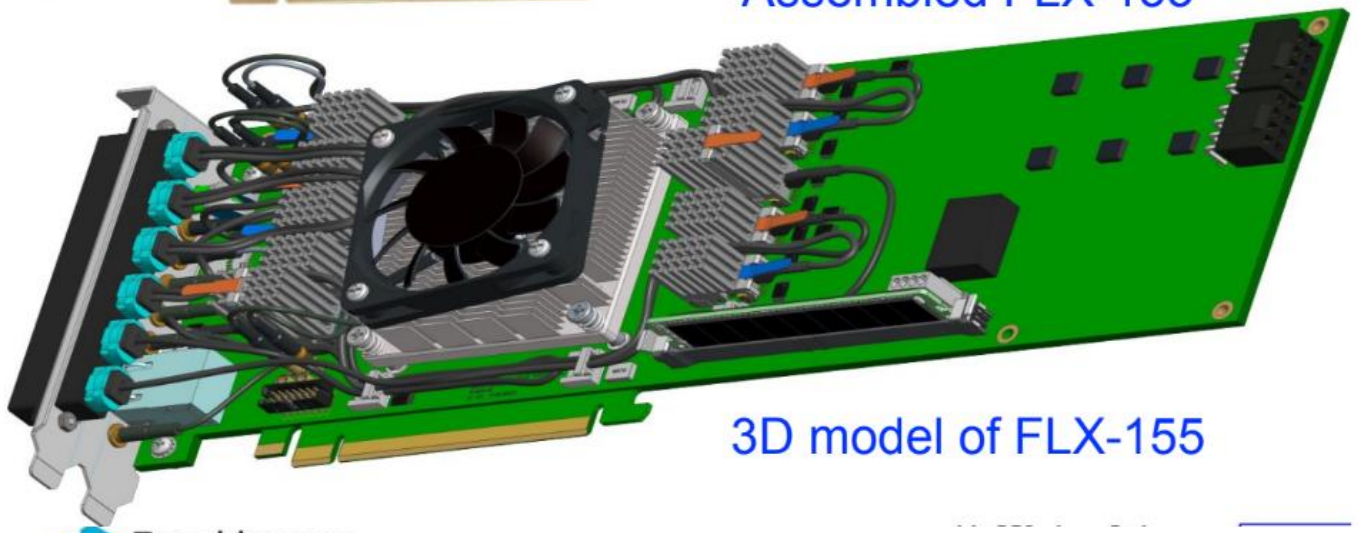
- FPGA: Xilinx Versal Prime XCVM1802
- PCIe Gen4 x16, 256 GT/s
- 24 FireFly links with 3 possible configurations
  - 24 links up to 25 Gb/s
  - 24 links up to 10 Gb/s (CERN-B FireFly)
  - 12 links up to 25 Gb/s + 12 links up to 10 Gb/s
- 4 FireFly links with 2 possible configurations with 14 or 25 Gb/s FireFly TRx
  - LTI interface
  - 100 GbE
- Built-in self test, online configuration and monitoring
- White Rabbit
- DDR4 Mini-UDIMM
- GbE/SD3.0/PetaLinux

Table 10: **Versal Prime Series**

	VM1102	VM1302	VM1402	VM1502	VM1802	VM2152	VM2202	VM2302	VM2502	VM2902
System Logic Cells	328,720	703,360	1,237,600	981,120	1,968,400	757,120	1,139,040	1,574,720	1,969,240	2,233,280
CLB Flip-Flops	300,544	643,072	1,131,520	897,024	1,799,680	692,224	1,041,408	1,439,744	1,800,448	2,041,856
LUTs	150,272	321,536	565,760	448,512	899,840	346,112	520,704	719,872	900,224	1,020,928
Distributed RAM (Mb)	4.6	9.8	17.3	13.7	27.5	10.6	15.9	22.0	27.5	31.2
Block RAM Blocks	155	503	1,150	954	967	759	600	1,405	1,341	1,981
Block RAM (Mb)	5.4	17.7	40.4	33.5	34.0	26.7	21.1	49.4	47.1	69.6
UltraRAM Blocks	155	179	286	462	463	191	264	453	677	645
UltraRAM (Mb)	43.6	50.3	80.4	129.9	130.2	53.7	74.3	127.4	190.4	181.4
Accelerator RAM (Mb)	32	–	–	–	–	–	–	–	–	–
DSP Engines	464	848	1,696	1,312	1,968	1,704	1,312	1,904	3,984	2,672
Maximum DSP Cascade	116	212	212	164	164	142	164	238	166	334
APU	Dual-core Arm Cortex-A72; 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC									
RPU	Dual-core Arm Cortex-R5F; 32 KB/32 KB L1 Cache; TCM w/ECC									
Memory	256 KB On-Chip Memory w/ECC									
Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)									
NoC to PL Master / Slave Ports	5	9	18	21	28	12	21	30	28	42
DDR Bus Width	64	128	256	192	256	128	192	192	256	192
DDR4 Memory Controllers (DDRMC)	1	2	4	3	4	–	3	3	4	2
DDR5 Memory Controllers (DDRMC5C)	–	–	–	–	–	4	–	–	–	–
PCIe w/DMA (CPM4)	–	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16	–	–	–	–	–
PCIe w/DMA (CPM5)	–	–	–	–	–	–	2 x Gen5x8	–	2 x Gen5x8	–
PCIe (PL PCIE4)	–	2 x Gen4x8	2 x Gen4x8	4 x Gen4x8	4 x Gen4x8	–	–	–	–	–
PCIe (PL PCIE5)	1 x Gen4x8	–	–	–	–	2 x Gen5x4	4 x Gen5x4	2 x Gen5x4	–	2 x Gen5x4
100G Multirate Ethernet MAC	1	2	2	4	4	2	2	6	–	6
600G Ethernet MAC	–	–	–	–	–	1	–	–	–	–
High-Speed Crypto Engines	–	–	–	–	–	1	–	–	–	–
GTY Transceivers[(1)]	–	24	24	44	44	–	–	–	–	–
GTYP Transceivers[(1)]	8	–	–	–	–	8	32[(2)]	8	16[(2)]	8
GTM Transceivers[(1)] 58 Gb/s (112 Gb/s)	–	–	–	–	–	8 (4)	–	36 (0)	–	36 (0)

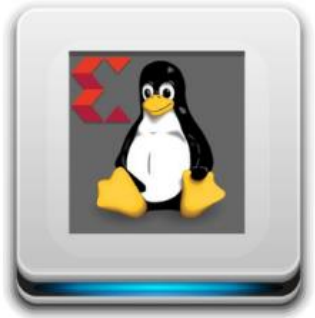
FLX-155 Hardware

Assembled FLX-155



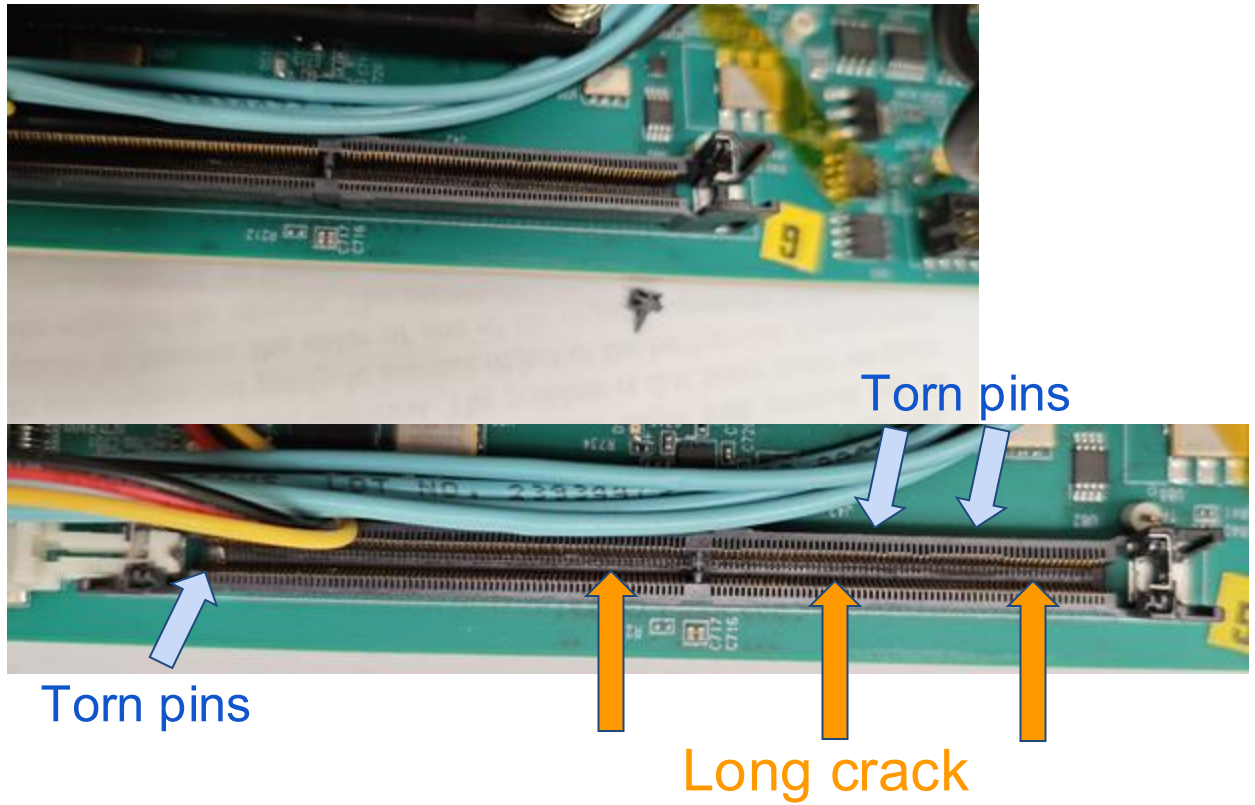
3D model of FLX-155

- AMD/Xilinx Versal Premium FPGA: XCVP1552-2MSEVSVA3340
- 2 x PCIe Gen5 x8 512 GT/s
- 56 FireFly optical links
  - Compatible with various options
  - Default configuration for ATLAS
    - 48 data links up to 25 Gb/s
    - 4 links for LTI
  - Optional 4 links for 100 GbE
- Electrical IOs
- Built-in self test, online configuration and monitoring
- 1 16GB DDR4 Mini-UDIMM
- USB-JTAG/USB-UART
- GbE/SD3.0/PetaLinux
- Optional White Rabbit



	VP1002	VP1052	VP1102	VP1202	VP1402	VP1502	VP2502	VP1552	VP1702	VP1802	VP2802	VP1902
System Logic Cells	833,000	1,185,800	1,574,720	1,969,240	2,233,280	3,763,480	3,737,720	3,836,840	5,557,720	7,351,960	7,326,200	18,506,880
CLB Flip-Flops	761,600	1,084,160	1,439,744	1,800,448	2,041,856	3,440,896	3,417,344	3,507,968	5,081,344	6,721,792	6,698,240	16,920,576
LUTs	380,800	542,080	719,872	900,224	1,020,928	1,720,448	1,708,672	1,753,984	2,540,672	3,360,896	3,349,120	8,460,288
Distributed RAM (Mb)	12	17	22	27	31	53	52	54	78	103	102	258
Block RAM Blocks	535	751	1,405	1,341	1,981	2,541	2,541	2,541	3,741	4,941	4,941	6,808
Block RAM (Mb)	19	26	49	47	70	89	89	89	132	174	174	239
UltraRAM Blocks	345	489	453	677	645	1,301	1,301	1,301	1,925	2,549	2,549	2,200
UltraRAM (Mb)	97	138	127	190	181	366	366	366	541	717	717	619
Multiport RAM (Mb)	80	80	-	-	-	-	-	-	-	-	-	-
DSP Engines	1,140	1,572	1,904	3,984	2,672	7,440	7,392	7,392	10,896	14,352	14,304	6,864
AI Engines (AIE)	-	-	-	-	-	-	472	-	-	-	472	-
AIE Data Memory (Mb)	-	-	-	-	-	-	118	-	-	-	118	-
APU	Dual-core Arm Cortex-A72; 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC											
RPU	Dual-core Arm Cortex-R5F; 32 KB/32 KB L1 Cache; TCM w/ECC											
Memory	256 KB On-Chip Memory w/ECC											
Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)											
NoC to PL Master / Slave Ports	22	22	30	28	42	52	52	52	76	100	100	192
DDR Bus Width	128	128	192	256	192	256	256	256	256	256	256	896
DDR Memory Controllers (DDRMC)	2	2	3	4	3	4	4	4	4	4	4	14
PCIe w/DMA (CPM4)	2 x Gen4x4	2 x Gen4x4	-	-	-	-	-	-	-	-	-	-
PCIe w/DMA (CPM5)	-	-	-	2 x Gen5x8	-	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	-
PCIe (PL PCIE4)	1 x Gen4x8	1 x Gen4x8	-	-	-	-	-	-	-	-	-	-
PCIe (PL PCIE5)	-	-	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	8 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	16 x Gen5x4
100G Multirate Ethernet MAC	3	5	6	2	6	4	4	4	6	8	8	12
600G Ethernet MAC	2	3	7	1	11	3	3	1	5	7	7	4
600G Interlaken	1	2	-	-	-	1	1	-	2	3	3	0
High-Speed Crypto Engines	1	1	3	1	4	2	2	2	3	4	4	0
GTY Transceivers[1]	8	8	-	-	-	-	-	-	-	-	-	-
GTYP Transceivers[1]	-	-	8	28[3]	8	28[3]	28[3]	68[3]	28[3]	28[3]	28[3]	128
GTM Transceivers[1] 58Gb/s (112 Gb/s)	24 (12)	36 (18)	64 (32)	20 (10)	96 (64)[2]	60 (30)	60 (30)	20 (10)	100 (50)	140 (70)	140 (70)	32 (16)

Procurement of a Felix-182 Card



Felix-182 board on loan from Jlab arrived in Rome end of December ’24 (thanks David Abbott!).

Unfortunately it showed damages to the DRAM slot:

- **torn contact pins**
- **a crack along the inner side of the slot**

They likely occurred due to the pressure of a DRAM module left in the slot during the delivery.

As a consequence, DRAM is not detected by the system.

We tried to load some standard firmwares to the board but it was not possible because the DRAM check failed.

We consulted:

- the INFN Electronics Laboratory in Rome
- CERN EP-ESE Electronic Systems for Experiments (thanks Markus Joos!)

Both agreed that is extremely difficult to repair the DRAM slot and not worth the effort considering the costs and the likely not optimal result, we were ready to send it back, BUT…

Installation of a Felix-182 Card @ APE Lab

- We got advice from Carlo Alberto Gottardo (Coordinator of the FELIX project) about the fact that the DRAM is used only by the PS (ARM SoC) and that in current FW versions the PS performs just ancillary functions (BIST,…), while all the design core functionalities are implemented in the PL.
- Still flashing the bitstream of the official FW release through JTAG was impossible due to the failing check of DRAM…

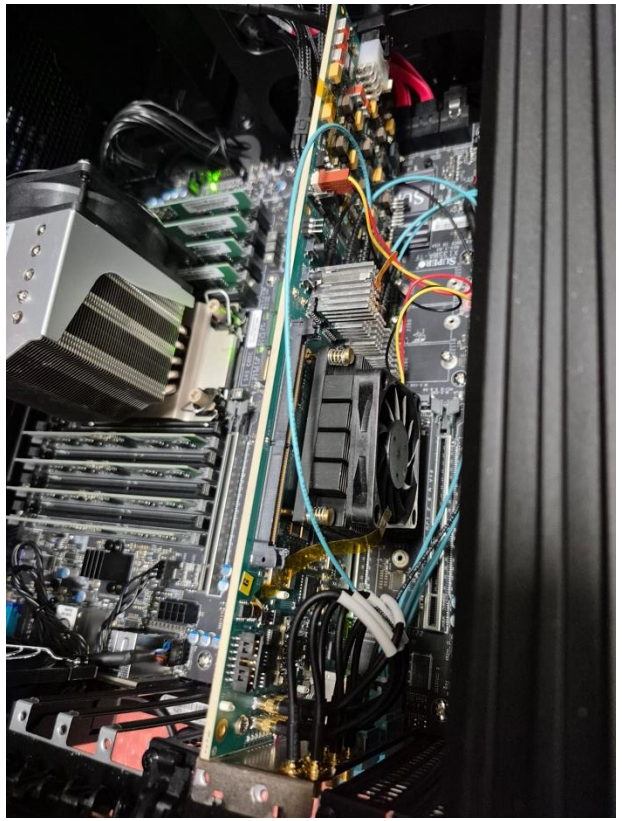
1. Carlotta Chiarini modified the release FW removing the PS (and DRAM) from the design → modified FW loaded and board detected!
2. Francesca Lo Cicero found the setting for the AXI NoC component in the block design cips_BD_BNL182, Startup Options: DDRMC Calibration Status at Startup to SKIP. The default behavior for the Versal PLM at boot is to gate the assertion of the Configuration DONE signal if a DDRMC fails calibration. If this option is set to SKIP then the DDRMC calibration status will be ignored at startup and DONE will assert regardless of the DDRMC status. → Release FW loaded and board detected!

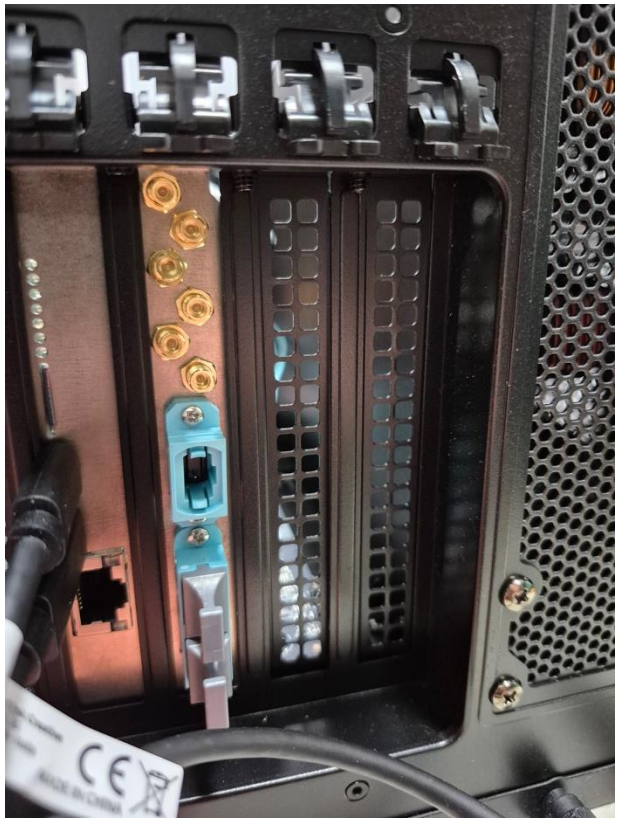
```
[locicero@apestation0 ~]$ lspci -vvvvvv | grep CERN
34:00.0 Network controller: CERN/ECP/EDU Device 0428
        Subsystem: CERN/ECP/EDU Device 0038
35:00.0 Network controller: CERN/ECP/EDU Device 0427
        Subsystem: CERN/ECP/EDU Device 0038
```

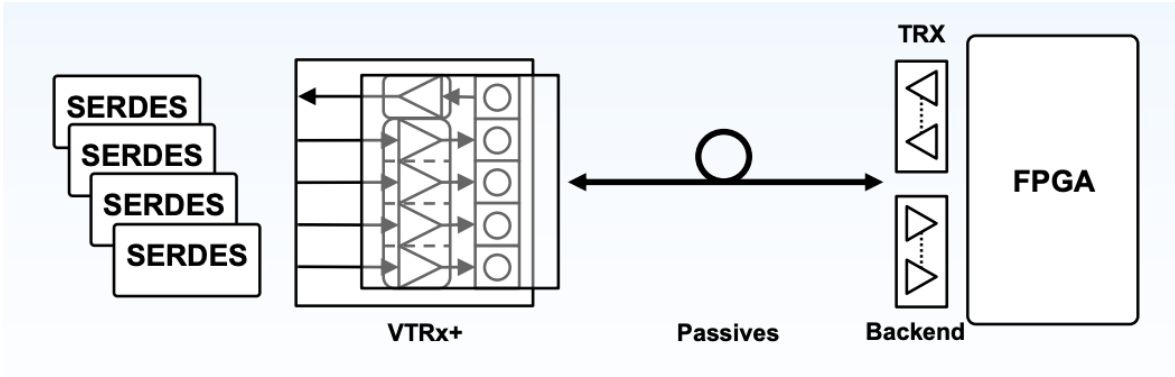
2 PCIe Gen4 x8 (on a bifurcated x16 slot)

Installation of a Felix-182 Card @ APE Lab

```
lonardo@apestation0 x86_64-el9-gcc13-opt]$  bin/flx-init
2025-05-14 18:06:05 Opening card 0 (device 0)...
2025-05-14 18:06:05 Card type: FLX-182
2025-05-14 18:06:05 Firmware : FULL
2025-05-14 18:06:05 Clock    : Local
2025-05-14 18:06:05 FLX soft reset
2025-05-14 18:06:05 SI5345A hard reset
2025-05-14 18:06:07 ### SI5345A part nr: read 0xFF, expected 0x45; device not
present/accessible?
2025-05-14 18:06:07 Found SI5345A_BETA
…
2025-05-14 18:06:12 Links soft reset
2025-05-14 18:06:12 Setting up links...
2025-05-14 18:06:19 Links set up
2025-05-14 18:06:19 WARNING: 4 channels not aligned
2025-05-14 18:06:19 Resetting FireFly devices...
2025-05-14 18:06:19 FIREFLY_TX1: PartNr="CERNBY12040213M ",
SerNr="UA2042001A"
2025-05-14 18:06:19 FIREFLY_RX1: PartNr="CRRNBY12040213M ",
SerNr="UA2042001A"
2025-05-14 18:06:20 FIREFLY_TX2: PartNr="CERNBY12040213M ",
SerNr="UA2042001F"
2025-05-14 18:06:20 FIREFLY_RX2: PartNr="CRRNBY12040213M ",
SerNr="UA2042001F"
2025-05-14 18:06:20 FIREFLY_TXRX: PartNr="B042804005170",
SerNr="UA231005DX"
2025-05-14 18:06:20   WARNING: CDR not changed, part expected "B042504005170"
2025-05-14 18:06:20 FireFly done
…
2025-05-14 18:06:20 INA226 configured
2025-05-14 18:06:20 Initializing LTI...
2025-05-14 18:06:20 LTI alignment: NO
```







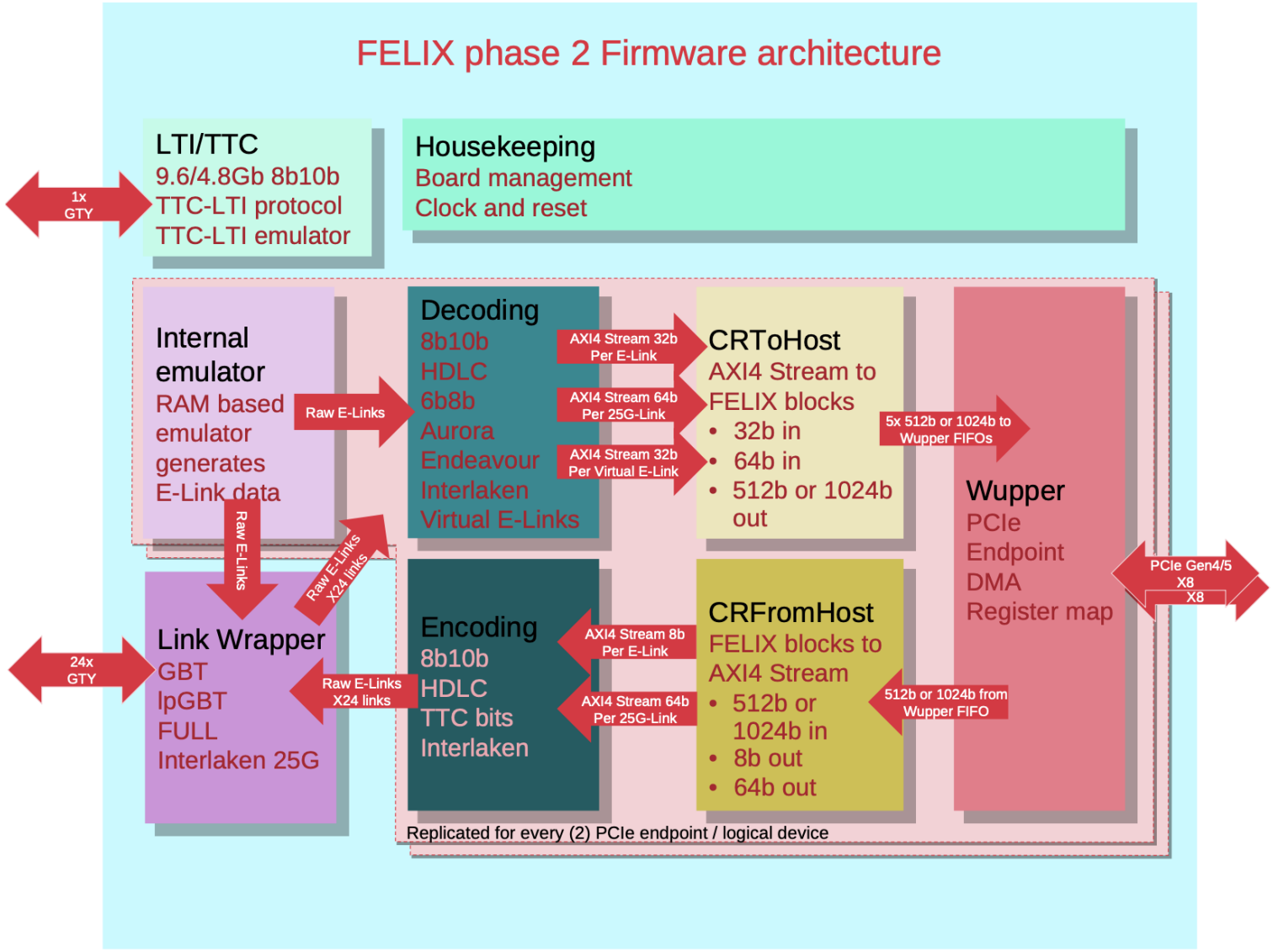


Figure 2.1: The FELIX firmware top level block diagram using PCIe Gen4. On Gen5 capable hardware, the diagram will have 4 endpoints, each with a PCIe Gen5x4 link.

FPGA Resources Occupancy on Felix-182 (FULL Flavour)

Name	Registers (1799680)	CLB LUTs (899840)	LUT as Logic (899840)	LUT as Memory (449920)	LOOKAHEAD8 (112480)	SLICE (112480)	CLB Registers (1799680)	Block RAM Tile (967)	URAM (463)	Bonded IOB (692)	BUFGCE_DIV/MBUFGCE_DIV (40)	BUFG_PS/MBUFG_PS (12)	BUFG_GT/MBUFG_G (168)
N felix_top	11.30%	13.58%	13.00%	1.16%	1.13%	26.87%	11.30%	19.23%	37.58%	27.75%	2.50%	16.67%	10.7

Felix Phase-II Firmware Flavours

Flavour	Link Wrapper	Decoders	Encoders	Remarks
0: GBT	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The GBT mode flavour is available in 8 and 24 channel versions, with a complete set of encoders / decoders, and a so called SemiStatic configuration where some decoders/encoders are left out. FELIX aims to provide a 24 channel fully configurable version for FLX712, it has been demonstrated to work but with high resource count (78% LUTs)
1: FULL	ToHost FULL, FromHost GBT or LTI	FULL 8.4.15 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14 LTI-tx 8.6	The FULL mode flavour is available in 24 channels for FLX712 and FLX128. The ToHost side/decoding is using 9.6Gb/s 8b10b data without logical links. FromHost/encoding is identical to GBT, with an option to transmit a copy of the LTI-TTC link data at 9.6Gb 8b10b with additional fields for XOFF
2: LTDB	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	LTDB mode is a 48 channel version of GBT mode, but with reduced e-link configurability. This flavour only includes the EC and IC e-links, as well as an AUX e-link (Egroup 4, link 7) with HDLC/8b10b/Direct configuration. Additionally TTC distribution is available on all FromHost/ToFrontend e-links.
4: PIXEL	lpGBT	HDLC (EC/IC) 8.4.14 Aurora 8.4.11 TTCToHost 8.4.17 BusyToHost 8.4.18	RD53A/B 8.5.8 TTC 8.5.14 HDLC (IC/EC) 8.5.12	The Pixel flavour was designed to read out the ITk Pixel detector over lpGBT with Aurora e-links. The encoder uses a custom protocol for RD53 and includes a trigger and command state machine.
5: STRIP	lpGBT	HDLC (IC) 8.4.14 Endeavour (EC) 8.4.10 8b10b 8.4.13, 8.4.9 TTCToHost 8.4.17 BusyToHost 8.4.18	HDLC (EC) 8.5.12 Endeavour (EC) 8.5.7 LCB 8.5.9 R3L1 8.5.10	The Strip flavour was designed to read out the ITk Strip detector over lpGBT with 8b10b e-links. The encoder uses a strip custom protocol with so called trickle merge.
9: LPGBT	lpGBT	HDLC (EC/IC) 8.4.14 8b10b 8.4.13 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The lpGBT Flavour is the lpGBT equivalent of the GBT flavour. It involves 8b10b, HDLC and TTC protocols and the aim is to have a fully configurable 24 channel build available. The LPGBT flavour will include encoding and decoding schemes for the HGTD
10: INTERLAKEN	64b67b	ToHost Interlaken, FromHost LTI 8.4.19	LTI-tx 8.6	The Interlaken Flavour has 24x 25.78125 Gb/s Interlaken links in ToHost direction. Note that no more than 12 links can be fully occupied as otherwise the PCIe Gen4 bandwidth will be saturated. As encoders, the Interlaken flavour implements the TTC-LTI encoder, a copy of the received LTI frame but with additional XOFF bits.

		KU115	VM1802	VP1552
GBT 24 channel	LUT	80.65%	69.60%	35.71%
	FF	77.03%	50.94%	26.13%
	BRAM	70.00%	89.45%	34.04%
	URAM		62.20%	22.14%
FULL 24 channel	LUT	52.59%	44.35%	22.75%
	FF	38.40%	33.21%	17.03%
	BRAM	40.46%	20.99%	7.99%
	URAM		62.20%	22.14%
LPGBT 24 channel	LUT	112.51%	82.94%	42.55%
	FF	52.39%	38.62%	19.81%
	BRAM	68.94%	79.52%	30.26%
	URAM		62.20%	22.14%
PIXEL 24 channel	LUT	82.40%	60.75%	31.17%
	FF	62.04%	45.74%	23.46%
	BRAM	61.20%	62.25%	23.69%
	URAM		62.20%	22.14%
STRIP 24 channel	LUT	67.04%	49.42%	25.35%
	FF	49.94%	36.81%	18.88%
	BRAM	121.43%	104.45%	39.75%
	URAM		145.14%	51.65%
INTERLAKEN 8 channel	LUT		9.15%	4.69%
	FF		7.89%	4.05%
	BRAM		40.43%	15.39%
	URAM		0.00%	0.00%

Table 5.2: Resource utilization for all firmware flavours estimated for the

Felix Phase-II Firmware Flavours

Flavour	Link Wrapper	Decoders	Encoders	Remarks
0: GBT	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The GBT mode flavour is available in 8 and 24 channel versions, with a complete set of encoders / decoders, and a so called SemiStatic configuration where some decoders/encoders are left out. FELIX aims to provide a 24 channel fully configurable version for FLX712, it has been demonstrated to work but with high resource count (78% LUTs)
1: FULL	ToHost FULL, FromHost GBT or LTI	FULL 8.4.15 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14 LTI-tx 8.6	The FULL mode flavour is available in 24 channels for FLX712 and FLX128. The ToHost side/decoding is using 9.6Gb/s 8b10b data without logical links. FromHost/encoding is identical to GBT, with an option to transmit a copy of the LTI-TTC link data at 9.6Gb 8b10b with additional fields for XOFF
2: LTDB	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	LTDB mode is a 48 channel version of GBT mode, but with reduced e-link configurability. This flavour only includes the EC and IC e-links, as well as an AUX e-link (Egroup 4, link 7) with HDLC/8b10b/Direct configuration. Additionally TTC distribution is available on all FromHost/ToFrontend e-links.
4: PIXEL	lpGBT	HDLC (EC/IC) 8.4.14 Aurora 8.4.11 TTCToHost 8.4.17 BusyToHost 8.4.18	RD53A/B 8.5.8 TTC 8.5.14 HDLC (IC/EC) 8.5.12	The Pixel flavour was designed to read out the ITk Pixel detector over lpGBT with Aurora e-links. The encoder uses a custom protocol for RD53 and includes a trigger and command state machine.
5: STRIP	lpGBT	HDLC (IC) 8.4.14 Endeavour (EC) 8.4.10 8b10b 8.4.13, 8.4.9 TTCToHost 8.4.17 BusyToHost 8.4.18	HDLC (EC) 8.5.12 Endeavour (EC) 8.5.7 LCB 8.5.9 R3L1 8.5.10	The Strip flavour was designed to read out the ITk Strip detector over lpGBT with 8b10b e-links. The encoder uses a strip custom protocol with so called trickle merge.
9: LPGBT	lpGBT	HDLC (EC/IC) 8.4.14 8b10b 8.4.13 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The lpGBT Flavour is the lpGBT equivalent of the GBT flavour. It involves 8b10b, HDLC and TTC protocols and the aim is to have a fully configurable 24 channel build available. The LPGBT flavour will include encoding and decoding schemes for the HGTD
10: INTERLAKEN	64b67b	ToHost Interlaken, FromHost LTI 8.4.19	LTI-tx 8.6	The Interlaken Flavour has 24x 25.78125 Gb/s Interlaken links in ToHost direction. Note that no more than 12 links can be fully occupied as otherwise the PCIe Gen4 bandwidth will be saturated. As encoders, the Interlaken flavour implements the TTC-LTI encoder, a copy of the received LTI frame but with additional XOFF bits.

Potential problem scaling to 48 channels!

		KU115	VM1802	VP1552
GBT 24 channel	LUT	80.65%	69.60%	35.71%
	FF	77.03%	50.94%	26.13%
	BRAM	70.00%	89.45%	34.04%
	URAM		62.20%	22.14%
FULL 24 channel	LUT	52.59%	44.35%	22.75%
	FF	38.40%	33.21%	17.03%
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	URAM		0.00%	0.00%

Table 5.2: Resource utilization for all firmware flavours estimated for the

PicoDAQ development --- Streaming DAQ Milestones

Detector Install: FY29Q2 - FY31Q2
Cosmics: FY31Q3
Early CD-4: FY32Q4

DAQ Releases:

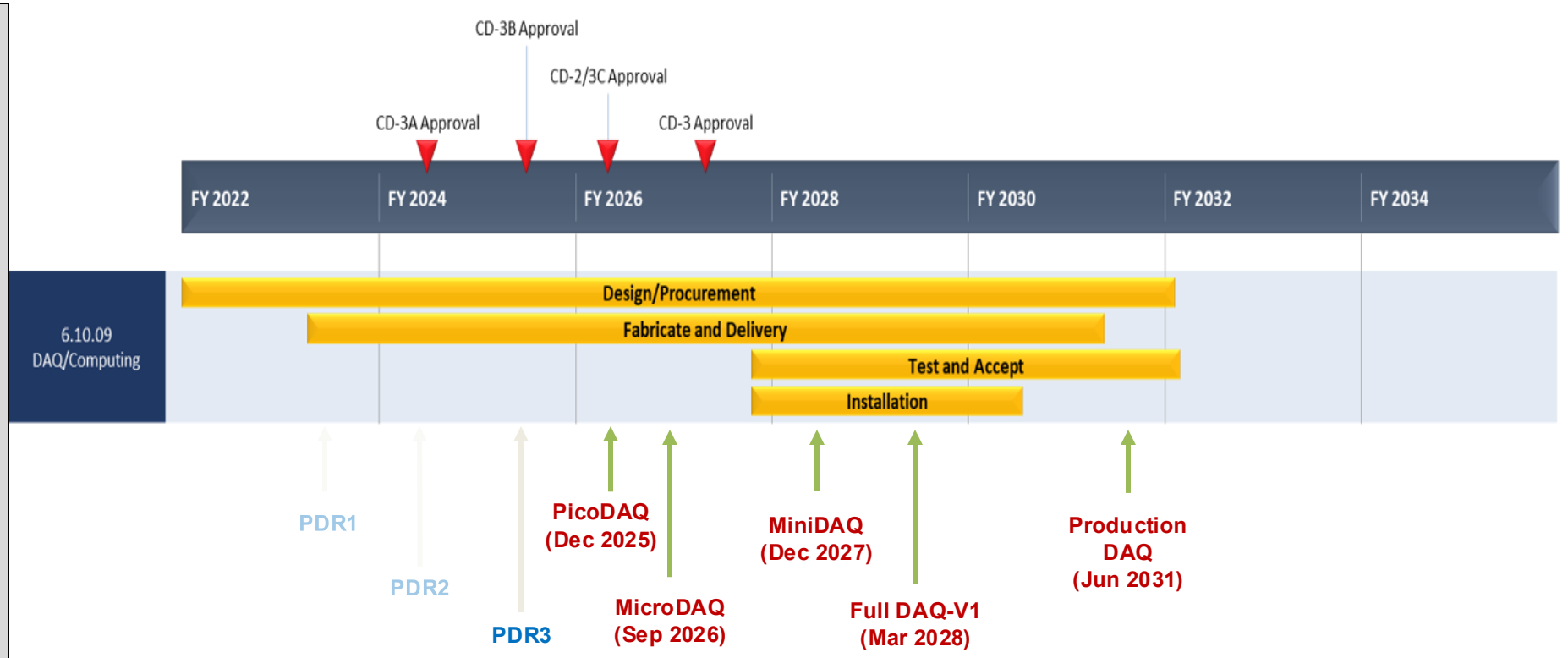
PicoDAQ
FY26Q1
Readout test setups

MicroDAQ: FY26Q4
Readout detector data in test stand using engineering articles

MiniDAQ: FY28Q1
Readout detector data using full hardware and timing chain

Full DAQ-v1: FY29Q2
Full functionality DAQ ready for full system integration & testing

Production DAQ: FY31Q3
Ready for cosmics



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Full functionality DAQ ready for full system integration & testing

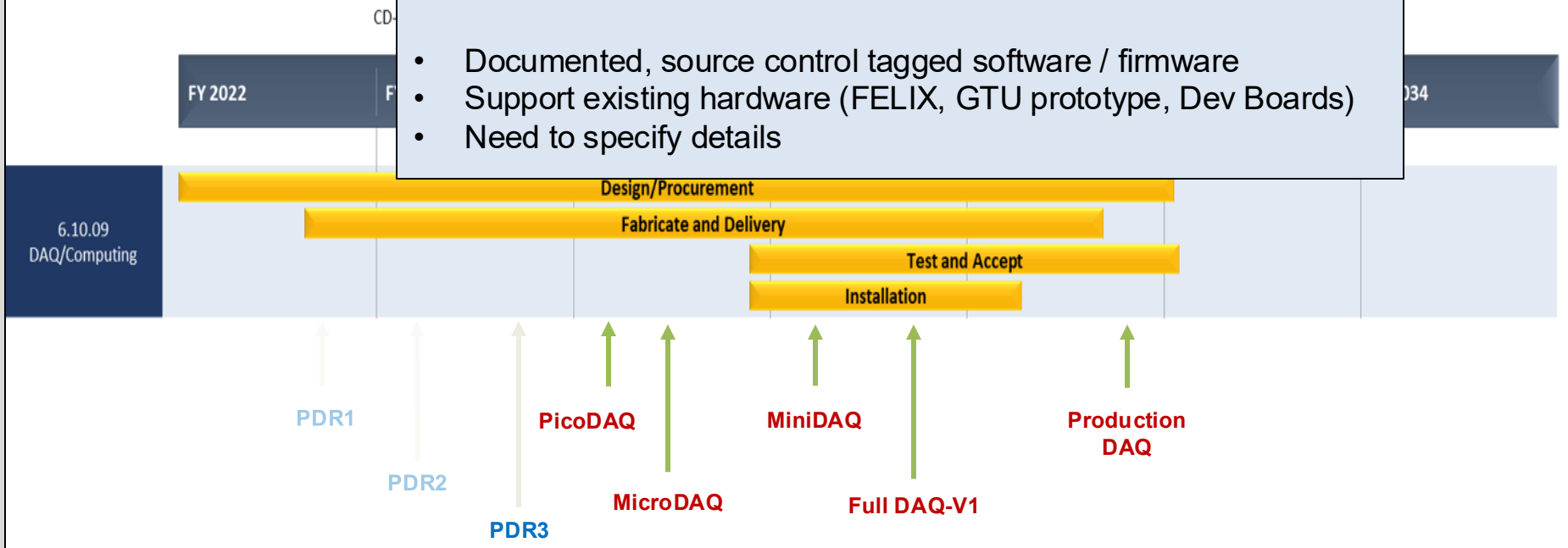
Production DAQ: FY31Q3
Ready for cosmics

PicoDAQ Milestone, ~~7~~ 6 months away!

- Need it to be well defined and show progress by PDR3
- Will help the collaboration develop test stands consistent with our eventual plans for epicDAQ
- Will help avoid duplication of effort when possible

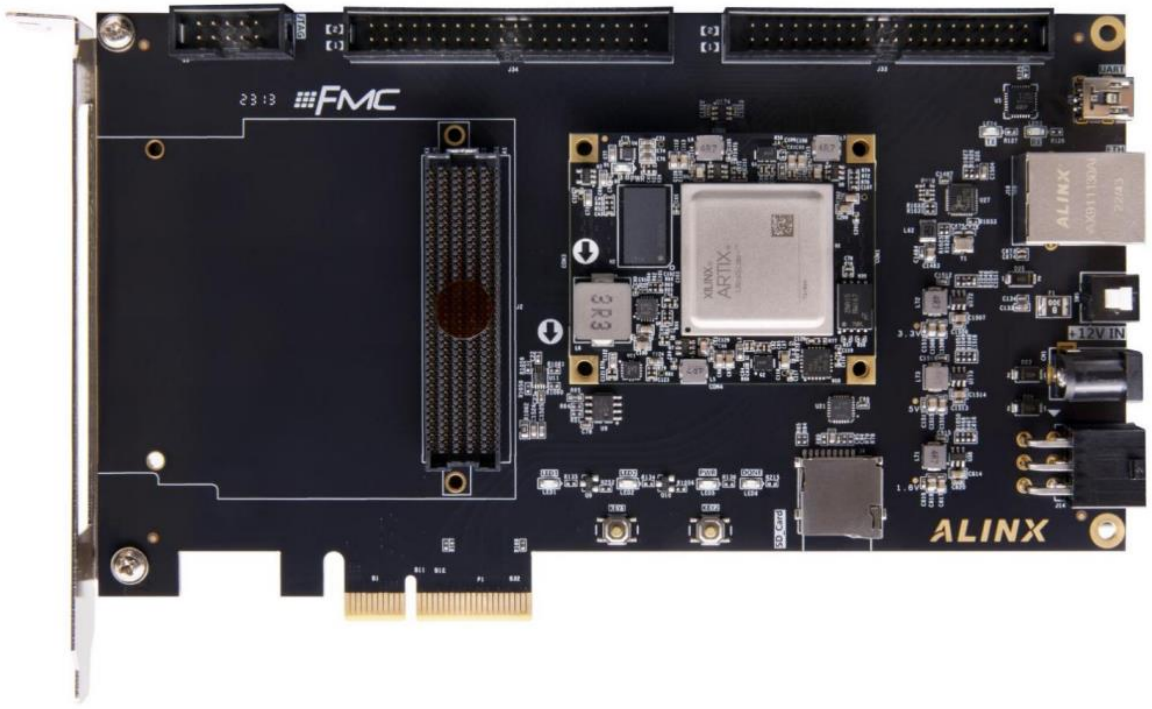
What is it?

- Documented, source control tagged software / firmware
- Support existing hardware (FELIX, GTU prototype, Dev Boards)
- Need to specify details

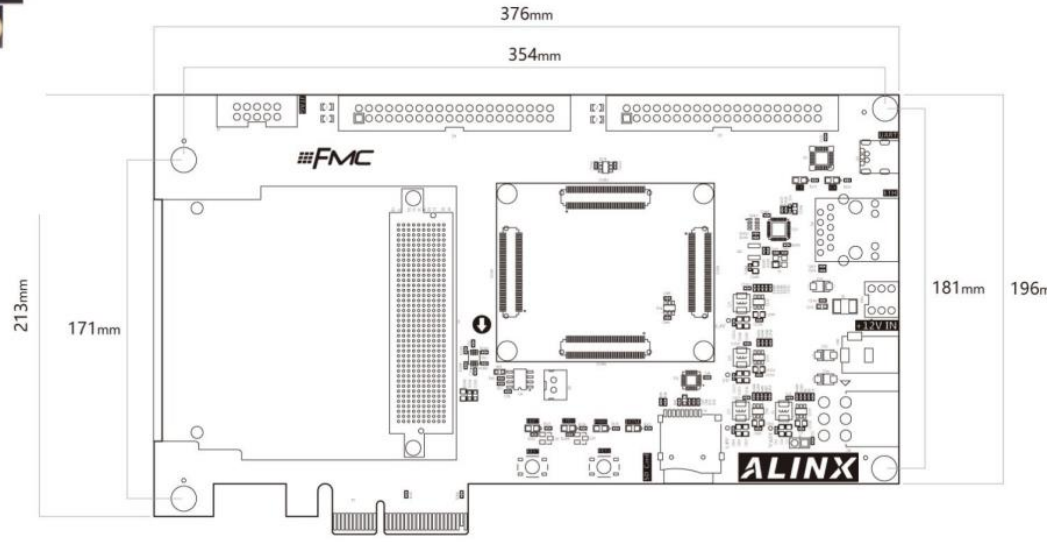


«Felix-lite» for PicoDAQ

Alinx AXAU15

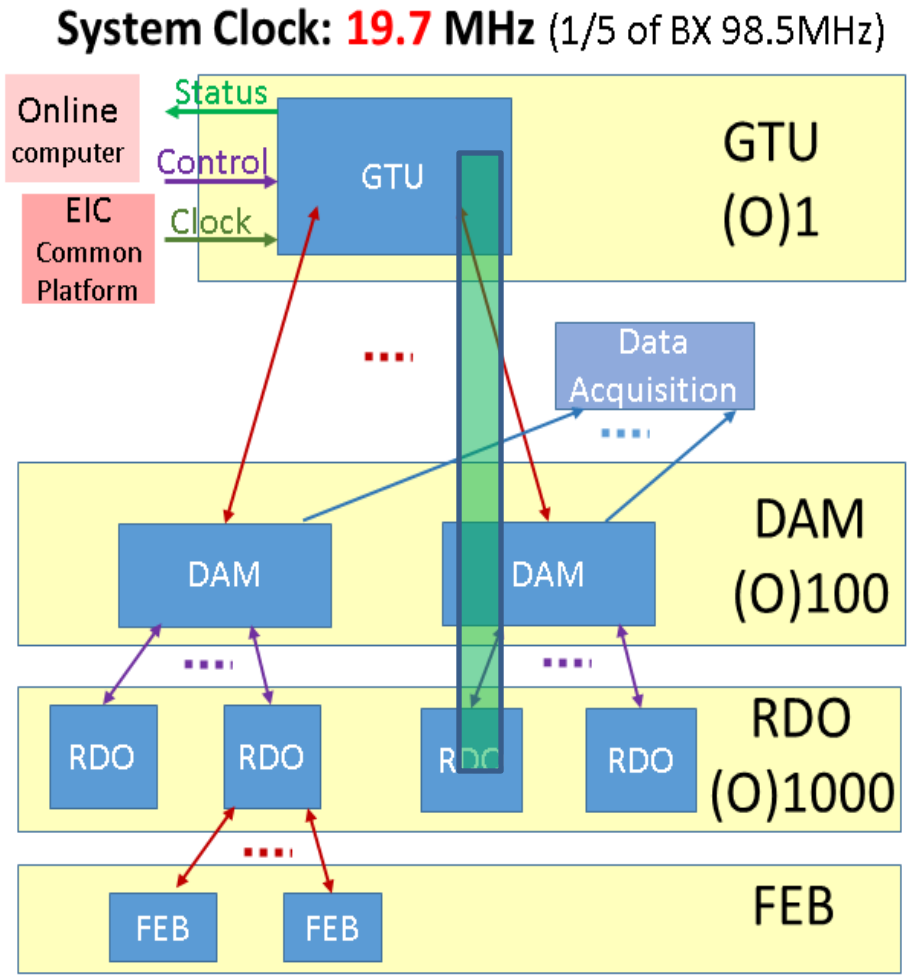


- **small, compact**
- Artix xcau15p FPGA (& associated PROM)
- FMC HPC (for fiber or direct ASIC Test Board)
- PCIe x4
- Mini USB UART Console (connected to the soft CPU core in the FPGA)
- Gb Ethernet (unused, anyone interested?)
- JTAG port
- 40 pin Expansion Ports (I only use them for debugging with a scope but TBD)
- External Power Supply connector (when on the bench)
- PC Power Supply connector (when installed in the computer)
- Micro SD slot (unused)



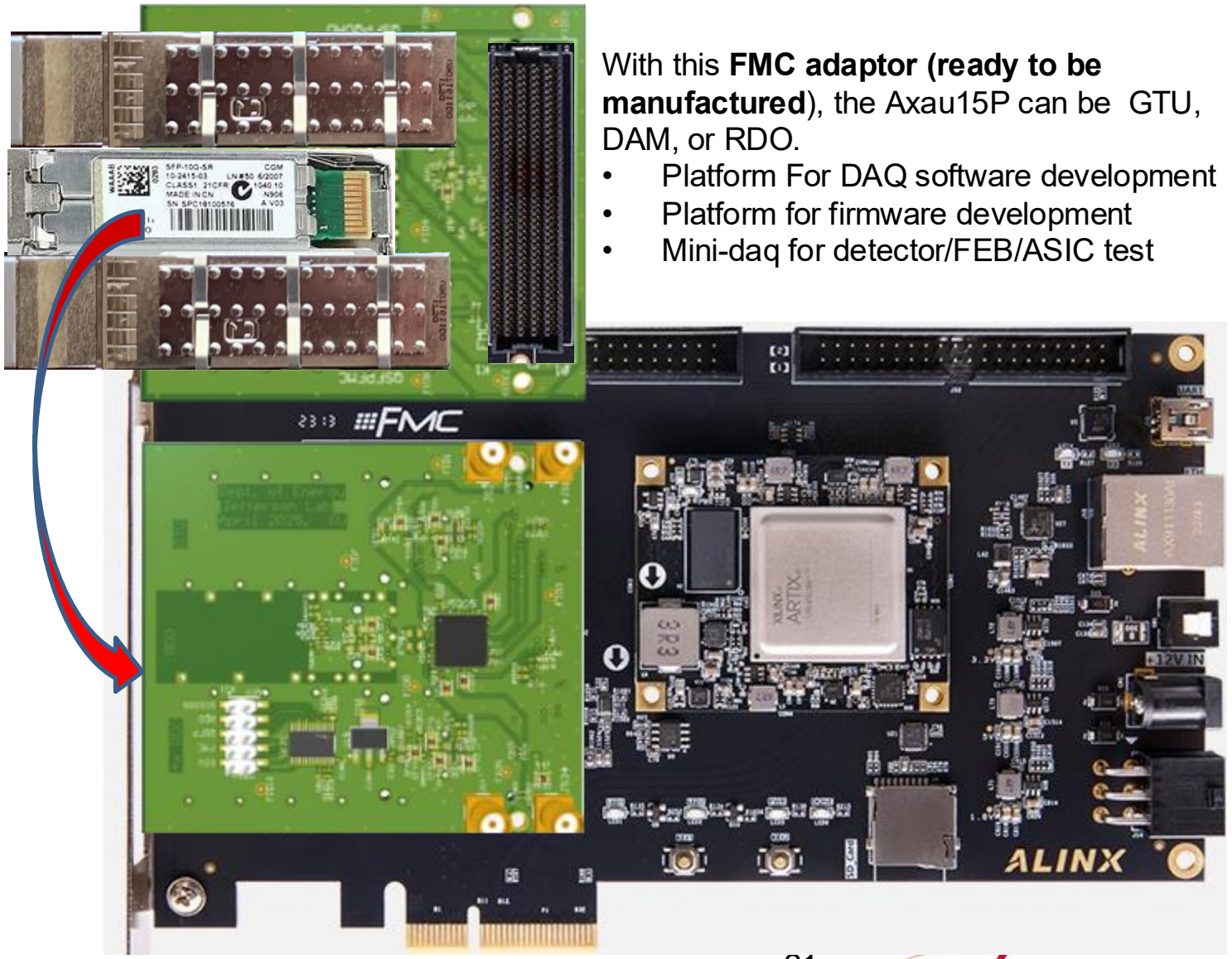
Top View

1. The ePIC designs



Mini_DAQ, functionally includes GTU, DAM, and RDO

2. FMC/(Q)SFP adaptor



With this **FMC adaptor (ready to be manufactured**), the Axau15P can be GTU, DAM, or RDO.

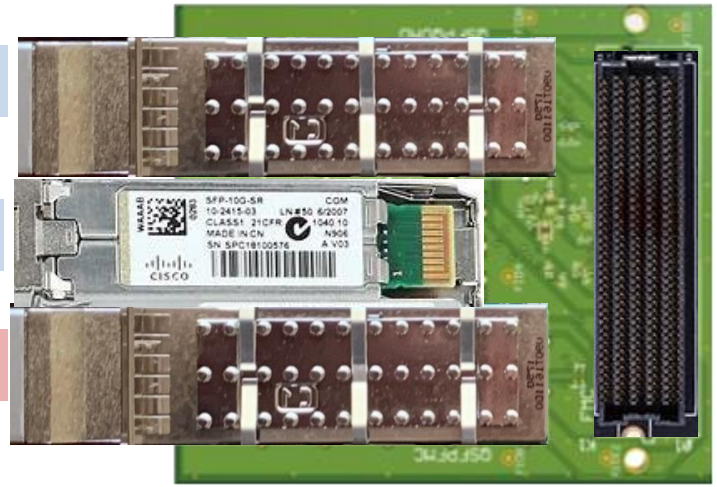
- Platform For DAQ software development
- Platform for firmware development
- Mini-daq for detector/FEB/ASIC test

3. (Q)SFP connection details

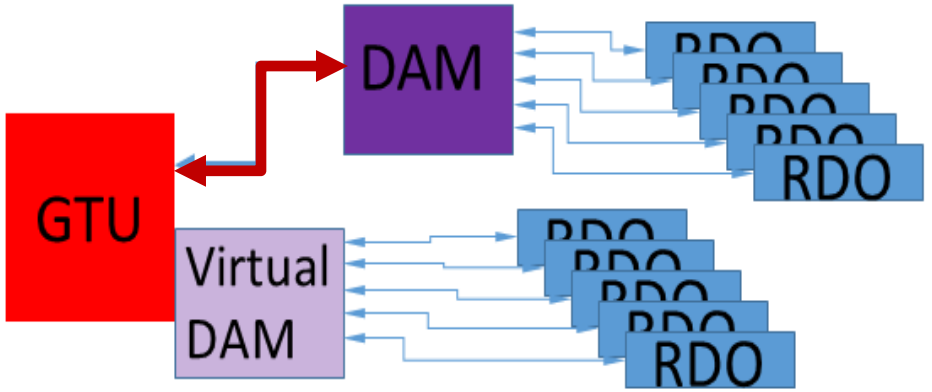
QSFP: 4x DAM ←→ RDO

SFP: 1x DAM ←→ RDO

QSFP: 1x GTU ←→ DAM



4. (max) system setup



One GTU
Two DAM
Ten RDO

DAM Regular ‘DAM’:

Master-mode ‘DAM’: built in GTU

Four pieces are being ordered.
Expected delivery: one month.

Streaming DAQ Milestones

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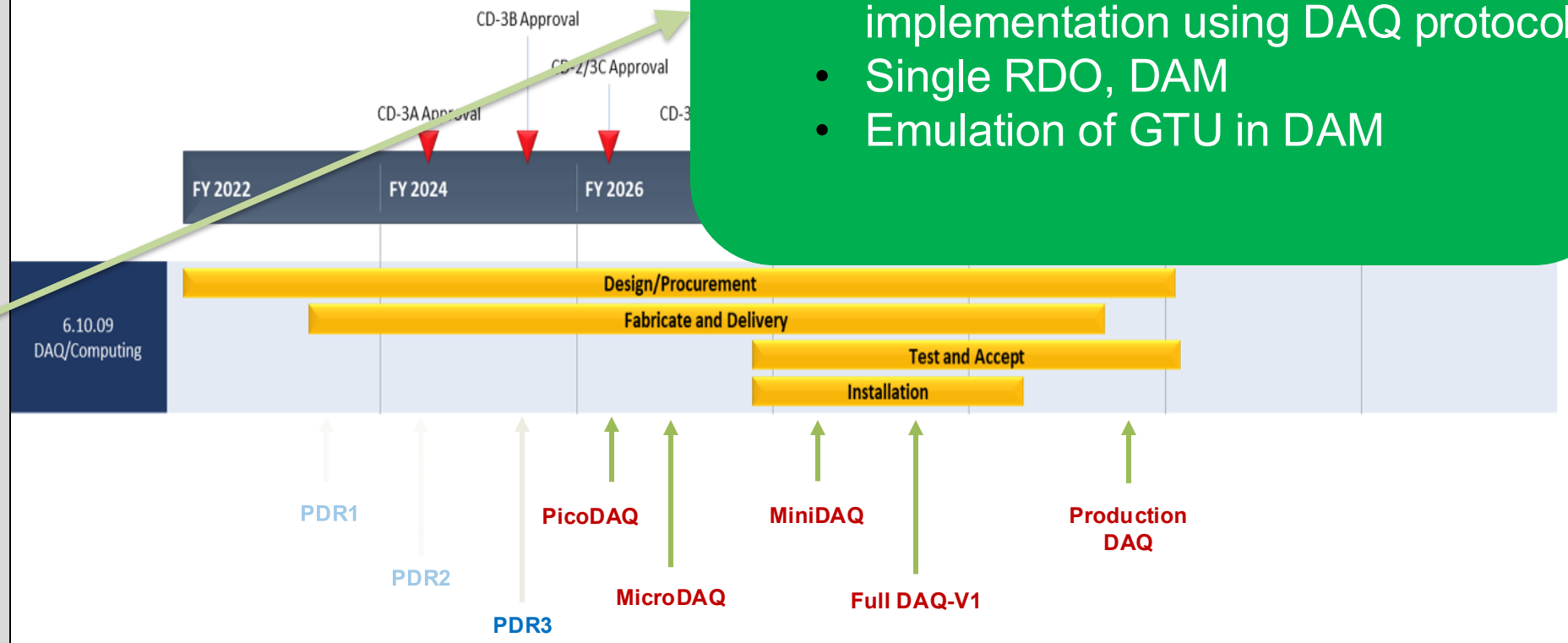

"MicroDAQ" – Readout detector data in test stand w engineering articles

- Stand alone FEB -> RDO -> DAM implementation using DAQ protocol
- Single RDO, DAM
- Emulation of GTU in DAM

Streaming DAQ Milestones

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Early CD-4: FY32Q4

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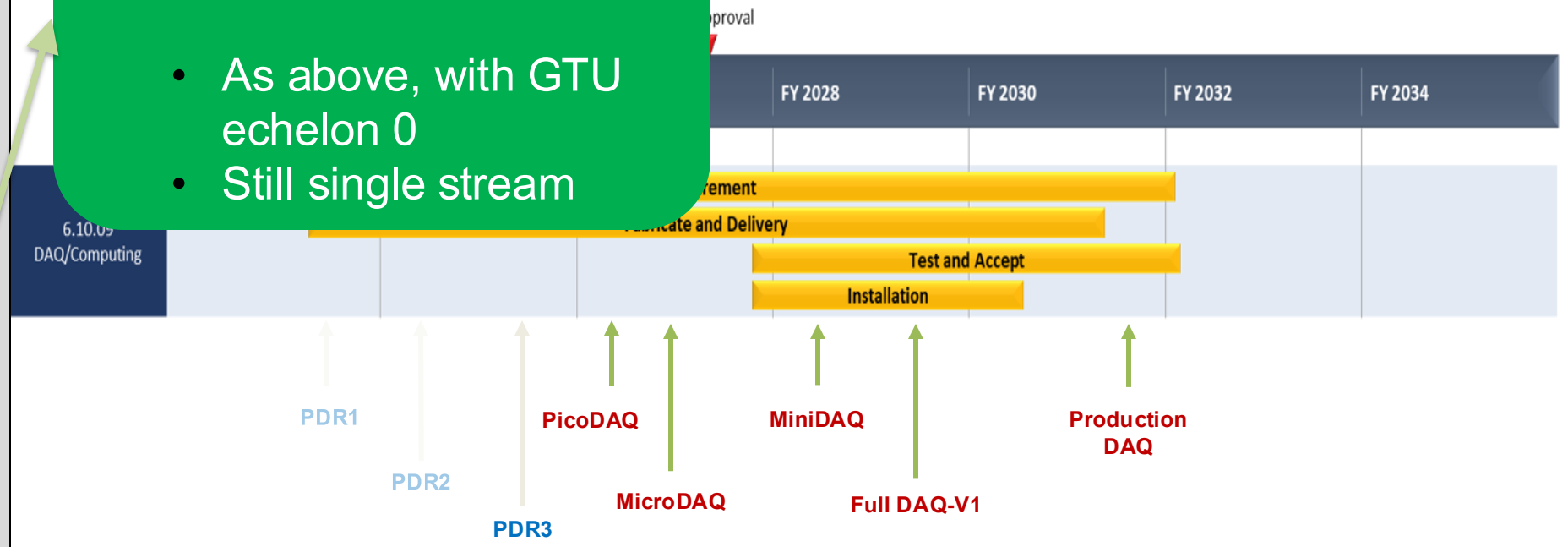
Readout detector data using full hardware and timing chain

Full DAQ-v1: FY29Q2
Full functionality DAQ ready for full system integration & testing

Production DAQ: FY31Q3
Ready for cosmics

"MiniDAQ" – Readout detector data using full hardware and timing chain

- As above, with GTU echelon 0
- Still single stream



Streaming DAQ Milestones

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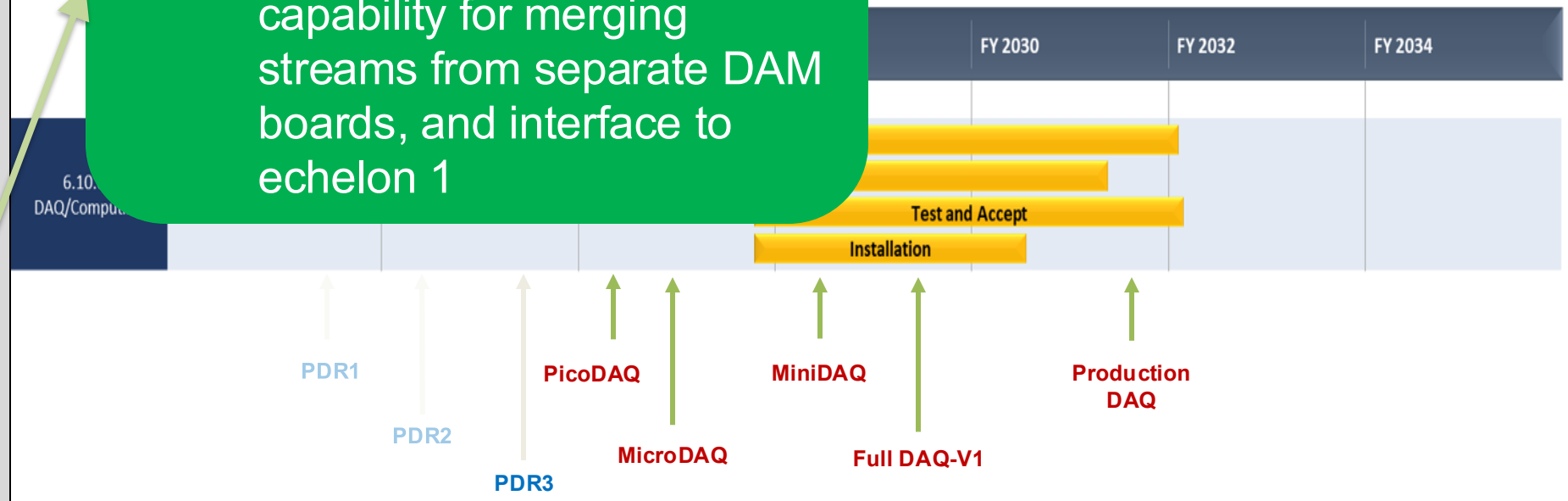
Full DAQ-v1: FY29Q2
Full functionality DAQ ready for full system integration & testing

Production DAQ: FY31Q3
Ready for cosmics

"FullDAQ-v1 – Full functionality DAQ ready for system integration

- Includes run control, capability for merging streams from separate DAM boards, and interface to echelon 1



Development Plan

PicoDAQ (Dec 2025)

- Same readout chain configuration used in 2024 test beams (IPBUS / Ethernet for data transmission and devoted setup for clock distribution) but using optical links (and possibly with prototype RDO).
- Definition of the RDO-DAM communication protocol and preliminary validation tests on a dedicated testbed integrating RDO/Alinx AXAU15/Felix-182.
  Given the complexity of the Felix firmware selecting one of the supported flavours would help greatly the completion of this process.
- Source control tagged software / firmware, documentation.

MicroDAQ (Sep 2026)

- Demonstrate the integration of RDO and DAM (probably still Felix-182 version) and GTU (if available, or use emulator).
- Source control tagged software / firmware, documentation.

Backup Slides