The ALCOR ASIC for the ePIC dRICH

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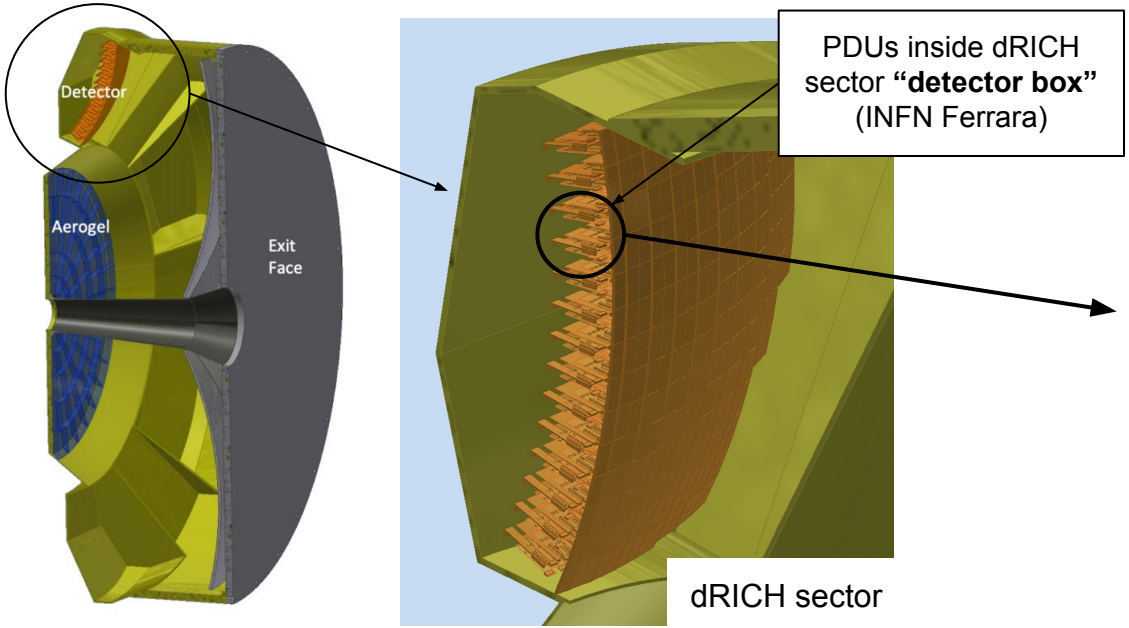
on behalf of the ALCOR group

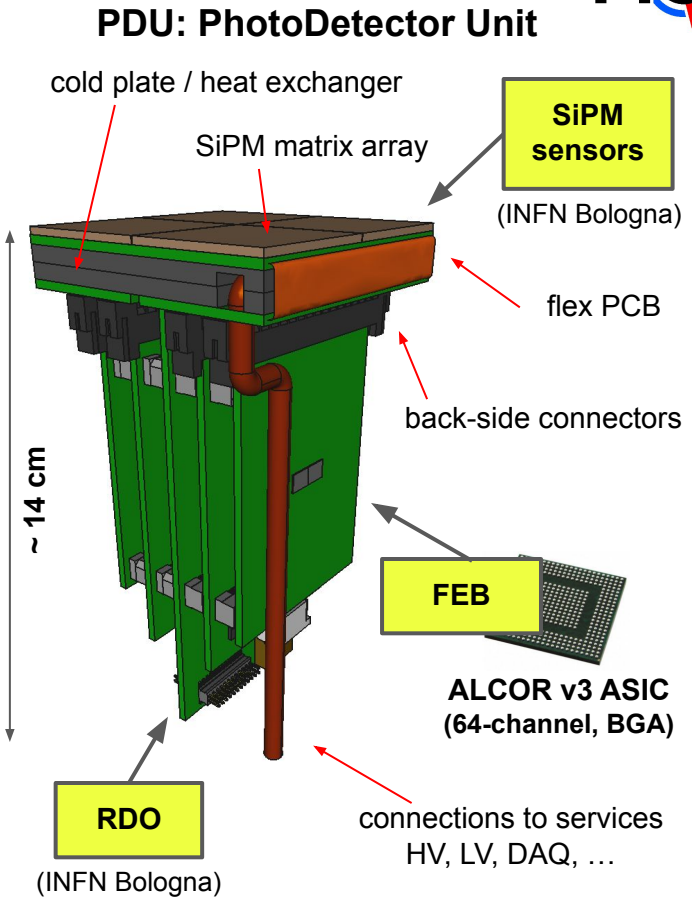
Giornate Nazionali ePIC Italia
Padova, 16-18 June 2025

Outline

- ALCOR ASIC requirements and architecture overview
- Main results from ALCOR v2
- ALCOR v3: design upgrades and BGA packaging
- ALCOR FEB
- Towards production and QA/QC
- Conclusions

dRICH electronics





- **1 PDU**: 4x64 SiPM array device (256 channels), **4 FEBs, 1 RDO**
- **1 ALCOR** (64 channels) per **FEB:** 8x8 SiPM matrix readout
- 6 sectors: 208 PDUs/sector → 1248 PDUs for full dRICH readout
- **4992 FEBs → 4992 ALCOR v3** (64-channel)
- **319488** readout **channels**

Motivation and status

Main requirements:

- Provide **single-photon time tagging** (**$\sigma_t \simeq 150$ ps**) of signals coming from SiPM sensors
- Cope with **SiPM DCR: 300 kHz/channel** (at max SiPM radiation damage)

ALCOR v2.0 - v2.1 (ALCOR-32)

- Extensively used within the dRICH Collaboration during 2023-25: lab tests, beam-tests, irradiation tests

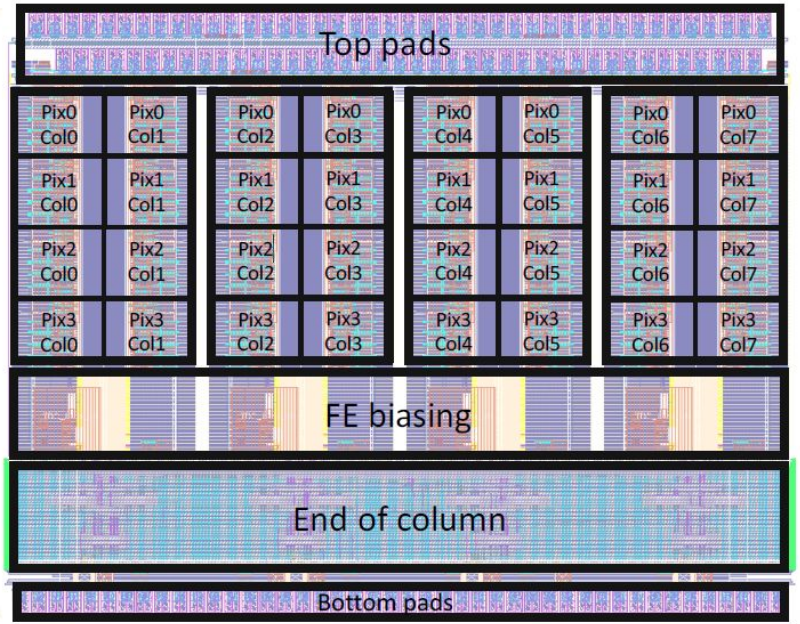
ALCOR v3 (ALCOR-64)

- First version to include all features and specifications required for the ePIC dRICH:
  - 64 channels, BGA package
  - Shutter + other EIC-driven features
- **MPW tapeout on Apr 8th 2025** (delay due to MPW run canceled by UMC: Nov 2024 → Apr 2025)
- Started production of **BGA substrate**
- Now adapting DAQ and test setups for new version, **electrical characterization** expected to start **this Fall**

ALCOR: **A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout

ALCOR-32 (ALCOR v2 - v2.1)

- **32-pixel** matrix (8x4) mixed-signal ASIC (4.95 × 3.78 mm^2)
- Single-photon time tagging + **Time-over-Threshold** or **Slew-Rate** measurements for **time walk correction**
- On-chip **signal amplification**, **conditioning** and **digitization**, 32-bit event word
- Trigger-less readout with fully digital output: **4 LVDS 320 MHz** DDR Tx links
- Power consumption **~10-12 mW/channel**
- **0.11 µm CMOS technology**



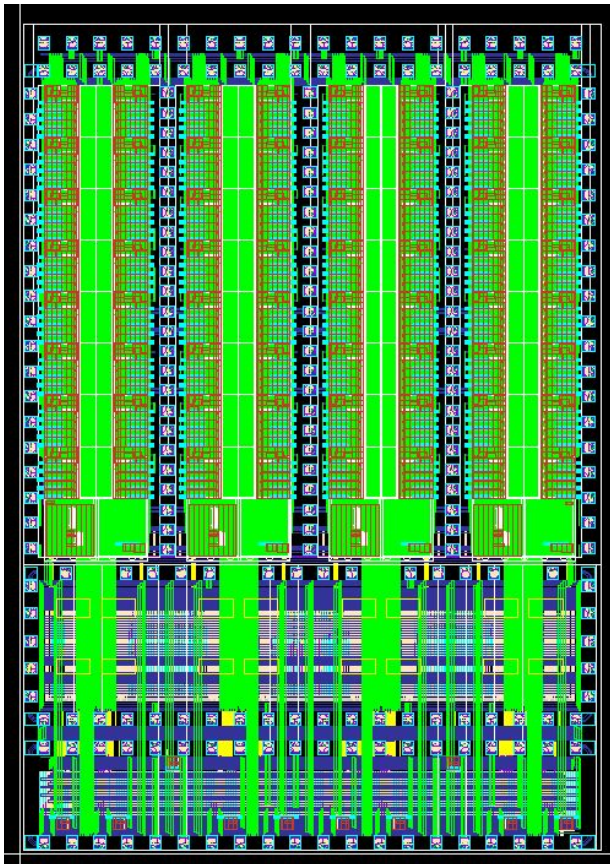
https://doi.org/10.1016/j.nima.2024.169817

ALCOR: **A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout

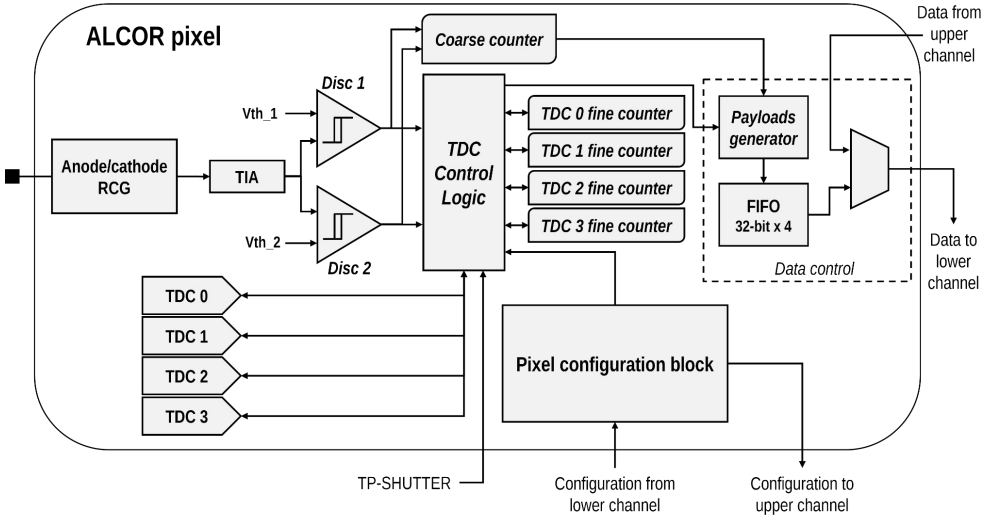
ALCOR-64 (ALCOR v3)

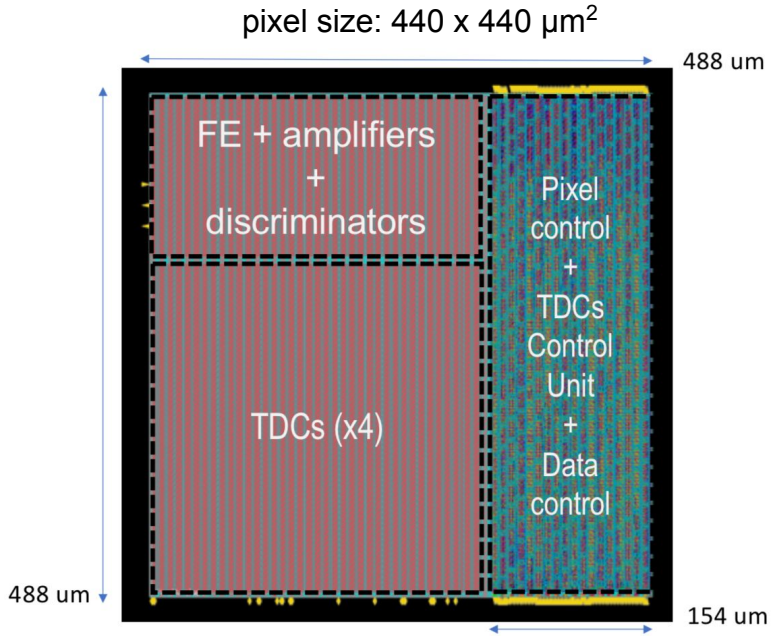
- **64-pixel** matrix (8x8) mixed-signal ASIC (4.95 × 7.02 mm^2)
- Single-photon time tagging + **Time-over-Threshold** or **Slew-Rate** measurements for **time walk correction**
- On-chip **signal amplification**, **conditioning** and **digitization**, 32-bit event word
- Trigger-less readout with fully digital output: **8 LVDS 394 MHz** DDR Tx links
- Power consumption **~12 mW/channel**
- **0.11 µm CMOS technology**

✓ **MPW tapeout on Apr 8th 2025**



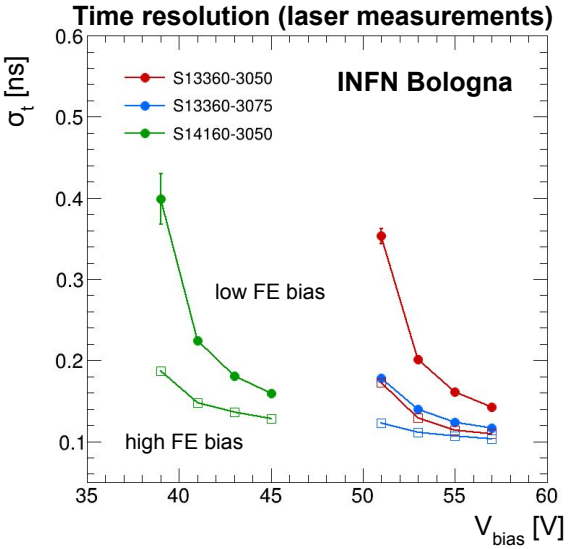
Pixel architecture

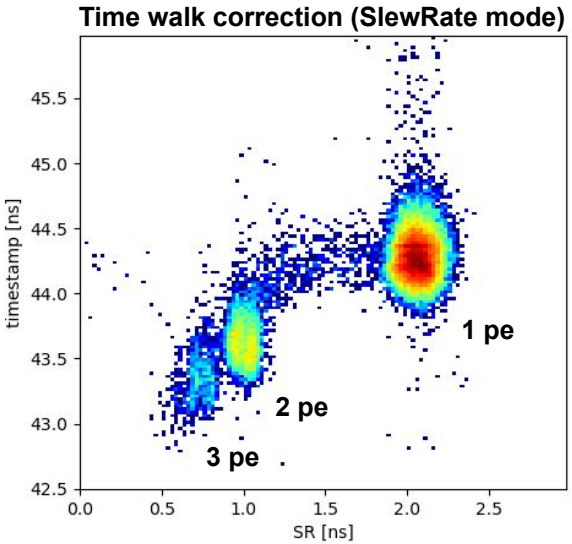


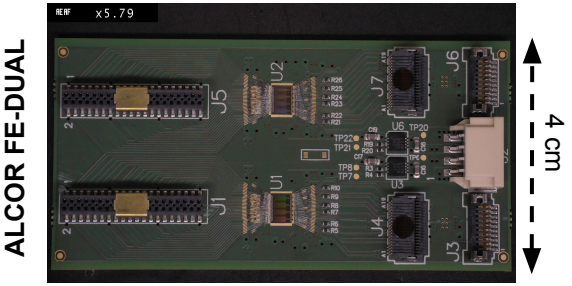


- **Dual-polarity RCG input stage** current conveyor (**Z_{in} = 10-20 Ω**) + **TIA** with 4 gain settings → **σ_t ≃ 150 ps**
- **2 leading edge discriminators** with independent (and per pixel) threshold settings (6-bit DAC) → **V_{th} = 0.5 p.e.**
- **4 TDCs** based on **analogue interpolation** with **20-40 ps** time-bin (at 394 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration, operating mode and data transmission
- TP-**Shutter** to inhibit events digitization (asynchronous with ns time window in **ALCOR-64**) and suppress out-of-time SiPM DCR hits

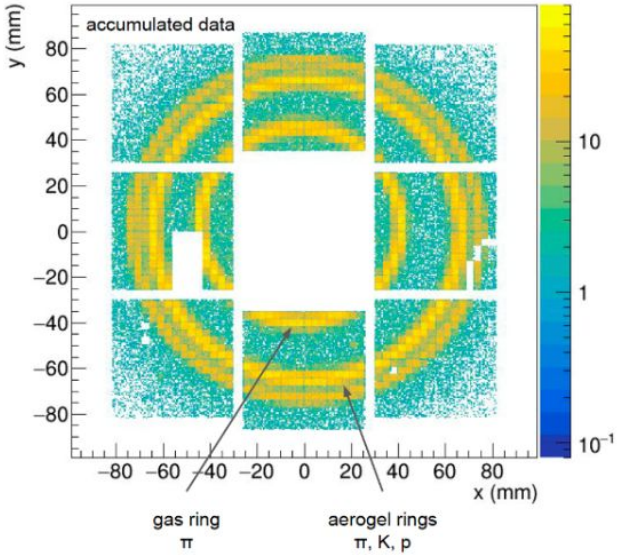
ALCOR v2 results







Beam test with prototype dRICH and PDUs (CERN-PS, May 2024)



- Better **time resolution** with 75 µm SPADs, comfortably below σ_t = 150 ps also at low V_{bias}
- **Time walk correction**: SlewRate mode provides good separation between afterpulses (slow-rise time, large ToT) and cross-talk (fast rise-time, large ToT)

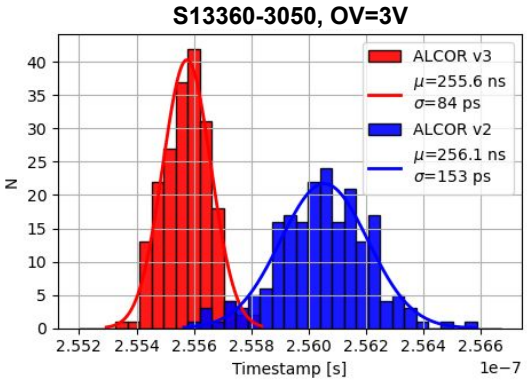
32 FE-DUAL (64 ALCOR, **2048 channels**)
SiPM: HPK **S13360-3050** and **S13360-3075** (3x3 mm^2, T = -30/-40°C)

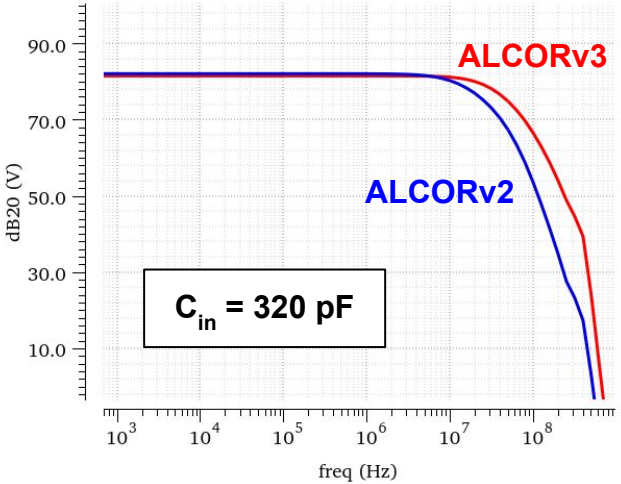
ALCOR v3 - analogue

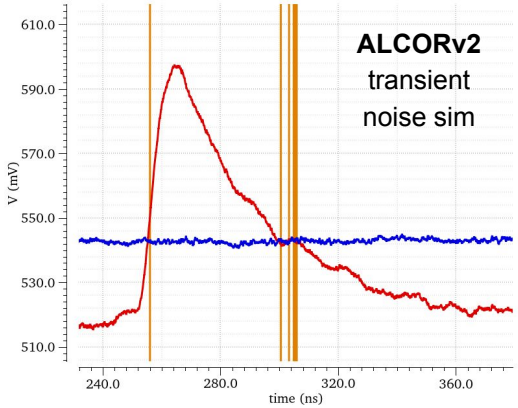
Small revisions on ALCOR FE design

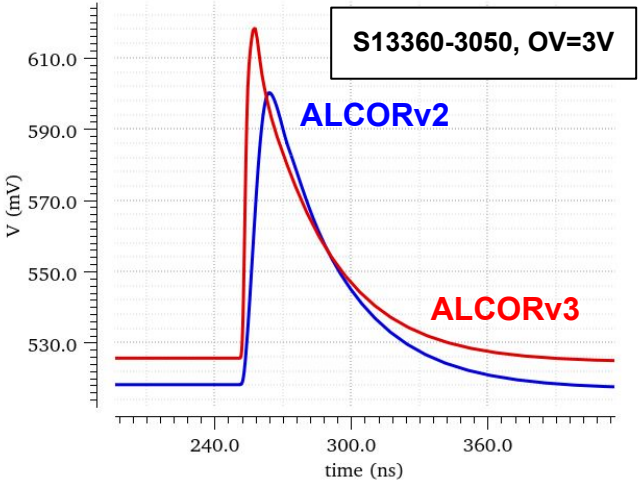
- **Increased amplifier bandwidth** to improve time resolution
  - transient noise simulations
  - Vth = 0.5 p.e.
  - **jitter: 153 ps → 84 ps**

- **Discriminator** with programmable **hysteresis** to avoid re-triggering on slow tail with low thresholds









ALCOR v3 - shutter

ePIC streaming data acquisition system (no traditional hardware trigger)

- Operation at **0.5 p.e. threshold** → DCR noise up to **300 kHz/channel** (at max SiPM radiation damage)
- **Digital shutter**: “inhibit” pixel digital logic to suppress out-of-gate DCR hits and **reduce data throughput**
- ~10.2 ns bunch crossing, ~300 ps bunch length, select **2-3 ns time window**
- Asynchronous digital shutter implemented in ALCOR v3 pixel logic using external test-pulse signal
- **Programmable delay chain**: 4 configuration bits at channel-level (LSB ≃ 350 ps) and at the chip periphery (LSB ≃ 100 ps) to adjust offsets between different pixels and columns
- Shutter needed only when DCR becomes higher due to SiPMs taking radiation damage over time → use first period of ePIC data taking to optimize **shutter calibration** (understand electronics and physics contributions)

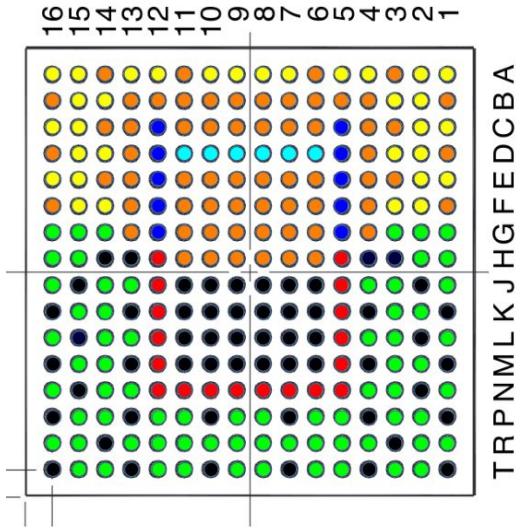
Possible problem of an **excessive data bandwidth** (**> 1 Tbps**) for the ePIC DAQ system when **DCR** approaches **300 kHz**. Two complementary approaches are being considered:

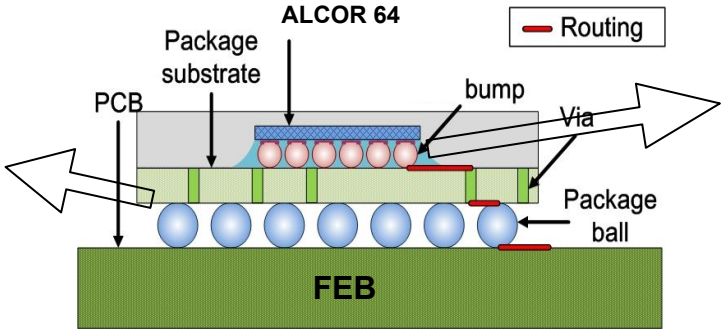
1. **dRICH interaction tagger** (INFN Genova): dedicated sub-detector (scintillating fibers + SiPM + ALCOR based readout) tagging relevant interactions → S. Vallarino talk
2. **ML online data filtering** (INFN Roma) at sub-detector level (FELIX DAMs) against pure dark-count event → C. Rossi talk

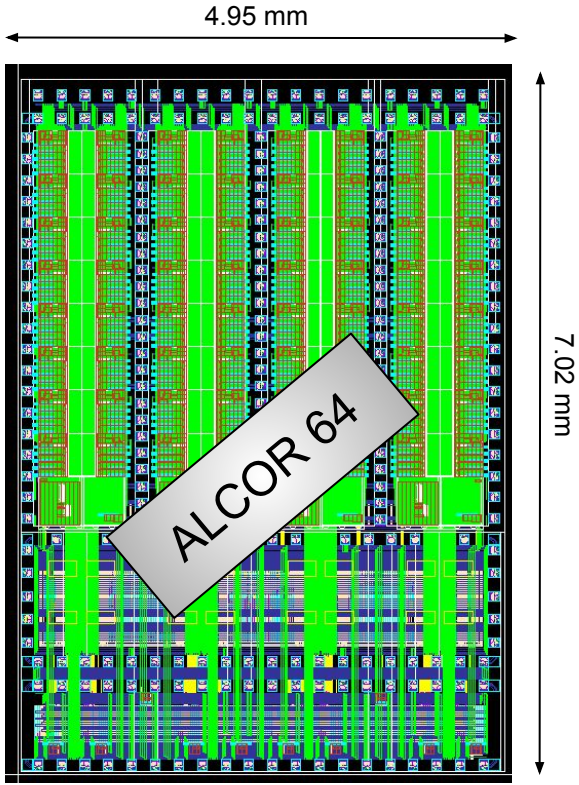
ALCOR BGA package

FC-BGA: flip-chip ball grid array

- BGA substrate designed by INFN Torino (M. Mignone)
- Substrate production, flip-chip assembly and packaging done by I-Tronics (https://www.itronics-sg.com/)



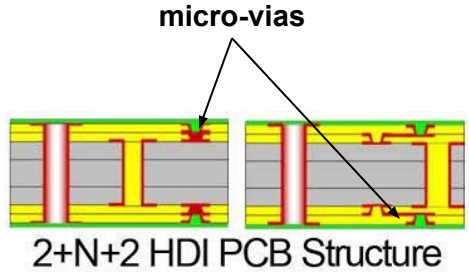


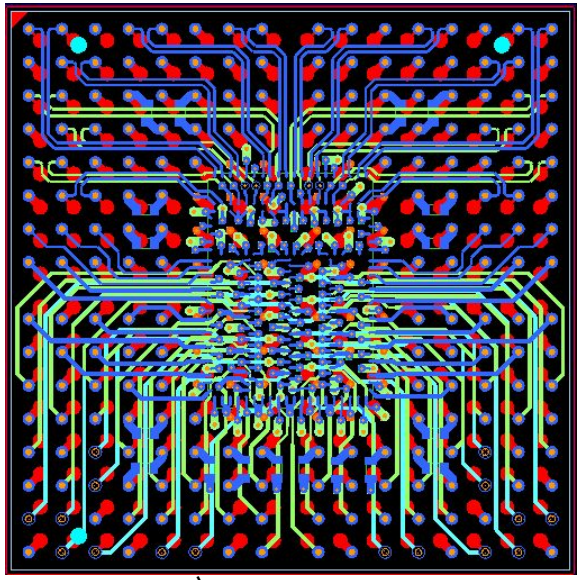


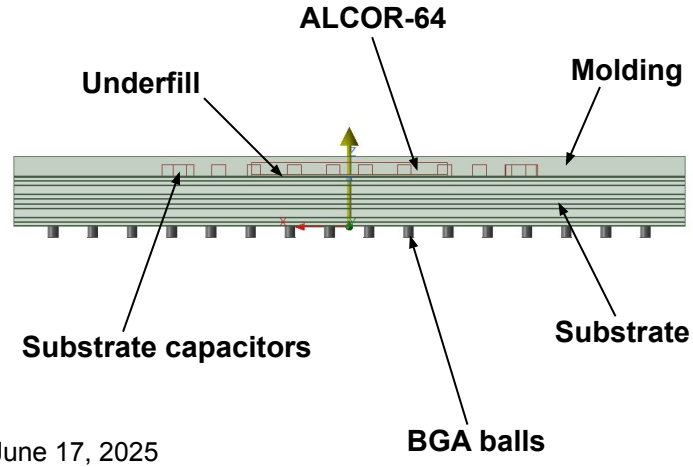
ALCOR BGA

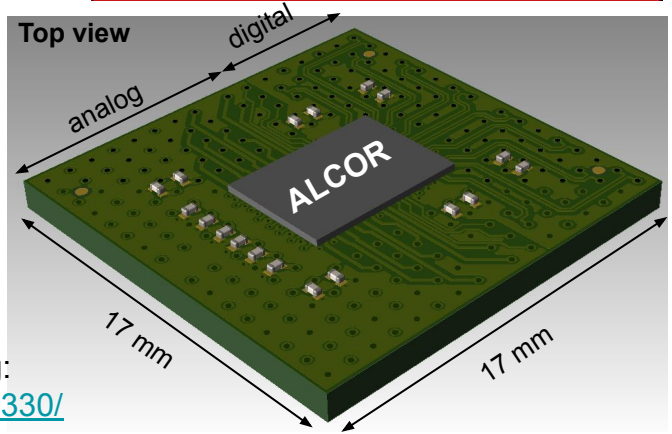
- BGA 256 Ball 17x17mm 1mm-pitch
- BT-Epoxy
- 10 Layers (2+N+2)
- Thickness: 1.27 mm
- Decoupling capacitors (0201)
- Design completed on Jan 2025
- Verification: electrical and thermal simulations

✓ **Sent for production on Apr 2025**





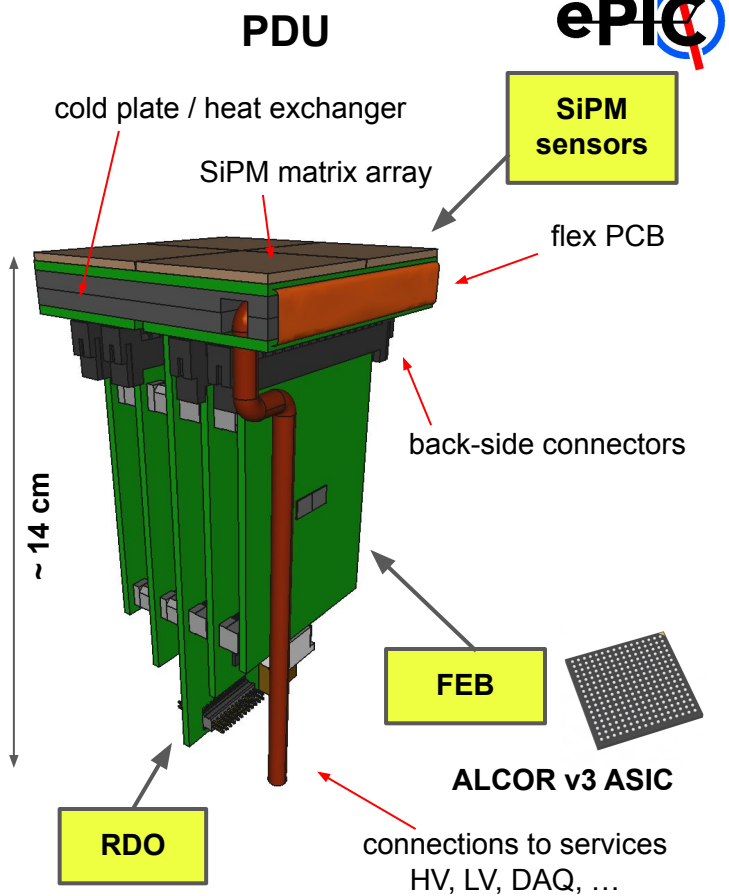




More details presented at the 12th Feb 2025 dRICH Meeting: https://indico.bnl.gov/event/26330/

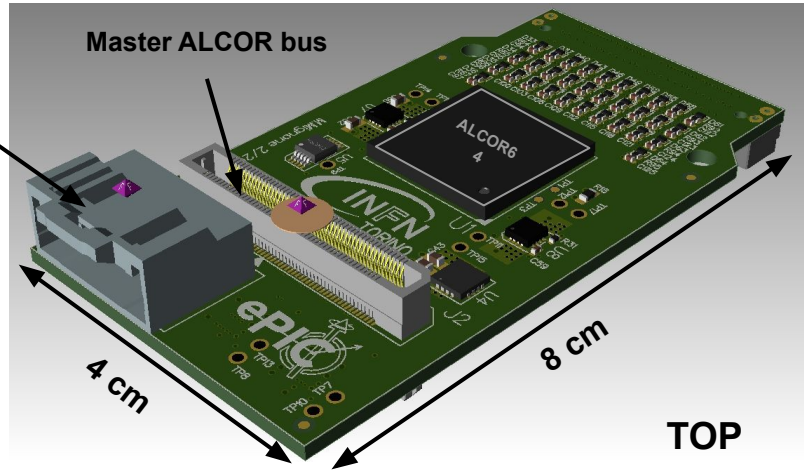
dRICH ALCOR FEB

- **4 FEBs** in each PDU (**256** readout **channels**), managed by **1 RDO** (INFN Bologna)
- FEB designed by INFN Torino (M. Mignone), close cooperation with Bologna-Ferrara colleagues to match *RDO design, SiPMs requirements* and *space constraints*
- 2 slightly different FEB versions, they share the ALCOR BUS connector (interface with RDO):
  - ***Master***: internal FEB
  - ***Slave***: external FEB

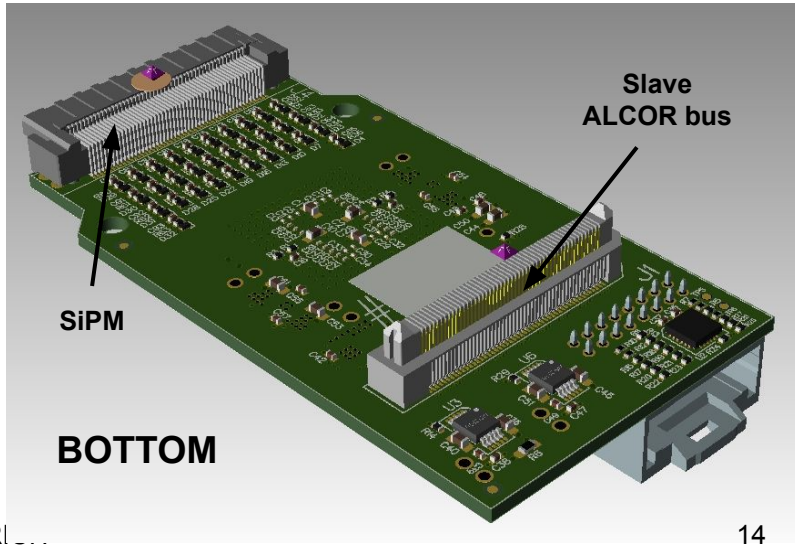


dRICH ALCOR FEB

- I-Tera MT40, 10 layers
- Connectors towards RDO (ALCOR bus), detector (SiPM carrier), off-detector (Services)
- Linear Regulators, current monitors, I2C expander, AC-coupling + annealing circuitry
- Power segmentation: LV → 64 ch., HV → 32 ch.



➢ Dedicated PCB section for SiPMs HV routing
  - 2 $V_{bias/annealing}$ PCB layers/sections, each serving 32 SiPMs
  - **SiPM online annealing**: forward-bias, **I = 60-100 mA** to reach **T = 150°C** on SiPM matrix board
  - Expected FEB temperatures **up to 100°C**
  - **Annealing diodes** to provide path to ground for SiPM annealing current → trade-off between C_{in} and power

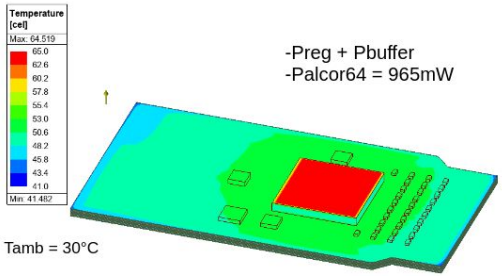


✓ **Design completed on May 2025**

Thermal simulations and SMA-annealing FEB

Preliminary and simplified thermal simulations of one FEB board during normal operations and while performing annealing embedded in a **static T = 30°C ambient** → need **simulations with realistic detector box cooling**

Normal mode (ALCOR ON)



-Preg + Pbuffer
-Palcor64 = 965mW

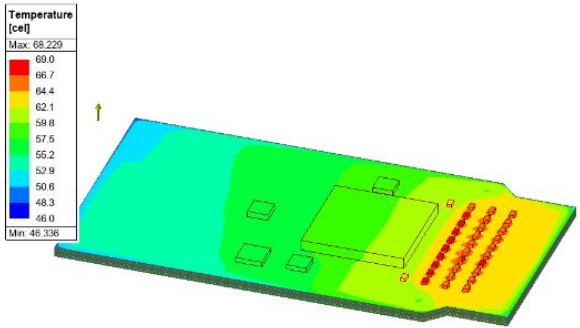
Tamb = 30°C

-BGA
Tj = 64.8 °C

-PCB(Top):
Tmax = 53°C
Tmean = 50°C

-PCB(Bot):
Tmax = 52.7°C
Tmean = 50°C

Annealing mode (V_f = 0.43 V @70°C x 60 mA → 26 mW)



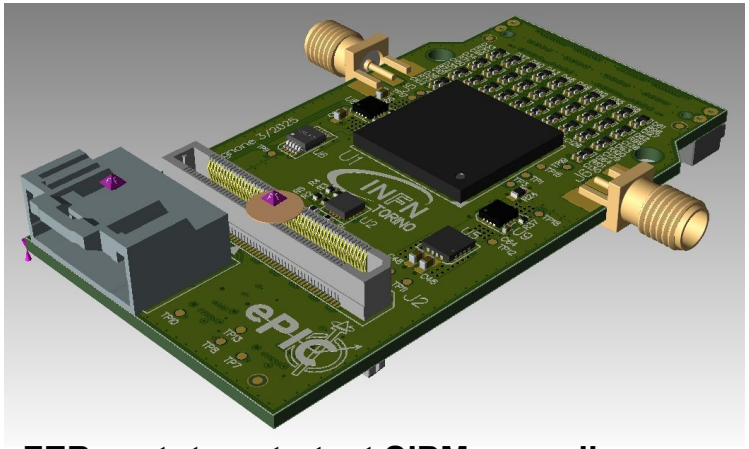
Tamb = 30°C

-DIODI:
64 x 26 mW
Tmax = 68°C

-BGA:
Tmax = 61°C
Tmean = 59°C

-PCB(Top):
Tmax = 67°C
Tmean = 57°C

-PCB(Bot):
Tmax = 68°C
Tmean = 57°C



FEB prototype to test SiPM annealing

- like final FEB, with all annealing circuitry
- added **2 SMA connectors** to inspect SiPM signals on scope → can be used also without ALCOR-64

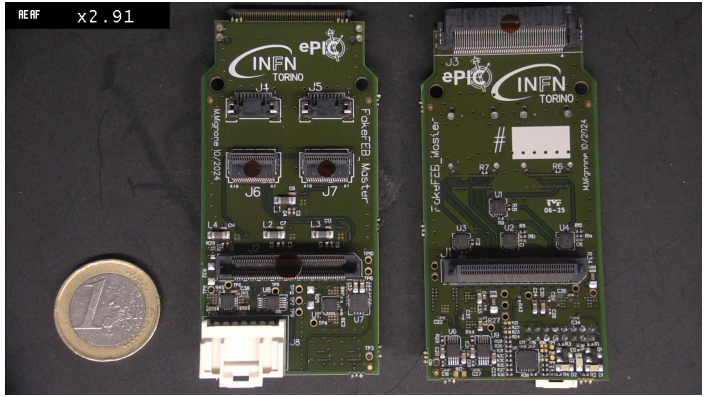
✓ **Purchase order issued 2-3 weeks ago**

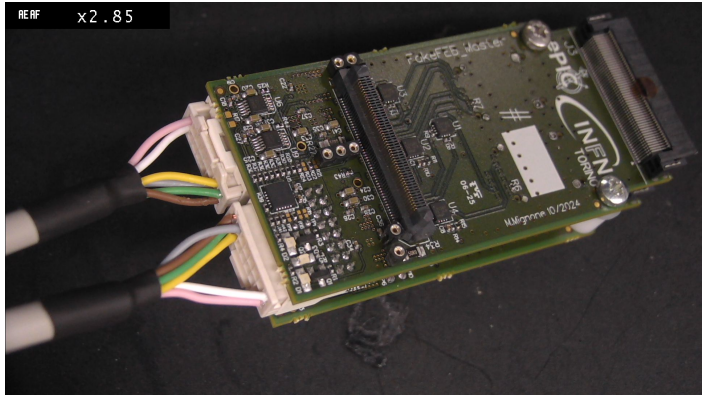
“Fake” FEB

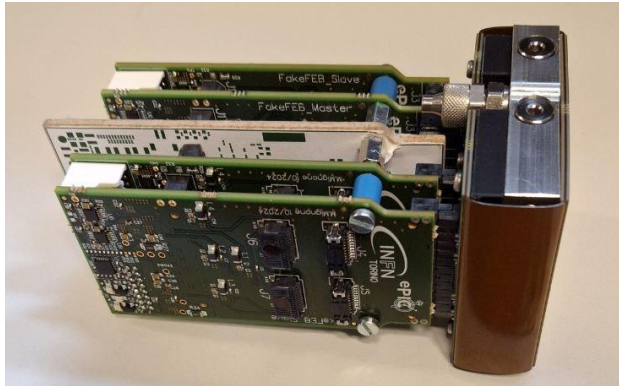
- Support **2025 dRICH activities** (Nov 2025 beamtest) when final FEB and ALCOR v3 are not available yet, allowing **test of RDO with current ALCOR-FE-DUAL** boards (with FireFly cables)
- Designed using specifications of final FEB: same space constraints, very similar components and same connectors (SiPM, RDO, and services)

✓ 10+10 “Fake” FEBs received mid March

✓ Assembly of first “Fake” PDU in Bologna last week







“Fake” PDU = 4 “Fake” FEBs + 1 RDO

Radiation tolerance

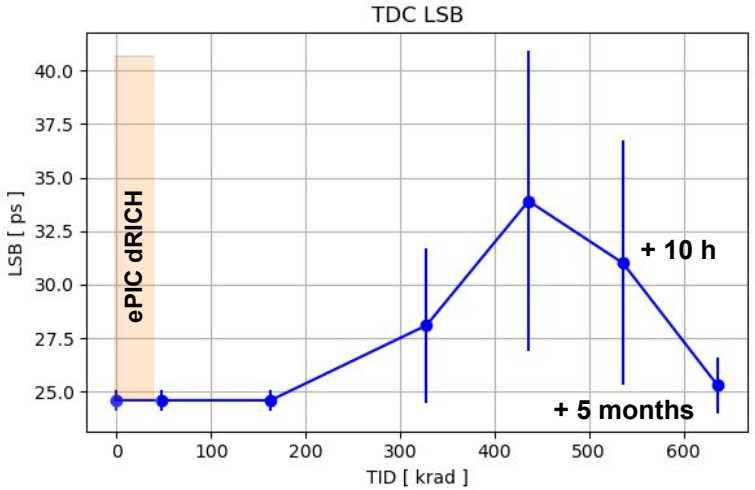
The dRICH-PDUs are in a moderately hostile radiation environment

- Φ (p+n > 20 MeV) = 200 Hz/cm^2
- TID ≅ 2.3 krad (for 1000 fb^{-1})

} safety factor of 5 included

➢ Irradiation tests campaign: SEU/SEL and TID tests at Centro of Proton-Therapy in Trento with ALCOR-32 in Jul 2024 and Dec 2024

- **Technology is sufficiently radiation tolerant** to be used in the ePIC dRICH environment
- **SEU rate is within the expected manageable levels**: in ALCOR v3 TMR SEU protection added also for periphery registers, Hamming code SEU protection for FSMs
- **Other FEB components need be tested and validated**



Detailed results presented at the 29th Jan 2025 dRICH Meeting: https://indico.bnl.gov/event/26313/

towards construction

2022
electronics v1

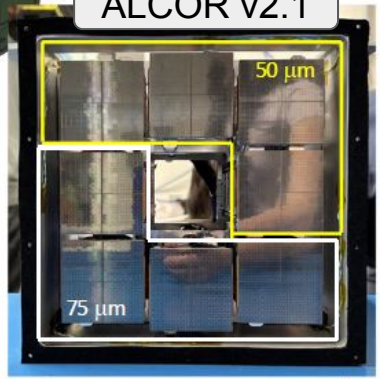
ALCOR v1

2023
electronics v2

ALCOR v2

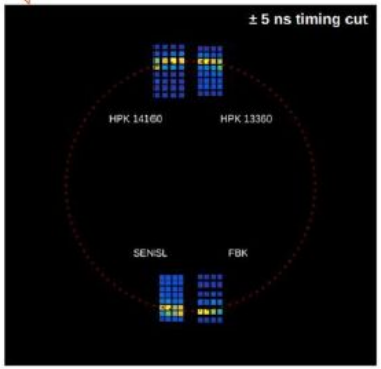
2024
electronics v2.1

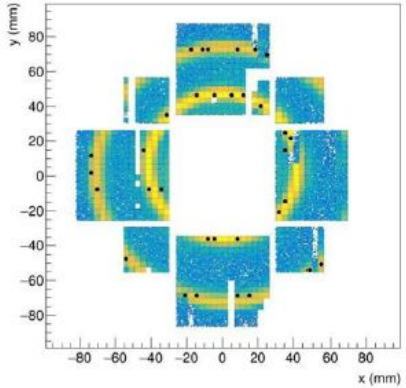
ALCOR v2.1

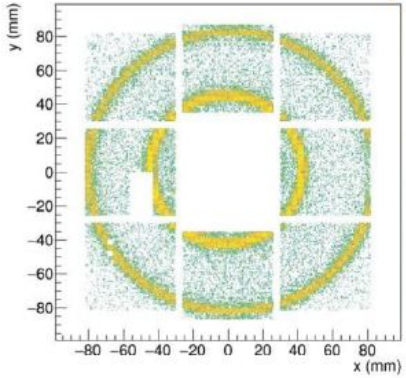


2025/26
electronics v3

ALCOR 32 ch







Full size engineering test article

2025 + SiPM carrierv3 + RDO

2026 + ALCOR 64ch + FEB 64

Next steps towards production

ALCOR-64 MPW tapeout on Apr 2025, 50 singulated dies expected for Sep 2025, then packaging

ALCOR-64 testing

- **End of 2025**: test ALCOR-64 from MPW → first **electrical characterization** in Torino
- **Start of 2026**: **tests with SiPM sensors** and RDO together with Bologna → fully assembled PDU
- Final validation at **beam-test during 2026**

Preparation for production

- Mid 2026: design revision

Start of production

- **End 2026 - Start 2027: Engineering run**

This is the **best case scenario**, we have contingency time for extra MPW run in 2026 and production during 2027

FEB and ALCOR are part of INFN IKC

- The whole production batch will be delivered in Italy for QA and integration, with fully assembled detector boxes shipped to BNL
- Updating quotations for ALCOR engineering run, packaging and FEB production

ALCOR QA/QC

QA is organized to allow essential acceptance tests on 100% of components plus in-depth sample characterization (1-2%)

- **Acceptance tests**: power-on, current absorption, configuration, data alignment, TDC scan, Vth scan
- **In-depth sample characterization**: SiPM DCR scan, laser measurements (jitter, shutter)
- Special test board card will be developed to test ALCOR standalone (also without RDO) and support readout of 1 SiPM matrix
- Different options are currently being evaluated: **in-house testing** (parallel QA stations) or **external company** (previous experience: CMS ECAL ASIC: 80k LiTE-DTU chips being tested by Microtest)
  - N. FEBs: 4992 → N. ALCOR: 4992 (increase number to include production phase risk mitigation)
  - 7500 ALCOR → 85% yield → 6375 ALCOR
  - **7500 ASIC · 8 min./ALCOR = 60000 min. = 1000 h → 30 weeks → 7-8 months**
- After **ALCOR/FEB validation**, FEB will be moved to **PDU assembly line**: FE electronics tested again after being integrated inside PDU (4 FEBs + 1 RDO + SiPM matrices)

Summary

- ALCOR is a 64-channel mixed-signal ASIC adopted for the readout of the SiPM sensors for the ePIC dRICH detector
- ALCOR has been extensively used within the dRICH Collaboration in the last 4-5 years: several laboratory and beam tests demonstrated the ALCOR-based readout capability to measure single photons with good time resolution and rate capability
- ALCOR v3 is the first version to include all features and specifications required for the ePIC dRICH:
  - 64 channels, BGA package
  - Digital shutter to reduce data throughput, 394.08 MHz clock frequency
  - ASIC tape-out in Apr 2025
- Upgrades of DAQ systems to test ALCOR-64 ongoing → define requirements for QA/QC setup

Backup Slides

Istituto Nazionale di Fisica Nucleare
SEZIONE DI TORINO

C. Alice, A. Bortone, M. Chiosso, F. Cossio, M. D. Da Rocha Rolo, G. Dellacasa, C. Ferrero, D. Giordano, M. Mignone, A. Rivetti, M. Ruspa, R. Wheadon

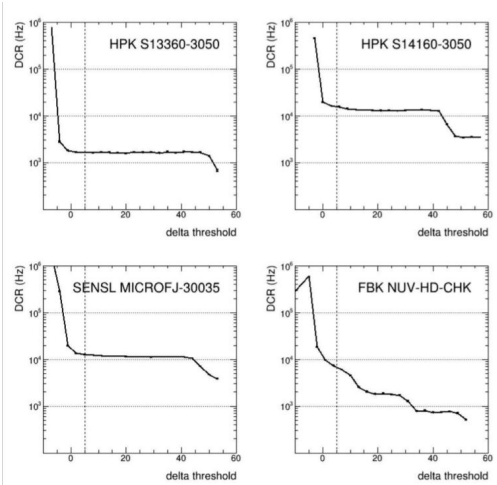
fcossio@to.infn.it

ALCOR v1

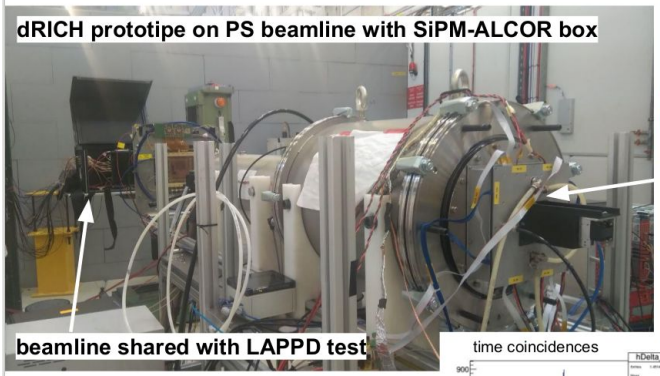
Developed by INFN for the readout of SiPMs at 77K, in the framework of Darkside (Dec 2019)

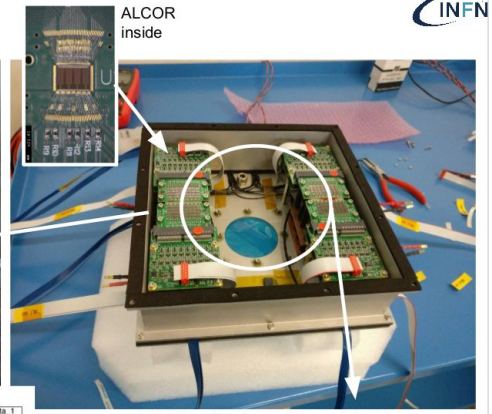
- Pixel matrix layout to explore solutions towards the development of an active silicon interposer for the integration of large area SiPMs for future massive frontier LAr Dark Matter Experiments

Extensively used within the EIC dRICH Collaboration during 2021-2022

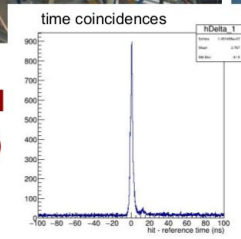


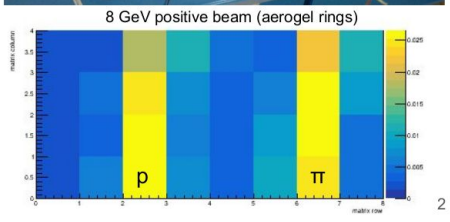
2022 test beam at CERN-PS





successful operation of SiPM
irradiated (with protons up to 10^{10})
and annealed (in oven at 150 C)





ALCOR v2

ALCOR v2

- MPW, submitted in Dec 2022
- 60 chips, received in **June 2023**
- **First version developed for ePIC**, includes new features targeted for ePIC dRICH and bug fixes:
  - ✓ TDC logic critical error at high rates solved also for DCR rate at room temperature
  - ✓ New FE gain settings more suited for single photon applications
  - ✓ On-chip test-pulse also for ePIC SiPM polarity
- Successfully validated in **2023 beam test**: 20 FE-DUAL (40 ALCOR v2.0, **1280 channels**)

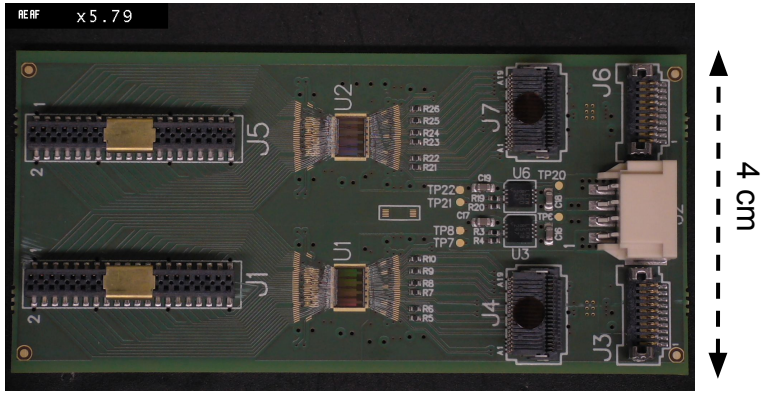
ALCOR v2.1

- INFN internal engineering run, chips received in **Jan 2024**
- Version currently used, includes small bug fixes w.r.t. ALCOR v2 (TDC Tfine ambiguity)
- Very high number of chips available to increase instrumented area for dRICH prototype and assemble other test setups
- Successfully validated in **2024 beam test**: 32 FE-DUAL (64 ALCOR v2.1, **2048 channels**)

dRICH prototype readout system

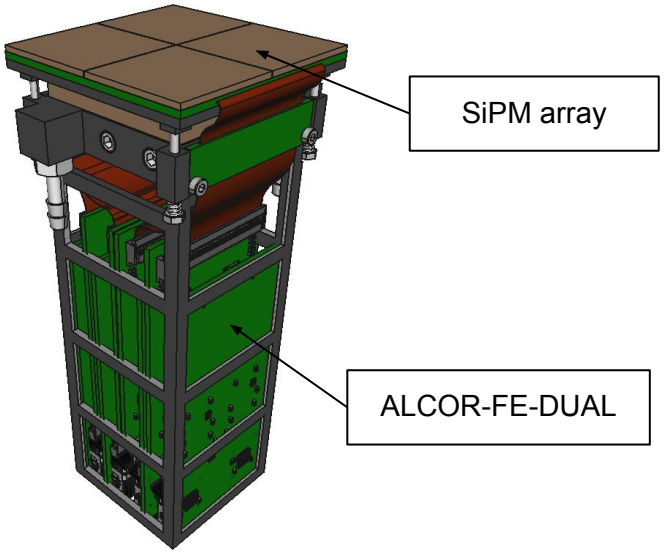
ALCOR-FE-DUAL board

- Two **32-channel** ALCOR ASICs **wire-bonded** on the PCB
- **4 ALCOR-FE-DUAL** boards for each PDU (**256 channels**)
- System used for **2023-2024** ePIC dRICH beam tests



Designed using specifications close to final FEB: very similar space constraints and same number of channels (64)

ePIC dRICH Prototype photodetector unit (PDU)



Prototype to test and validate PDU geometry and functionality (no RDO)

ALCOR v3 - digital interface

- Clock frequency: **394.1 MHz** (4x EIC clock: 98.52525 MHz)
- **8 LVDS Tx links**: one for each column, DDR output at **788 Mb/s**
- Data format
  - **32-bit words** with **8b/10b encoding** (2x event words in ToT/SR mode)
  - Frames with *header* + *data* + *trailer*
  - Frame duration set by *coarse counter roll-over* or *New Orbit reset*
- External **reset** with 3 different features depending on signal width:
  - 24-31 xCLK: ***Hard Reset***
  - 16-23 xCLK: ***Start*** (Frame Counter = 0 and Coarse Counter = 0)
  - 8-15 xCLK: ***New Orbit*** (Frame Counter +1 and Coarse Counter = 0) → forces a *rollover* condition (ALCOR rollover = 2^{15} clk cycles ≈ 83 μs, EIC orbit period ≈ 12.8 us)
- **Test Pulse**: analogue FE injection and TDC calibration; also used for **shutter** signal; propagated from EoC to each pixel
- **SPI** interface for registers configuration

FIFO position	Data (32-bit word)
1	K28.0 (Frame header)
2	Frame number
3 + …	Event words Column X
n	K28.2 (Frame trailer)
n+1	Frame info (frame_len, ev_lost)
n+2	*K28.3 (Status header)*
n+3	*Status words Column X (8x)*
n+11	*End of Column status word*
n+12	K28.4 (Checksum header)
n+13	CRC value

Summary of key differences between ALCOR versions

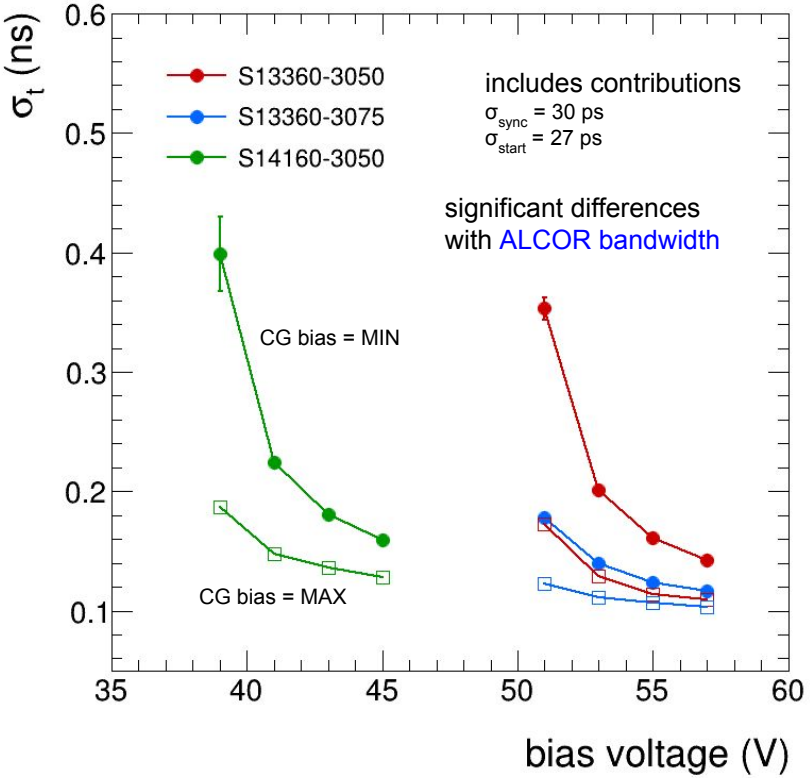
	ALCOR-32	**ALCOR-64**
Channels	32	64
Die size	4.95 x 3.78 mm^2	4.95 x 7.02 mm^2
Assembly	Wire-bonded on PCB	BGA package
Clock frequency	320 MHz	394.08 MHz
Time resolution	< 200 ps	< 150 ps
Shutter	synchronous, width > 100 ns	asynchronous, width ~ 2-3 ns
SEU protection	only pixels	pixels + EoC
Dataframe duration	2^{15} clock cycles	2^{15} clock cycles or user defined
Power consumption	10 mW/ch	12 mW/ch

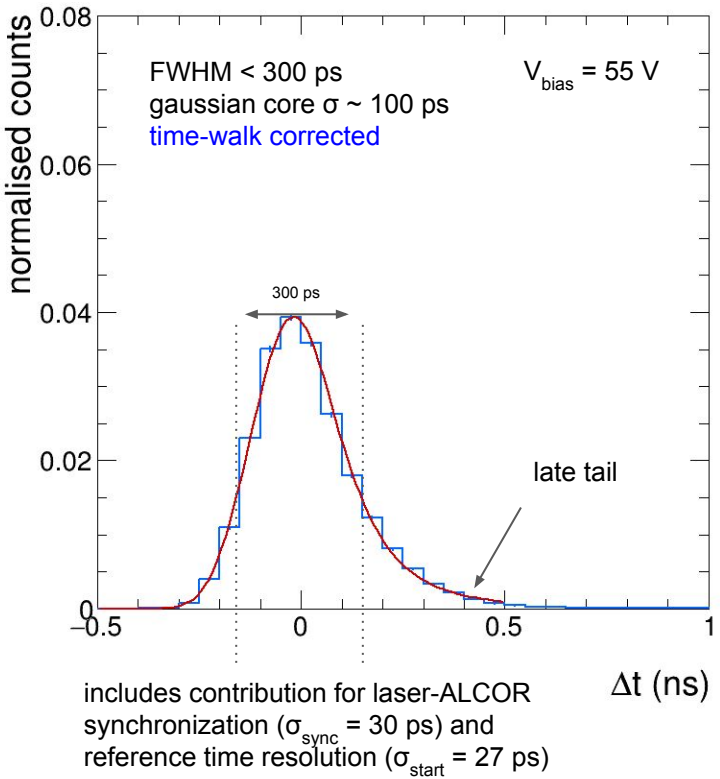
Summary of ALCOR specs for the dRICH detector

Function	Digitization from SiPMs with 1 p.e. sensitivity
Mode	Single-photon tagging or time and charge
Tech Node	110 nm CMOS
Channels	64 (8x8), dual polarity
Cdin	<1 nF
Digitization	20-40 ps TDCs, ToA + ToT; Timing < 150 ps
Shutter	Width: 2 - 3 ns, programmable latency
Input Rate	<2.4 MHz (up to 5 MHz on single channel)
Clock	394.08 MHz operation from BX 98.52 MHz
Links	788 Mbps LVDS, SPI configuration
Power	12 mW/ch
Package	BGA
Rad Tolerance	Radiation hard

→ 788 Mbps / (40 bits * 8 pixels) = 2.4 MHz
(assuming no extra control words)

Laser timing measurements





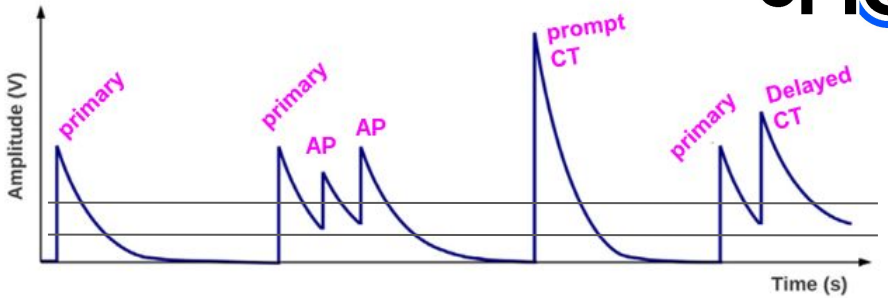
includes contribution for laser-ALCOR synchronization (σ_{sync} = 30 ps) and reference time resolution (σ_{start} = 27 ps)

➔ Better time resolution with **75 µm SPADs**

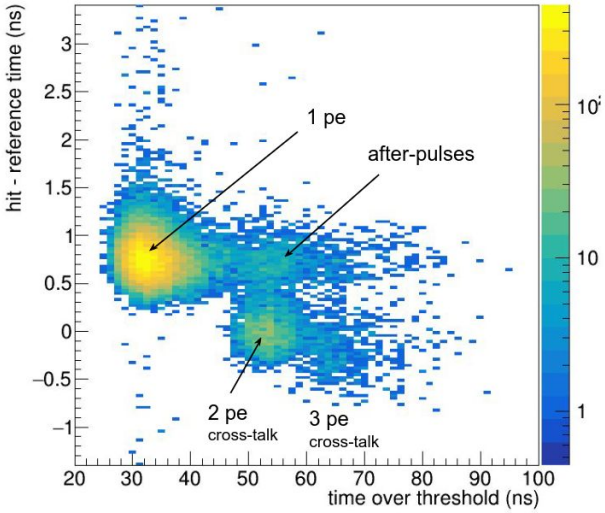
➔ Comfortably below **σ_t = 150 ps** also at low Vbias

Time walk correction

Time walk correction needed to improve overall time resolution → studies with laser setup using ***ToT*** and ***SlewRate*** measurements



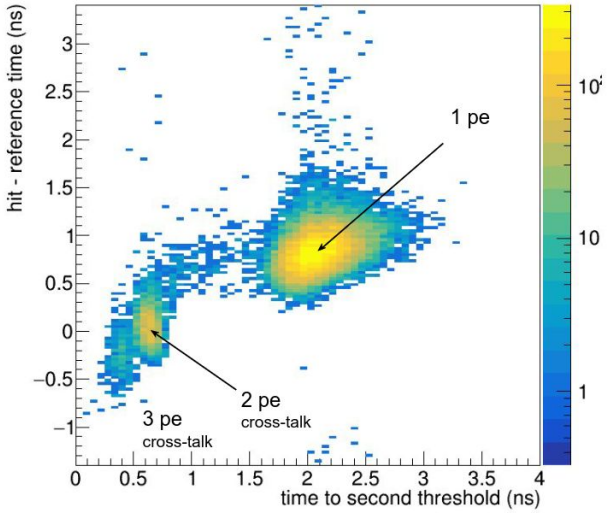
ALCOR ToT mode



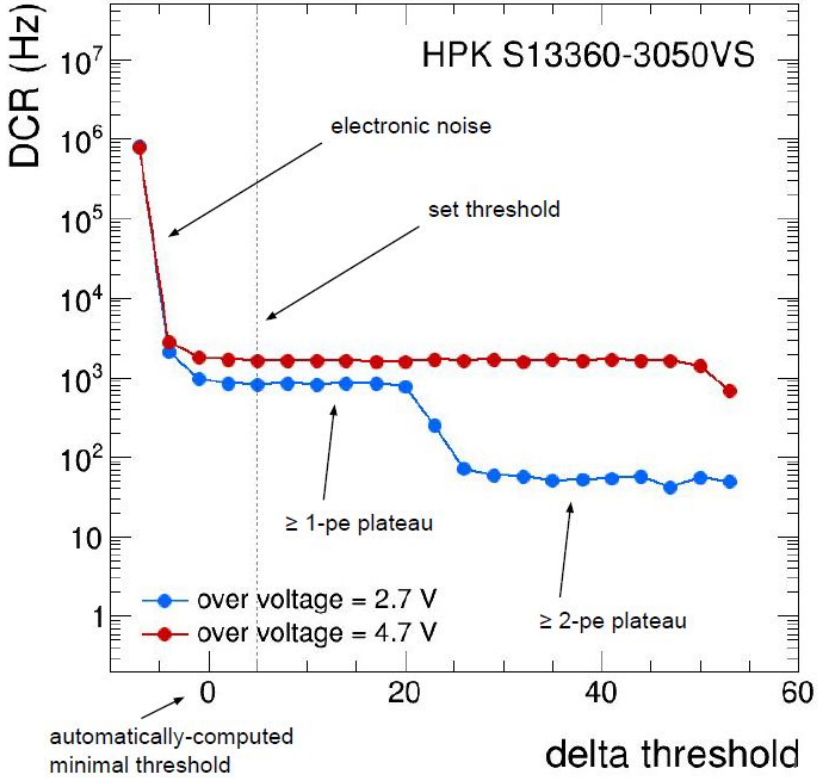
✗ ***ToT mode*** cannot distinguish between afterpulses (slow-rise time, large ToT) and cross-talk (fast rise-time, large ToT)

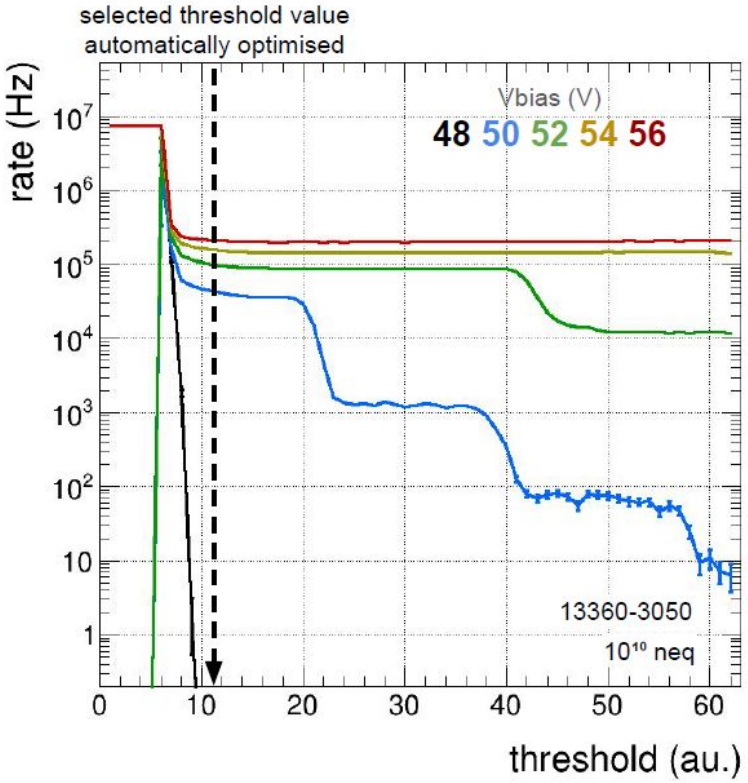
✓ ***SR mode*** provides better separation

ALCOR slew-rate mode



ALCOR threshold scan

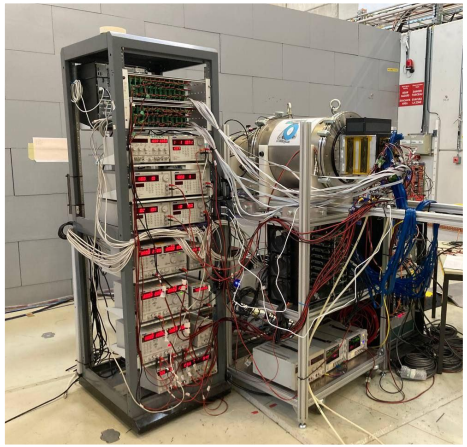


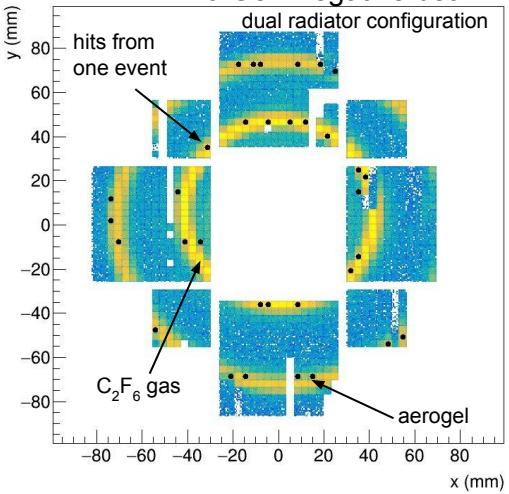


Beam tests at CERN-PS

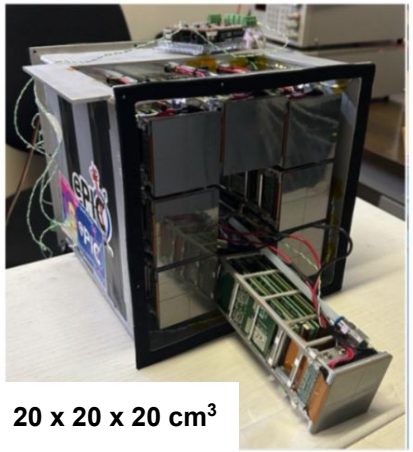
Successful beam tests with prototype dRICH and PDUs (CERN-PS, October 2023, May 2024)

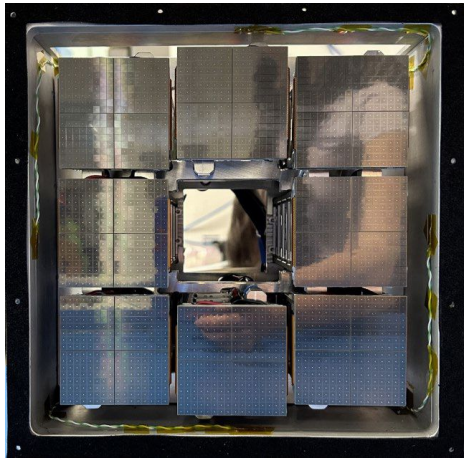
- HPK S13360-3050 and S13360-3075 (3x3 mm^2, T = -30/-40°C)
- 32 FE-DUAL (64 ALCOR v2.1, **2048 channels**)
- DAQ: Xilinx Kintex 7 KC705



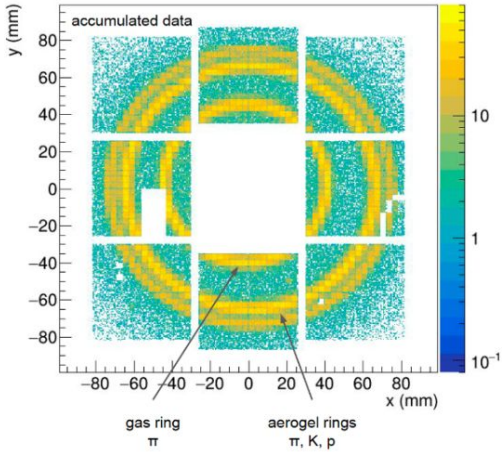


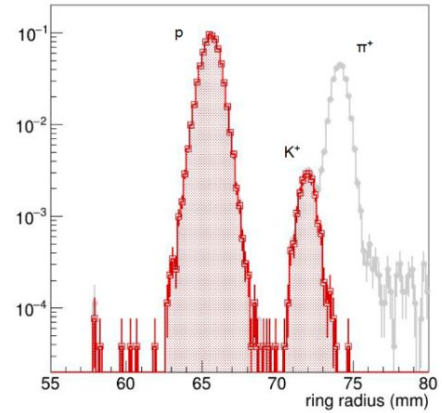
Realistic detector plane based on dRICH PDUs Validated



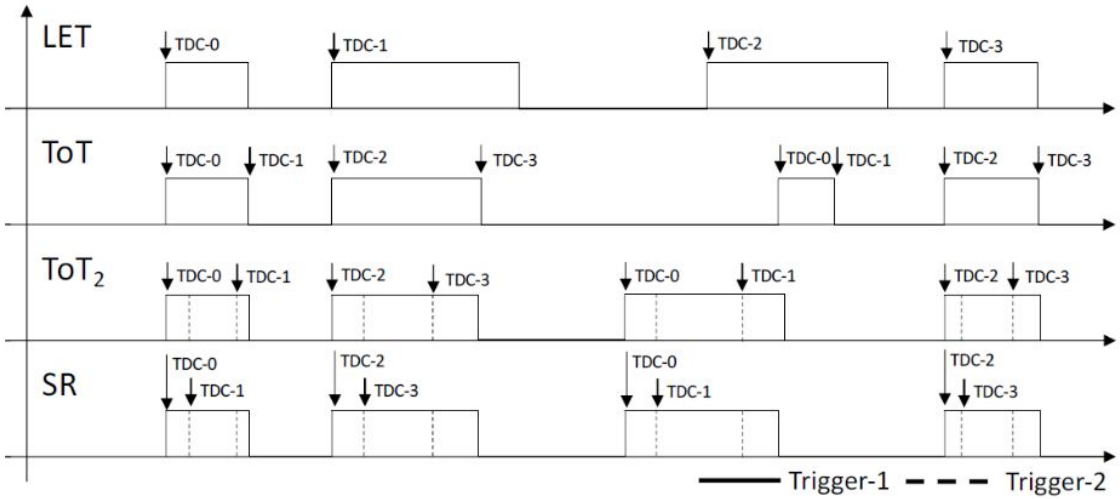


dRICH prototype got the expected performance and radiator interplay





ALCOR pixel operating modes



4 operating modes:

- **LET**: leading edge measurement
- **ToT**: Time-over-Threshold measurement using the first discriminator for both edges
- **ToT2**: Time-over-Threshold measurement using both discriminators
- **SR**: slew-rate measurement

Each mode can be set to:

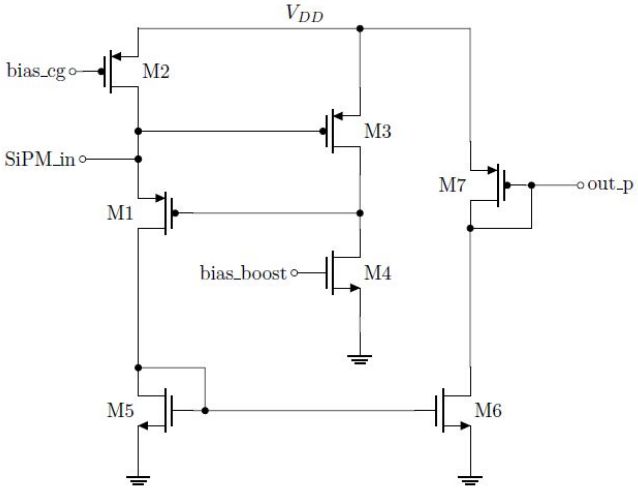
- **FE**: normal operation mode
- **FE_TP**: send test-pulse to analogue front-end
- **TDC_TP**: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

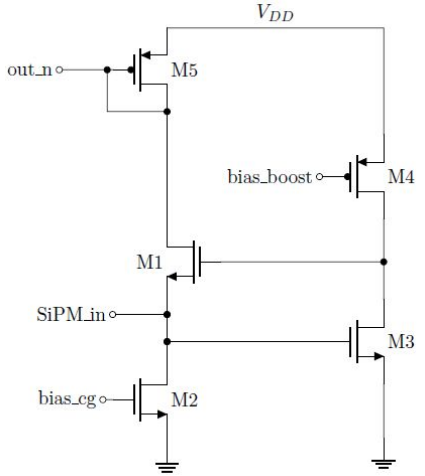
Each pixel can also be disabled

ALCOR Front-End

Input stage

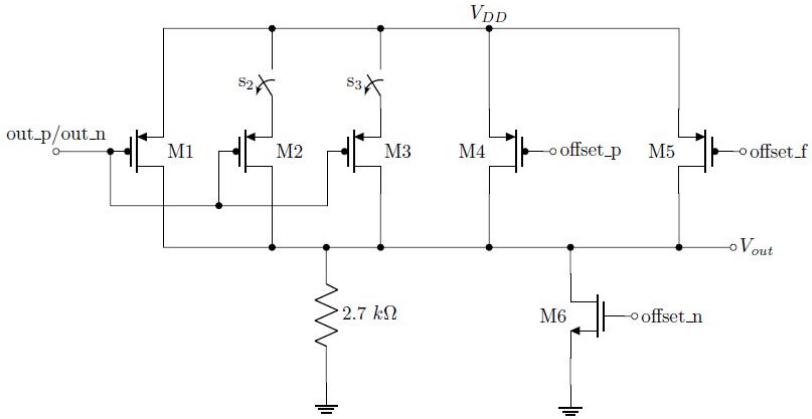
- Dual-polarity RCG current conveyor
- Programmable bias currents: CG (30-100 µA) and BOOST (1-4 mA)
- Z_{in} ~ 10-20 Ω





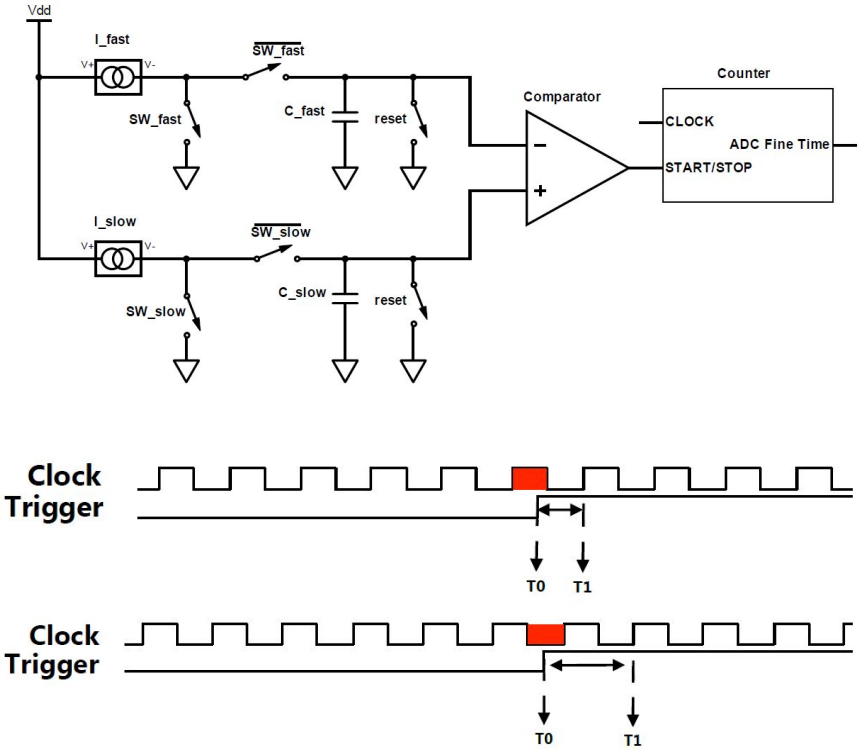
Output stage

- TIA gain: 2.7 kΩ
- 4 gain settings: 1/3, 4/3, 7/3 and 10/3
- DC coupled: baseline compensation based on gain and CG bias current settings + fine offset adjustment (3-bit)



Time to Digital Conversion

- Coarse time: 15-bit clock counter
- Time conversion performed by **TDC** based on **analogue interpolation** (9-bit fine time):
  - ***fast ramp***: constant current to charge C_{fast} → measure phase between event trigger and clock
  - ***slow ramp***: smaller constant current to charge C_{slow} → counts clock cycles until C_{slow} and C_{fast} are equal
- I.F. 64 or 128 → LSB = 20-40 ps @394 MHz
- Measured time interval: 0.5 - 1.5 clk period
- TDC conversion time: [160, 500] ns
- 4 TDCs per pixel for **event derandomization**



Shutter mixed-signal simulation

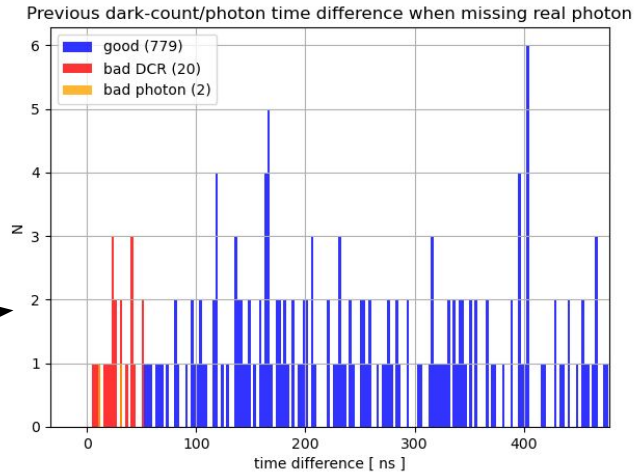
Shutter: periodic test-pulse (width = 2.5 ns)

Spectre netlist simulates different SiPM SPADs:

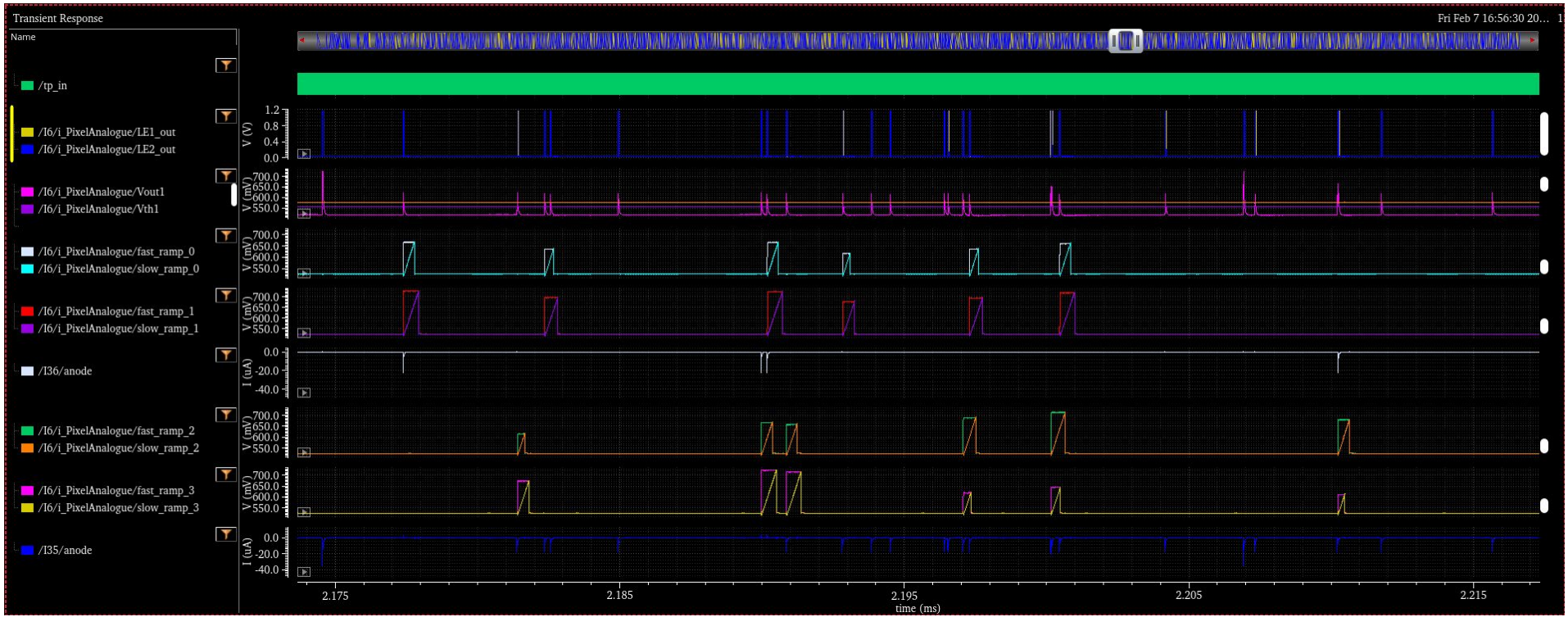
- Each **SPAD** is modeled with a current pulse generator, each with a different period
- **Real photons**: current pulse generators are synchronized with the shutter signal
- **Dark-count signals**: current pulse generators are not synchronized

Decode data, calibrate TDCs (from DCR asynchronous signals), extract ToA, compare with input netlist to evaluate shutter efficiency:

```
Total simulation time = 19532690.640 ns
Total number of dark counts = 10006
Dark count rate = 512.269 kHz
Dark counts cut by shutter: 8411
Dark counts passed through shutter: 1595
Shutter cut: 84.06%
Good events: 842
Missing events: 22
Efficiency: 97.45%
```



Shutter mixed-signal simulation (SlewRate mode)



Shutter efficiency vs DCR (mixed-signal sim)

- Shutter width = 2.5 ns
- Input rate = 20 kHz
- Sim time = 20 ms

Ongoing: digital simulations (with improved DCR and photons signals model) to verify shutter distribution for the whole ALCOR chip and provide better statistics

```
Total simulation time = 19989730.664 ns
Total number of dark counts = 811
Dark count rate = 40.571 kHz

Dark counts cut by shutter: 650
Dark counts passed through shutter: 161
Shutter cut: 80.15%

Good events: 409
Missing events: 1
Efficiency: 99.76%
```

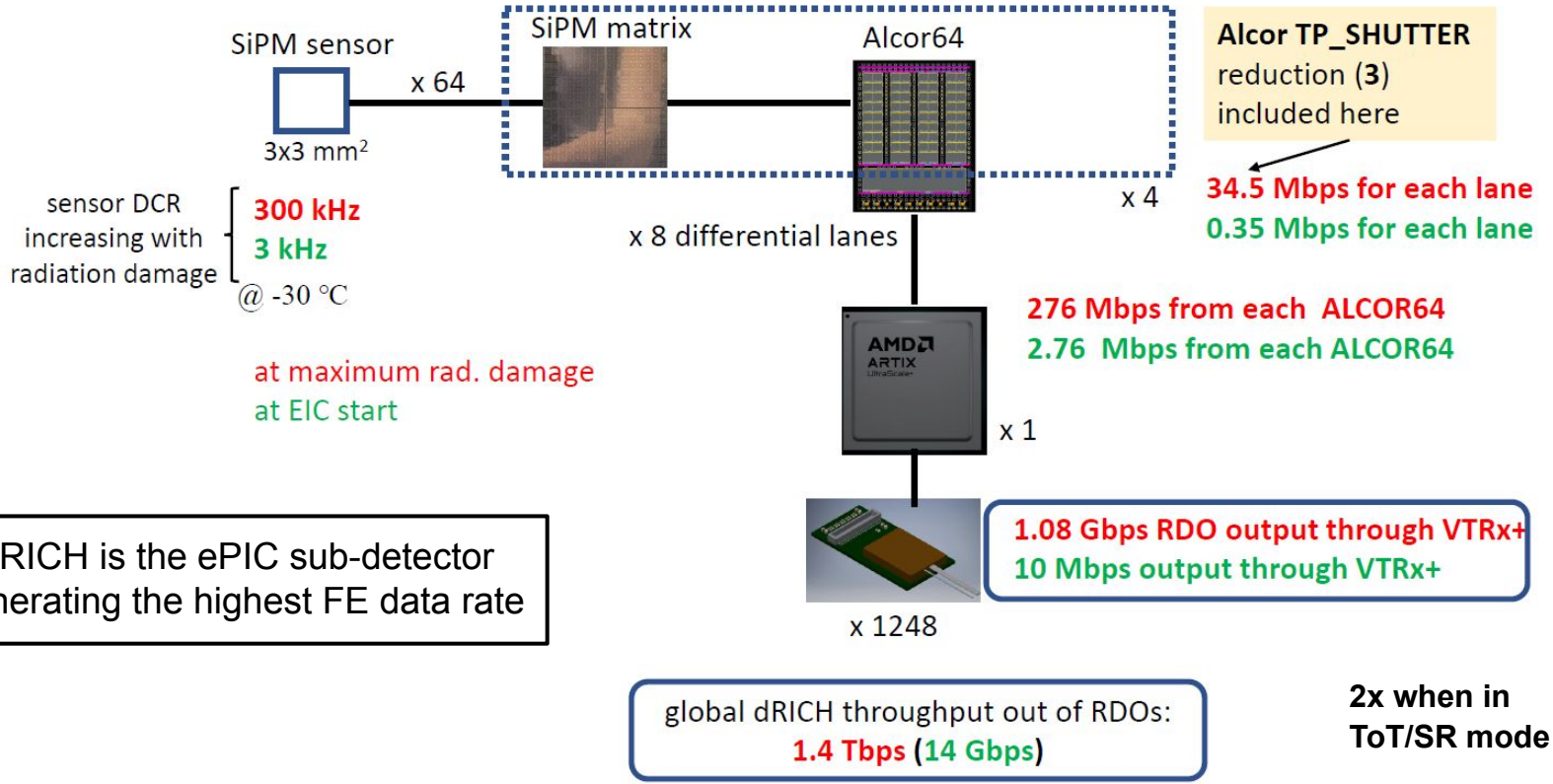
```
Total simulation time = 19962950.756 ns
Total number of dark counts = 1604
Dark count rate = 80.349 kHz

Dark counts cut by shutter: 1309
Dark counts passed through shutter: 295
Shutter cut: 81.61%

Good events: 413
Missing events: 3
Efficiency: 99.28%
```

```
Total simulation time = 19427451.802 ns
Total number of dark counts = 3082
Dark count rate = 158.641 kHz

Dark counts cut by shutter: 2546
Dark counts passed through shutter: 536
Shutter cut: 82.61%

Good events: 388
Missing events: 2
Efficiency: 99.49%
```

```
Total simulation time = 19996870.504 ns
Total number of dark counts = 6325
Dark count rate = 316.299 kHz

Dark counts cut by shutter: 5286
Dark counts passed through shutter: 1039
Shutter cut: 83.57%

Good events: 412
Missing events: 7
Efficiency: 98.33%
```

```
Total simulation time = 19532690.640 ns
Total number of dark counts = 10006
Dark count rate = 512.269 kHz

Dark counts cut by shutter: 8411
Dark counts passed through shutter: 1595
Shutter cut: 84.06%

Good events: 842 (was 40 kHz)
Missing events: 22
Efficiency: 97.45%
```

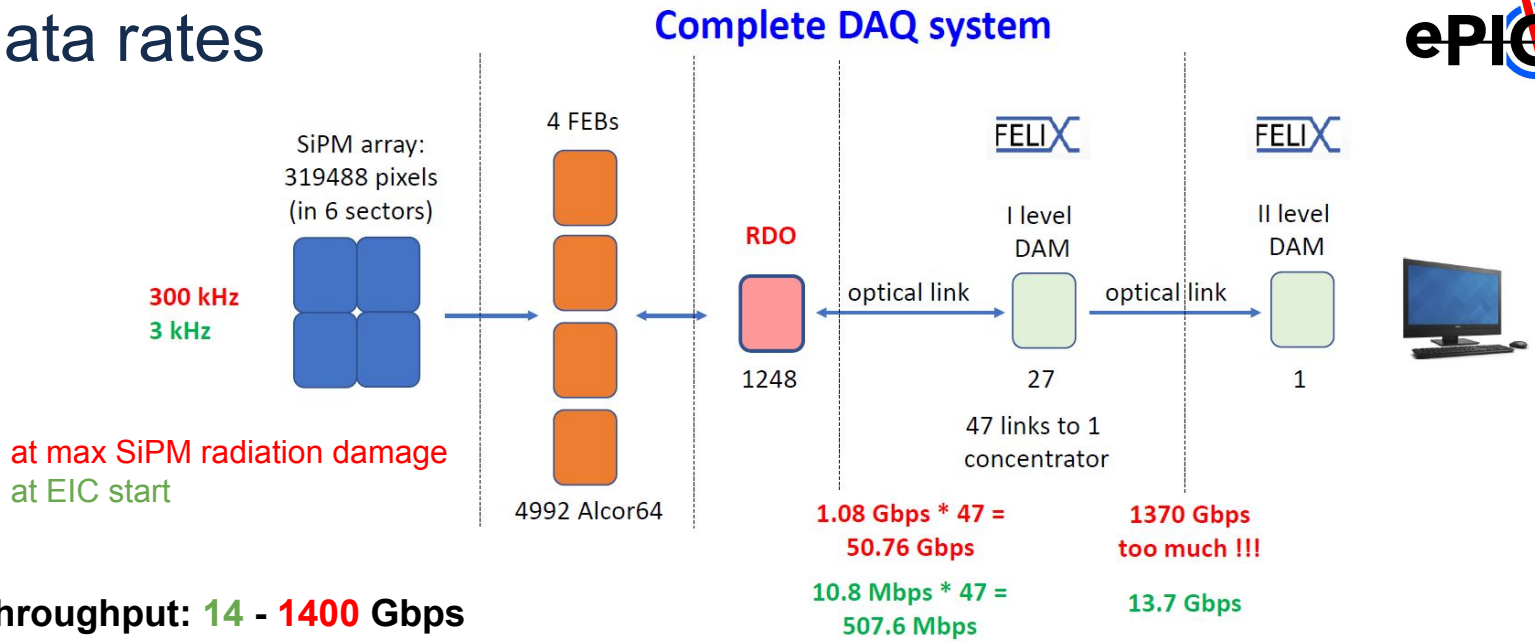
Data throughput from sensor to RDO optical link



dRICH is the ePIC sub-detector generating the highest FE data rate

The dRICH DAQ system has to be able to cope with such data rates: 14 Gbps ←→ 1.4 Tbps

dRICH data rates



Full detector throughput: 14 - 1400 Gbps

Possible problem of an excessive data bandwidth for the ePIC DAQ system when DCR = 300 kHz.
Two complementary approaches are being considered:

1. **dRICH interaction tagger** (INFN Genova): dedicated sub-detector (scintillating fibers + SiPM + ALCOR based readout) tagging relevant interactions
2. **ML online data filtering** (INFN Roma) at sub-detector level (Felix DAMs) against pure dark-count event

Power consumption

Estimated power consumption: **~12 mW/ch → < 1 W/chip**

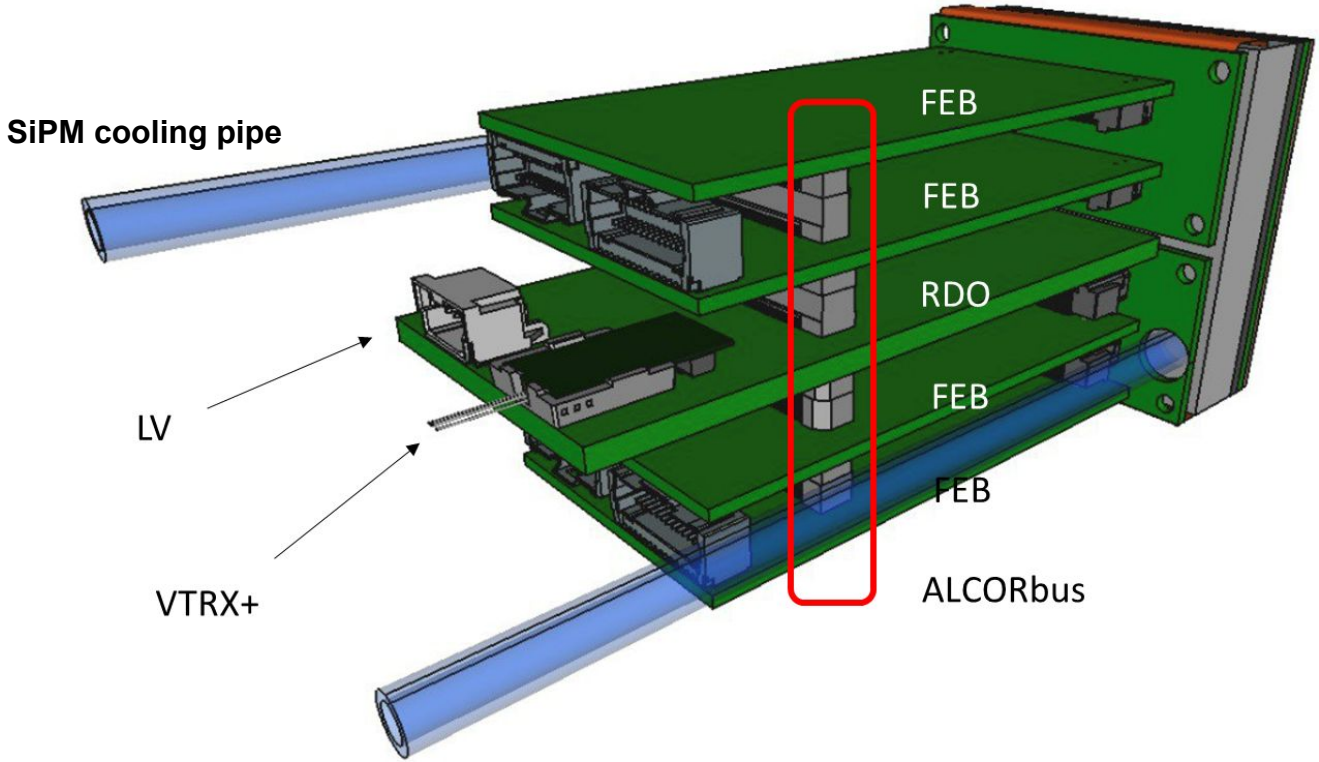
ALCOR requires 3 different power supplies

- **AVDD**: **1.2 V** analogue core (<500 mA)
- **DVDD**: **1.2 V** digital core (~275 mA)
- **DVDDIO**: **2.5 V** digital IOs (~80 mA)

Generated on the FEB using LDO linear regulators (V_{in} = **1.4 V** and **2.7 V**)

✓ dRICH ALCOR **FEB design completed**: already including services for LV (analogue and digital VDD, linear regulators, current monitors, connectors towards off-detector power supply distribution boards), more details in next slides

dRICH photodetector unit (PDU)



ALCOR FEB

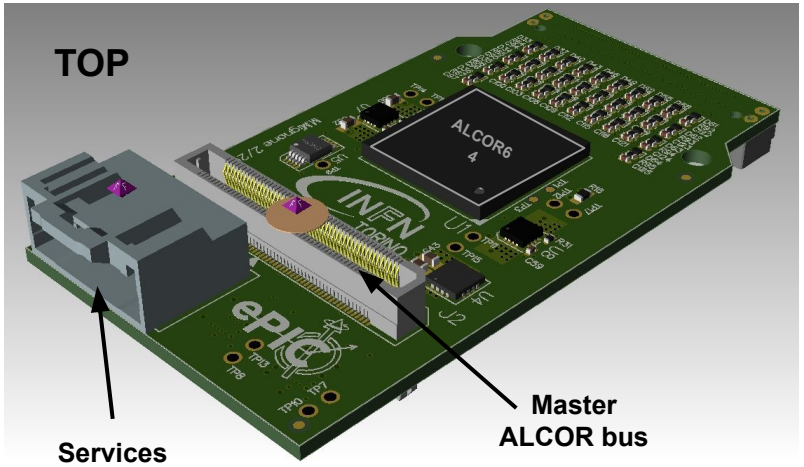
Connectors:

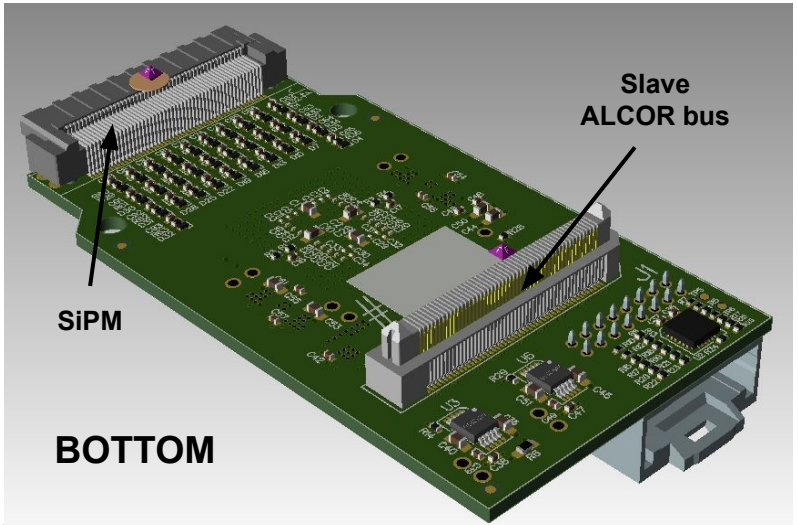
- **Master ALCOR bus** (between RDO and 1st FEB, LVDS signals): *Samtec ERM5-050-04.0-L-DV-TR*
- **Slave ALCOR bus** (between 1st and 2nd FEB, LVDS signals): *Samtec ERF5-050-05.0-L-DV-K-TR*
- **Services connector** (SiPM $V_{bias/annealing}$, ALCOR LV, SiPM NTC sensor, 16 pins, max 2 A each): *Molex 2086591640*
- **SiPM connector** (SiPM signals, V_{bias} and $V_{annealing}$): *Samtec LSHM-150-01-L-RH-A-N-K-TR*

➢ Dedicated PCB section for SiPMs HV routing

- 2 $V_{bias/annealing}$ PCB layers/sections, each serving 32 SiPMs
- **SiPM online annealing**: forward-bias, **I=60-100 mA** to reach **T=150°C** on SiPM matrix board
- FEB to support **T up to 100°C**

- Material: **I-Tera MT40**
- N layers: **10**





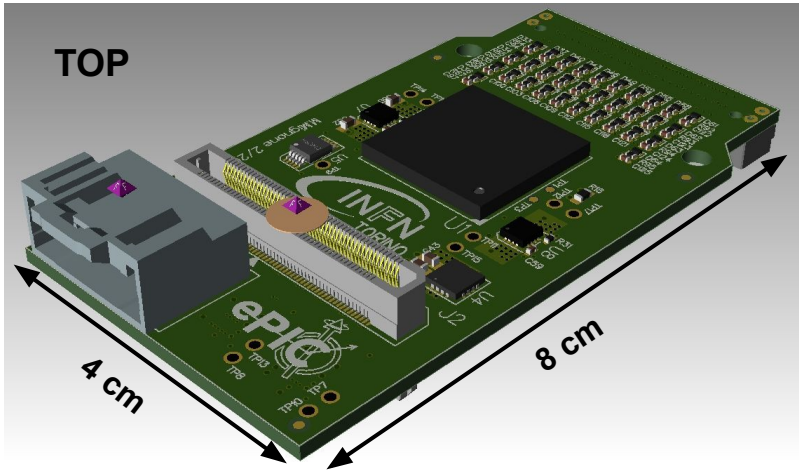
ALCOR FEB

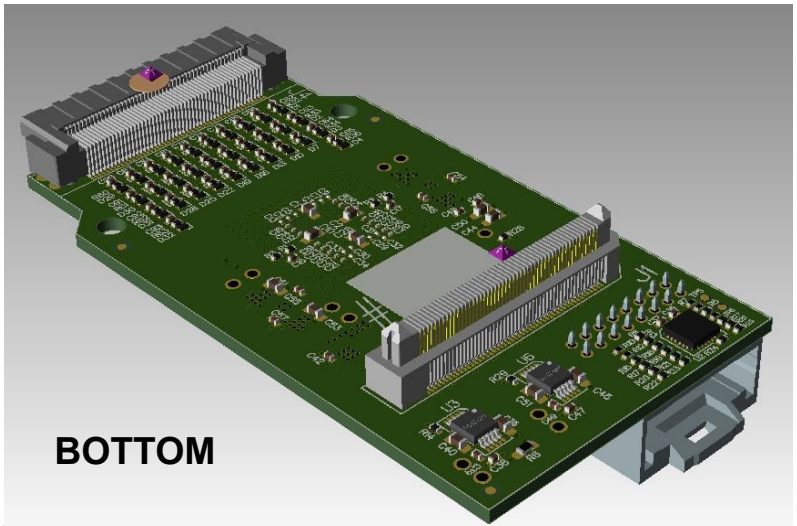
Main components:

- **Linear Regulators** (2.5 V DVDD_IO, 1.2 V DVDD, 1.2 V AVDD): *Analog Devices ADP1752ACPZ-2.5-R7, ADP1761ACPZ-R7*
- **Current monitors** (before regulators): *Microchip Technology MIC2040-1YMM-TR*
- **I2C to Parallel-Port Expander** (RDO can read/control regulators and current monitors): *Texas Instruments PCF8575RGER*
- **RC high pass filter** (AC-coupling between SiPMs and ALCOR) + **annealing circuitry** (diodes)

Power segmentation:

- LV: 64 channels
- HV: 32 channels





Annealing + AC coupling circuit

AC coupling circuit

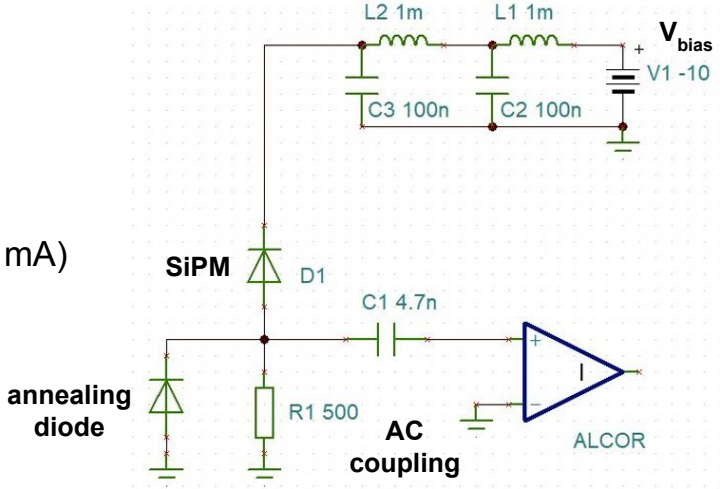
- cut SiPM signals tail
- protect ALCOR input from SiPM current during annealing

Annealing diode

- provide path to ground for SiPM annealing current (up to 100 mA)
- trade-off between C_{in} and power

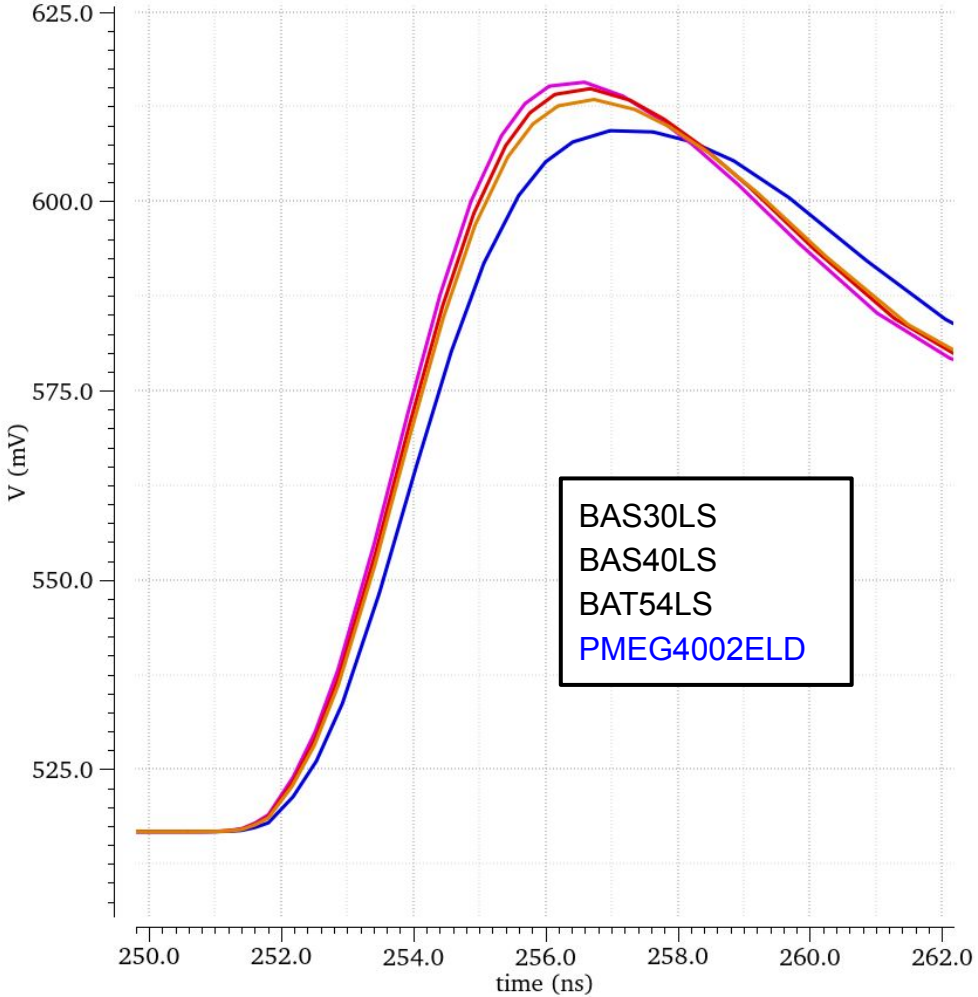
FEB prototype production

➔ select 2 different diodes but keep same footprint:
SMD0402, SOD882BD package



Annealing diodes survey:

BAS30LS	C = 2 pF	V_f = 0.85 V	→	P = 51 mW	(I_f = 60 mA)
BAS40LS	C = 5 pF	V_f = 0.68 V	→	P = 41 mW	(I_f = 60 mA)
BAT54LS	C = 10 pF	V_f = 0.48 V	→	P = 29 mW	(I_f = 60 mA)
PMEG4002ELD	C = 14-20 pF	V_f = 0.30 V	→	P = 18 mW	(I_f = 60 mA)



ALCOR + ann. diodes simulations

Test input line capacitive loading due to diode capacitance

Larger C diode slightly reduces signal slope and thus time resolution (<10%)

Proposal for FEB prototypes (master + slave):

- 3+3 FEBs with **PMEG4002ELD**
- 3+3 FEBs with BAT54LS
- 1+1 FEBs without diodes

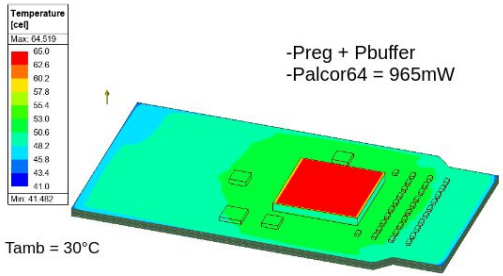
Thermal simulations (preliminary)

Preliminary thermal simulations of one FEB board during **normal operations** and while performing **annealing** embedded in a static T = 30°C ambient

Note: this is a first and simplified simulation of the board without air circulation and without taking into account other heat sources and the complexity of the surrounding environment

- first guidance on the possible **temperature profiles**
- useful to put **requirements** on **dRICH box cooling**
- valuable to **compare** with simplified **test benches**

Normal mode (ALCOR ON)

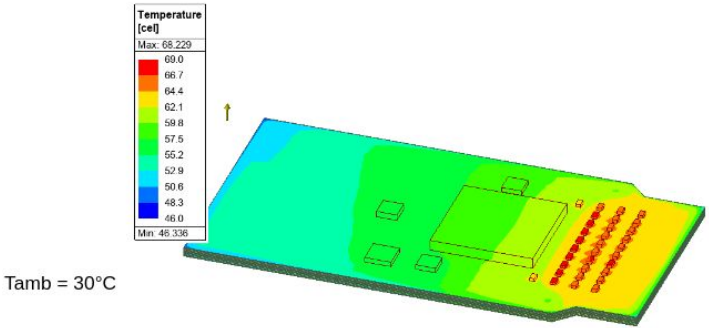


-**BGA**
Tj = 64.8 °C

-**PCB(Top):**
Tmax = 53°C
Tmean = 50°C

-**PCB(Bot):**
Tmax = 52.7°C
Tmean = 50°C

Annealing mode (V_f = 0.43 V @70°C x 60 mA → 26 mW)



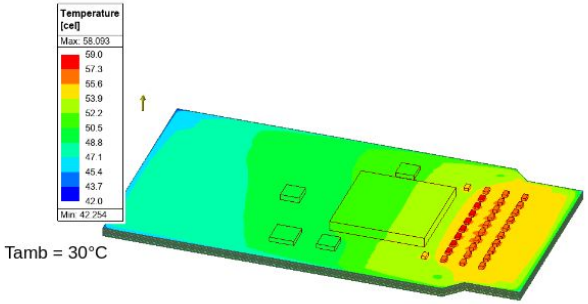
-**DIODI:**
64 x 26 mW
Tmax = 68°C

-**BGA:**
Tmax = 61°C
Tmean = 59°C

-**PCB(Top):**
Tmax = 67°C
Tmean = 57°C

-**PCB(Bot):**
Tmax = 68°C
Tmean = 57°C

Annealing mode (V_f = 0.30 V @55°C x 60 mA → 18 mW)



-**DIODI:**
64 x 18 mW
Tmax = 58°C

-**BGA:**
Tmax = 53°C
Tmean = 52°C

-**PCB(Top):**
Tmax = 58°C
Tmean = 51°C

-**PCB(Bot):**
Tmax = 58°C
Tmean = 51°C

SMA-annealing FEB

FEB prototype to test SiPM annealing

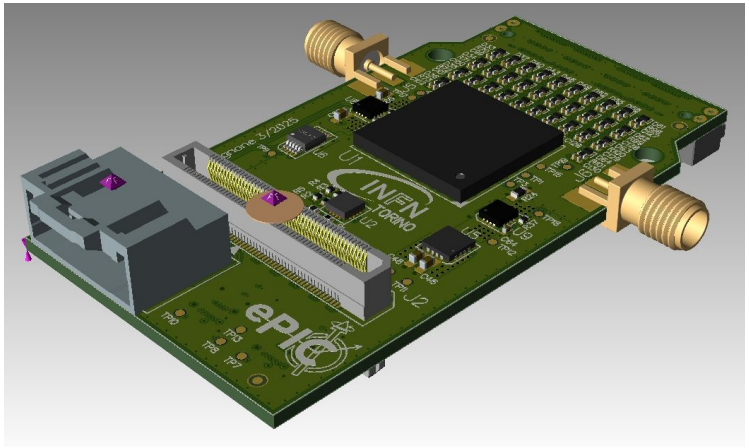
- like final FEB, with all annealing circuitry
- added **2 SMA connectors** to inspect SiPM signals (ALCOR inputs) on scope → initially can be used also without ALCOR-64

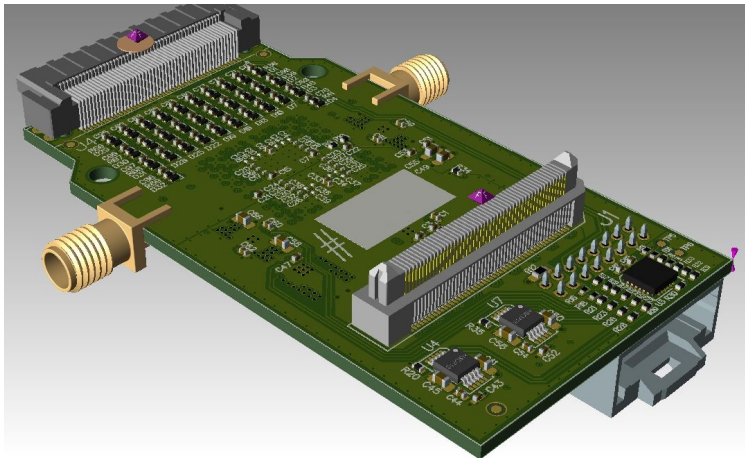
Goals:

➔ test **realistic dRICH annealing electronics**

➔ study annealing process details and provide critical guidance for the final engineering and important reference data for **simulation of heat-dissipation** and the **design of the cooling system**

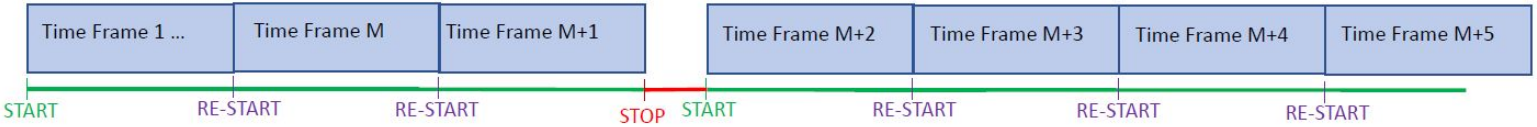
✓ **Purchase order issued 2-3 weeks ago**

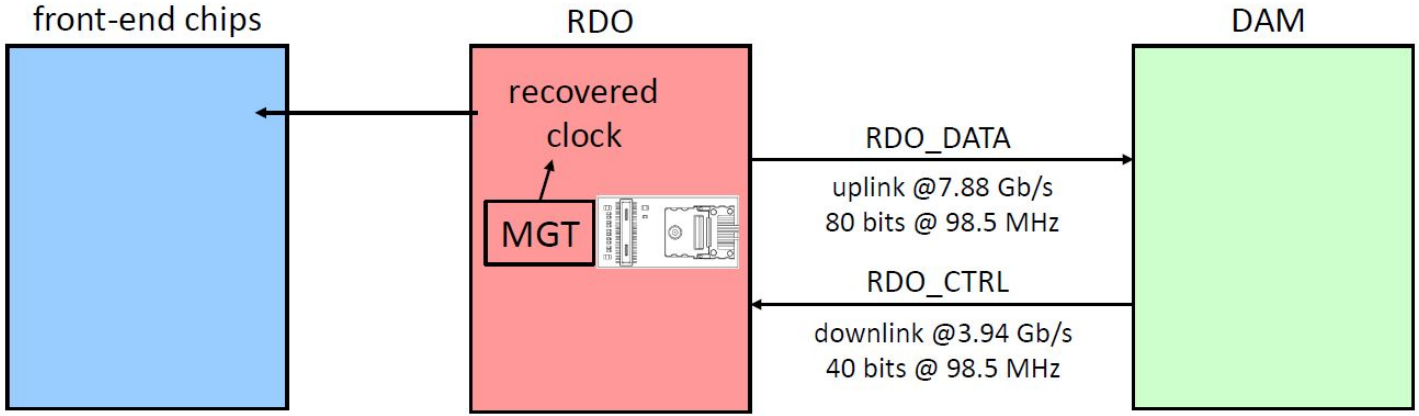




Streaming readout

The ePIC detector will take data using a streaming data acquisition system with no traditional HW trigger





EIC clock = 98.5 MHz
BC = 10.15 ns
EIC orbit period = 12.7886 μs = 1260 BCs
Time Frame = 2^{16} BCOs = 0.66 ms

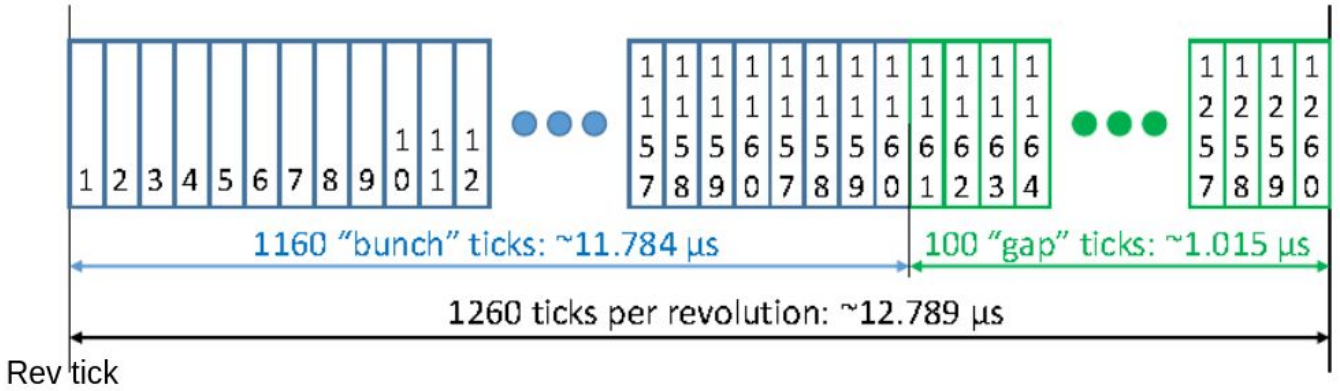
RDO_CTRL synchronous commands:

- SYNC_RESET: defines reference for time
- RUN_START: set internal state for readout
- RUN_RESTART: new time frame
- RUN_STOP: stop run

30

EIC beam structure and bunch crossing timing

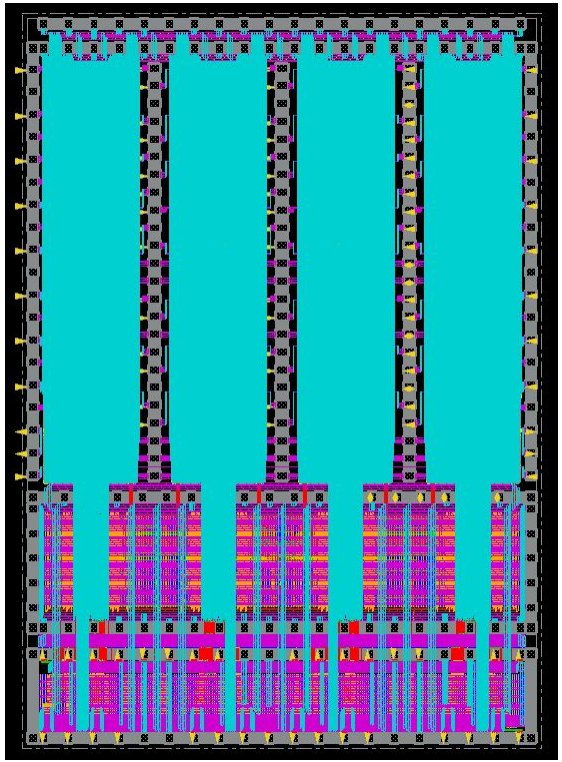
- Beam structure repeats every ~12.7886 μs
  - → Revolution frequency: ~78.195 kHz
- 1260 clock ticks in each revolution
  - → Clock period: ~10.14968 ns, frequency 98.52525 MHz ⟶ **ALCOR shutter frequency**
  - → 1160 filled "bunch" ticks, may be not all filled with particles
  - → 100 "gap" ticks without particles ⟶ **use for frame reset**



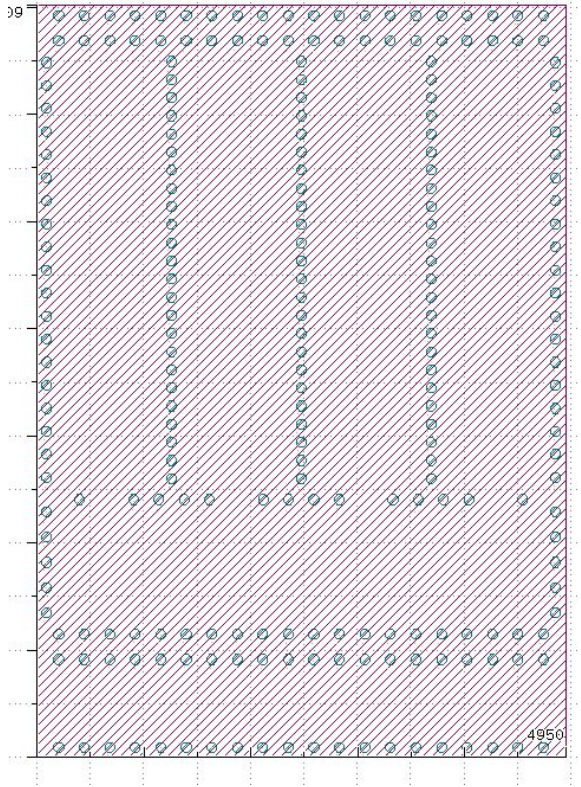
ALCOR v3

- ALCOR-64:
  - 7.02mm x 4.95mm
  - 234 PADs
- No dedicated redistribution layer (**RDL**) available in UMC 110nm technology
  - ASIC bump pads geometry not uniform
  - fan-out to BGA balls done on the interposer/substrate
- Bump pads pitch:
  - ~170 µm (analog inputs)
  - ~215 µm

ALCOR-64 top layout



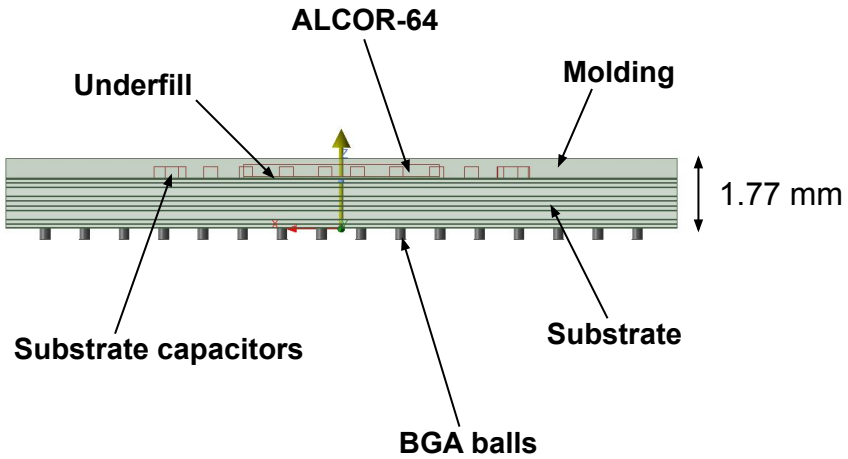
ALCOR-64 bump pads

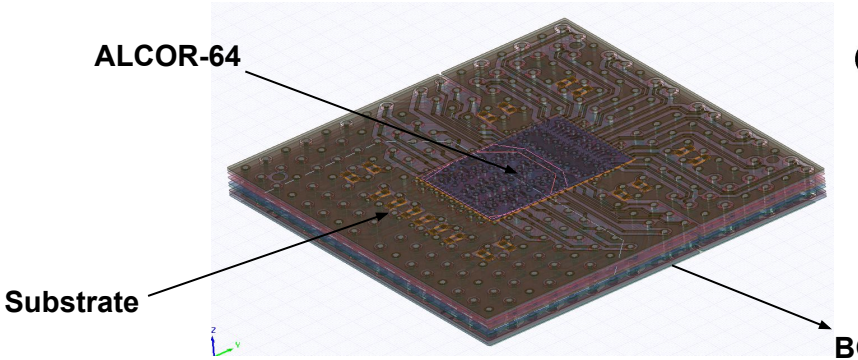


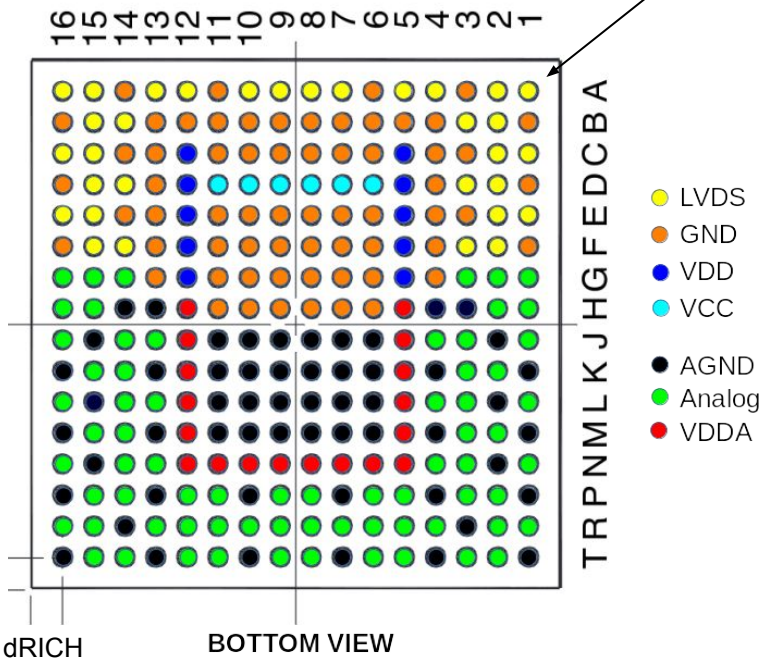
ALCOR BGA package

FC-BGA: flip-chip ball grid array

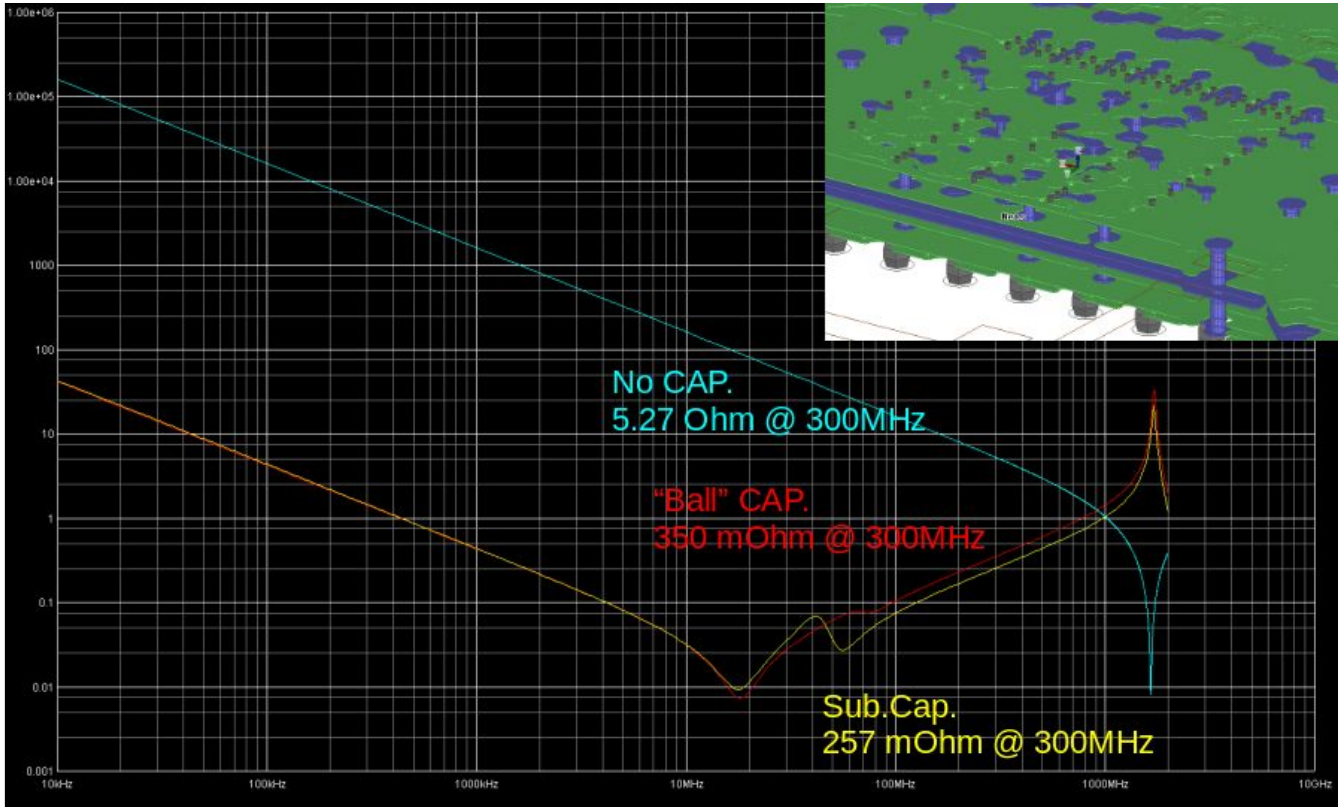
- BGA 256 (16 x 16)
- Size: 17 mm x 17 mm
- Ball pitch: 1 mm







ALCOR-64 substrate - simulations (Ball+PCB+Bump)

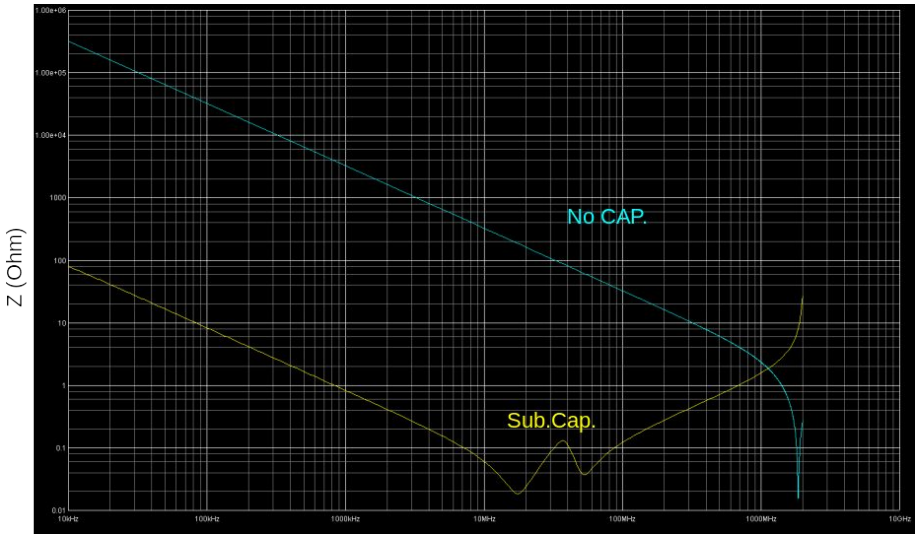


VDD-PDN (analog core supply power distribution network)

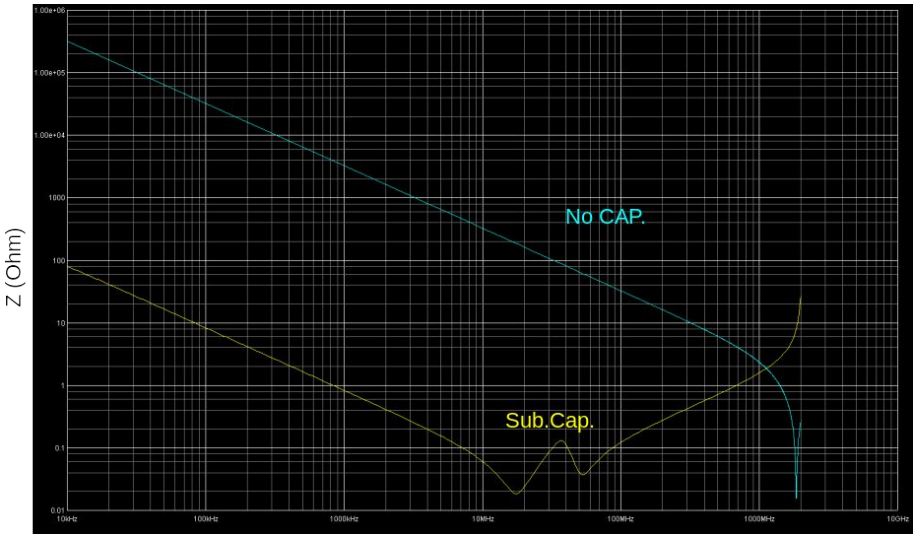
- **Sub.CAP**: substrate capacitors provides lower impedance
- **Ball CAP**: ideal case (not feasible)

Back-annotate this model into ALCOR simulations

ALCOR-64 substrate - simulations (Ball+PCB+Bump)



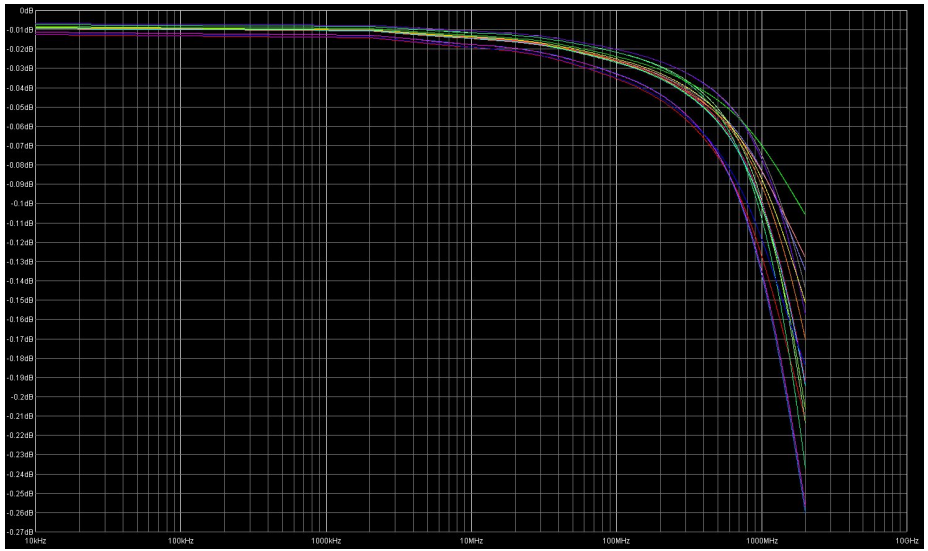
VDD-PDN (Digital core power supply)

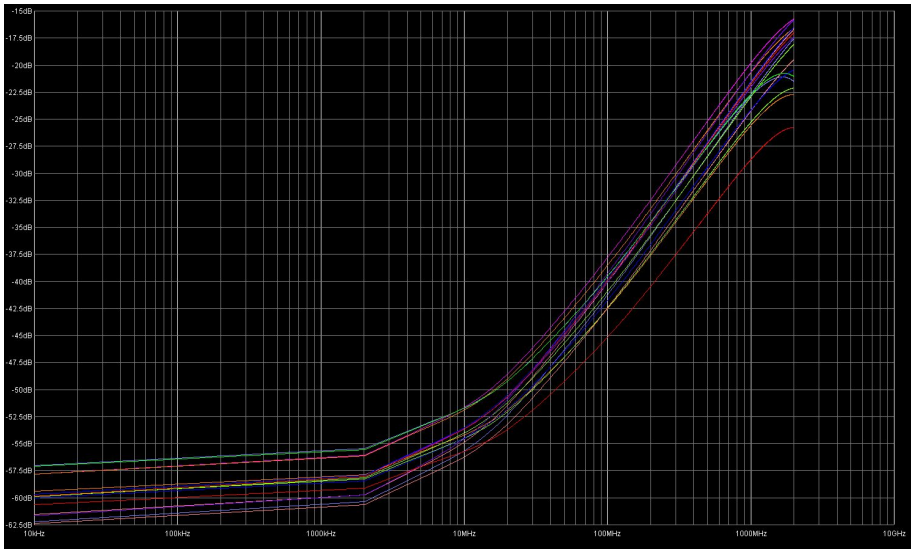


VCC-PDN (Digital IO power supply)

ALCOR-64 substrate - simulations (Ball+PCB+Bump)

Digital IO - LVDS transmission lines



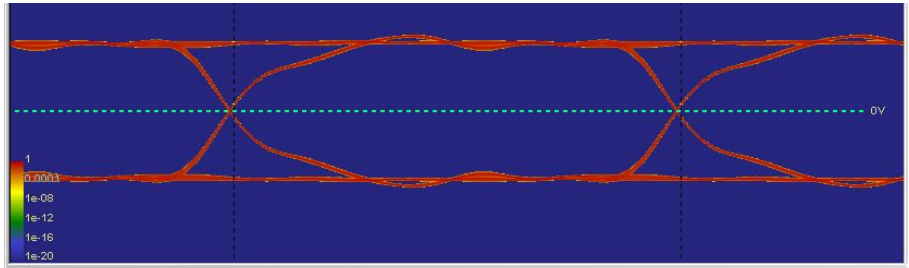


Insertion loss: amount of energy that a signal loses as it travels along the PCB trace

Return loss: loss of signal power due to signal reflection (impedance mismatch)

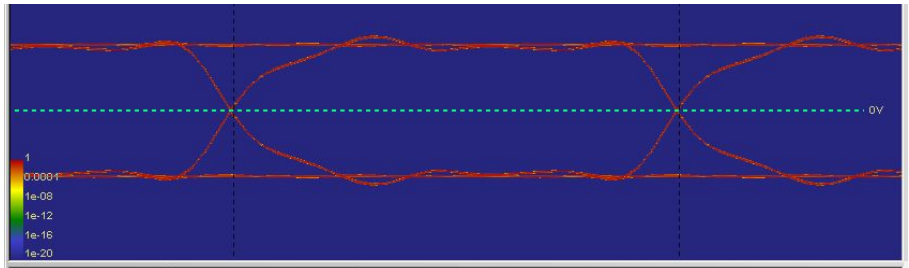
ALCOR-64 substrate - simulations (Ball+PCB+Bump)

Digital IO - LVDS transmission lines



Simulation date	Probe name	Simulation results					
		Highest BER	Pass/fail eye mask	Eye mask margin		Eye opening	
				Time, UI	Voltage, V	Time, UI	Voltage, V
Mon Sep 16 15:04:07 2024	U8.494P (at die)/U8.494N (at die)	0	Passed	0.187982	0.125092	0.987982	0.601042

ALCOR substrate=Ball+Via+Line+Bump
Q0-PRBS 19bit 800Mbps



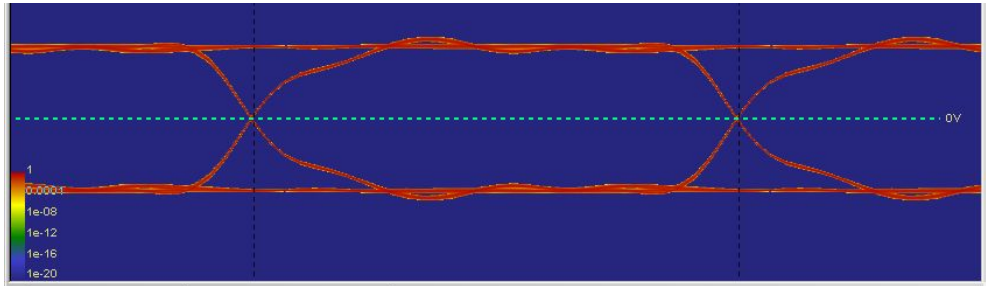
Simulation date	Probe name	Simulation results					
		Highest BER	Pass/fail eye mask	Eye mask margin		Eye opening	
				Time, UI	Voltage, V	Time, UI	Voltage, V
Mon Sep 16 15:09:00 2024	U34.494P (at die)/U34.494N (at die)	0	Passed	0.187982	0.133418	0.987982	0.581125

“Ideal” TLINE
Q0-PRBS 19bit 800Mbps

Tx and Rx model used is
LVDS_2V5 Driver (Artix UltraScale+)

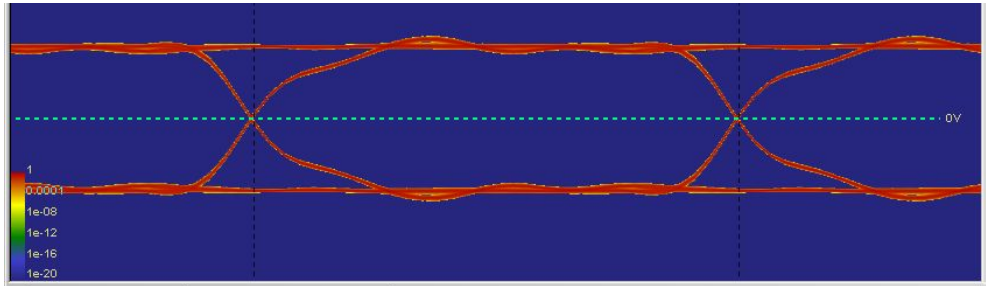
Crosstalk

Q3-PRBS 19bit 800Mbps

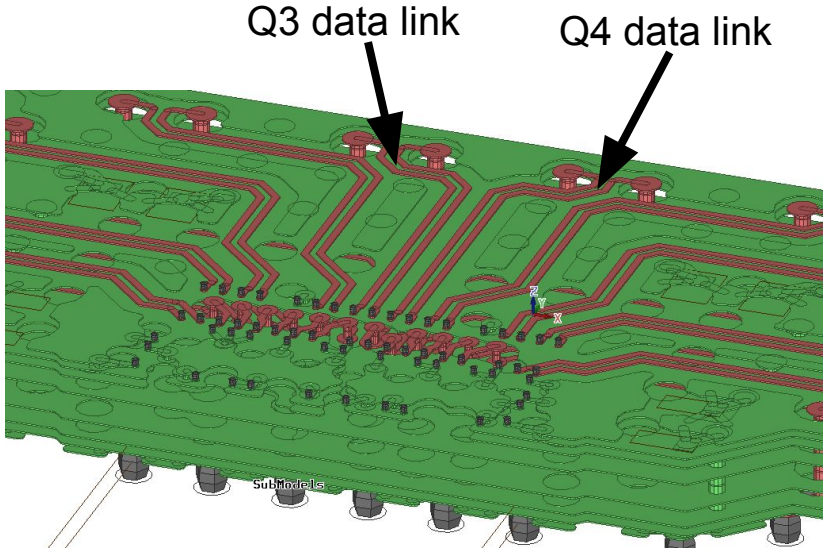


Simulation date	Probe name	Simulation results					
		Highest BER	Pass/fail eye mask	Eye mask margin		Eye opening	
				Time, UI	Voltage, V	Time, UI	Voltage, V
Wed Sep 18 10:00:58 2024	U14.494P (at die)/U14.494N (at die)	0	Passed	0.187982	0.131482	0.987982	0.567655

Q3-PRBS 19bit 800Mbps
(+**Q4 “Aggressor” Crosstalk** PRBS 19bit 800 Mbps)



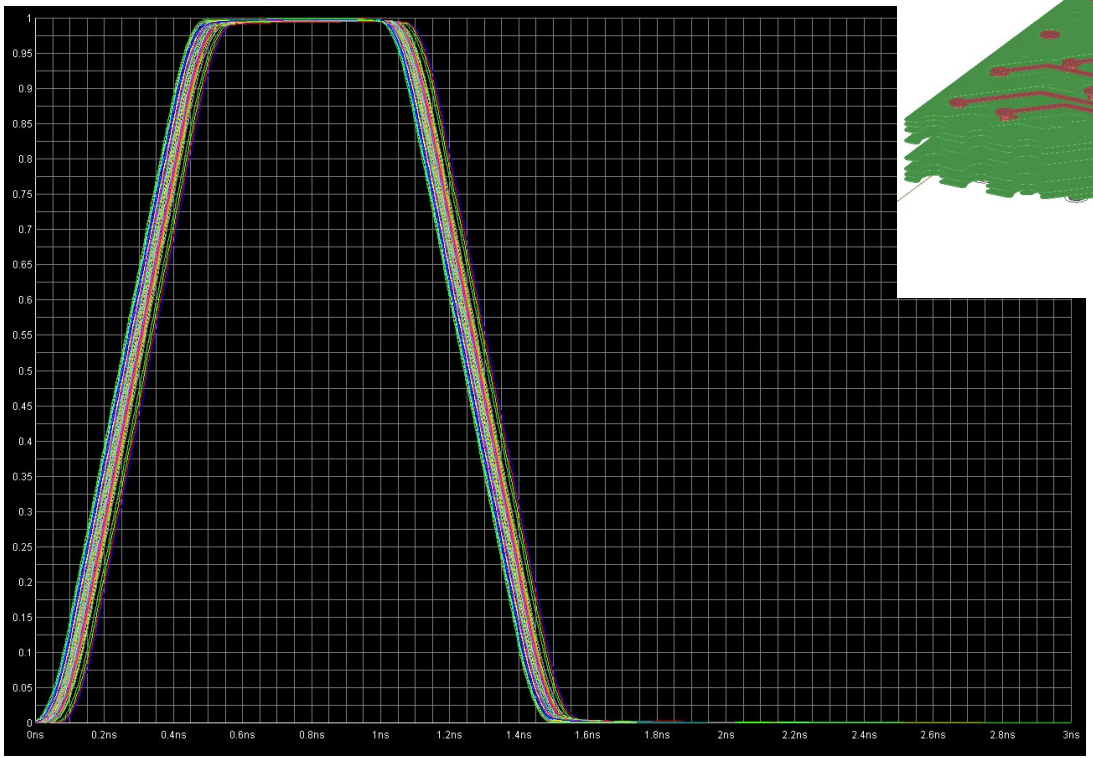
Simulation date	Probe name	Simulation results					
		Highest BER	Pass/fail eye mask	Eye mask margin		Eye opening	
				Time, UI	Voltage, V	Time, UI	Voltage, V
Wed Sep 18 10:06:52 2024	U14.494P (at die)/U14.494N (at die)	0	Passed	0.187982	0.129136	0.987982	0.562963

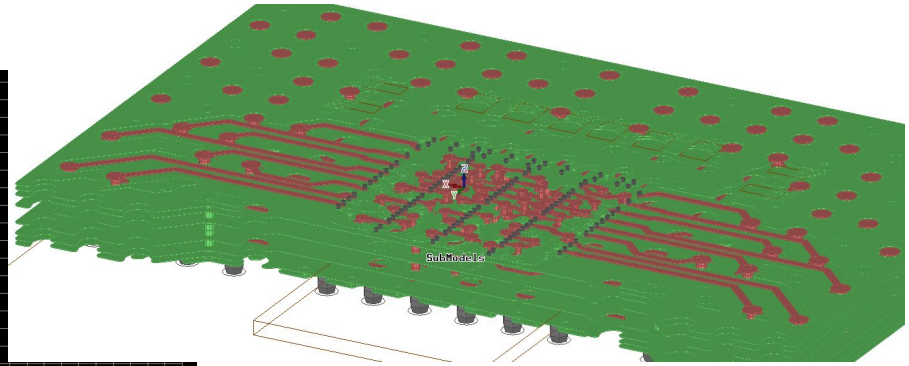


Tx and Rx model used is
LVDS_2V5 Driver (Artix UltraScale+)

ALCOR-64 substrate - simulations (Ball+PCB+Bump)

Analog inputs - 64 channels

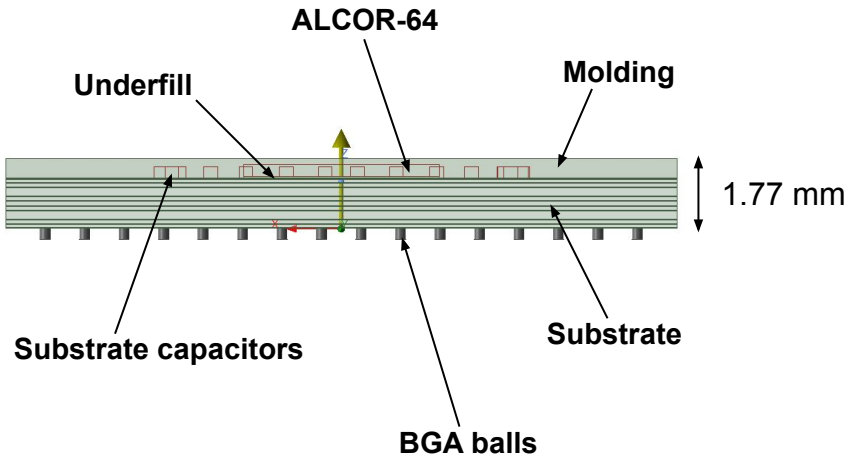




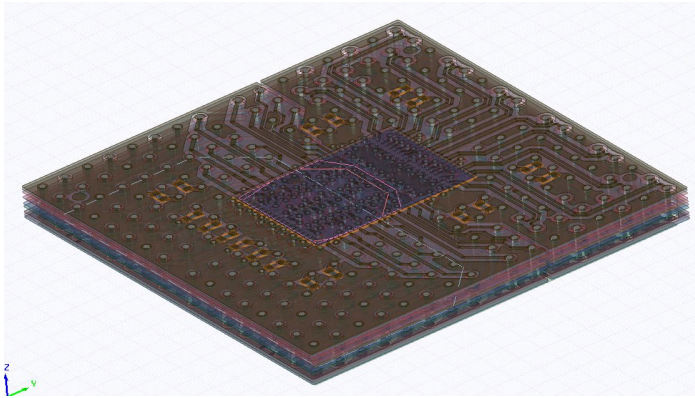
Input waveform:

T_p = 1 ns
T_r = 400 ps
T_f = 400 ps
Z_O = 50 Ω
Z_L = 50 Ω

Package Thermal Resistance



- Molding 0.5 mm (0.16 mm above ASIC)
- ALCOR-64
- Underfill
- Substrate



Package Thermal Resistance

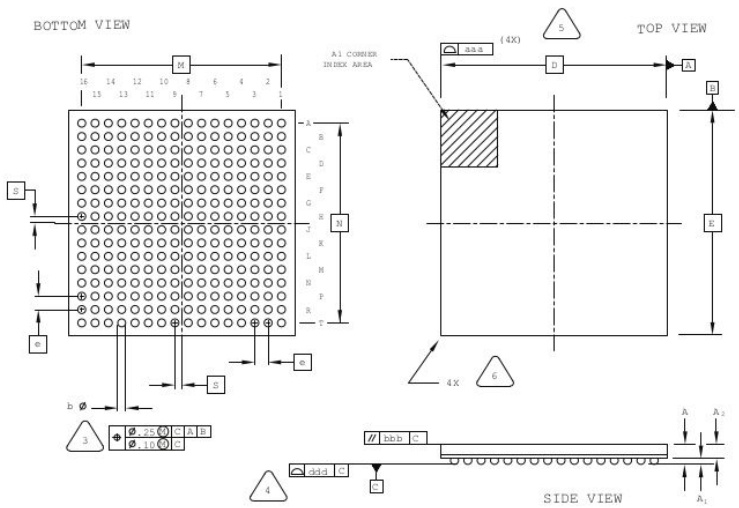
- $\theta_{JB} \approx 12.9$ °C/W (Junction-to-Board)
- $\theta_{JC} \approx 3.3$ °C/W (Junction-to-Case)

} Good match with specs from commercial BGA datasheet

Commercial 256-ball BGA package datasheet

256-Ball ftBGA Package C

Dimensions in Millimeters



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C
4. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

SYMBOL	MIN.	NOM.	MAX.
A	1.30	1.70	2.10
A1	0.30	0.50	0.70
A2		1.40 REF	
D/E		17.0 BSC	
M/N		15.0 BSC	
S		0.50 BSC	
b	0.50	0.60	0.70
e		1.0 BSC	
aaa	-	-	0.20
bbb	-	-	0.25
ddd	-	-	0.20

Geometry very similar to ALCOR BGA

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimensions	Pin Count	θ_{JA} (0lfm) °C/W	θ_{JA} (200lfm) °C/W	θ_{JA} (500lfm) °C/W	θ_{JB} °C/W	θ_{JC} °C/W
LatticeECP2M™	LFE2M20E	FPBGA	17 x 17 mm	256	24.2	20.2	17.8	12.6	3.2
	LFE2M20E	FPBGA	23 x 23 mm	484	18.1	15.6	13.8	9.5	5.1
	LFE2M35E	FPBGA	17 x 17 mm	256	22.4	18.5	16.2	11.0	2.5
	LFE2M35E	FPBGA	23 x 23 mm	484	16.8	14.3	12.5	8.1	4.0
	LFE2M35E	FPBGA	27 x 27 mm	672	15.5	13.0	11.1	5.9	3.1
	LFE2M50E	FPBGA	23 x 23 mm	484	15.6	13.1	11.3	6.9	3.1
	LFE2M50E	FPBGA	27 x 27 mm	672	14.2	11.9	10.2	5.9	2.6
	LFE2M50E	FPBGA	31 x 31 mm	900	12.5	10.4	9.1	6.1	1.9
	LFE2M70E	FPBGA	31 x 31 mm	900	11.7	9.5	8.1	5.3	1.5
	LFE2M70E	FPBGA	35 x 35 mm	1152	13.7	12.0	11.0	6.5	2.0
	LFE2M100E	FPBGA	31 x 31 mm	900	10.8	8.6	7.1	4.5	1.2
	LFE2M100E	FPBGA	35 x 35 mm	1152	13.2	11.2	9.8	5.7	1.5
LatticeECP3™	LFE3-17	FTBGA	17 x 17 mm	256	24.5	20.6	18.2	12.9	3.3
	LFE3-17	CSBGA	10 x 10 mm	328	30.8	27.8	25.5	12.5	6.1
	LFE3-17	FPBGA	23 x 23 mm	484	18.4	15.8	14.1	9.8	5.4
	LFE3-35	FTBGA	17 x 17 mm	256	24.5	20.6	18.2	12.9	3.3
	LFE3-35	FPBGA	23 x 23 mm	484	18.4	15.8	14.1	9.8	5.4
	LFE3-35	FPBGA	27 x 27 mm	672	17.1	14.7	12.7	9.5	4.5
	LFE3-70	FPBGA	23 x 23 mm	484	15.7	13.2	11.4	7	3.2
	LFE3-70	FPBGA	27 x 27 mm	672	14.3	12	10.3	6	2.7
	LFE3-70	FPBGA	35 x 35 mm	1156	12.9	11.5	10.6	7.3	2.3

Package Thermal Resistance

- θ_{JB} = 12.9 °C/W (Junction-to-Board)
- θ_{JC} = 3.3 °C/W (Junction-to-Case)

Results from our simulations match quite well specs from commercial BGA

Radiation tolerance

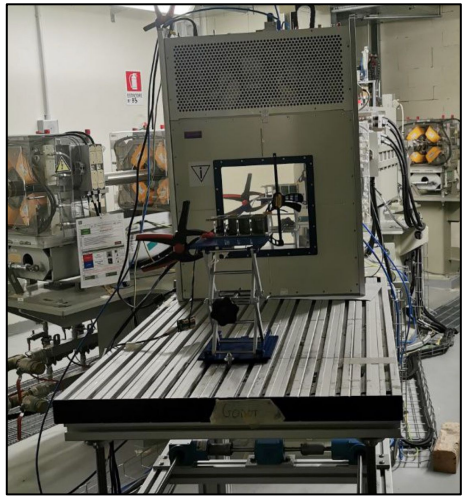
The dRICH-PDUs are in a moderately hostile radiation environment

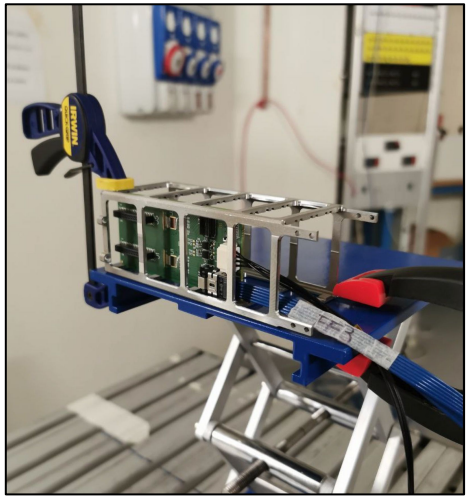
- Φ (p+n > 20 MeV) = 200 Hz/cm^2
- TID ≅ 2.3 krad (for 1000 fb^{-1})

} safety factor of 5 included

➢ Irradiation tests campaign: SEU/SEL and TID tests at Centro of Proton-Therapy in Trento with ALCOR-32 in Jul 2024 and Dec 2024
  - Beam: 100 MeV proton
  - Intensity: 10 - 100 nA
  - Runs: typically 600 s
  - Fluence collected per run: 10^{11} - 10^{12} p/cm^2

- **Total fluence: 4.64 · 10^{12} p/cm^2** (Jul 2024) and **3.2 · 10^{12} p/cm^2** (Dec 2024)
- **Total TID: 436 krad**





Detailed results presented at the 29th Jan 2025 dRICH Meeting: https://indico.bnl.gov/event/26313/

SEU/SEL results (July 2024)

ECCR/BCR/PCR registers checked against SEU (every second)

- ECCR $\sigma = (9.4 \pm 1.8) \cdot 10^{-14}$ cm^2/bit — periphery register → no TMR in ALCOR v2.1
- BCR $\sigma = (7.6 \pm 1.1) \cdot 10^{-14}$ cm^2/bit — periphery register → no TMR in ALCOR v2.1
- **PCR** **$\sigma = (3.3 \pm 0.5) \cdot 10^{-15}$ cm^2/bit** — pixel register → TMR (with auto-correction bug)

SEU due to accumulating bit flips in triplicated registers over time

SEU rate in ePIC:

- dRICH Flux = 140 (h > 20 MeV) / (cm^2 s)
- ALCOR bits: (2048 + 192) = 2240 → ALCOR-64 bits will be 4480
- Total ALCOR: 4992
- Total bits: 4992 · 4480 = 2.2 · 10^7 bits

➢ $\sigma = 3.3 \cdot 10^{-15}$ cm^2/bit → **MTBF** = $9.8 \cdot 10^4$ seconds → every **27 hours**

➢ No latchup events (from power supply currents monitoring)

SEU rate is within the expected manageable levels

SEU/SEL results (December 2024)

ECCR/BCR/PCR registers checked against SEU (every second), **PCR re-written every 10 seconds to "mask" TMR auto-correction bug**

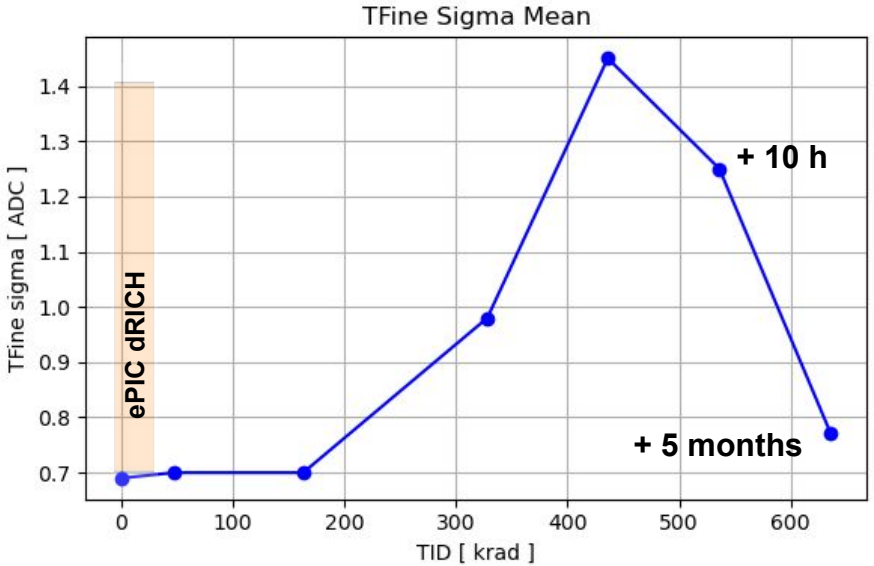
- ECCR $\sigma = 9.8 \cdot 10^{-14}$ cm^2/bit — periphery register → no TMR in ALCOR v2.1
- BCR $\sigma = 6.1 \cdot 10^{-14}$ cm^2/bit — periphery register → no TMR in ALCOR v2.1
- PCR **no SEU detected** — re-written every 10 seconds to avoid TMR auto-correction bug

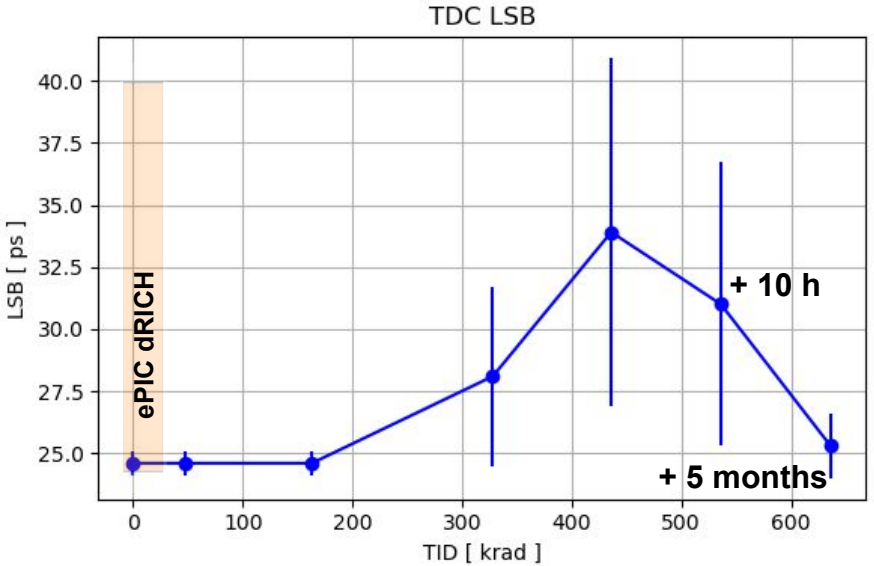
ALCOR v3: TMR SEU protection added also for periphery registers (used *CERN TMRG tool* for all registers), Hamming code SEU protection for FSMs

- All configuration registers: TMR with voting and self correction
- Pixel and EoC Readout FSMs: Hamming Code (Single Error Correction)
- EoC Reset FSM: TMR with voting and self correction
- SPI address counters: TMR with voting and self correction
- SPI shift register not protected

TID results - TDC error & LSB

***last two points = 436 krad after 10 hours and 5 months**





- Technology is sufficiently radiation tolerant to be used in the ePIC dRICH environment
- Similar results w.r.t. irradiation tests performed on another ASIC with same technology [1]
- Also other FEB components will be tested and validated

[1] F. Lenta *et al* 2024 *JINST* **19** C04047, DOI 10.1088/1748-0221/19/04/C04047