Istituto Nazionale di Fisica Nucleare
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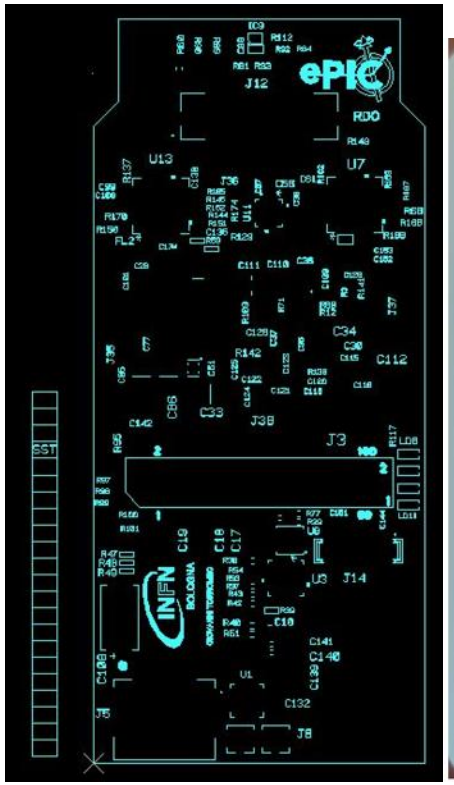


dRICH RDO

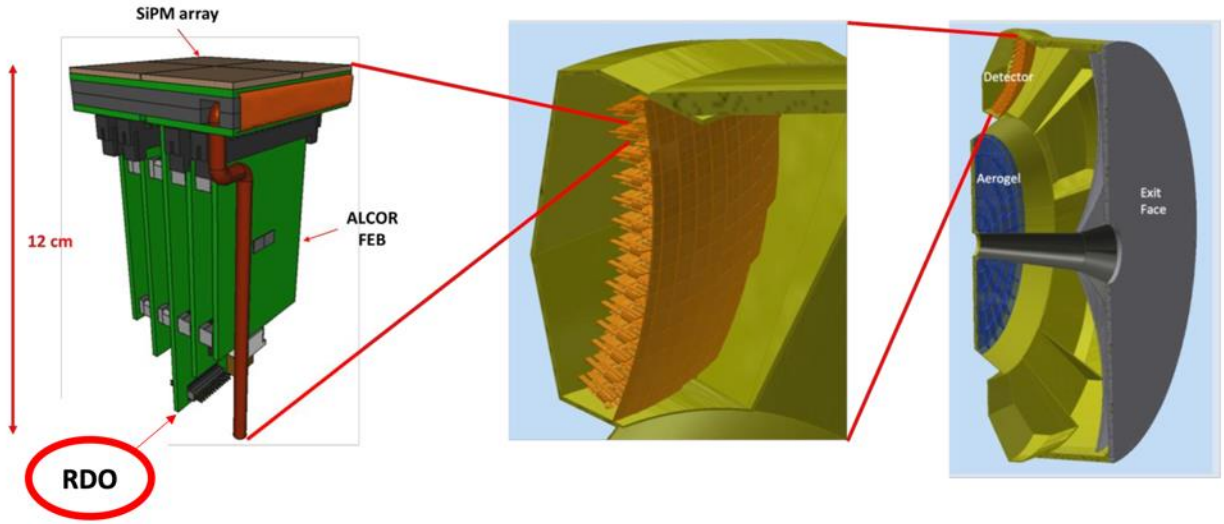
P. Antonioli , D. Falchieri, S. Geminiani,
L. Rignanese, G. Torromeo (INFN Bologna)

+ all the dRICH electronics group!

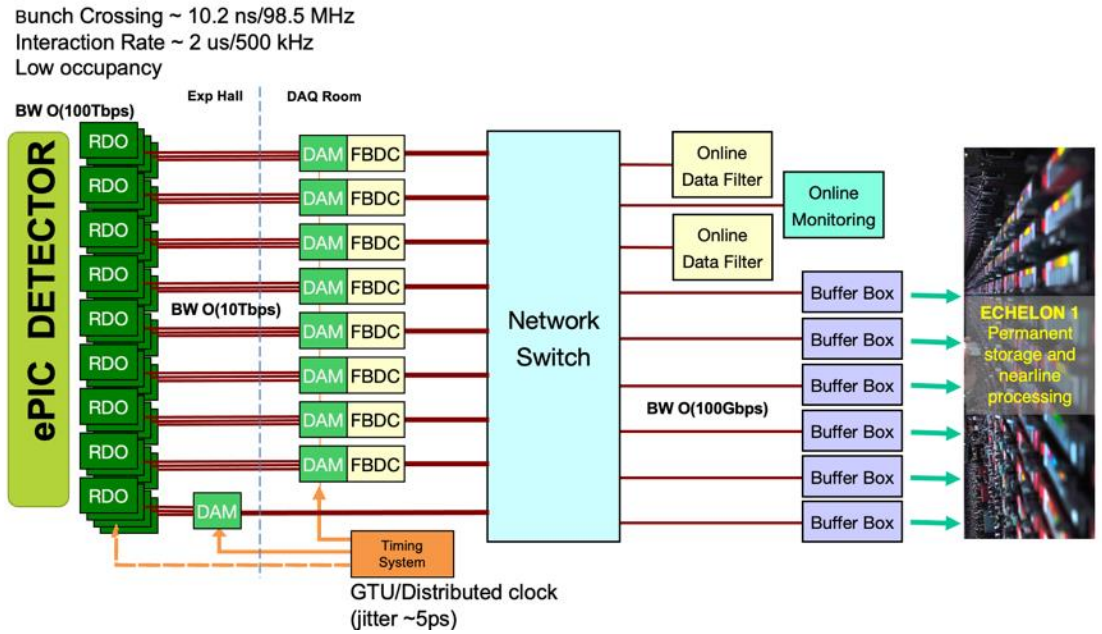
ePIC Italia
Padova 17 June 2025

dRICH RDO overview

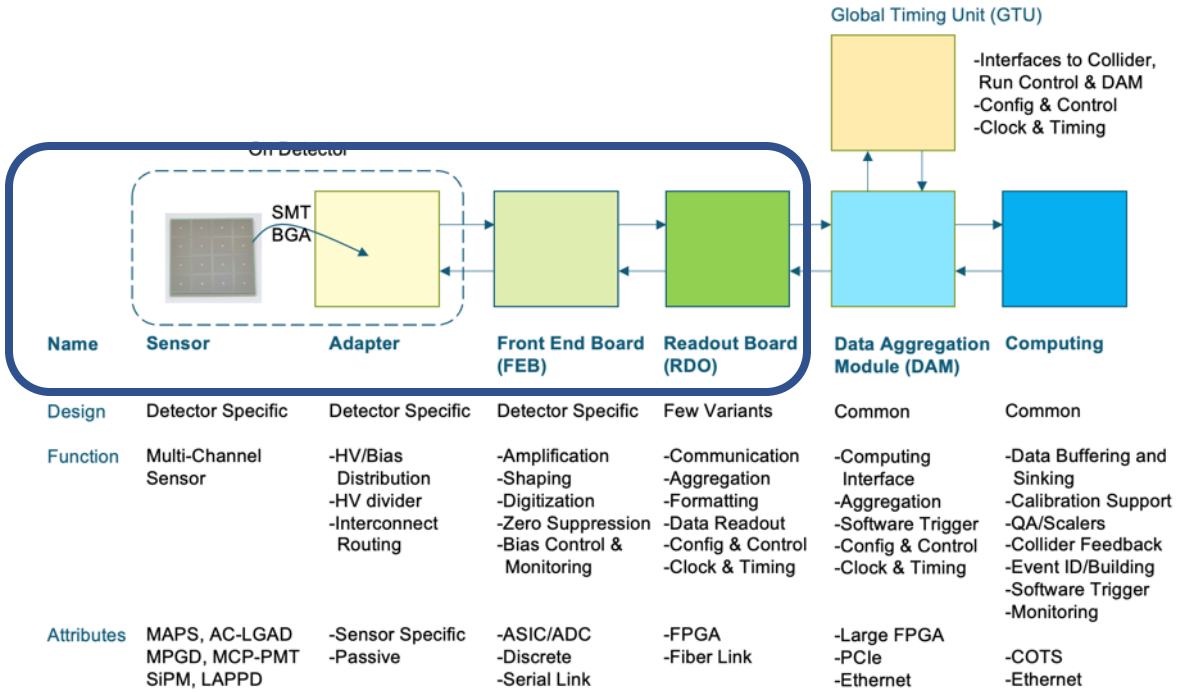
- RDO role in ePIC
- design choices for dRICH RDO ePIC
- miscellanea progresses and points of attention
  - VTRx+: light & pigtail saga
  - firmware
  - radiation tests
  - power consumption
  - cost estimate
- plannning and validation tests (including 2026 activities)
- lpGBT protocol for dRICH?



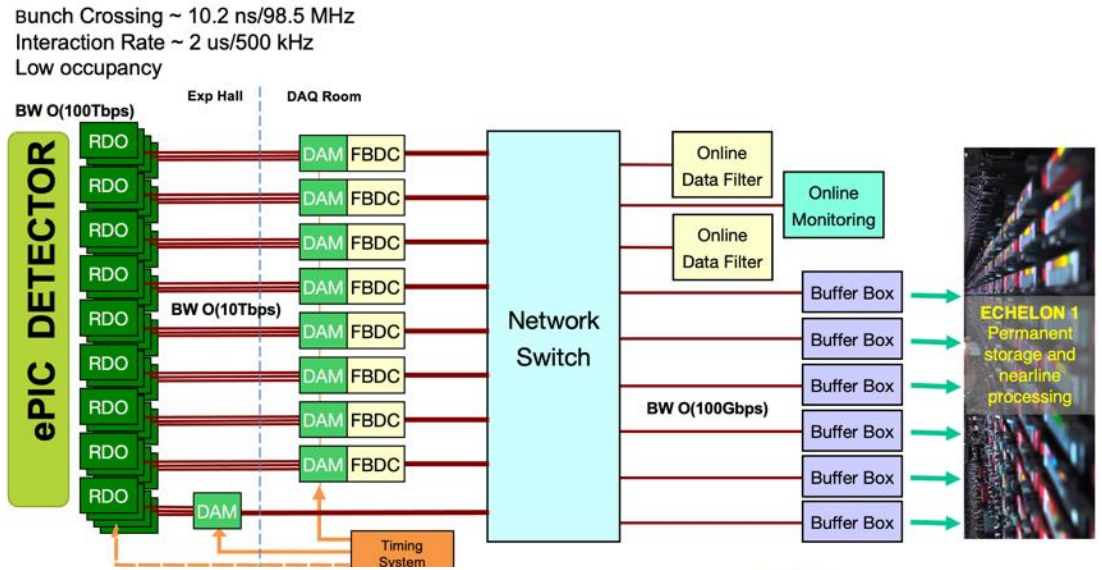
RDO role in ePIC



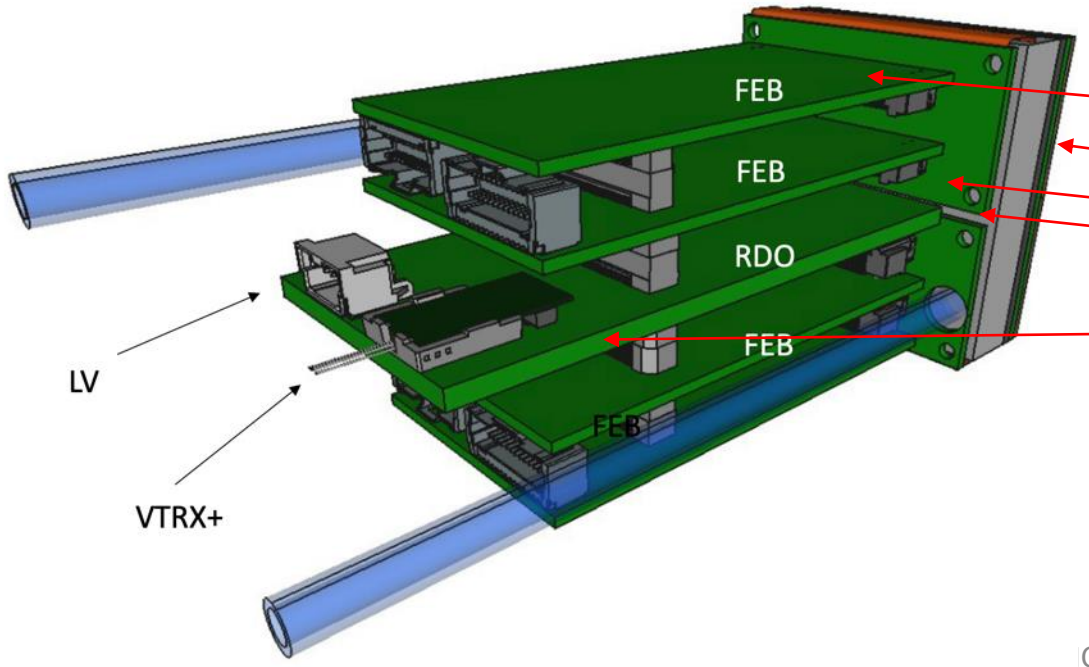
RDO as interface between detector specific ASIC and ePIC DAQ

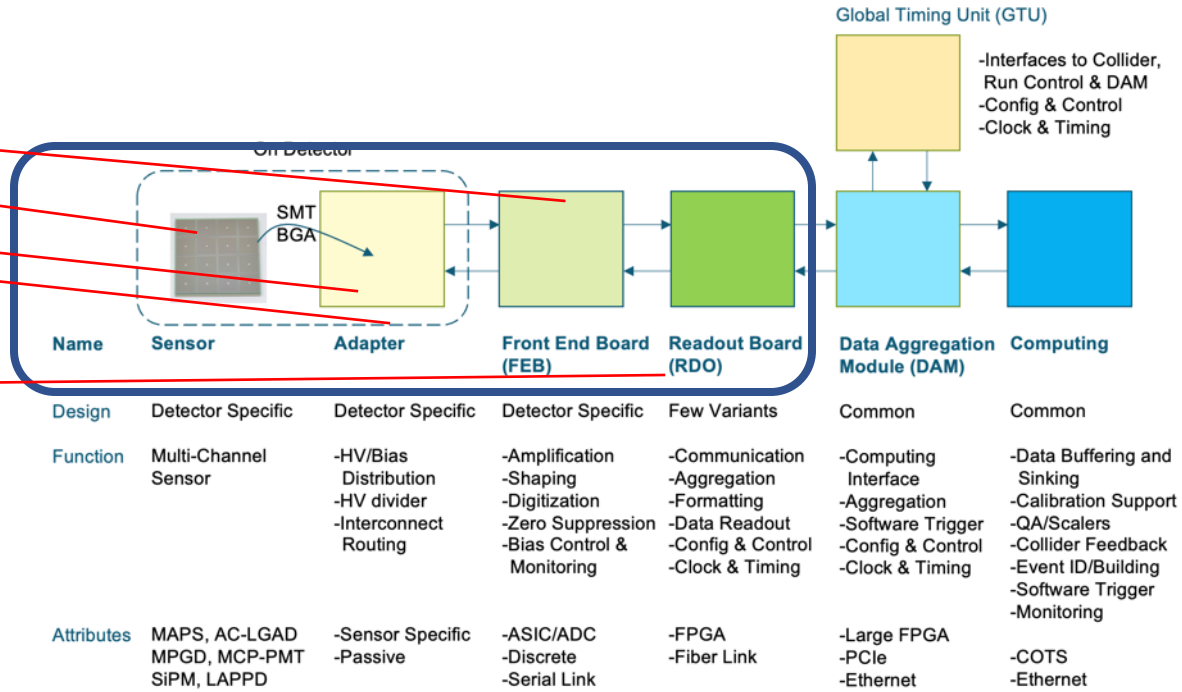


RDO role in ePIC and dRICH PDU

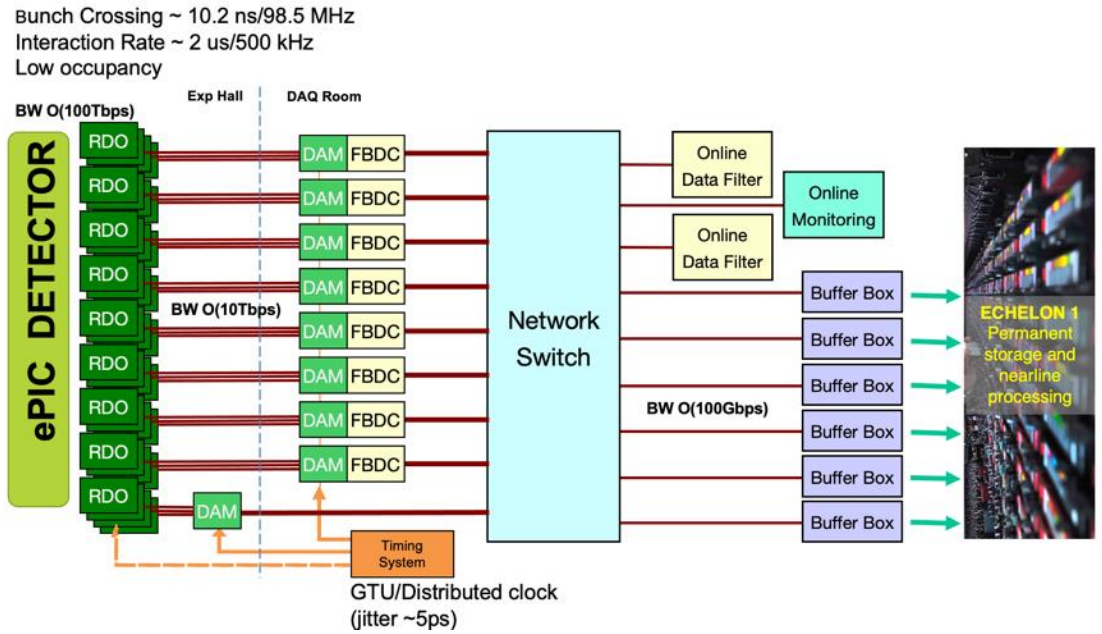


RDO as interface between detector specific ASIC and ePIC DAQ

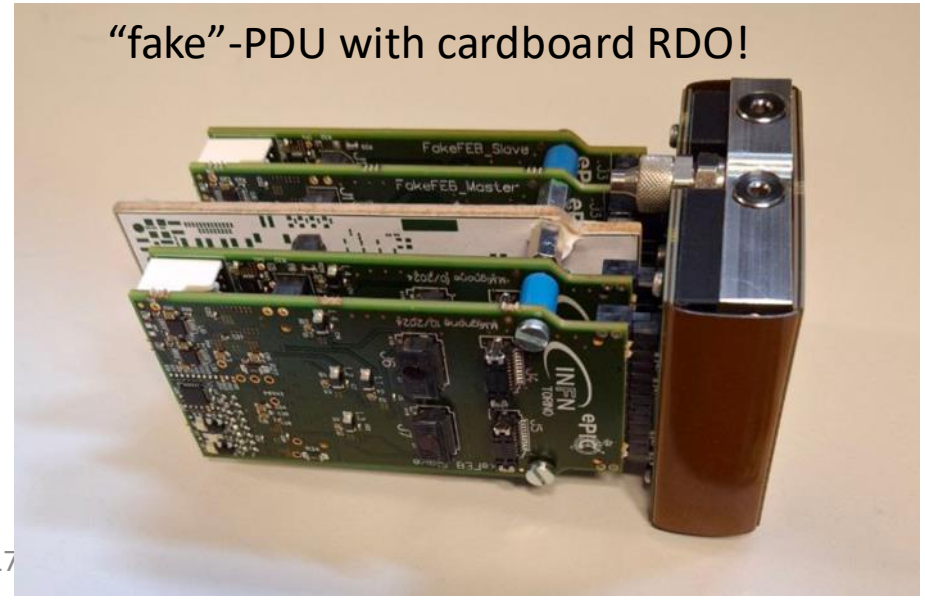


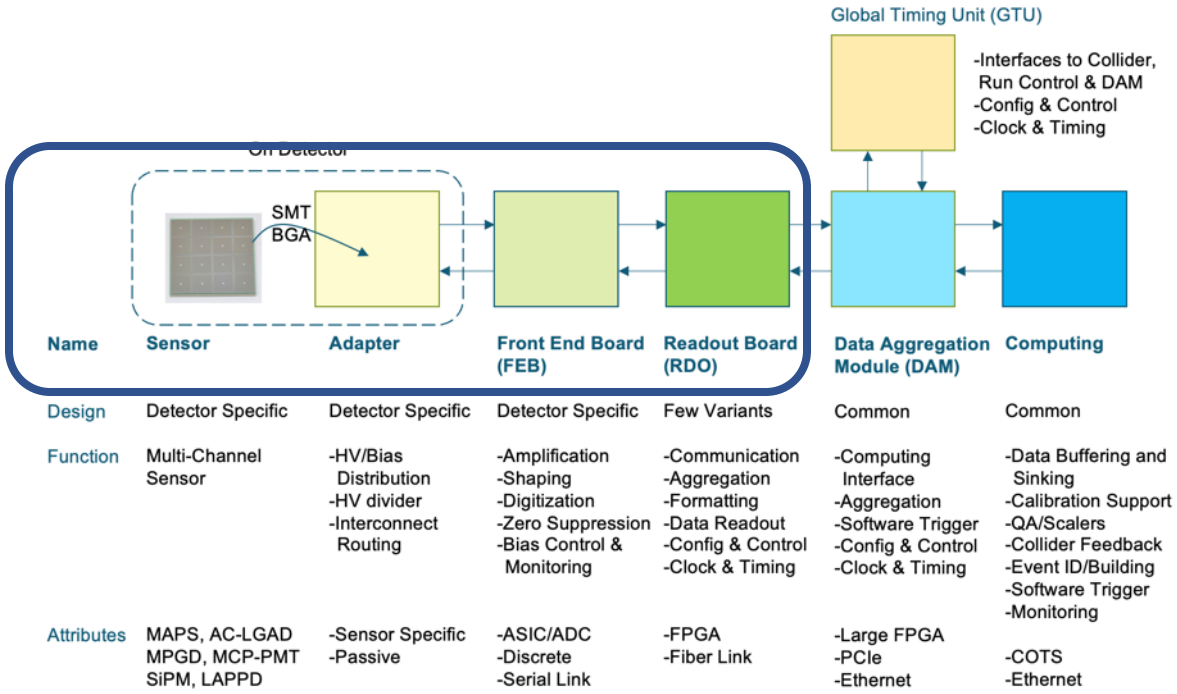


RDO role in ePIC and dRICH PDU



RDO as interface between detector specific ASIC and ePIC DAQ





requirements & design choices for dRICH RDO

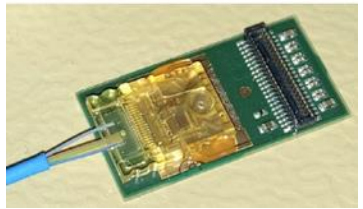
dRICH RDO requirements (from DAQ PDR review June 2024)

- **space**: 40 x 90 mm area
- RDO not accessible: **remote firmware upgrade** must be possible

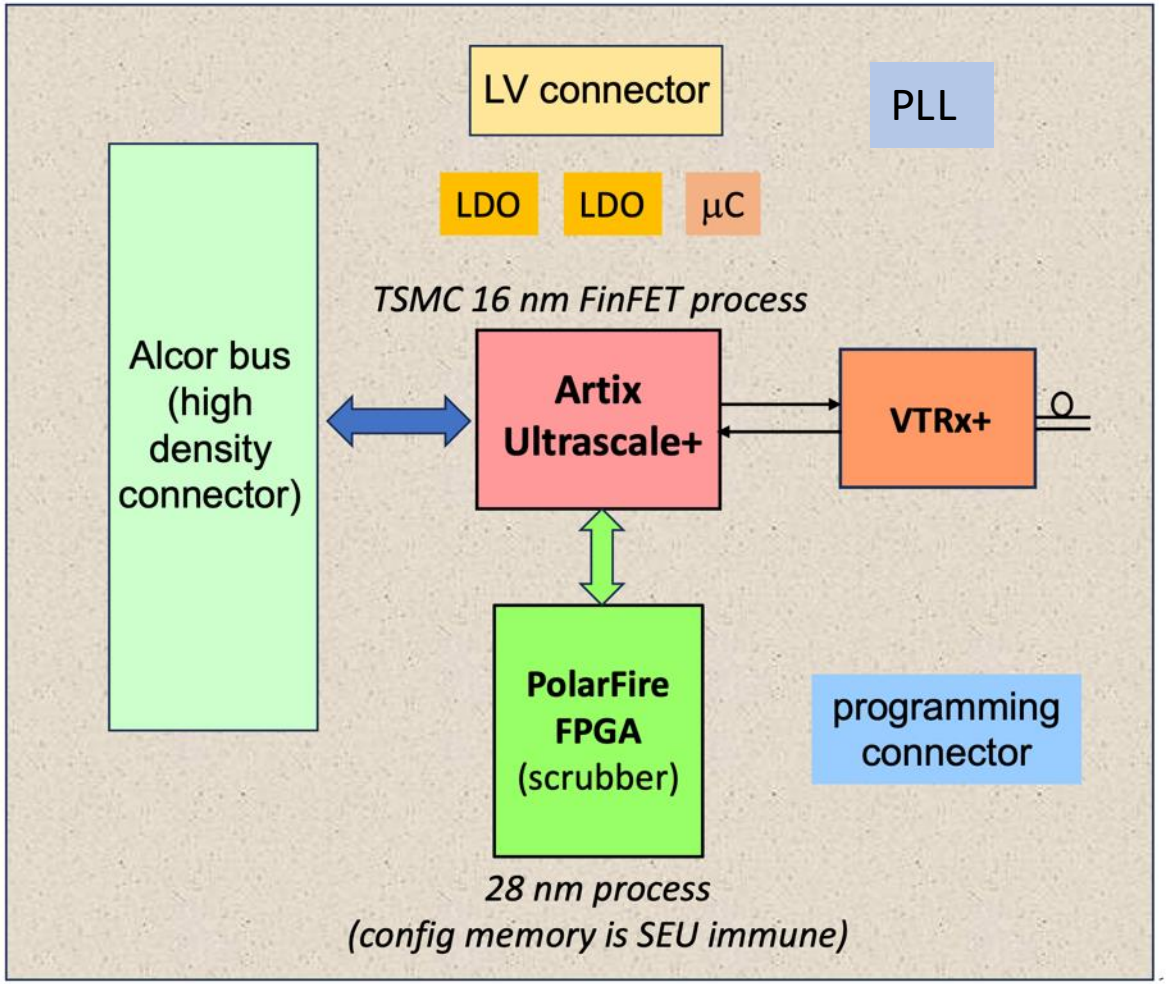
- RDO FPGA need **high speed** (“high performance”) 120 I/O pins to implement ALCOR bus (for TOP/BOTTOM FEB)
- RDO connector need high speed specs. and (minimum) 60 I/O pins each

- RDO must implement clean **clock** multiplication by factor 4 (ALCOR@394 MHz, EIC clock 98.5 MHz)
- RDO must reconstruct clock via optical link
- RDO must produce clean clock (minimize jitter)

- opt. tranceiver must minimize space/power consumption + “rad hard” and bandwitdh up to 10 Gbps (we have been the first pointing to VTRX+ in ePIC!)



requirements and design choices for dRICH RDO



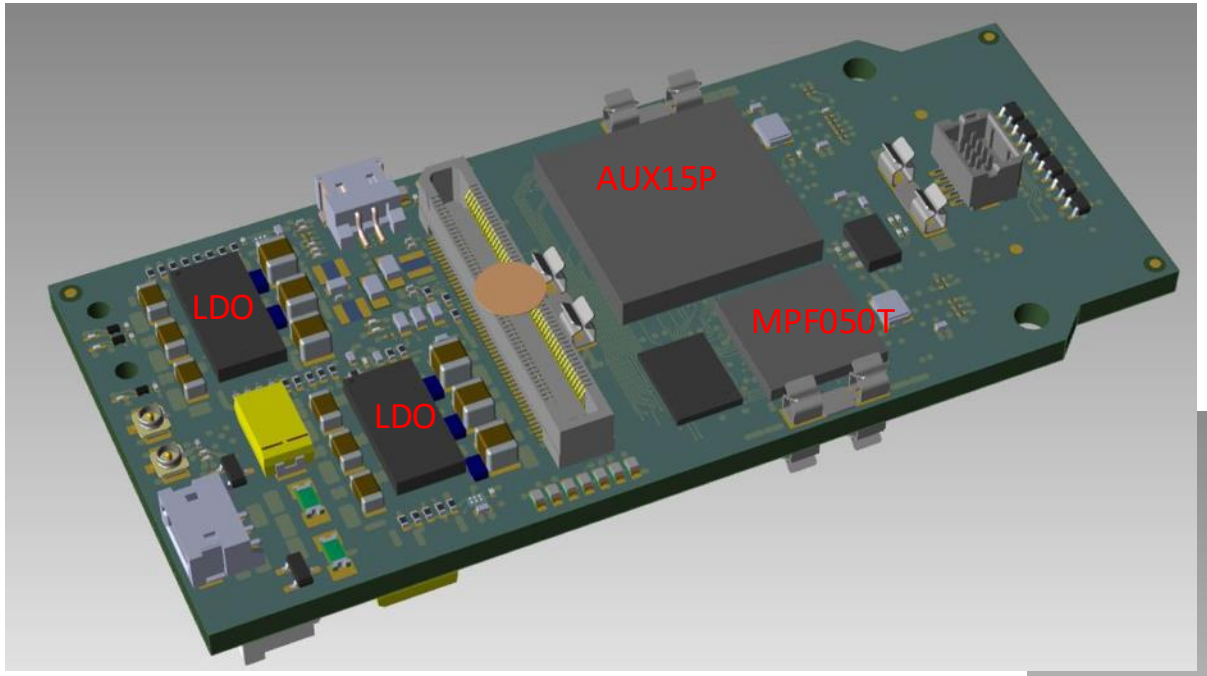
- a performing new generation FPGA (US+) + scrubbing
- devoted PLL to manage clock (SkyWorks 5319 / 5326)
- VTRX+ as optical tranceiver

Long and painful elaboration of exact RDO requirements + detailing project + components selection + layout time

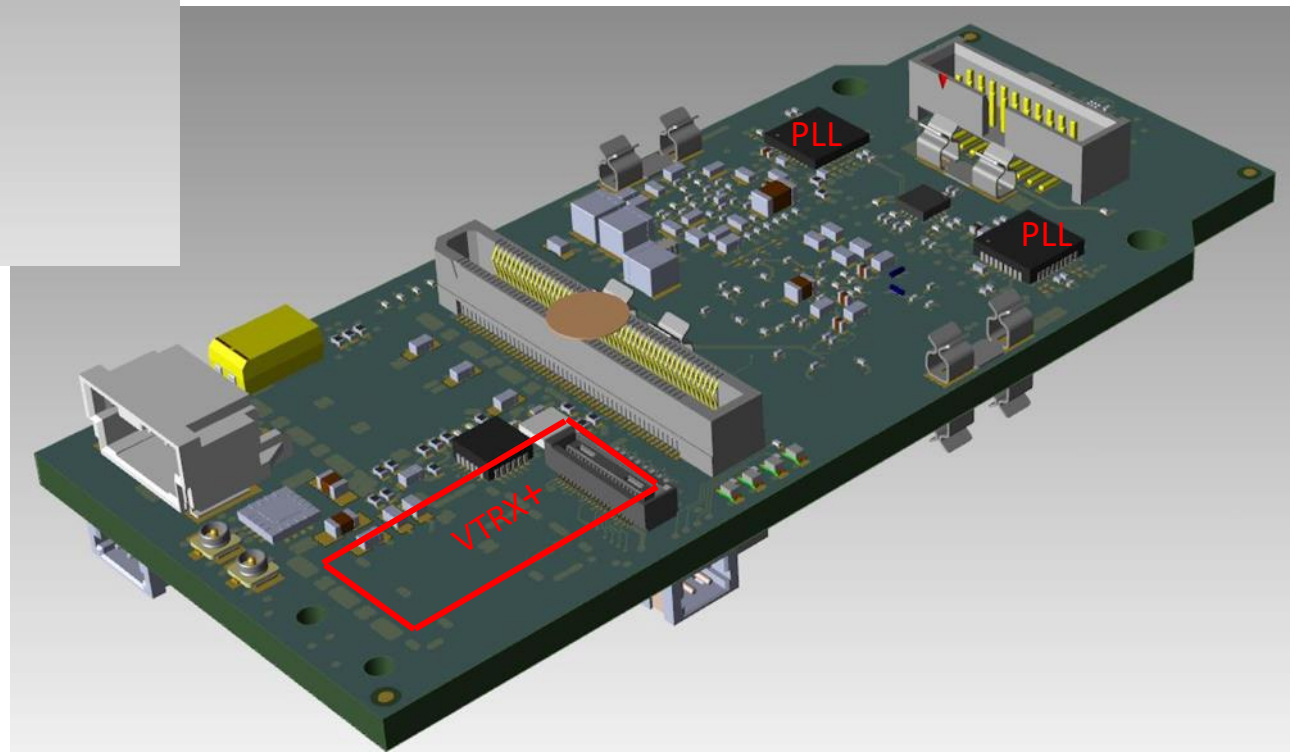
We should receive first 2 prototypes June 30!
(1.5 year after starting the design)

Much more details on D. Falchieri's talk at Workshop on Electronics for Physics Experiment and Applications @INFN (March 2025)

dRICH RDO: layout



Complex and small card, 16 layers layout

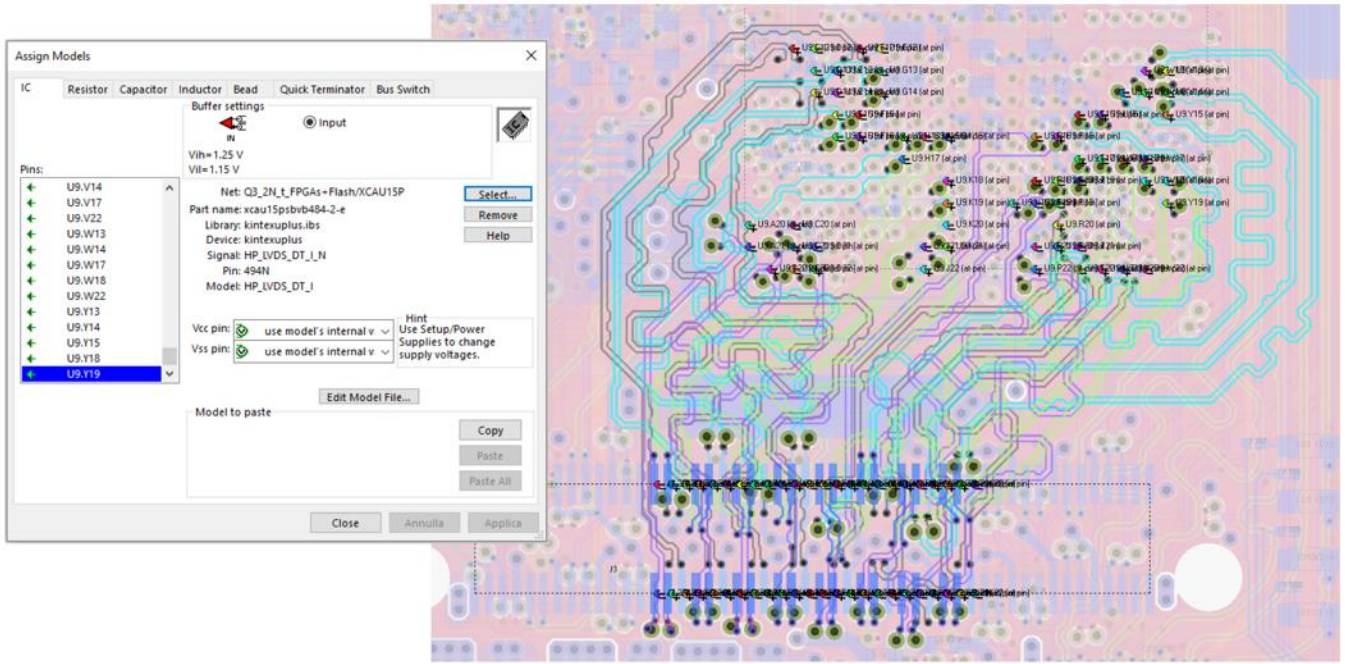


A small uC (ATTiny 417) acts as RDO power manager controlling LDOs

A lot of work on layout and cross-checks

optimization of FPGA pin assignment vs layout

Routing of 32 lanes ALCOR bus

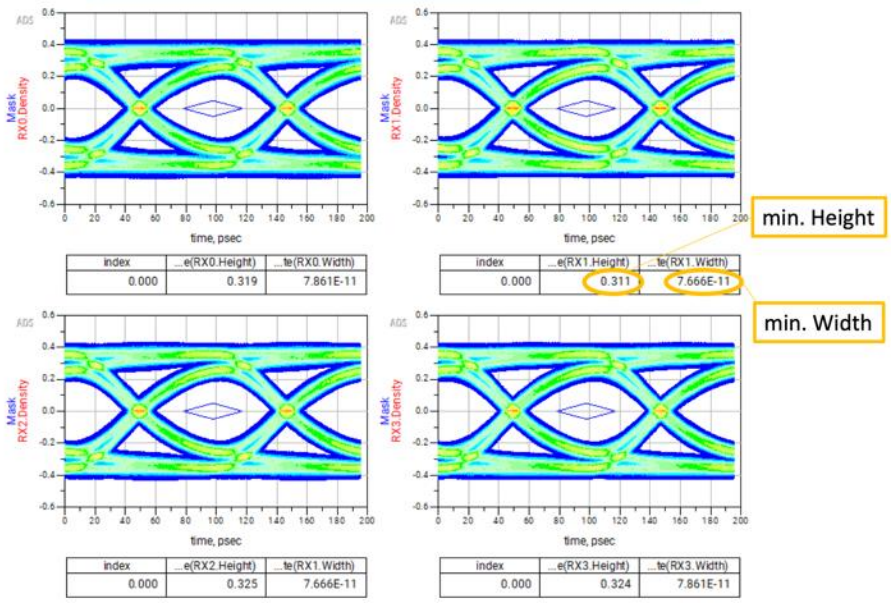


high-speed differential line modeling

ARTEL S.r.l. PCB ENGINEERING

4 Channels TX ARTIX Ultrascale+ GTH to VTRX+ receiver
AC coupling termination 100 Ω dielectric FR408HR

ADS Keysight



Much more details in D. Falchieri's presentation at WG Electronics and DAQ/eRD109 (April 2025)

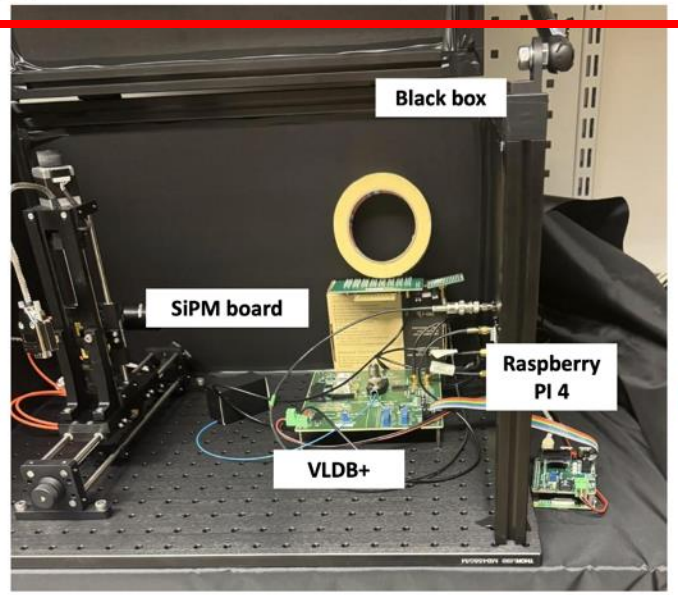
D. Falchieri, G. Torromeo

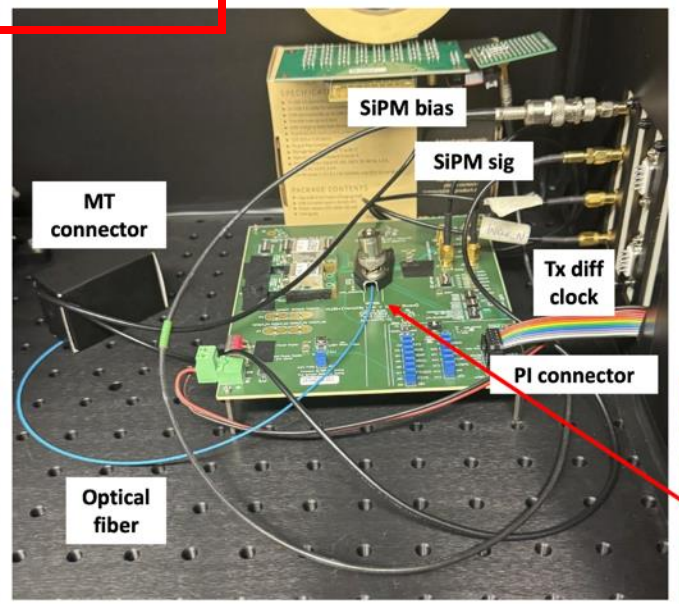
VTRx+ light + pigtail saga

VTRX+ light leakage tests

Context: LHCb colleagues told us VTRx+ has significant light leakage (from the transceiver + fiber)

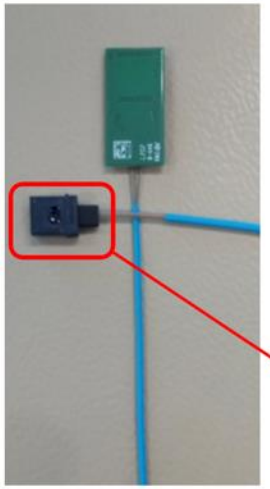
Test bench: black box + 1 SIPM

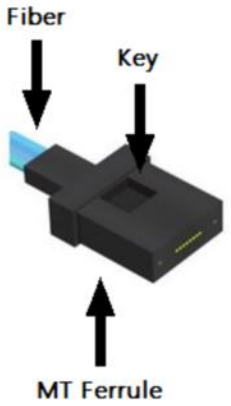


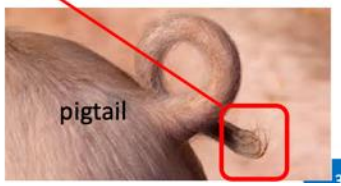


no cover of the fiber
SIPM in front of VTRX+ (not as PDU case, see next slide)
all leds of VLDB+ shielded with dark tape

"minimal" cover of VTRx+
(+ BNC adapter ;-) to keep it "tight"



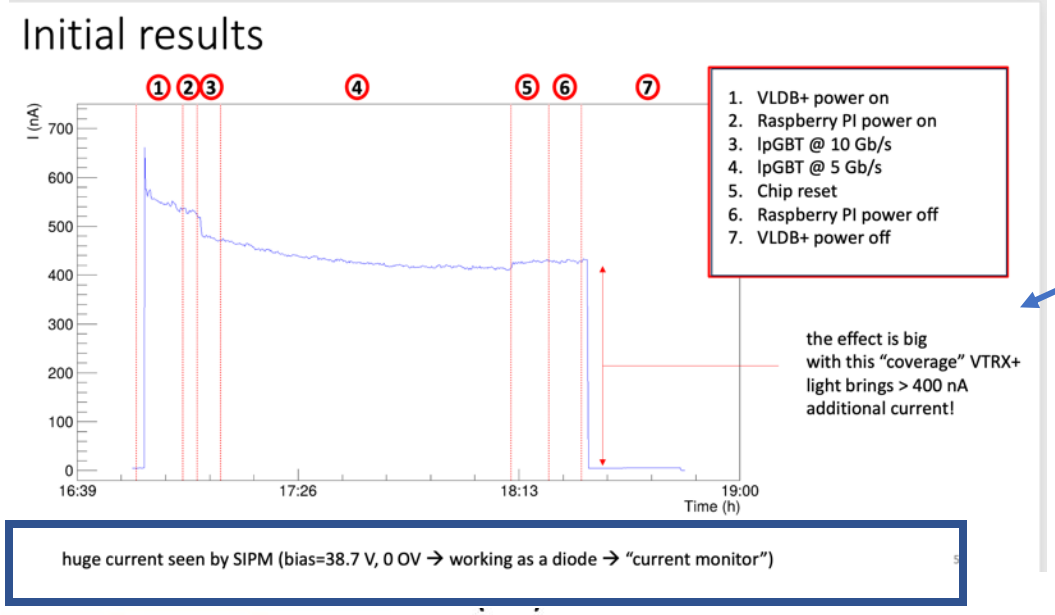




R. Preghenella/S.Geminiani/A. Paladino

More details on PA's talk at DAQ-Electronics WG/eRD109 (March 2025)

VTRx+ light + pigtail saga



Long story short:

- huge leak of light from VTRx+
- we will need to design effective shield
- initial results (room temperature only) encouraging
- and note after long debate we opted **for 20 cm pigtail length**

Additional VTRX+ plastic box + Thorlabs masking tape

→ No measurable extra-current: just 5 nA!

→ moved to 2.7 OV

With oscilloscope and measuring DCR (VLDB+ ON/OFF) we finally see:

(400.0 +- 1.8) kHz. VLDB+ ON
(398.4 +- 2.7) kHz VLDB+ OFF

(ON-OFF) = (1.9 +- 3.3) kHz

→ compatible with zero. Note that some kHz is however close to DCR @ - 30 C
→ need to move to -30 C to check

additional home-made "full VTRX+ plastic box"

Going shorter and avoid dangling?
We considered several options but for each of them the number of cons largely exceeds the pros. And if too short we can't come back. We don't have any convincing option for such scheme.

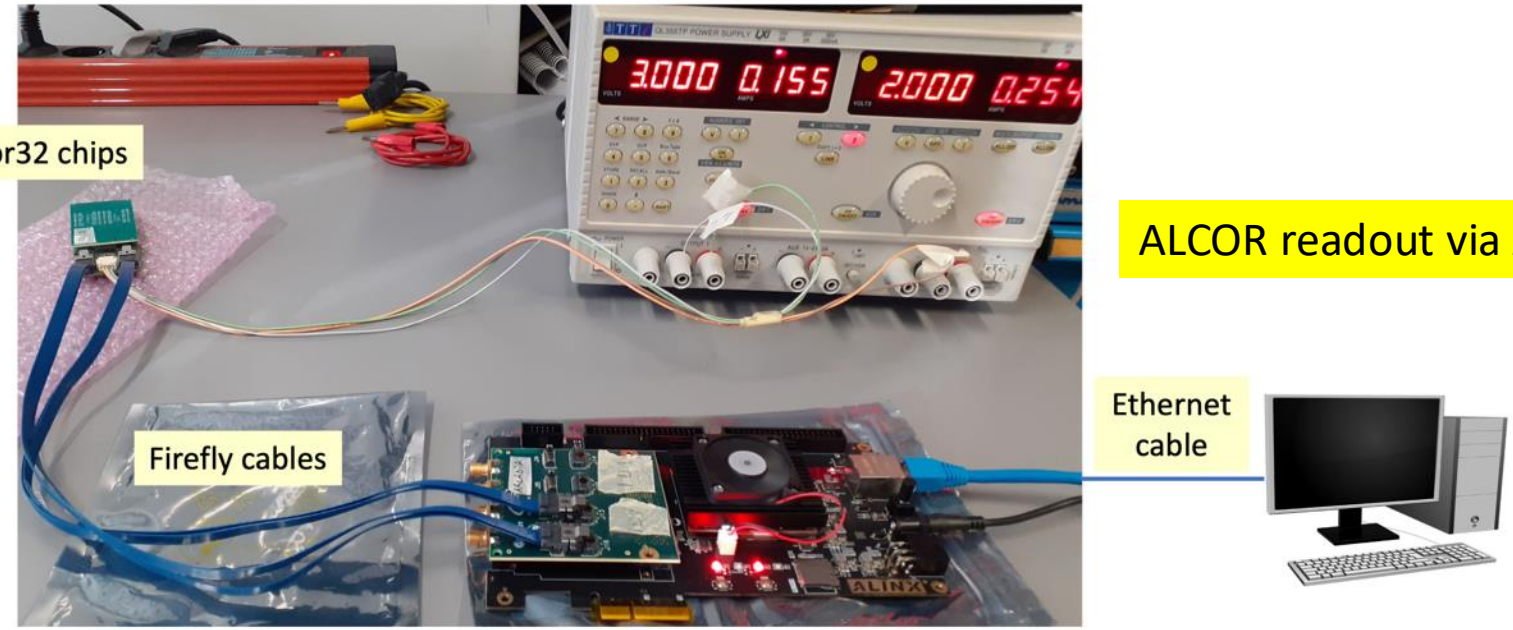
How to proceed? We go baseline
We select a 20 cm dangling pigtail
Design needs to be carefully followed up to setup proper access, secure maintenance etc. (but this is valid for almost what we are doing ;-)

dRICH option: 1500 VTRX+ with total length 20 cm

See PA's presentation at eRD109 (Feb. 2025)

RDO firmware progresses (I)

- pin placement for layout design
- intense use of ALINX AUX15P evb card (same FPGA) as RDO GYM (waiting for real cards!)



ALCOR readout via AUX15P

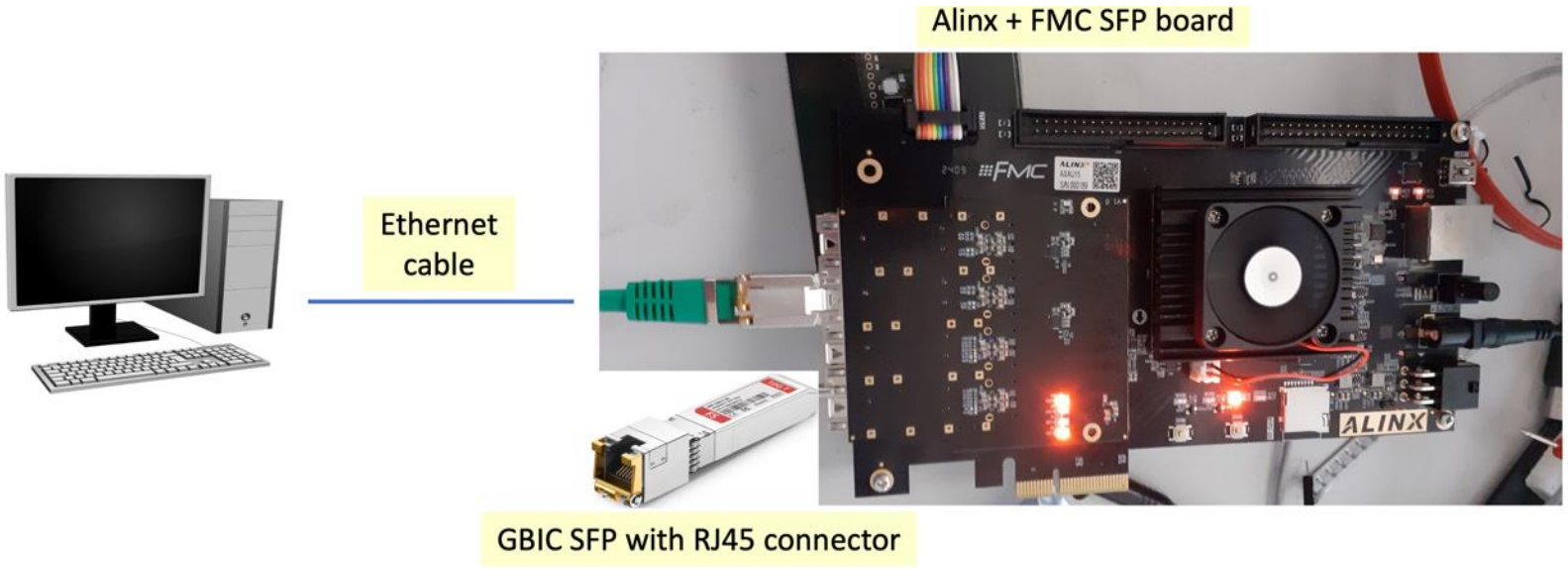
Ethernet cable

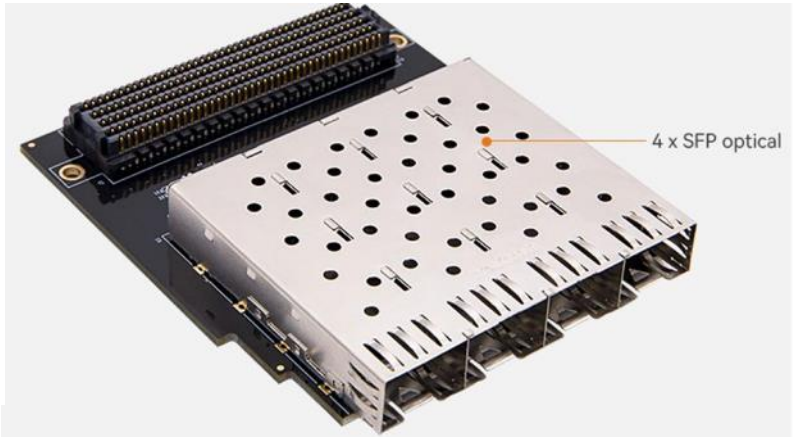
In order to test the Artix – Alcor interface, we implemented the IPbus firmware on the FPGA. Now we can program the Alcor registers via SPI and we can correctly receive the data

successfully ported KC705 FW (reading ALCOR) to AUX15P including SERDES
More details in D. Falchieri's talk at Electronics and DAQ WG/eRD109 (May 2025)

RDO firmware progresses (II)

- pin placement for layout design
- intense use of [ALINX AUX15P evb card] (same FPGA) as RDO GYM (waiting for real cards!)





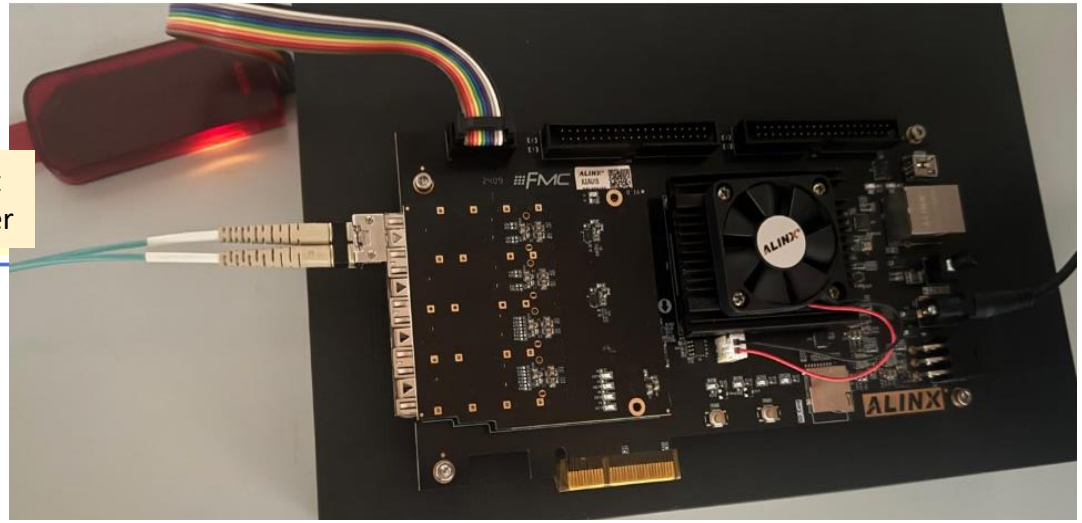
successfully implemented IPBUS communication over optical link (commercial SFP), first with GBIC SFP then with fiber

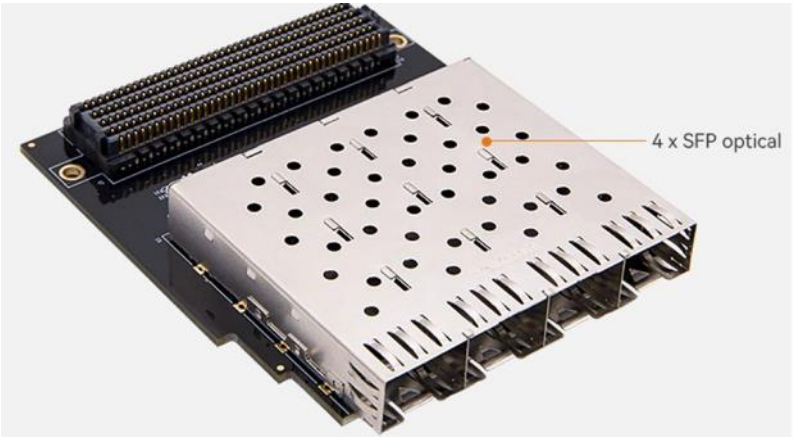
“collecting pieces of the firmware needed on RDO”
next: PLL programming at FPGA boot via I2C + uC FW

RDO firmware progresses (II)

- pin placement for layout design
- intense use of ALINX AUX15P evb card (same FPGA) as RDO GYM (waiting for real cards!)

Ethernet over fiber



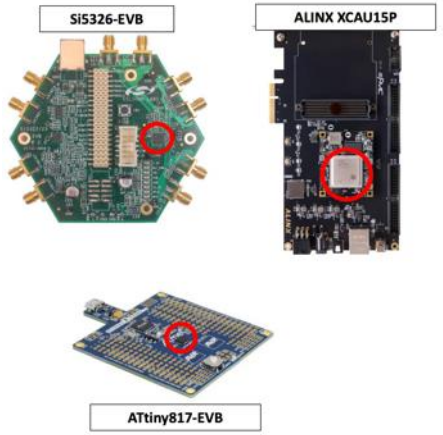


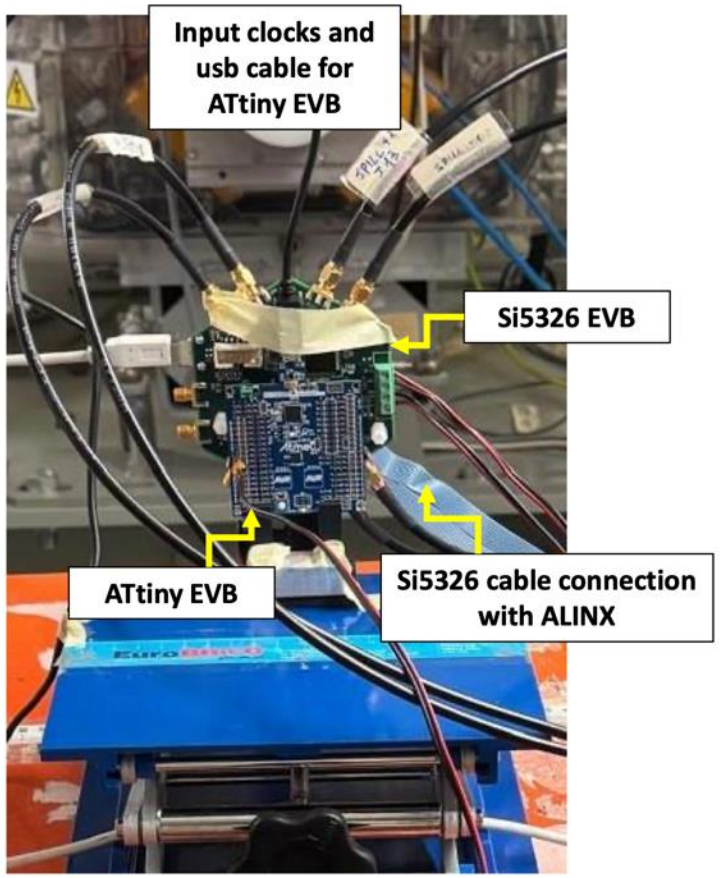
successfully implemented IPBUS communication over optical link (commercial SFP), first with GBIC SFP then with fiber:
→ configuration foreseen for test beam

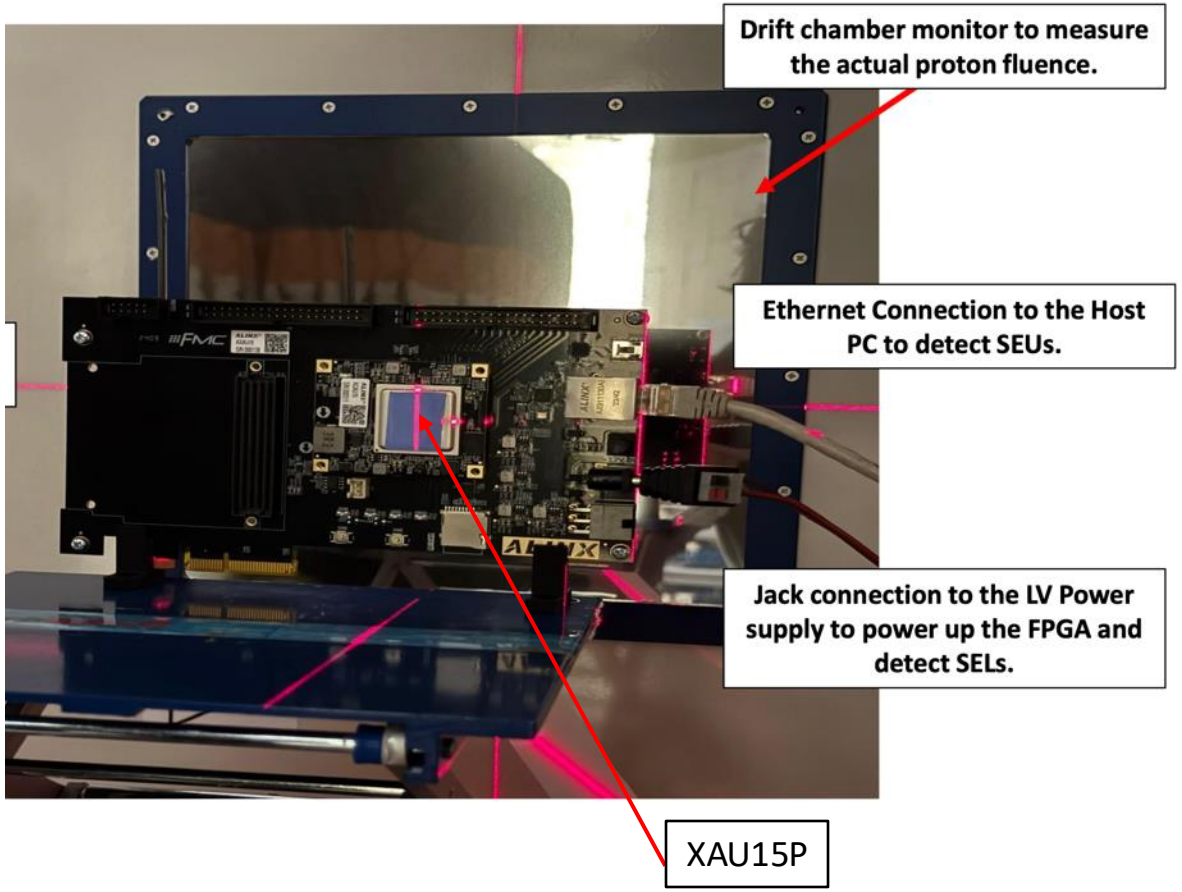
"collecting pieces of the firmware needed on RDO"
next: PLL programming at FPGA boot via I2C + uC FW

Irradiation tests

- Waiting for full RDO we tested several key components: PLL (Si5326), uC (ATtiny417) and AMD FPGA (AUX15P)
- irradiation with a proton beam at Centro di Protonterapia in Trento / December 2024
- TID ≅2.3 krad (1000 fb^{-1}) and Φ(h>20 MeV) ≅700 Hz/cm2 (including a safety factor 5)







See presentation by S.Geminiani @ePIC Collaboration meeting (Jan 2025)

Irradiation tests

MTBF= Mean Time Between Failure
SEU = Single Event Upset
SEL = Single Event Latchup

from conclusions presented in January:

1. We integrated $\mathbf{TID \sim 2.8 \cdot TID_5}$ for the AU15P, $\mathbf{TID \sim 10 \cdot TID_5}$ for the ATtiny and $\mathbf{TID \sim 18 \cdot TID_5}$ for the Si5326.

   No significative cumulative effect or SEL for Si5326 and AU15P, while the **ATtiny stopped working at TID = 23 krad**.

   → **Devices tested up to a TID largely exceeding expected TID @dRICH: no destructive effects seen for $\mathbf{TID \leq TID_5}$**

2. **Si5326: MTBF = 3.8 h (for 1248 RDOs)** and the jitter analysis showed the **output clock is very stable.**

   → **The RDO AU15P will control the chip configuration every $t \ll 3.8$ h.**

3. **ATtiny: SRAM MTBF = 4 h** and **FLASH MTBF > 43 h (for 1248 RDOs)** .

   → **The FLASH MTBF is a safety limit and key RAM registers will be implemented with TMR checks.**

Comments: investigation addendum for ATtiny + first measurements of this kind in ePIC

RDO power consumption estimates

LV Channel	Device	LDO	Vin (V)	Vout (V)	Iout (A)	Vdrop (V)	Ptotal (W)	Pdevice (W)	Ploss (W)
LVH 2.7 V	AUX15P	LTM4709-1H	2.7	1.20	0.1070	1.50	0.289	0.128	0.161
		LTM4709-2H	2.7	1.80	0.4820	0.90	1.301	0.868	0.434
		LTM4709-3H	2.7	2.50	0.0060	0.20	0.016	0.015	0.001
	MPF050T	LTM4709-2H	2.7	1.80	0.0025	0.90	0.007	0.005	0.002
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	VTRX+	LTM4709-1H	2.7	1.20	0.0150	1.50	0.041	0.018	0.023
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	MT25QU01	LTM4709-2H	2.7	1.80	0.0550	0.90	0.149	0.099	0.050
	Si5326	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	Si5319	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	TMP119	LTM4709-3H	2.7	2.50	0.0005	0.20	0.001	0.001	0.000
	ATtiny417	ADP1752	2.7	2.50	0.0030	0.20	0.008	0.008	0.001
	I2Cexp-4FEB	LTM4709-3H	2.7	2.50	0.0680	0.20	0.184	0.170	0.014
	LED		2.7	2.70	0.0000	0.00	0.000	0.000	0.000
	IBIAS-LDOH		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	IBIAS-LDOL		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	Total LV 2.7				**1.4290**		**3.86**	2.69	1.16
LVL 1.4 V	AUX15P	LTM4709-1L	1.4	0.85	1.6530	0.55	2.314	1.405	0.909
	AUX15P	LTM4709-2L	1.4	0.90	0.0430	0.50	0.060	0.039	0.022
	MPF050T	LTM4709-3L	1.4	1.00	0.2580	0.40	0.361	0.258	0.103
	Total LV 1.4				**1.9540**		**2.736**	1.702	1.034

Device	Total Power (W)	Area (mm2)	W/mm2
AUX15P	2.455	361	6.80
MPF050T	0.438	121	3.62
LDOH	1.155	72	16.04
LDOL	1.034	72	14.36
SI5326	0.457	36	12.70
SI5319	0.457	36	12.70
VTRX+	0.193	100	1.93

FPGA power consumption simulated **not completely** given FW is incomplete

Take home message:

1.5 A @ 2.7 V
2.0 A @ 1.4 V

→ **> ≈ 7 W/RDO**

discussed@dRICH Power Day (Ferrara 10 June)
PA's talk

RDO power consumption estimates

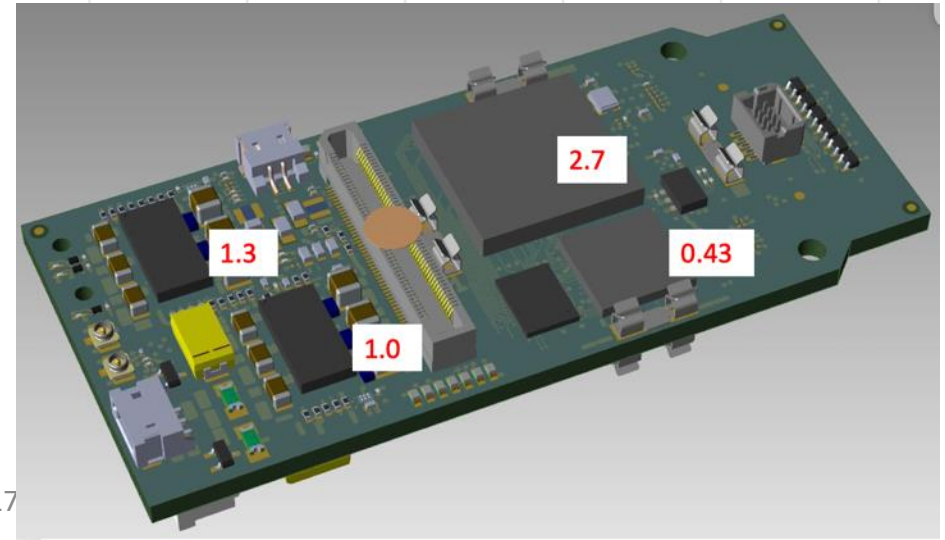
LV Channel	Device	LDO	Vin (V)	Vout (V)	Iout (A)	Vdrop (V)	Ptotal (W)	Pdevice (W)	Ploss (W)
LVH 2.7 V	AUX15P	LTM4709-1H	2.7	1.20	0.1070	1.50	0.289	0.128	0.161
		LTM4709-2H	2.7	1.80	0.4820	0.90	1.301	0.868	0.434
		LTM4709-3H	2.7	2.50	0.0060	0.20	0.016	0.015	0.001
	MPF050T	LTM4709-2H	2.7	1.80	0.0025	0.90	0.007	0.005	0.002
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	VTRX+	LTM4709-1H	2.7	1.20	0.0150	1.50	0.041	0.018	0.023
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	MT25QU01	LTM4709-2H	2.7	1.80	0.0550	0.90	0.149	0.099	0.050
	Si5326	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	Si5319	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	TMP119	LTM4709-3H	2.7	2.50	0.0005	0.20	0.001	0.001	0.000
	ATtiny417	ADP1752	2.7	2.50	0.0030	0.20	0.008	0.008	0.001
	I2Cexp-4FEB	LTM4709-3H	2.7	2.50	0.0680	0.20	0.184	0.170	0.014
	LED		2.7	2.70	0.0000	0.00	0.000	0.000	0.000
	IBIAS-LDOH		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	IBIAS-LDOL		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	Total LV 2.7				**1.4290**		**3.86**	2.69	1.16
LVL 1.4 V	AUX15P	LTM4709-1L	1.4	0.85	1.6530	0.55	2.314	1.405	0.909
	AUX15P	LTM4709-2L	1.4	0.90	0.0430	0.50	0.060	0.039	0.022
	MPF050T	LTM4709-3L	1.4	1.00	0.2580	0.40	0.361	0.258	0.103
	Total LV 1.4				**1.9540**		**2.736**	1.702	1.034

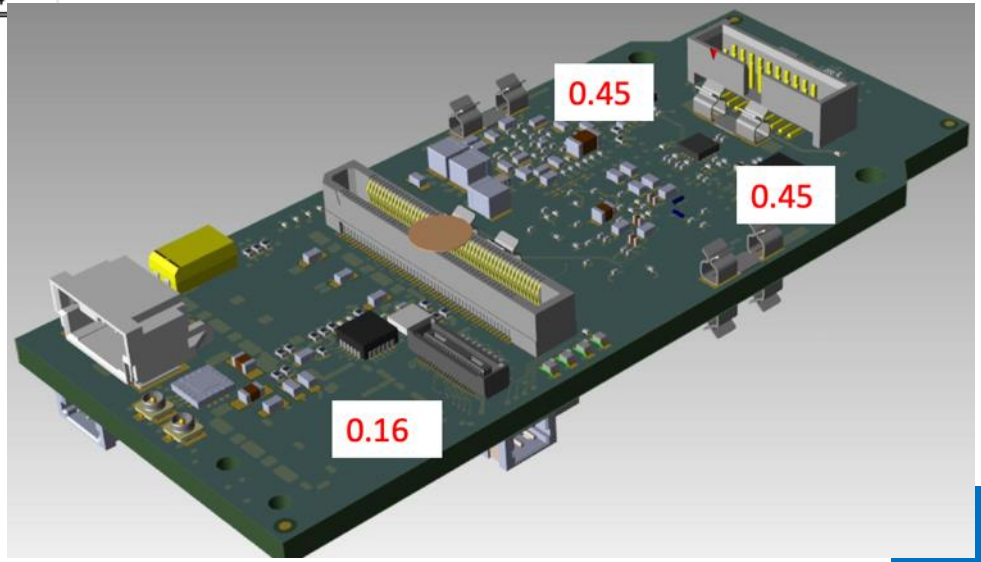
Actual FPGA power consumption simulated **not completely** given FW is incomplete

Take home message:

1.5 A @ 2.7 V
2.0 A @ 1.4 V

→ **> ≈ 7 W/RDO**



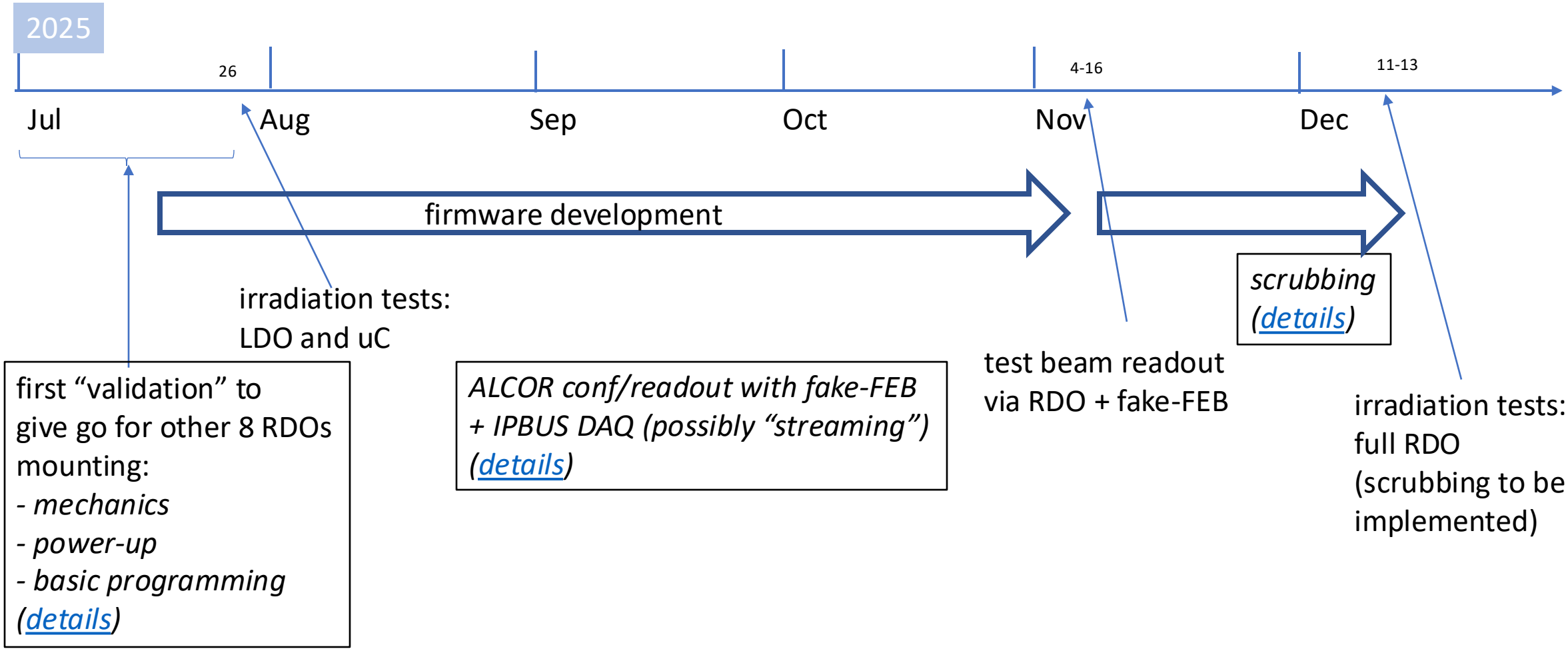


RDO cost estimates

- First estimate of production cost : 489 k€ (1500 cards + all components not including FPGAs and VTRx+, mounting)
- FPGA: 256 k€ (ARTIX) + 187 k€ (PF)
- Grand Total: 932 k€ + VAT = **1.1 M€** (not including VTRX+ costs, provided by EIC project)
- Almost in line with current budgeting (900 k€ + VAT)
- To be defined which production tests to be outsourced to ext. company

Spending could be distributed over two years buying in advance FPGAs?

Plannning and validation tests



2026 *remote programming, ePIC link implementation, test with FELIX, QA production test card (details)*

lpGBT protocol as EIC link protocol for dRICH?

PicoDAQ development --- Streaming DAQ Milestones

Detector Install: FY29Q2 - FY31Q2
Cosmics: FY31Q3
Early CD-4: FY32Q4

DAQ Releases:

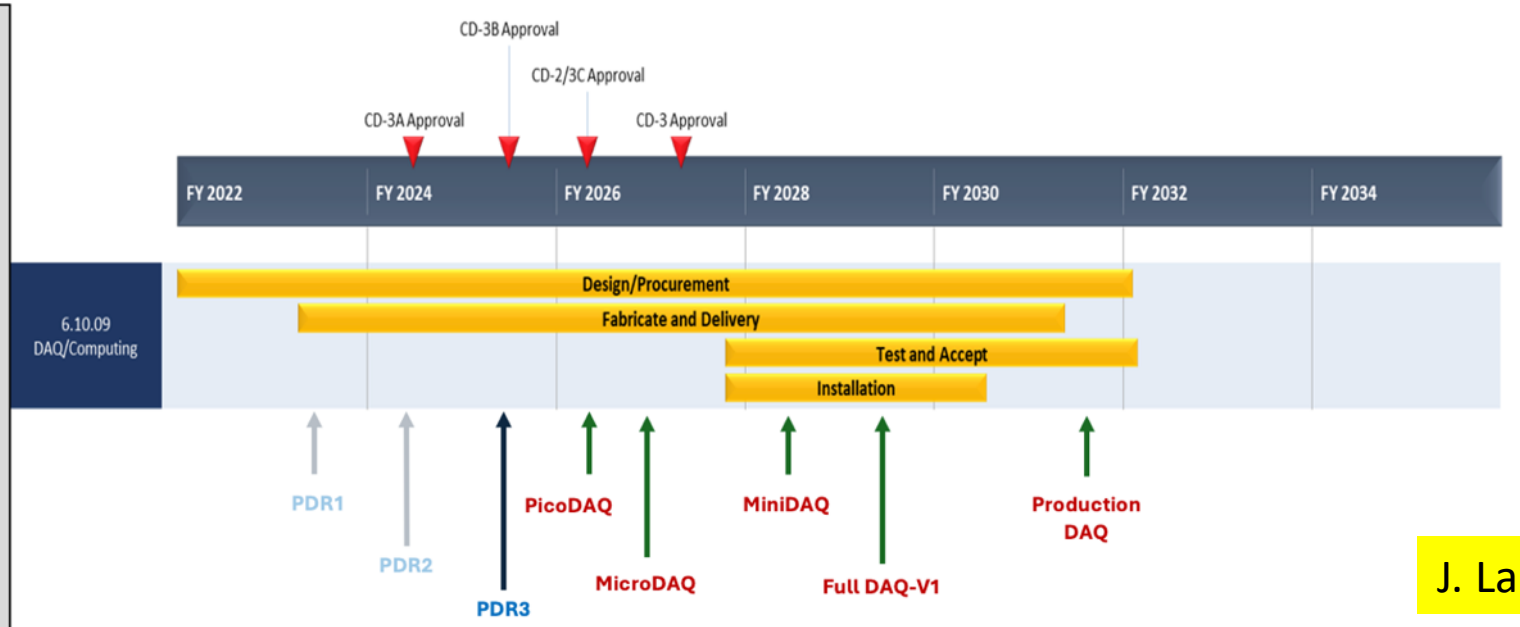
PicoDAQ FY26Q1
Readout test setups

MicroDAQ: FY26Q4
Readout detector data in test stand using engineering articles

MiniDAQ: FY28Q1
Readout detector data using full hardware and timing chain

Full DAQ-v1: FY29Q2
Full functionality DAQ ready for full system integration & testing

Production DAQ: FY31Q3
Ready for cosmics



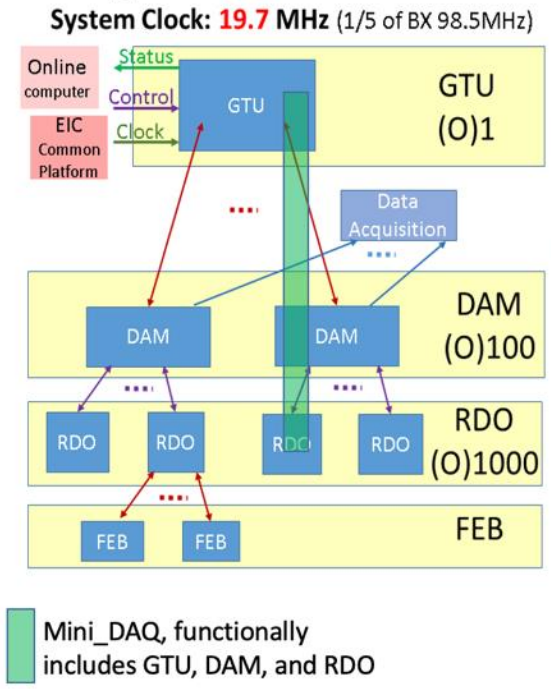
J. Landgraf

- The "EIC" link protocol is not yet there
- "MicroDAQ" will not provide that
- ALINX AUX15P is now popular and there are ideas to use it as "proto-RDO", proto-DAM and proto-GTU

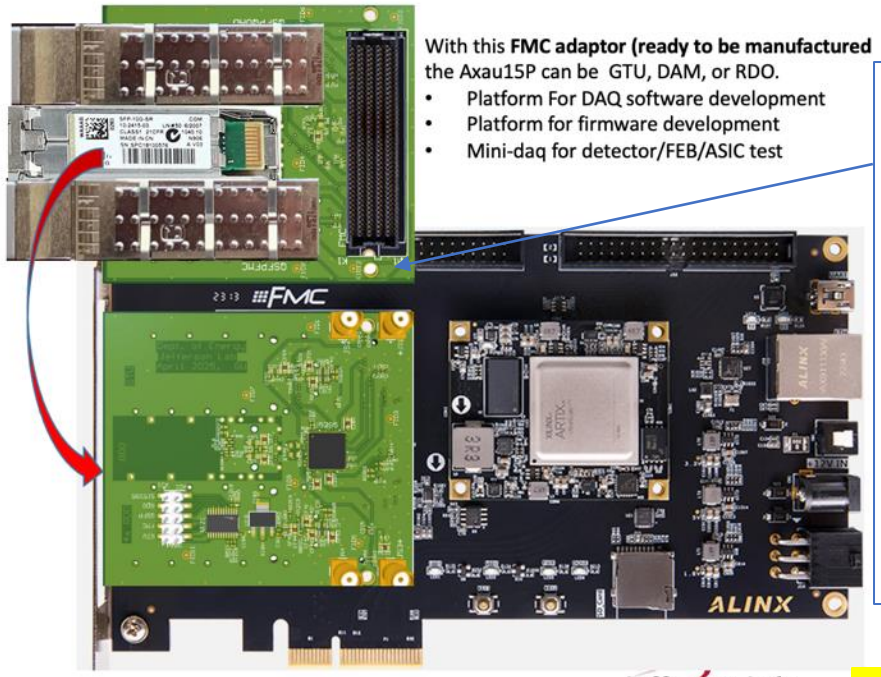
lpGBT protocol as EIC link protocol for dRICH?

this is to support detectors with lpGBT, but per se we could consider to use lpGBT protocol (this could make life easier with FELIX and for Rome1 Colleagues)

1. The ePIC designs



2. FMC/(Q)SFP adaptor



Once this piggy back card is produced (by JLab), this would allow us to use a pair of ALINX/AUX15P to mimic a "RDO" and a "FELIX" link

And we could use our RDO at that point...

ALINX AUX15P is regarded in ePIC as main initial development board.

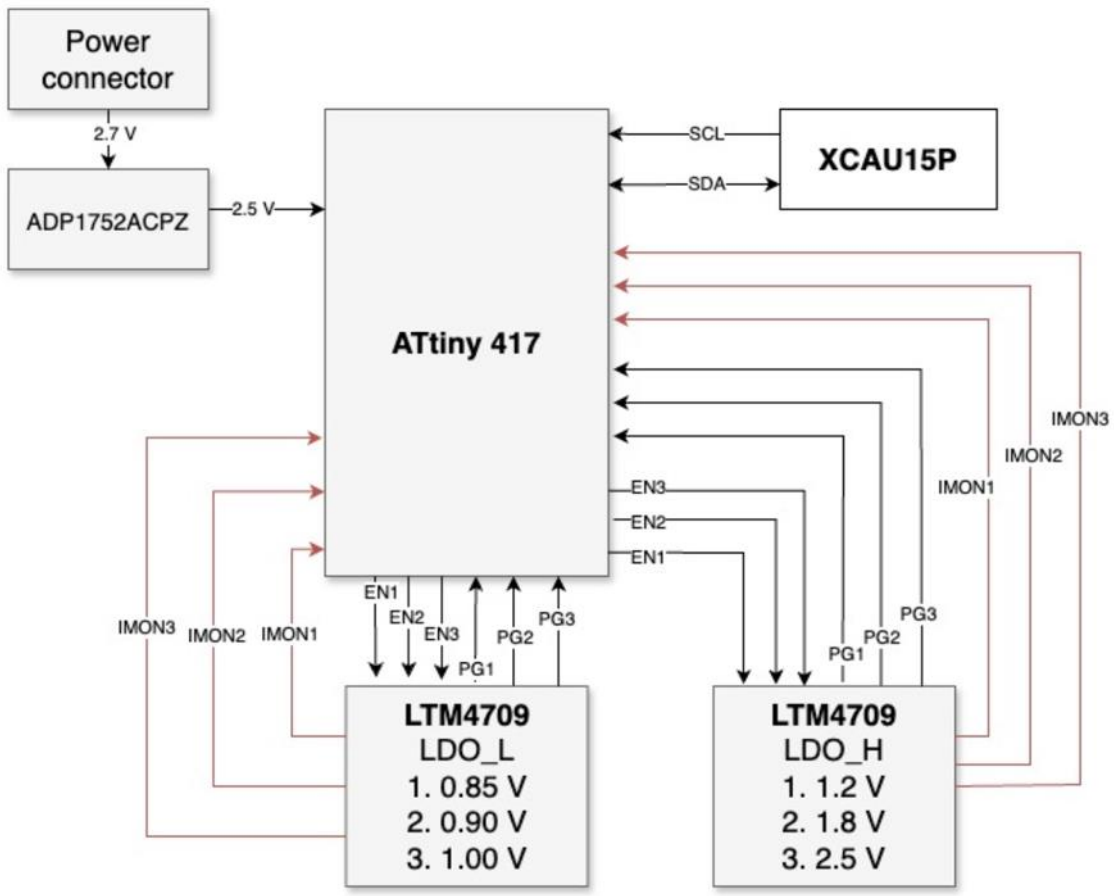
W. Gu

Summary

- eager to test real RDO prototypes (exp. 30 June)
- many pieces of work validating / to validate step by step design choices
- a lot of work ahead of us!
- we need to be sure by 2026 we are production-ready for RDO
- validating mysterious “EIC link” + overall PDU integration (incl. cooling and light shielding…) are main challenges

Backup

RDO power management



ATtiny417: Datasheet

ATtiny417 provides monitoring of “power good” signals and current monitoring

I^2C interface with AUX15P to report current values

L. Rignanese

RDO next steps for go for production (8 RDOs)

1. Mechanical pairing with fake-FEB
2. Power-up : 2.5 / 1.4 jumper to avoid power to other sections
3. Prg uC via external connector
4. Power-up with uC (post-programming uC): check Vout LDO
5. Prg Artix via external connector
6. Prg Polarfire via external connector
7. Prg Artix → SkyWorks (programming 125 MHz of Si5319)
8. Check consumptions
9. Check UFL I/Os
10. Link IPBUS via VTRX+ [MT-MPO adapter + "polipo"]
11. Prg ALCOR via fake-FEB (via IPBUS → VTRX+)
12. ALCOR readout (via IPBUS → VTRX+)

Note: we can't test everything before give the "go" for next 8 RDOs...

RDO next steps for test beam

1. External clock processed by SI5326 (note: we need 16 SMA-UFL cables)
2. Readout of all I2C sensors
3. I2C programming of regulators on fake-FEB
4. Manage different IP (without jumpers)
5. Cooling ?!
6. A mini rack: 8 RDO + fake-feb on both sides etc...

Optional (bonus):

1. IPBUS + UDP streaming

RDO next steps per test @TIFPA

1. Writing QSPI Flash via SPI (writing via JTAG)
2. Scrubbing
3. Comunication between PolarFire and Artix
4. Current monitor via uC
5. Communication between uC and ARTIX

Optional (bonus):

1. Polarfire program ARTIX at boot
2. QSPI Flash writing via IPBUS (Remote Programming!)
3. During the test: one fake-feb connected and we read 2 ALCOR32? (note: ALCOR not exposed to radiation)

RDO next steps towards full ePIC DAQ

- Check noise from charged pump
- Check noise (light) from VTRX+ / engineer “shield”
- Link EIC → clock reconstruction (need project input)
- Clock at 394 MHz/ ALCOR@394 MHz
- Polarfire program Artix at boot
- Remote programming (writing PolarFire via VTRX+)
- Remote programming (writing Flash memory via VTRX+)
- IPBUS —> EIC link over VC709/707
- Data format // buffering // “frame”
- Test with ALCOR64 + FEB
- Test with FELIX
- test in campo magnetico (PDU)
- PDU in detector box etc…

TB2026: dismount leds!!
TB2026: le FEB sono compatibili con RDO25

- **pre-production** during 2026 (if we don't need it before) “RDO26”
- test card for testing RDO