Digital SiPM for Dual-readout calorimetry and the ASPiDeS program

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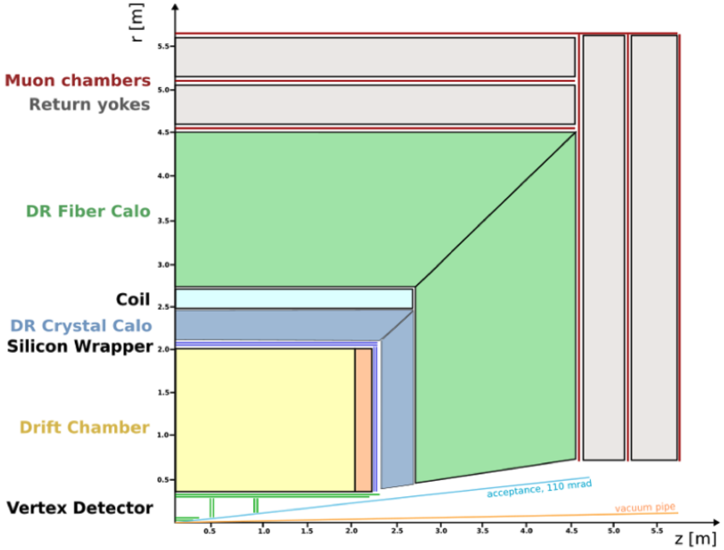
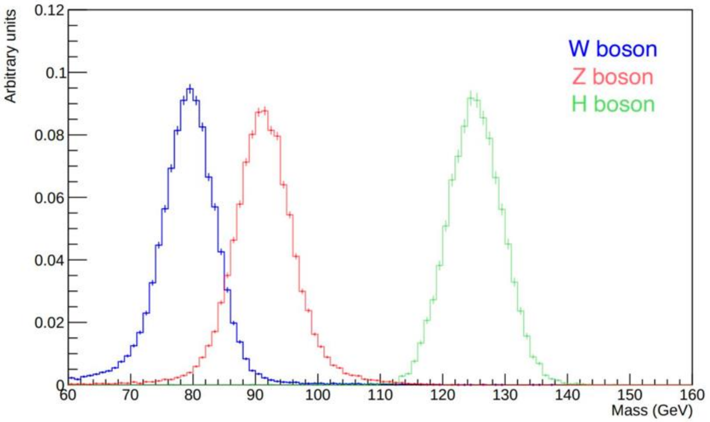
IDEA: new baseline concept

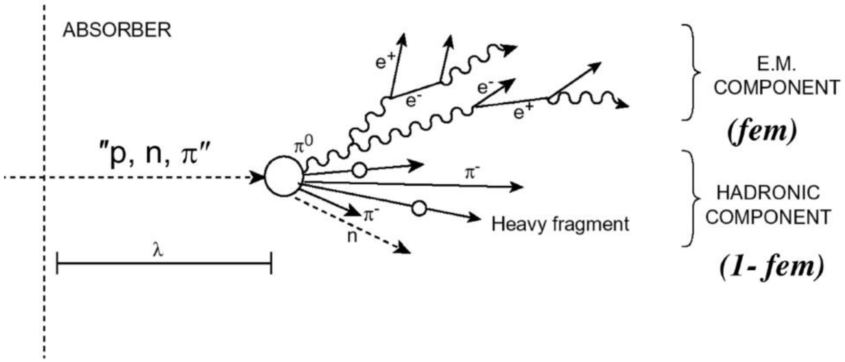
- Beam pipe: R ≈1.0 cm
- Highly transparent tracking
  - Si pixel vertex detector (monolithic technology)
  - Drift Chamber
  - Si wrappers (strips)
- Dual-readout crystal ecal: ≈ 22 X_0
- Thin superconducting solenoid: 3 T
- Dual-readout calorimetry 2 m / 7 λ_{int}
- Muon chambers
  - μ-RWELL in return yoke



Target jet-jet mass resolution $\frac{\sigma}{E} = \frac{30\,\%}{\sqrt{E}}$



Dual-Readout: the principle



- Non compensating calorimeter (h/e<1): has a different response to electromagnetic (fem) and hadronic component (1-fem)
- The fem is energy dependent: it induces a non-linear calorimetric response to hadrons and large fluctuations

- By reading two calorimetric signals (S and C) with different h/e, the fem can be measured event by event and the compensation can be achieved off-line

$$E_S = E\left(f_{\rm em} + \left(\frac{h}{e}\right)_S (1 - f_{\rm em})\right)$$

$$E_C = E\left(f_{\rm em} + \left(\frac{h}{e}\right)_C (1 - f_{\rm em})\right)$$

$$E = \frac{(E_S - \chi E_C)}{1 - \chi}$$

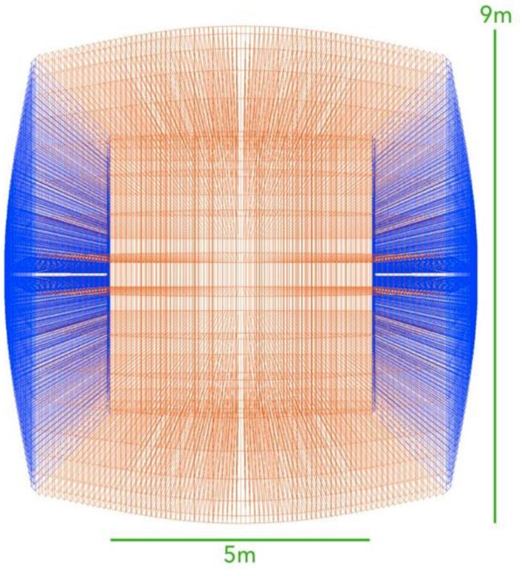
$$\chi = \frac{1 - \left(\frac{h}{e}\right)_S}{1 - \left(\frac{h}{e}\right)_C}$$

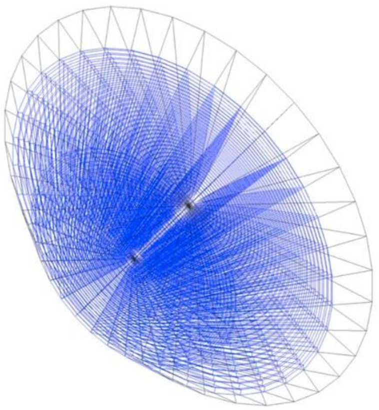
χ does not depend from energy and particle type. It is detector dependent: it can be measured on beam tests

S. Lee et al, RevModPhys, 90, 025002 (2018)
DOI: 10.1103/RevModPhys.90.025002

Dual-Readout in IDEA

- Almost 75 millions of 2 mm outer diameter stainless steel tubes
- In each tube there is a 1 mm diameter fibre connected to a SiPM
- Signals from 8-SiPMs grouped to reduce the number of channels to be read out



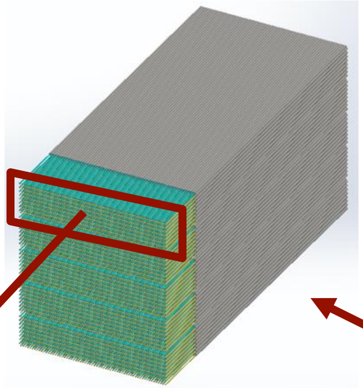


HiDRa project (supported by INFN) aims to identify a scalable and cost-effective solution to build a dual-readout calorimeter for IDEA.

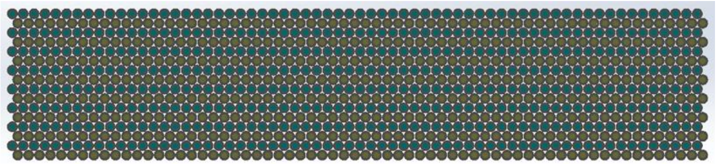
HiDRa: High-Resolution Highly Granular Dual-Readout Demonstrator

The Module

5 Mini-modules
~ 13 x 13 x 250 cm^3



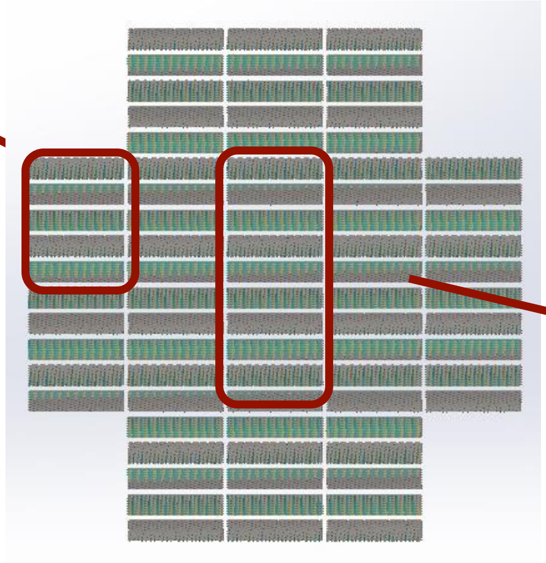
The Mini-Module



64 x 16 stainless steel capillaries, 2 mm outer diameter, equipped with scintillating and clear fibres (alternated in rows) to apply the dual-readout method

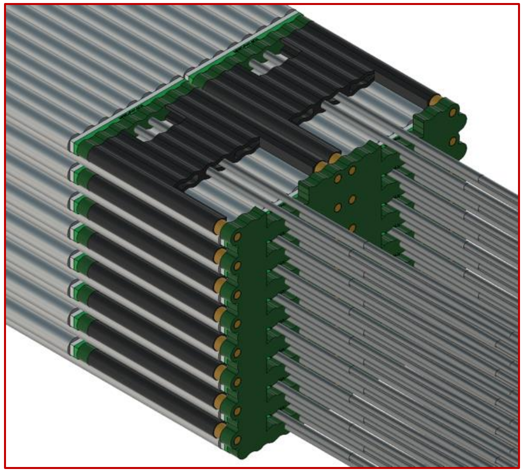
The HiDRa prototype

Designed to be scalable and large enough to measure the hadronic performances



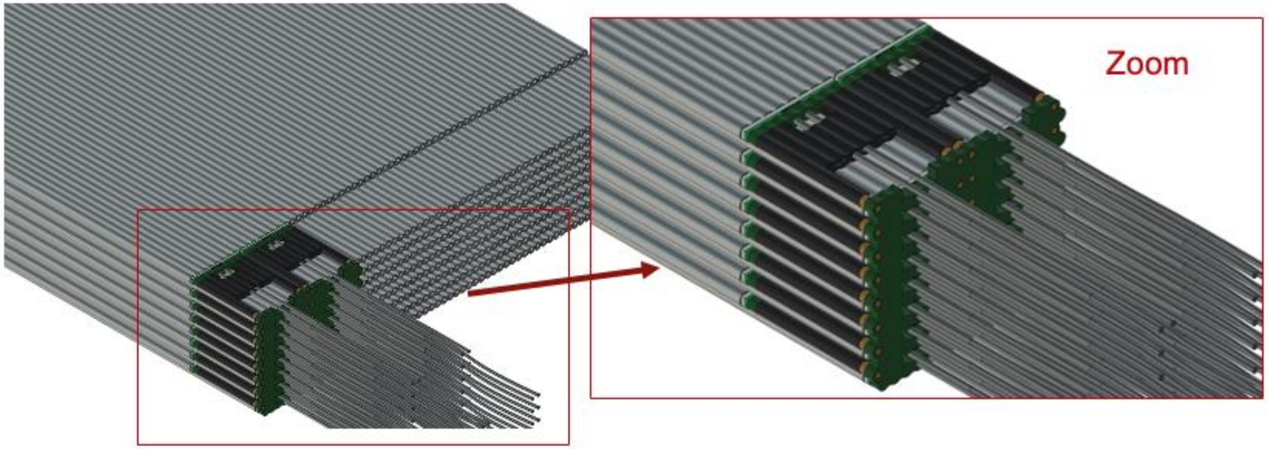
The highly granular modules

Two central modules read out with 10k SiPMs (one per fibre)

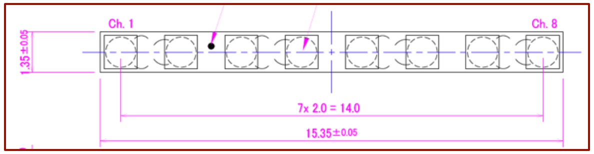


Challenging integration requiring a precise assembly procedure and the use of compact components (i.e. SiPMs, services and mechanical) to fit in the back of the calorimeter

Integration of highly granular modules



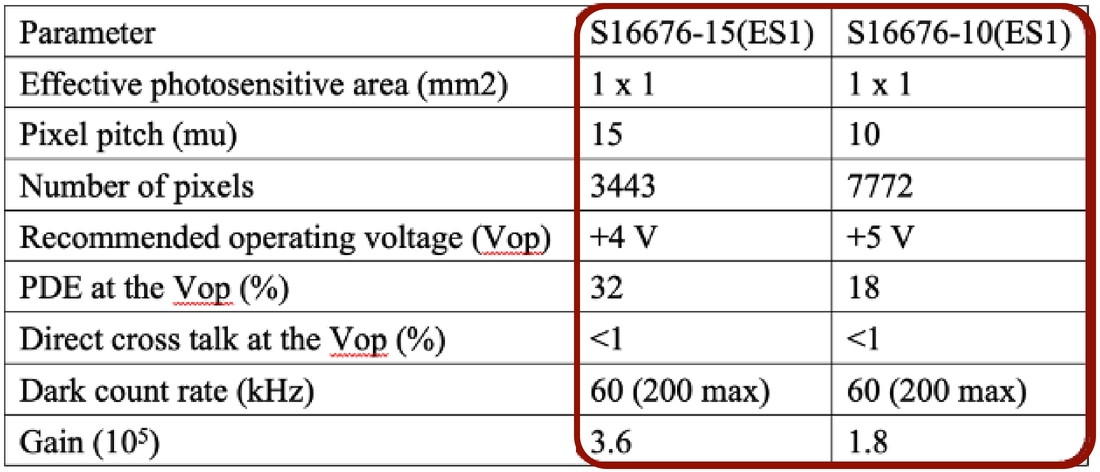
SiPM with 10 μm pitch for scintillating and 15 μm pitch for Cherenkov light



Customised package with 8 SiPMs, 2 mm spaced (S16676-15 / S16676-10)

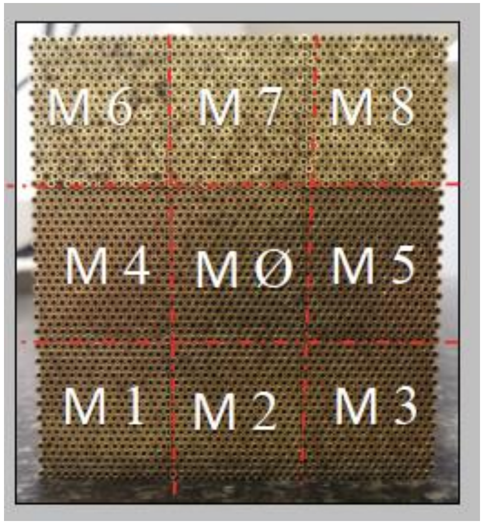
Analogue signals from 8 SiPMs connected in parallel

SiPM parameters (Hamamatsu datasheet)

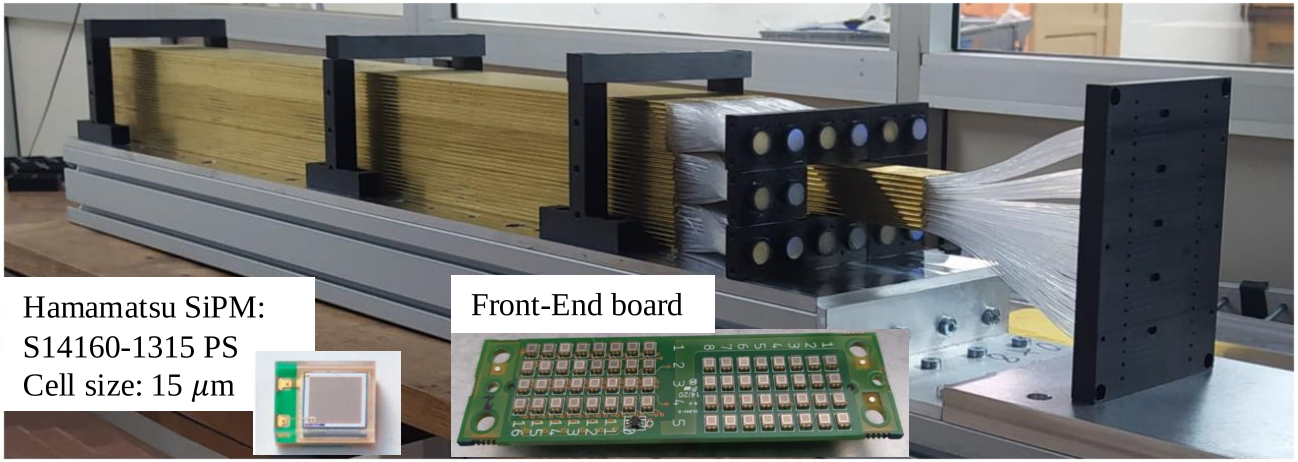


Parameter	S16676-15(ES1)	S16676-10(ES1)
Effective photosensitive area (mm2)	1 x 1	1 x 1
Pixel pitch (mu)	15	10
Number of pixels	3443	7772
Recommended operating voltage (Vop)	+4 V	+5 V
PDE at the Vop (%)	32	18
Direct cross talk at the Vop (%)	<1	<1
Dark count rate (kHz)	60 (200 max)	60 (200 max)
Gain (10^5)	3.6	1.8

The EM-size prototype tested on beam (2021 and 2023)

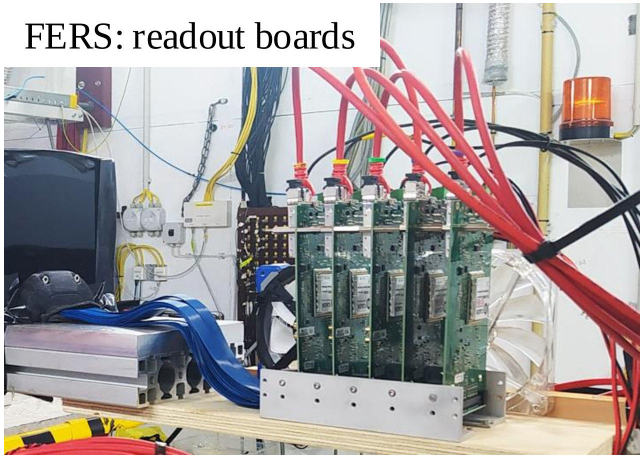


- EM-size prototype (10x10x100 cm^3)
  - 9 modules made of 16 x 20 capillaries (160 C and 160 Sc)
  - Brass capillaries: 2 mm outer diameter and 1.1 mm inner diameter
- EM-size prototype readout
  - Each capillary of the central module is equipped with its own SiPM: highly granular readout
  - 8 surrounding modules equipped with PMTs (each module will use 1 PMT for C and 1 PMT for Sc fibres)



Hamamatsu SiPM:
S14160-1315 PS
Cell size: 15 μm

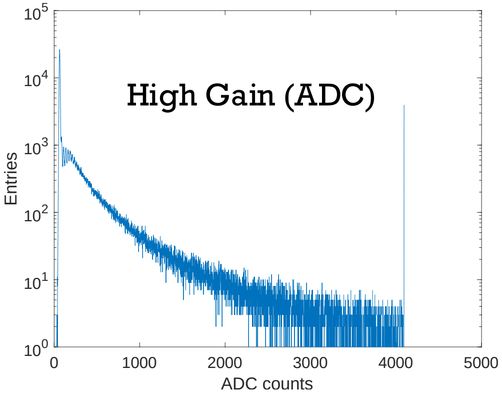
Front-End board

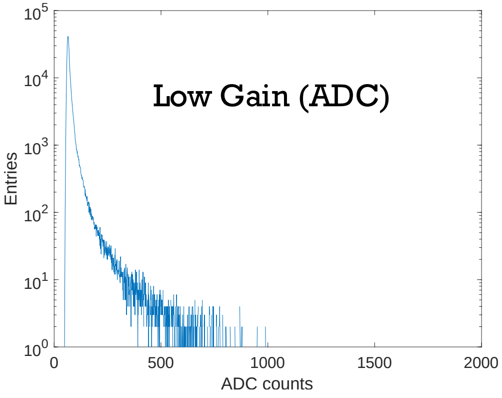


FERS: readout boards

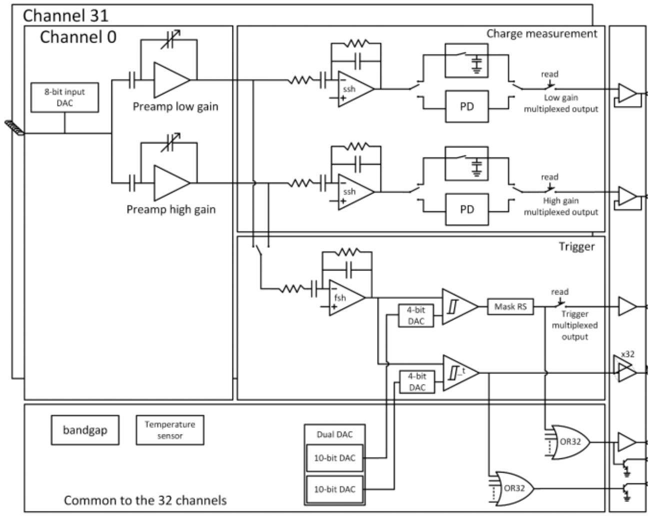
The importance of SiPM equalisation

We need single photons resolution and large dynamic range



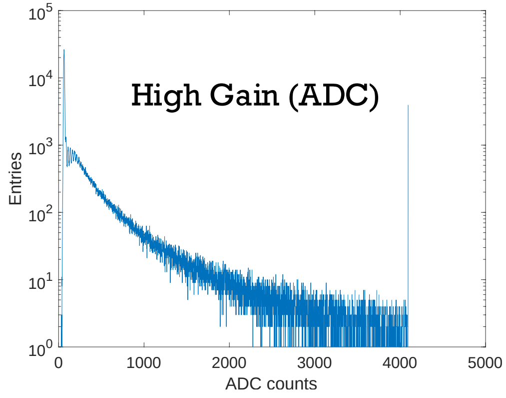


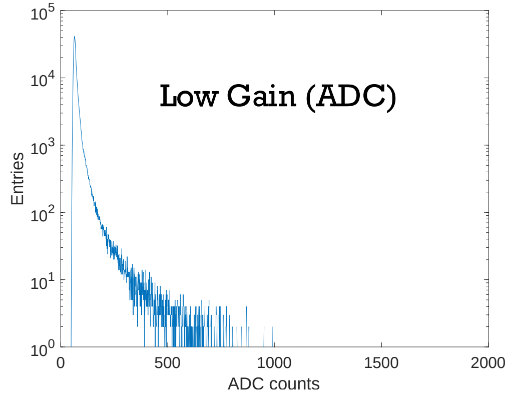
Citiroc1A – block-schema

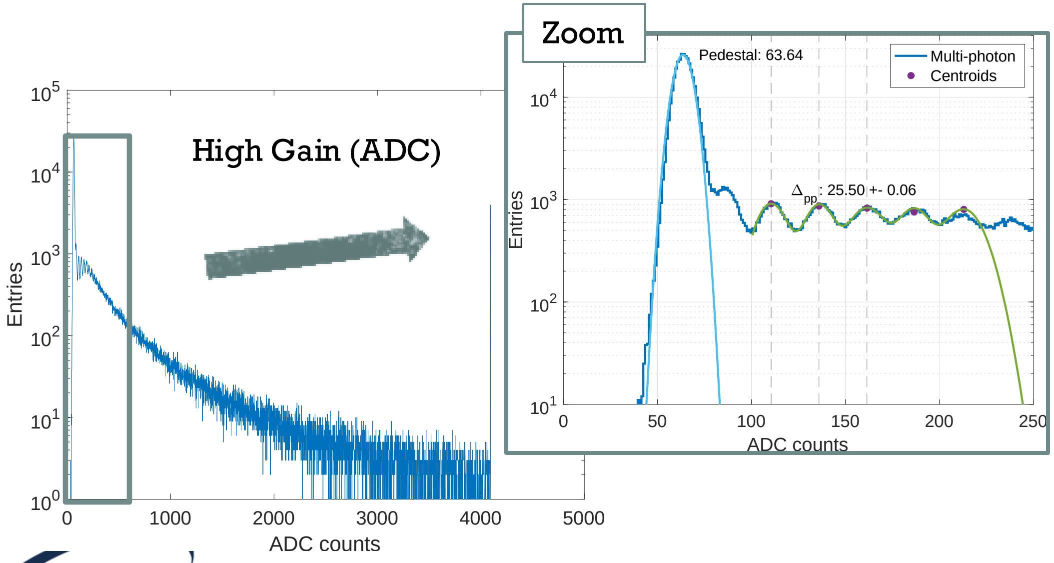


The importance of SiPM equalisation

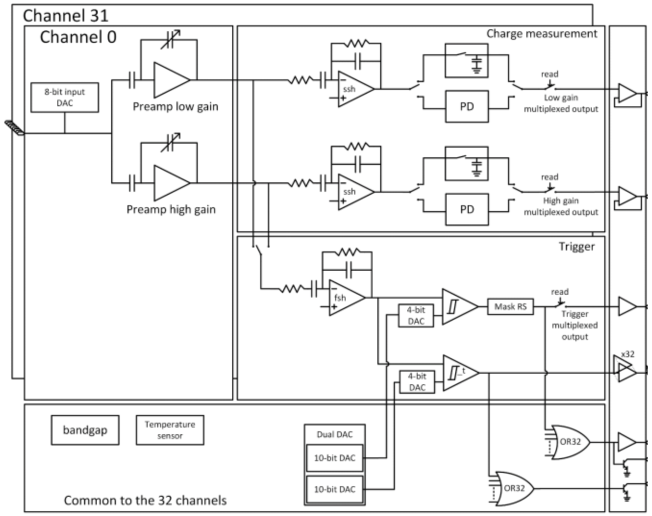
We need single photons resolution and large dynamic range







Citiroc1A – block-schema



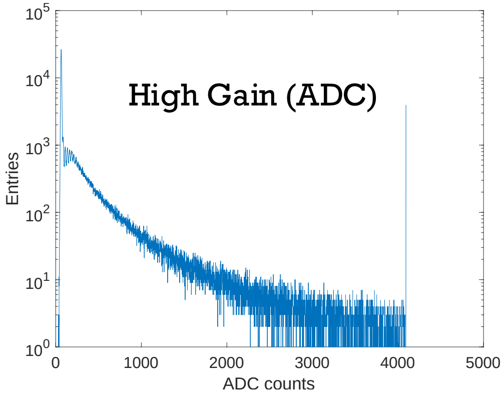
HG equalisation

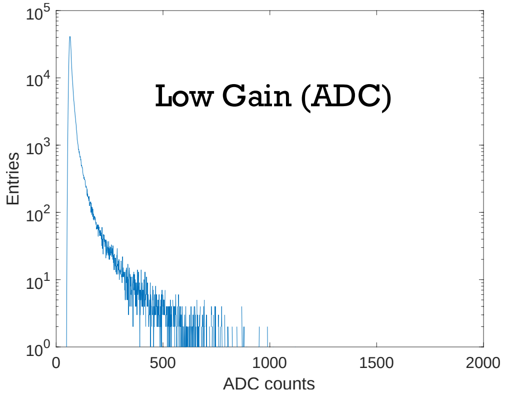
Dpp: used to convert ADC in Ph-e (monitored in all runs and for all SiPMs)

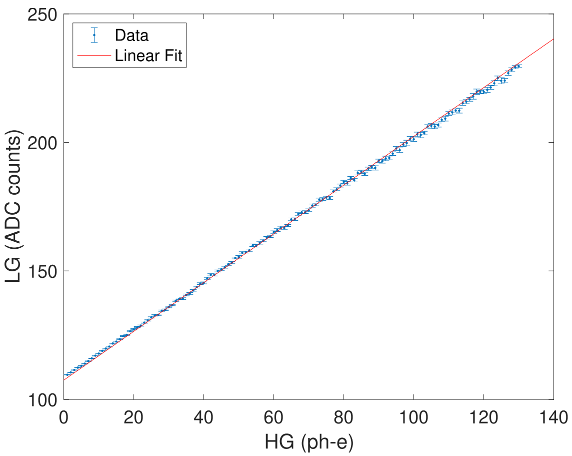
Pedestal width: used to measure the noise contribution to the energy resolution

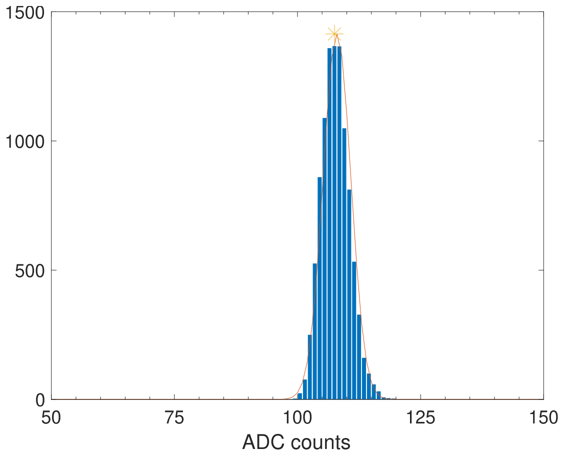
The importance of SiPM equalisation

We need single photons resolution and large dynamic range

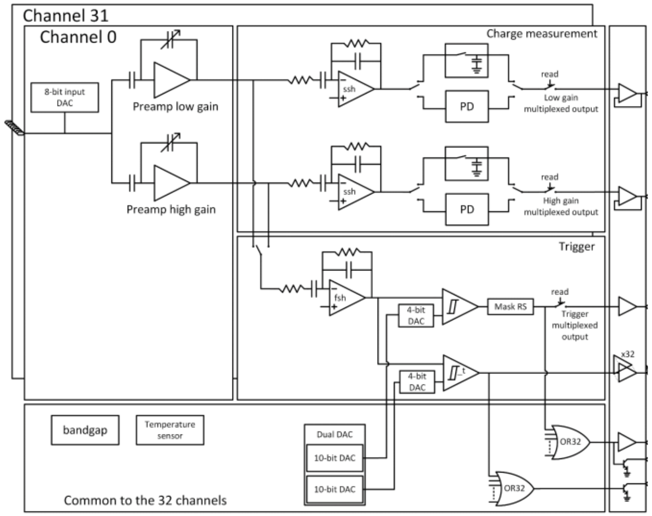








Citiroc1A – block-schema

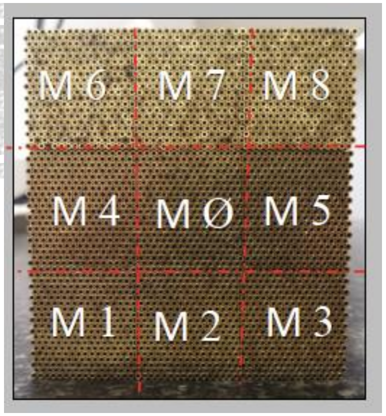


LG equalisation

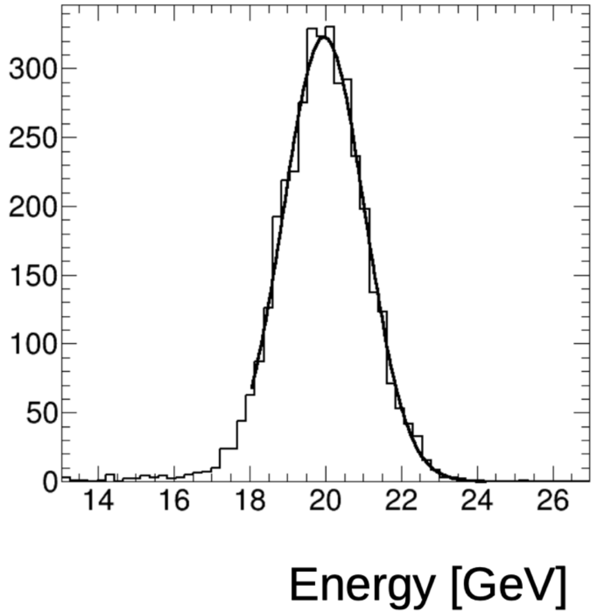
Slope of the correlation plot provides the ADC to Ph-e conversion factor

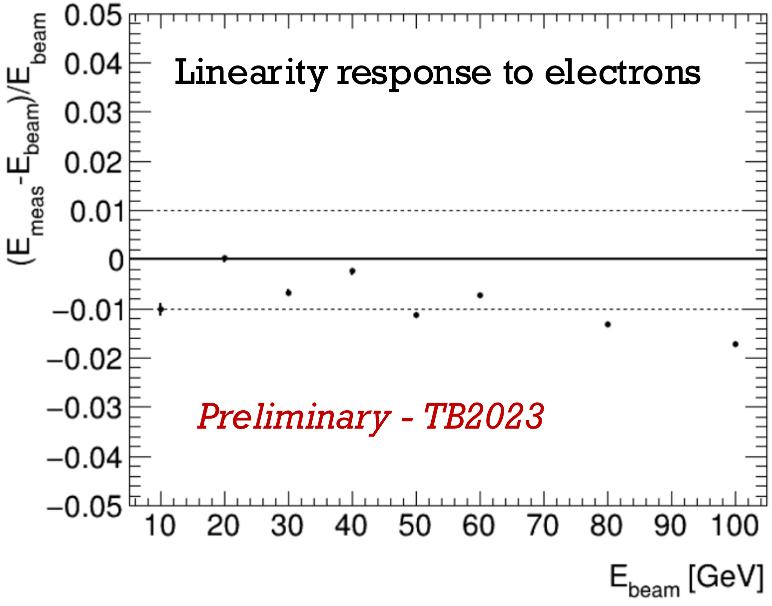
Pedestal width measured selecting noise events in the HG

Energy calibration and linearity



- ☐ The SiPM signals are summed after ph-e equalisation
- ☐ The 20 GeV beam is steered at the centre of M0 (read out with SiPM) to calibrate in energy





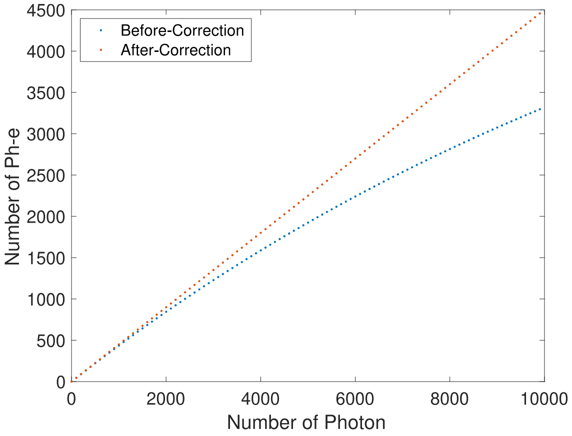
Pretty good linearity but never forget that SiPMs are digital sensors: the same cell cannot be fired twice

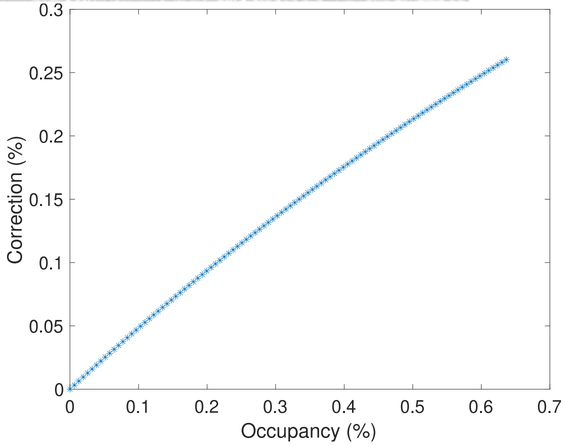
More on SiPM linearity

Parameter	S14160-1315PS
Effective photosensitive area (mm2)	1.3 x 1.3
Pixel pitch (mu)	15
Number of pixels	7284

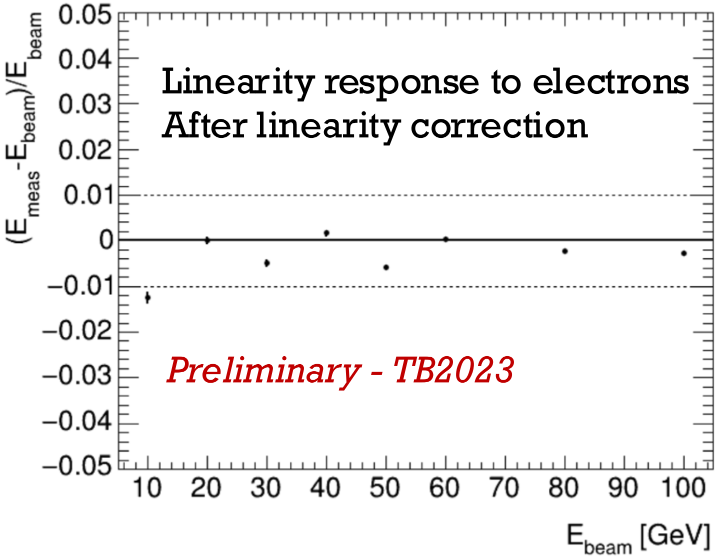
$$N_{\text{fired}} = N_{\text{cells}} \times \left[1 - \exp\left[-\frac{N_{\text{photons}} \times \text{PDE}}{N_{\text{cells}}}\right]\right]$$

With 700 Ph-e (10% occupancy) in a single fibre -> 5% correction to the signal





Improved linearity after the correction


Linearity response to electrons
After linearity correction

Preliminary - TB2023

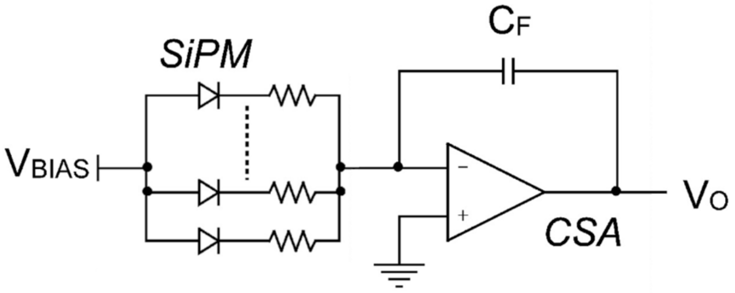
The take home message

DR High granularity modules have demanding and sometimes competing requirements:

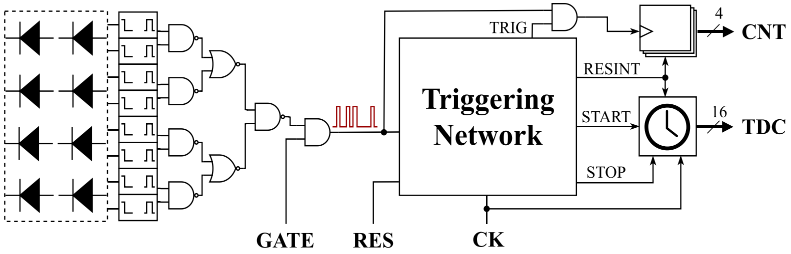
- SiPMs with:
  - High efficiency with single photon resolution
  - wide dynamic-range at fixed sensitive area to avoid non-linearity effects
- Readout coping with the SiPM dynamic range, preserving the single photon resolution
- Time resolution < 100ps to add longitudinal segmentation
- Signal grouping from SiPMs to reduce the number of channels to be read-out, knowing that:
  - It reduces the multi-ph quality and the timing performance
  - It requires that all SiPMs in the group must operate in linear regime: no-way to correct for non-linearity (they sampling different regions of the shower profile and are not uniformly illuminated)

Are dSiPMs a valid option to be considered?

SiPMs: analogue signal proportional to number of fired cells, readout performed externally



Digital (CMOS) SiPMs: readout functionalities implemented in the sensor substrate (e.g. binary counters, SPAD masking, TDCs …)



M. Perenzoni et al. 2017 – IEEE JSSC

- SPAD array in CMOS technologies may offer the following benefits:
  - Front-end can be optimised to preserve signal integrity (especially useful for timing)
  - Easier linearisation and calibration – direct digital output vs digital/analog (including noise + non uniformity)/digital conversion
  - The monolithic structure simplifies the assembly for large area detectors
  - Costs can be kept relatively low if the design is based on standard process

ASPiDeS: A CMOS SPAD and Digital SiPM platform for high energy physics

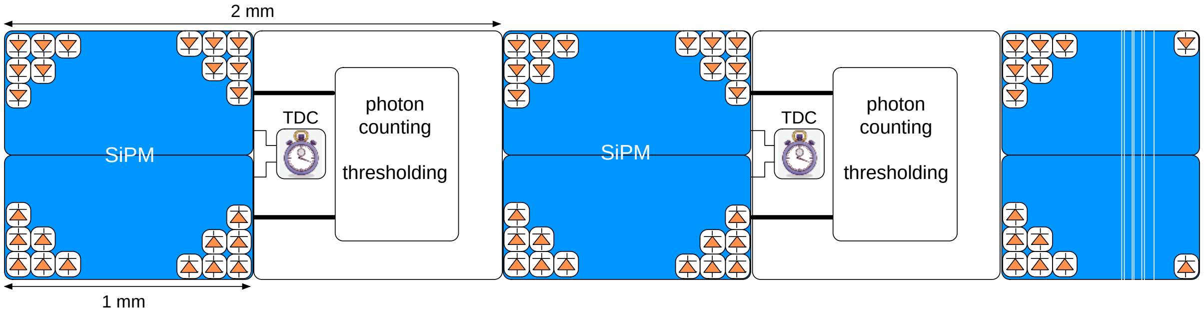
- A 3-year long INFN project lead by Lodovico Ratti (2025-2027)
- Goal: implementation and characterization of monolithic dSiPMs based on standard CMOS technology (a 110 nm CMOS process) for high energy physics applications
  - The chip will provide digitized output signals with low power consumption, fast read-out and low cost
- Different requirements on the floor:
  - High dynamic range for dual-readout calorimetry
  - High PDE and low DCR for low-light detection applications (RICH, dark matter and neutrino physics)
- Deliverables:
  - Demonstrator of CMOS-SPAD monolithic sensor fulfilling the HiDRa requirements
  - A prototype chip targeting low-light detection applications
  - Test structure for cryogenic applications

dSiPM specifications

Requirements	**Dual readout calorimetry**	**Cherenkov (eg RICH, IACT)**	**Dark Matter**	**Neutrino**
SiPM Unit area (mm^2)	1x1	mm scale	10x10	6x6
Micro-cell pitch (um)	15-20	40-50	25-30	50-150
Macro-pixel area (μm^2)	500x500			
PDE (%)	>20	> 40	>45	>35
DCR (kHz)	<100 kHz/mm^2	very low for single pe detection	<0.1 Hz/mm^2 (at LN)	<0.2 Hz/mm^2 (at LN)
AP (%)	<1	few	Total Correlated Noise Probability (Xtalk + AP) < 60 %	<5%
Xtalk (%)	few	few		<35%
Trigger	external, self	self, external	self	
Output data: light intensity	no. of fired cells in 1 or 2 time windows (10's of ns long)			
Output data: time	time of arrival of the first photon in the window, possibly of the last photon (TOT)	ToA and ToT	ToA and TOT	
Time resolution (ps)	<100	< 100 single pe		
Module size and form factor	strip with 8 units (1mm x 16 mm), pitch of 2 mm			
Connection	BGA			

Demonstrator for DR calorimetry

- Single building block of 8 dSiPM (1x1mm^2) and processing electronics in the common CMOS substrate
  - The SPAD electronic circuits will be kept to a minimum to guarantee high fill-factor
  - The inter-dSiPM spacing is used to accommodate the processing electronics
  - Each mm^2 dSiPM will be subdivided in sectors, each served by dedicated mixed analogue and digital electronics to improve timing performance



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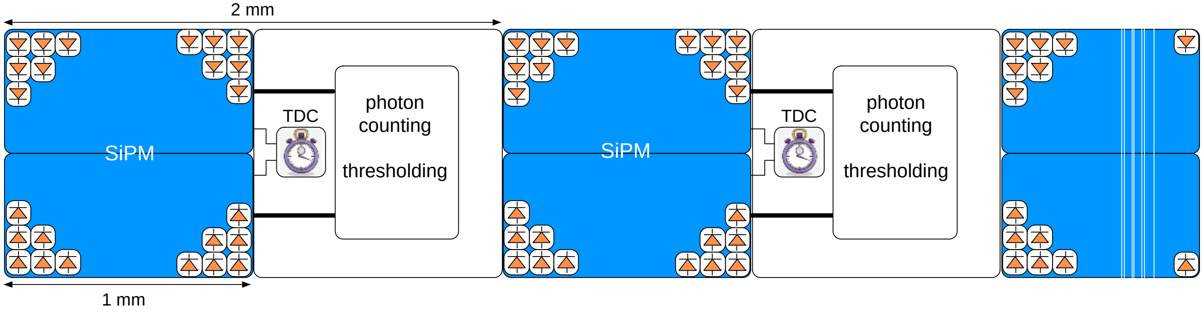
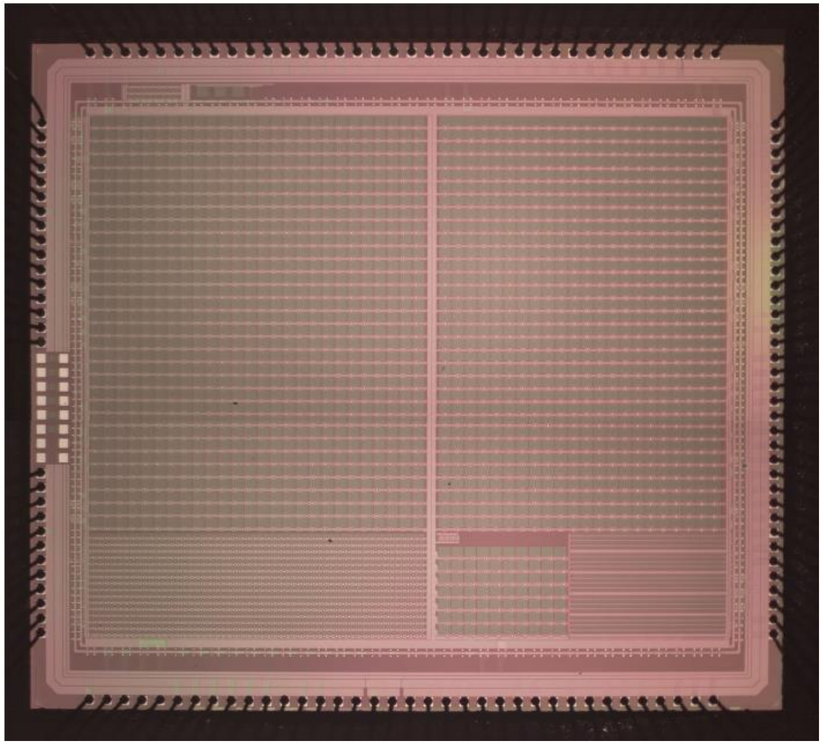
- Processing electronics:
  - Fully digital output obtained through a completely digital processing chain (or, mixed analogue and digital approach, through current or charge integration and A/D conversion)
  - Time of arrival of the first bunch of photons and bunch duration with better than 100 ps resolution
  - Possibility of individual micro-cell enabling
  - Threshold adjustment capabilities for noise rejection
  - Asynchronous counting over a more than three decade wide dynamic range of simultaneously firing micro-cells (order of a few thousands, 15-20 μm pitch)



ASAPLF110: a technology characterization platform

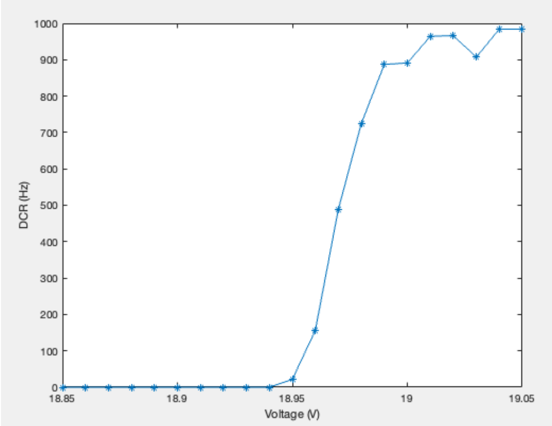
A test chip (ASAPLF110) with the same technology of interest is available from a previous project:

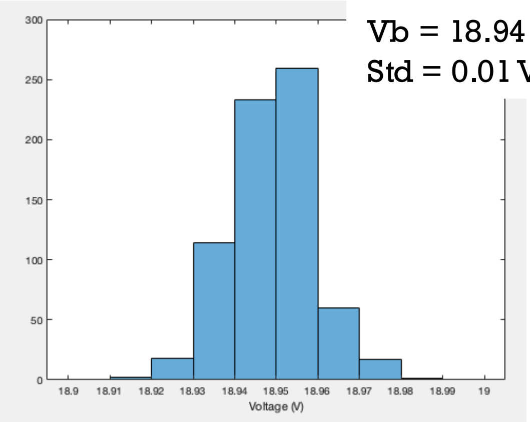


- ❑ 110 nm CIS technology;
- ❑ 136 pads involving supplies, voltage references and I/O digital signals.
- ❑ fully digital detection system embedding various SPAD arrays with different readout circuits;
- ❑ availability of single sensors enabling direct extraction of the I-V characteristics featured by the SPADs
- ❑ in-chip time to digital converter for DCR and afterpulsing characterization
- ❑ digital SiPMs based on a parallel counter architecture

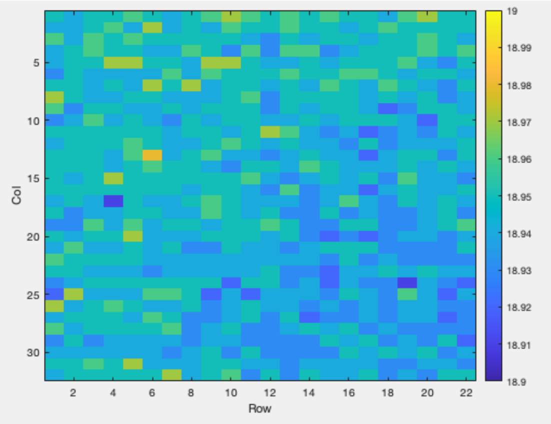
First measurements performed on the ASAPLF110

- Breakdown voltage
  - DCR VS voltage using 500 ms long gate windows
  - Scan performed with dV = 10 mV
  - Vb defined as the minimum voltage with DCR > 0 (Vb measured with IV-curves is 500 mV lower)



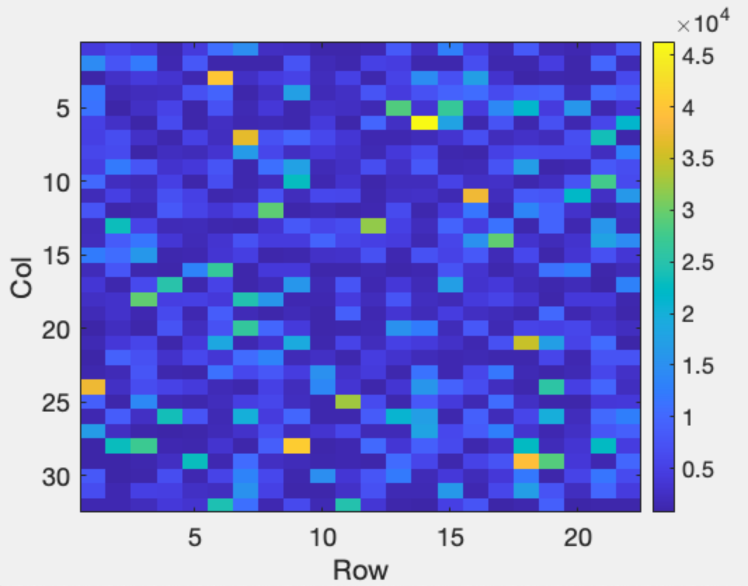


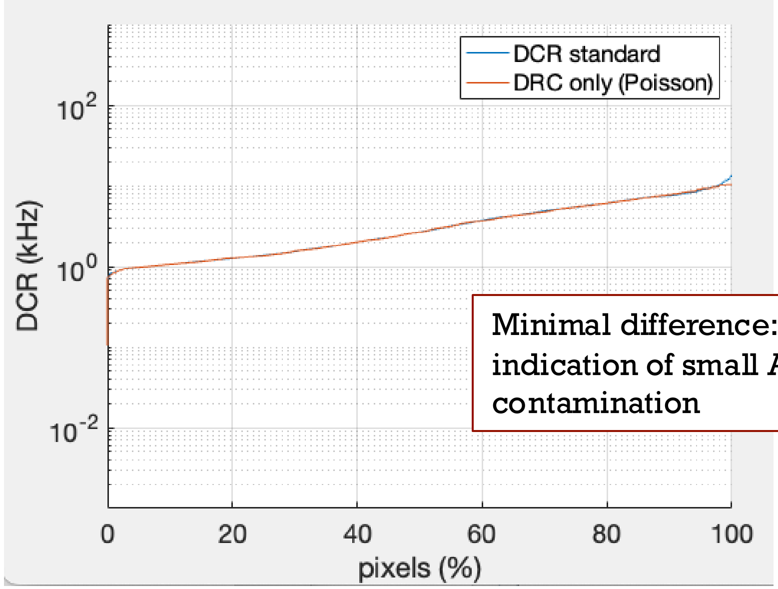
Vb = 18.94 V
Std = 0.01 V



First measurements performed on the ASAPLF110

- Breakdown voltage
- DRC @ 21V: measured with two methods
  - Count rates measured in 30k windows (1 ms long): average value is the DCR contaminated by AP (DCR standard)
  - Assuming DCR follows Poisson distribution, I'm measuring the probability of having 0 counts in 1ms long windows (μ of the Poisson distribution)

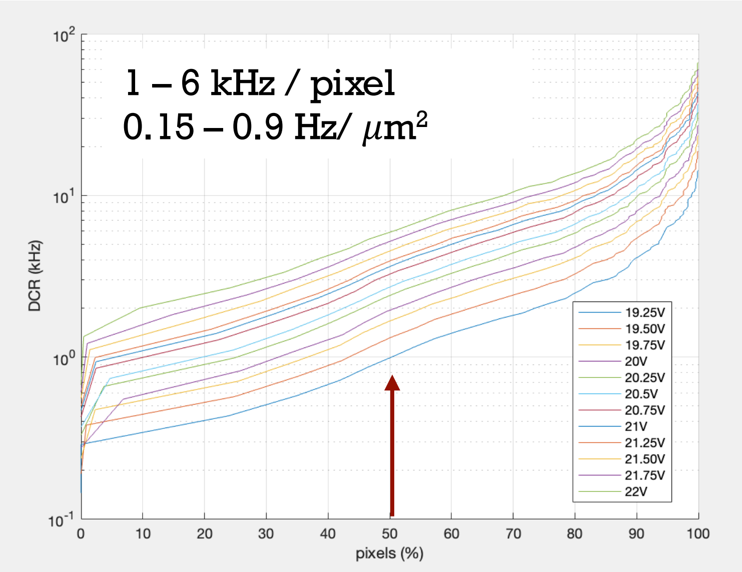




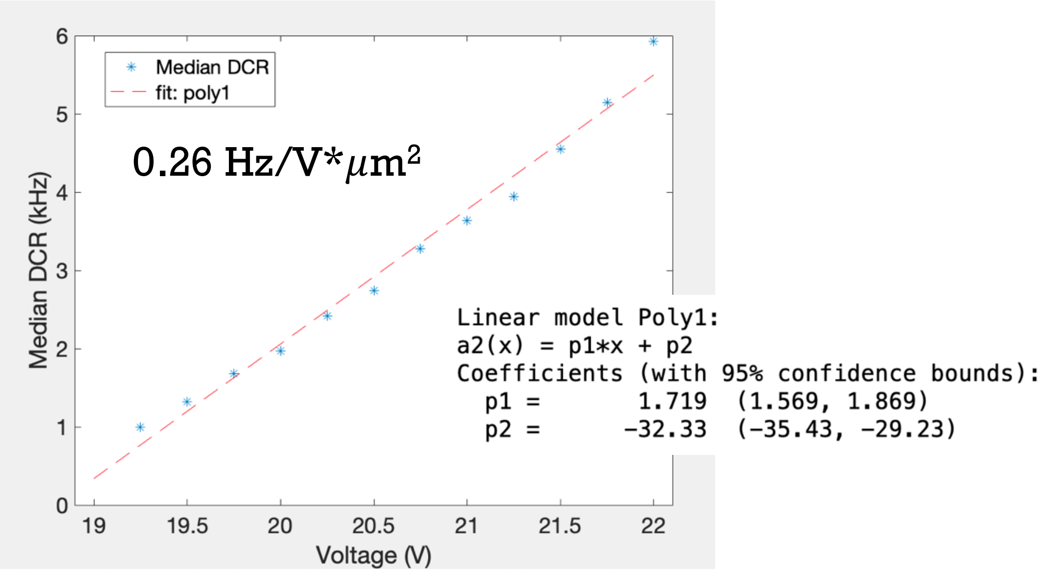
Minimal difference: first indication of small AP contamination

First measurements performed on the ASAPLF110

- ☐ Breakdown voltage
- ☐ DRC @ 21V: measured with two methods
- ☐ DCR VS bias voltage


1 – 6 kHz / pixel

0.15 – 0.9 Hz/ μm^2


0.26 Hz/V*μm^2

```
Linear model Poly1:
a2(x) = p1*x + p2
Coefficients (with 95% confidence bounds):
  p1 =       1.719  (1.569, 1.869)
  p2 =      -32.33  (-35.43, -29.23)
```

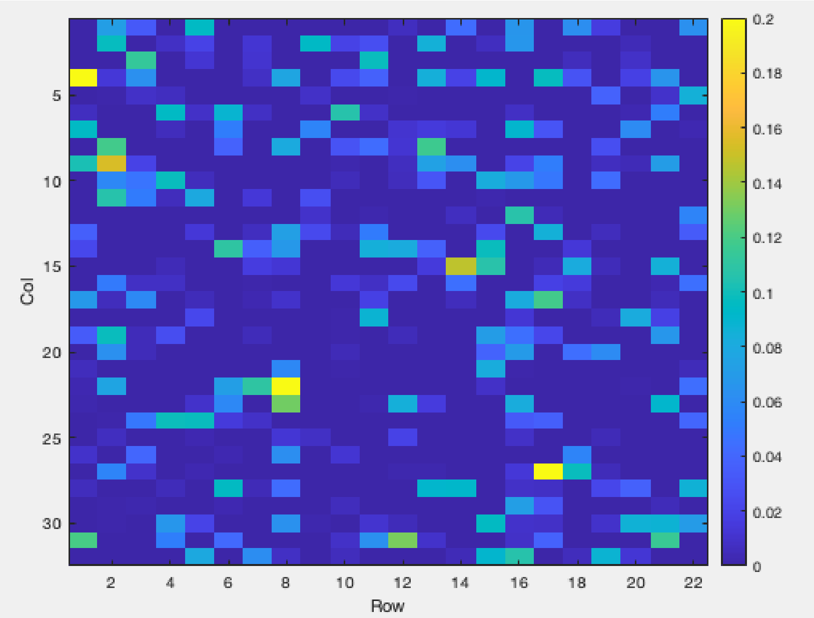
First measurements performed on the ASAPLF110

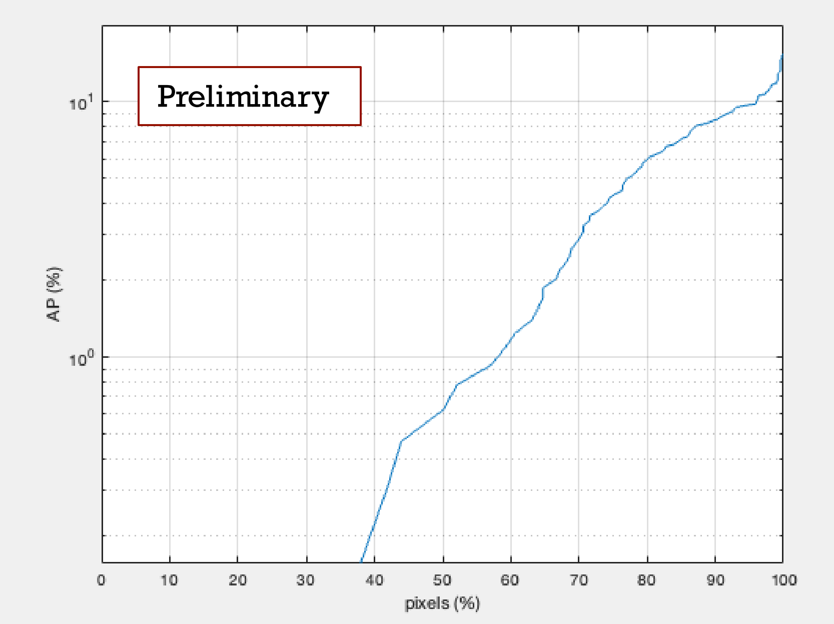
- Breakdown voltage
- DRC @ 21V: measured with two methods
- DCR VS bias voltage
- AP @ 21V
  - We count spurious pulses N_{tot} (DCR + AP) in gated windows
  - If DCR follow the Poissonian statistic, the μ of the distribution is measured by counting the number of empty windows and we can also estimate the N_{DCR}
  - AP is defined as follows:

$$AP = \frac{N_{tot} - N_{DCR}}{N_{tot}} = \frac{N_{tot} - \lambda \Delta T_{Tot}}{N_{tot}}, \ \lambda = \left(\frac{\mu}{\Delta T}\right), \ \Delta T = \text{ single integrating window}$$

First measurements performed on the ASAPLF110

- ❑ Breakdown voltage
- ❑ DRC @ 21V: measured with two methods
- ❑ DCR VS bias voltage
- ❑ AP @ 21V





First measurements performed on the ASAPLF110

- Breakdown voltage
- DRC @ 21V: measured with two methods
- DCR VS bias voltage
- AP @ 21V
- PDE and Cross talk will come soon

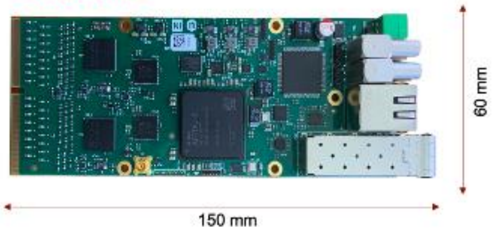
Summary

- ☐ HiDRa aims to build a dual readout calorimeter large enough to contain hadronic showers, using a scalable and cost-effective solution for the IDEA detector concept
- ☐ The highly granular modules, equipped with SiPMs, set challenging requirements in terms of readout, calibration technique and linearity correction
- ☐ Although SiPMs are the baseline solution, monolithic CMOS SPAD array (dSiPM) may have a strong impact for this detector R&D
- ☐ ASPIDES aims to design and characterise a demonstrator that meets the HiDRa requirements and will provide test structures of wider interest for high energy physics applications: stay tunes!

Backup

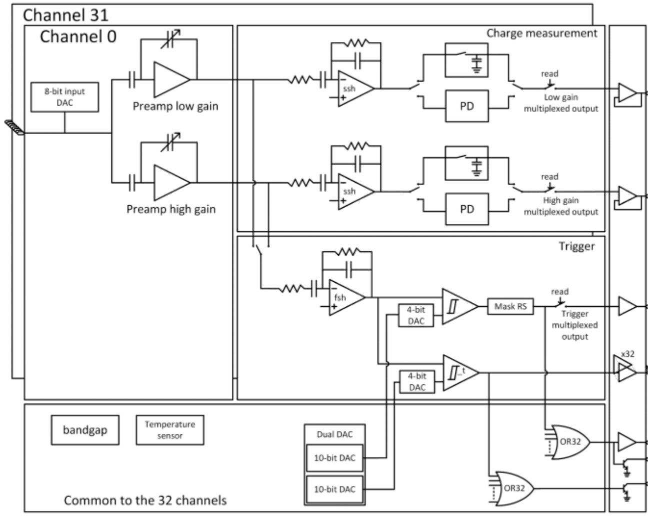
Integration and signal integrity

FERS: A5202

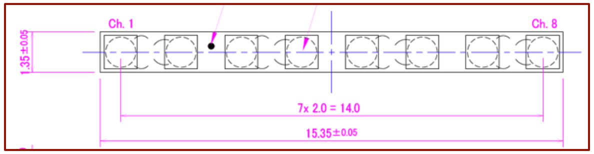


- Two Citiroc1A for reading out up to 64 SiPMs
- One (20 – 85V) HV power supply with temperature compensation
- Two 12-bit ADCs to measure the charge in all channels
- Timing measured with 64 TDCs implemented on FPGA (LSB = 500 ps)
- 2 High resolution TDCs (LSB = 50 ps)
- Optical link interface for readout (6.25 Gbit/s)

Citiroc1A – block-schema

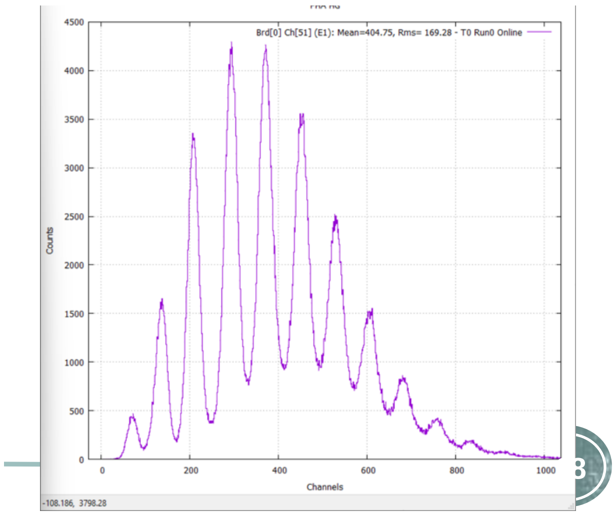


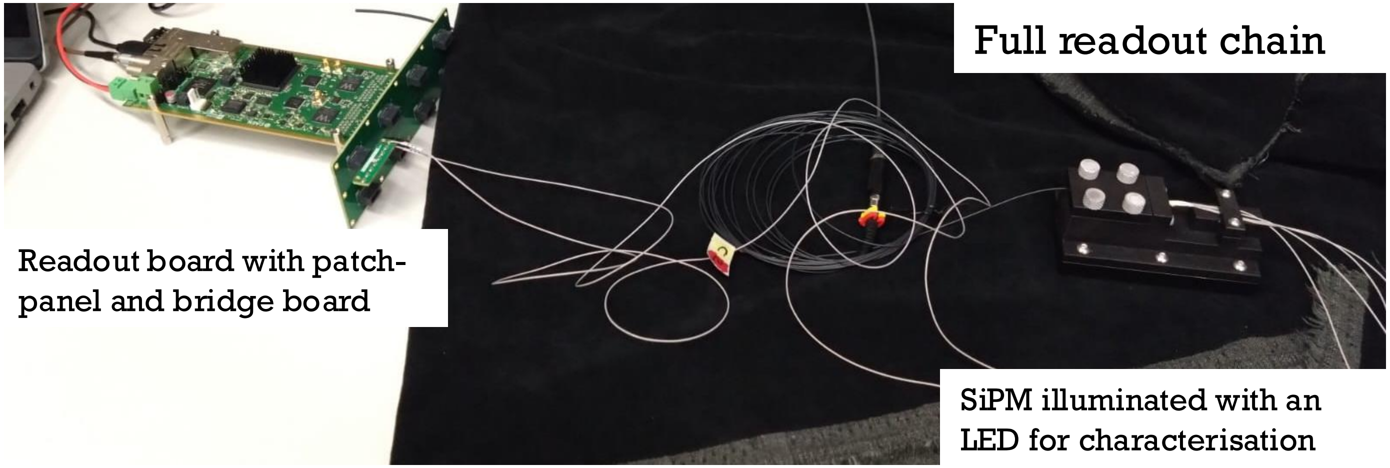
Customised package with 8 SiPMs, 2 mm spaced (S16676-15 / S16676-10)



SiPM with 10 μm pitch for scintillating and 15 μm putch for Cherenkov light (better PDE)

15 μm pitch SiPM operated at $\approx$ + 6 V Over-Voltage



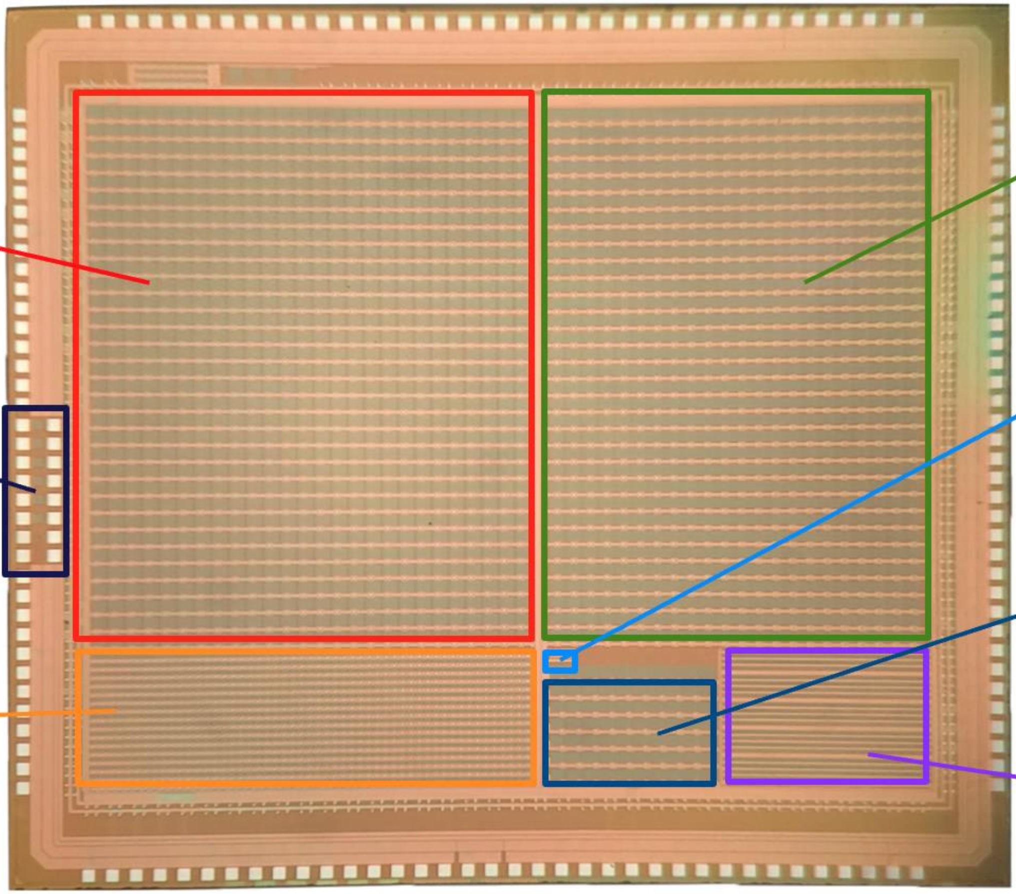


Full readout chain

Readout board with patch-panel and bridge board

SiPM illuminated with an LED for characterisation

ASAPLF110: a technology characterization platform



100 um pitch, passive quenching, 1 bit, FF=67%
(32x26)

100 um pitch, passive quenching, 10 bit, FF=64%
(32x22)

10b/20b TDC and ring oscillator

single SPADs

100 um pitch, active quenching, 1 bit, FF=67%
(7x10)

50 um pitch, passive quenching, 1 bit, FF=48%
(16x52)

Mini-SiPMs (4x4), 160 um pitch, FF=41%
(5x12)

ASAP110LF chip – Array A2

Array 2 (A2) cell:

- ❑ The avalanche is quenched by a passive network
- ❑ The monostable circuit modifies the duration of the sensor pulse (400 ps, 750 ps, 2 ns, transparent mode).
- ❑ A 10 bit counter automatically counts the pulses.