Update on 3D-related activities in Pavia/Bergamo

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AIDA

Outline

- Status of the new 3D submission
  - The Superpix1 chip: FE for hybrid pixels
  - The ApselVI chip: 3D DNW MAPS
- Test of 3D Tezzaron/GlobalFoudries MAPS prototypes
  - Tests on SDR1 digital circuits
  - Characterization of the APSEL5T-TC analog front-end
  - Effects of ionizing radiation on APSEL5T-TC and single transistors
- Conclusions and plans for the future

2nd 3D Prototype Submission

DNW MAPS

3.25x2 mm^2

Hybrid pixels single MOS

3.25x2 mm^2

Superpix1, front-end for hybrid pixels

128x32 pixels

10x3.5 mm^2

ApselVI, DNW MAPS matrix with fast sparsified readout

128x96 pixels

10x5.2 mm^2

- The VIPIX collaboration is at an advanced stage in the design work for a second MPW run with the 3D Tezzaron/Globalfoundries process
  - The Superpix1 chip
  - The ApselVI chip

Small test structures:

- Test chip for hybrid pixels
- DNW MAPS test chip

Superpix1 Analog Front-End

High resistivity sensor

$Q\delta(t)$ C_D

ANALOG LAYER

Preamplifier C_F

Polarity selector

PS

$V_{FBK,PA,N}$

$V_{FBK,PA,P}$

C_1

Shaper C_2

AVDD I_F

Discriminator V_{TH}

AVDD AGND

HIGH_GAIN

INJ_CK

Pulser

INJ_ENABLE

HIT

MASK

In-pixel logic

Digital Threshold Correction

DATA_IN

Shift register

DATA_CK

MASK INJ B0 B1 B2 B3

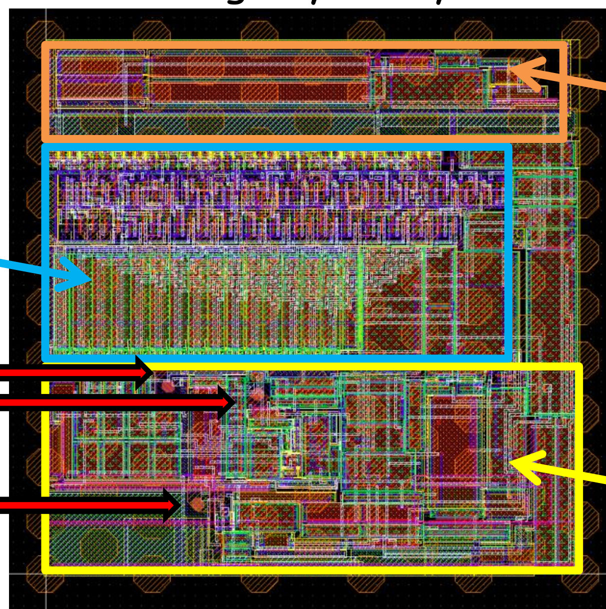
D Q D Q D Q D Q D Q D Q

DIGITAL LAYER

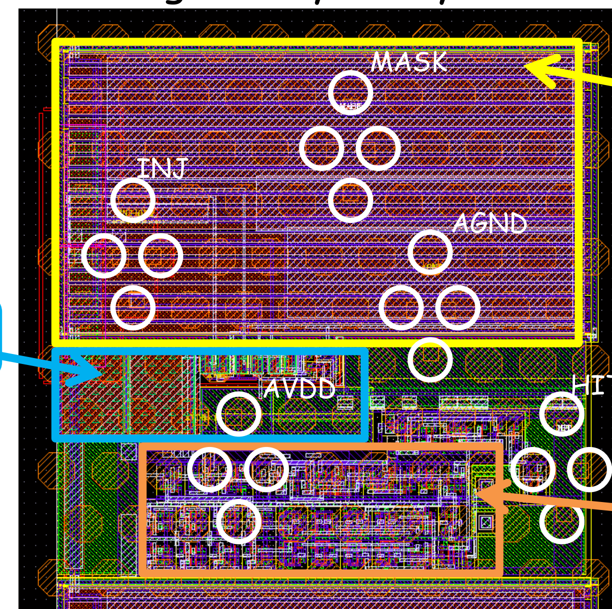
Superpix1 Analog Front-End

Main front-end design features	
Analog Power Dissipation [μW/pixel]	13.5
Peaking Time (Q_{inject} = 16000 e-) [ns]	250
Charge sensitivity [mV/fC] @ DAC outPUT	48
ENC @ C_D = 150 fF [e- rms]	180
Threshold dispersion (before/after correction) [e- rms]	560/65

Analog Layer Layout



Digital Layer Layout

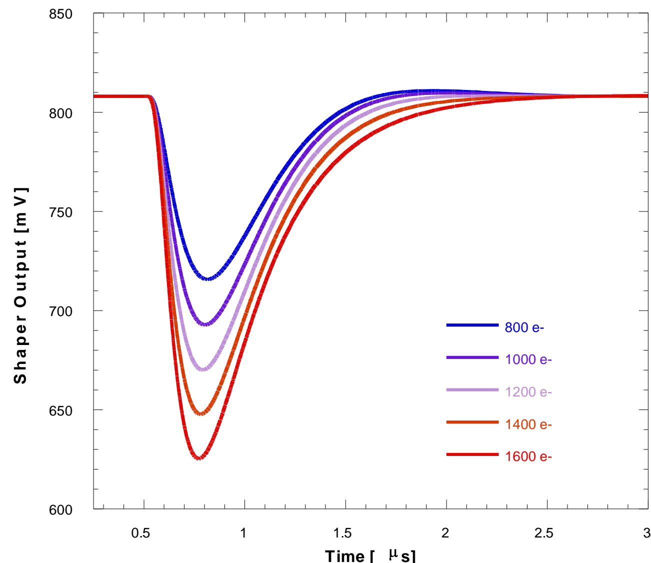


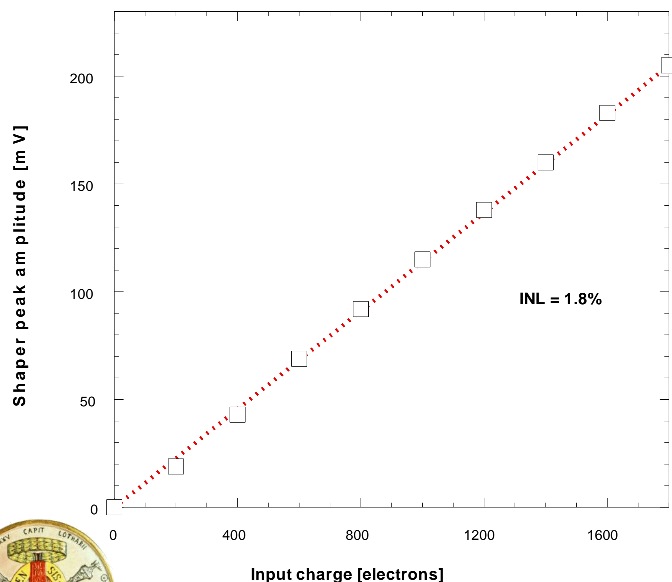
ApselVI front-end architecture

- DNW sensor
- Charge preamplifier with a $C_{f,pa}$ countinously discharged by an NMOS biased in deep subthreshold region
- RC-CR shaper with a transconductor feedback network:
  - Vref chip-wide distributed by an external voltage reference (not affected by voltage drop issues)

tier1, analog
tier2, digital
rif_comp
DAC_bias
AGND
AVDD
2
Vfbk,pa
Cf,pa
Gf
Vref
Cs2
Cs1
- A(s)
Vth
DAC
{b0,b1,b2,b3}
4
Shift register
KILL_bit
+
-
IN_PIXEL logic
PIXEL_HIT

ApselVI Main Analog Features

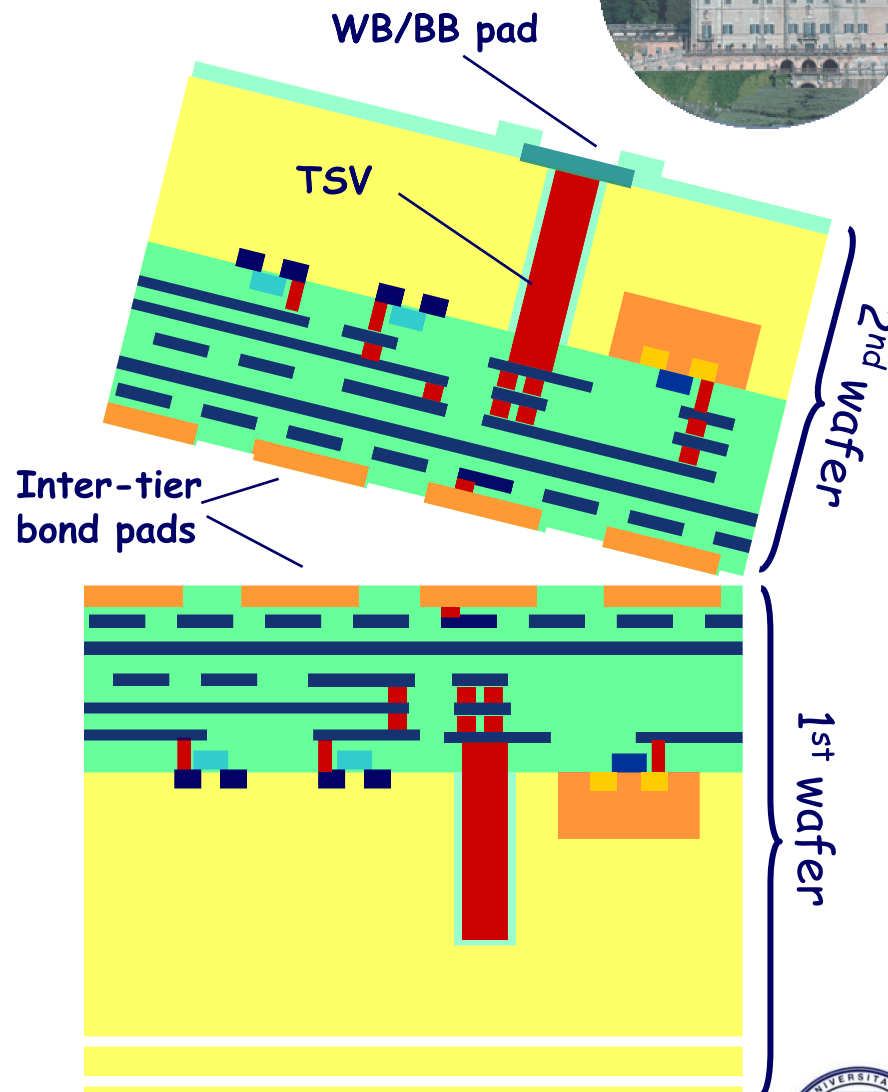




Main front-end design features	
Charge sensitivity [mV/fC] @ DAC outPUT	720
peaking time [ns]	300
ENC @ C_D=300 fF [e- rms]	40
Threshold dispersion before/after correction [e- rms]	106/15
INL (@ 0/2000 e-) [%]	1.8
Power consumption [μW]	36
Pixel pitch [μm]	50
Matrix size	128x96

1st 3D Tezzaron/Globalfoundries run

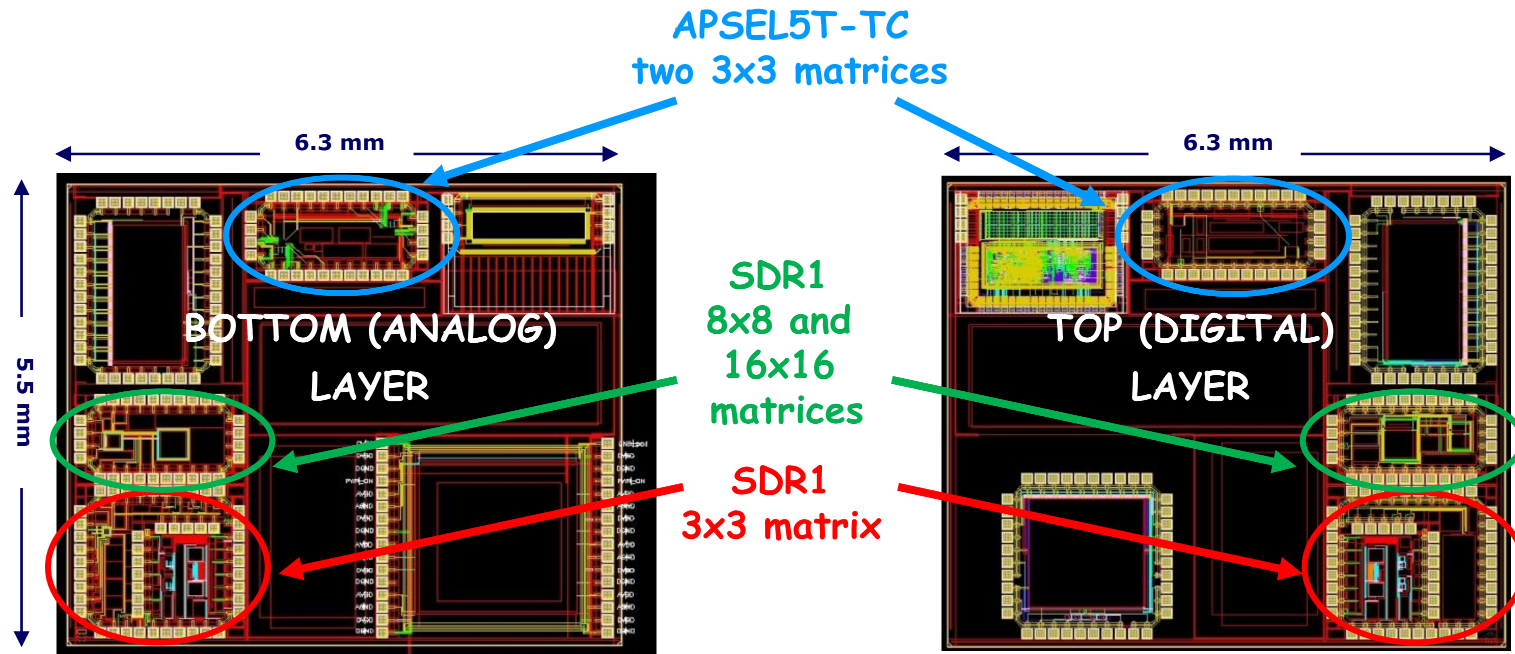
- In 2009, the Italian VIPIX collaboration submitted 3D active pixel devices in the first run of the 3DIC Consortium hosted by Fermilab
- In this run, we designed 3D MAPS with two layers ("tiers") of the 130 nm CMOS process by Chartered Semiconductor, vertically integrated with the Tezzaron interconnection technology
- Tests on structures belonging to the first run are ongoing



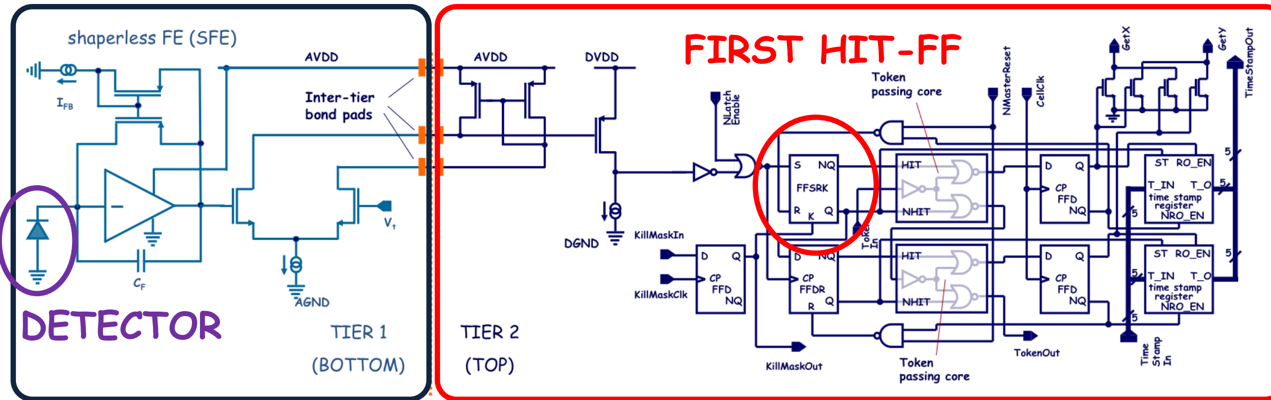
Tezzaron 3D Test Structures

- **SDR1 prototype**
  (Sparsified Digital Readout 1)
  - pitch = 20 μm
  - Application: ILC
  - FE: shaperless
  - DUTs: matrices with sparsified readout

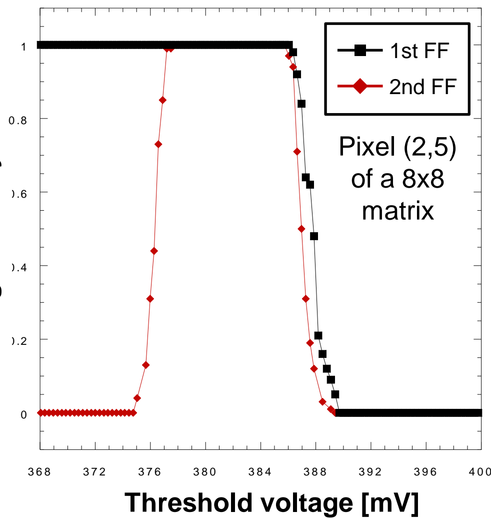
- **APSEL5T-TC prototype**
  (Active Pixel Sensor ELectronics)
  - pitch = 40 μm
  - Application: SuperB
  - FE: shaperless
  - DUTs: 3x3 matrices



SDR1 chip (Sparsified Digital Readout 1)



- Tests on SDR1 digital circuits show the full functionality of vertically integrated chips



CELL ENABLE (when it is low, it enables the FIRST-HIT FF)

MASTER RESET
(when it is low, it reset the FF)

VTH

PA OUTPUT

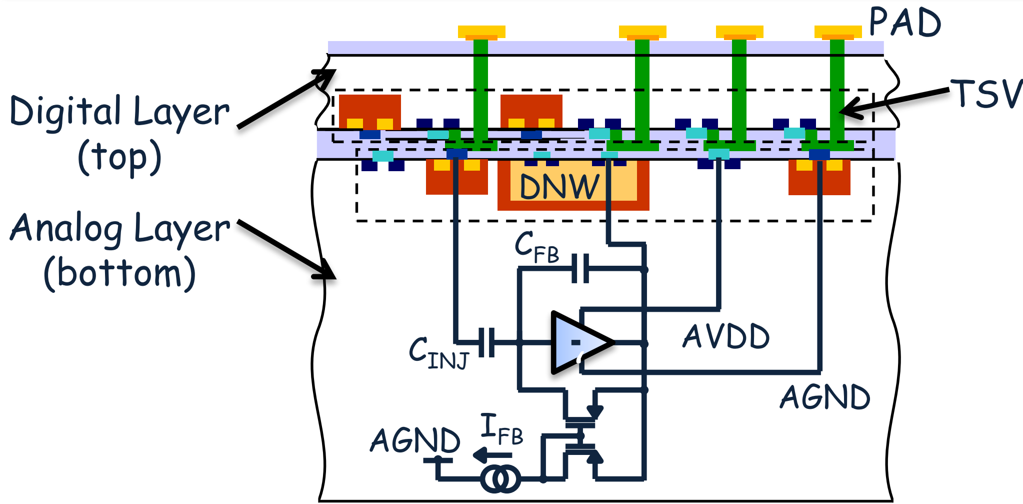
Hit

Reset

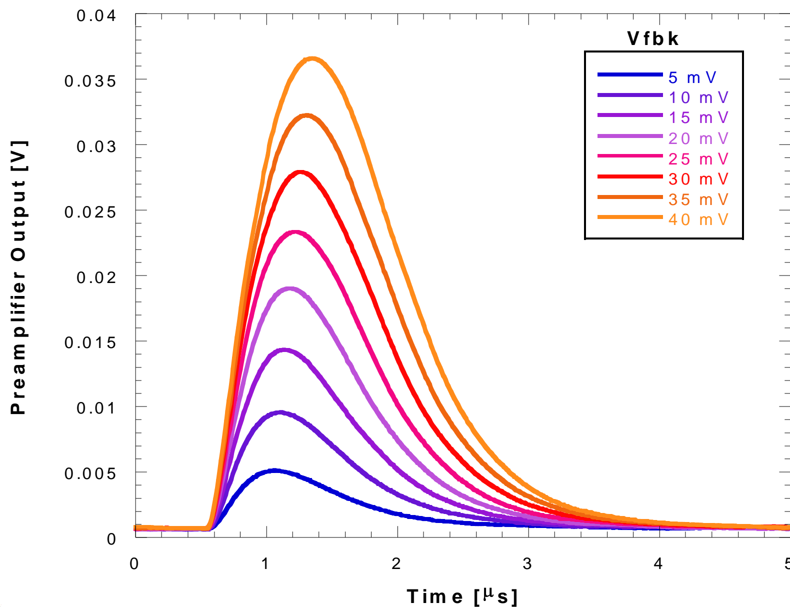
OUTPUT SIGNAL
of the FIRST-HIT FF

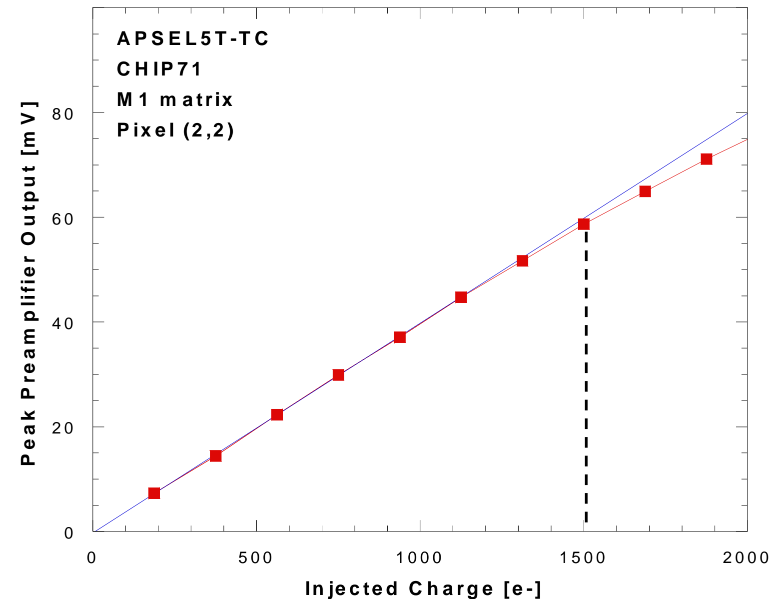
C1 AVG DC1M 2.00 V/div 2.040 V ofst 3.706 k#
C2 AVG DC1M 2.00 V/div 5.980 V ofst 2.157 k#
C3 AVG AC1M 100 mV/div -90.00 mV 4.269 k#
C4 AVG AC1M 2.00 V/div -7.080 V ofst 4.269 k#
Timebase -21.5 µs 5.00 µs/div 500 S 10 MS/s
Trigger C2 DC Auto 460 mV Edge Negative

APSEL5T-TC Analog Front-End Characterization



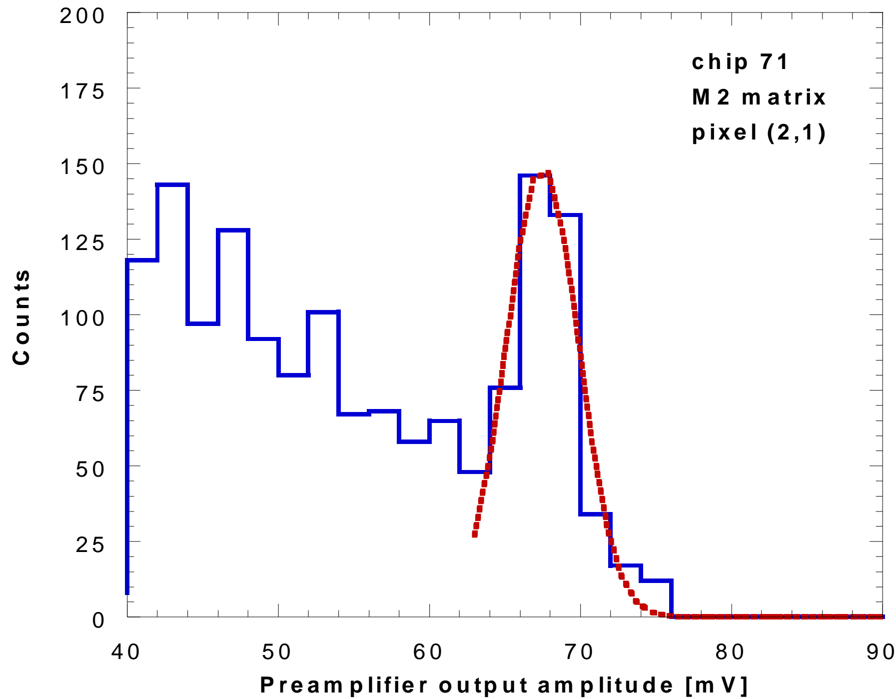
- Charge sensitivity: ~250 mV/fC
- Input dynamic range: ~1500 e-
- ENC: ~ 40 e- rms



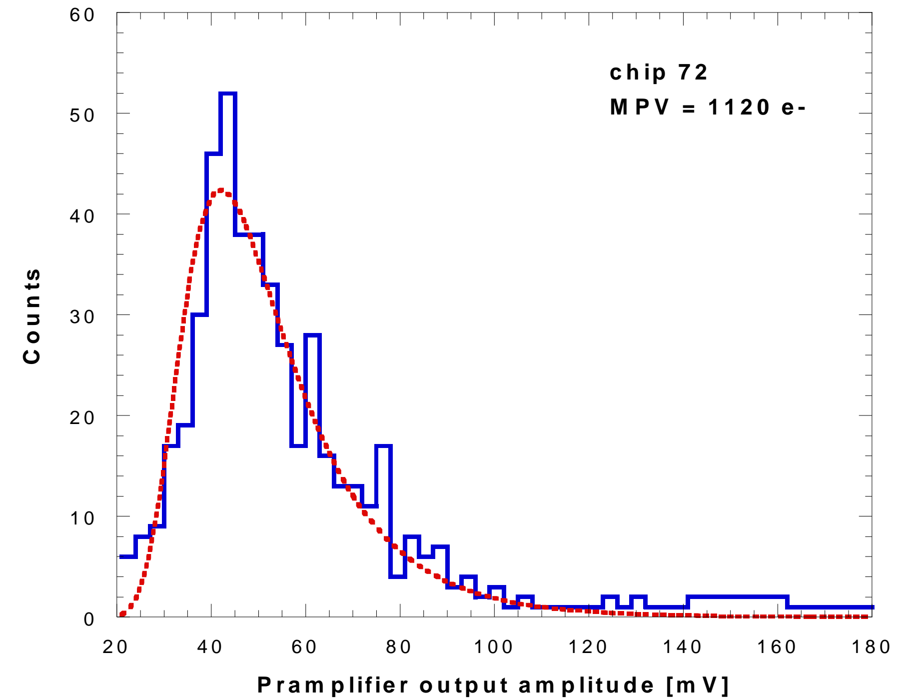


Tests with Radiation Sources

- Test with ^{55}Fe source



- Test with ^{90}Sr source

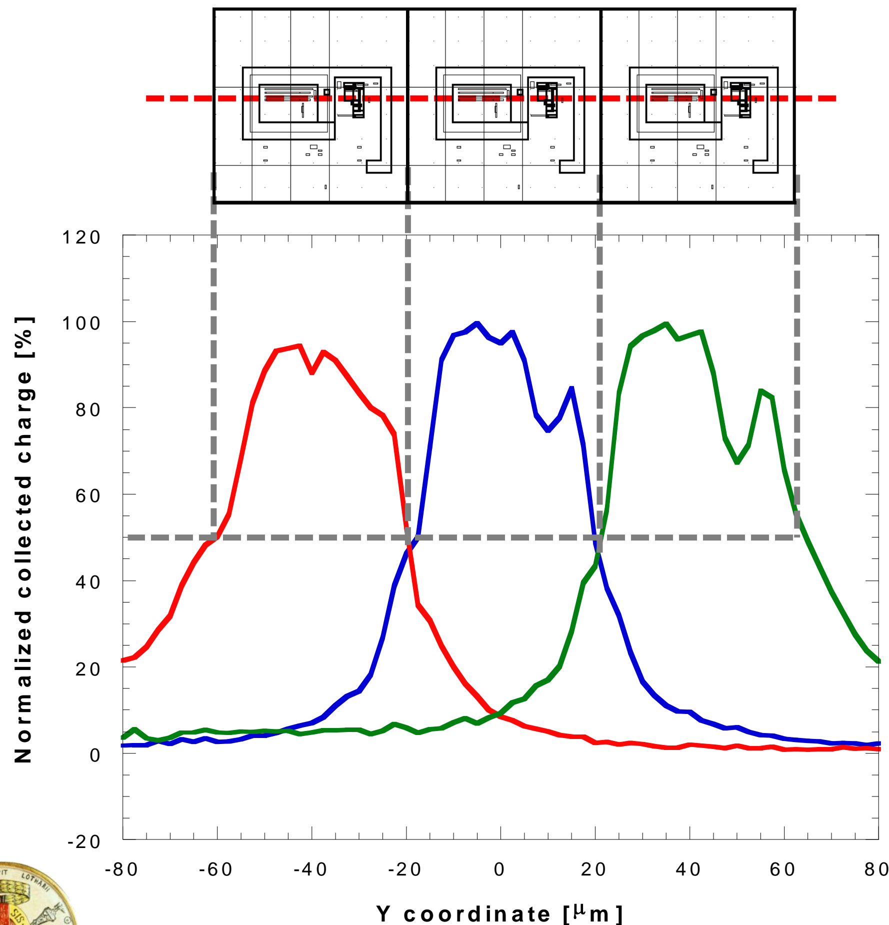


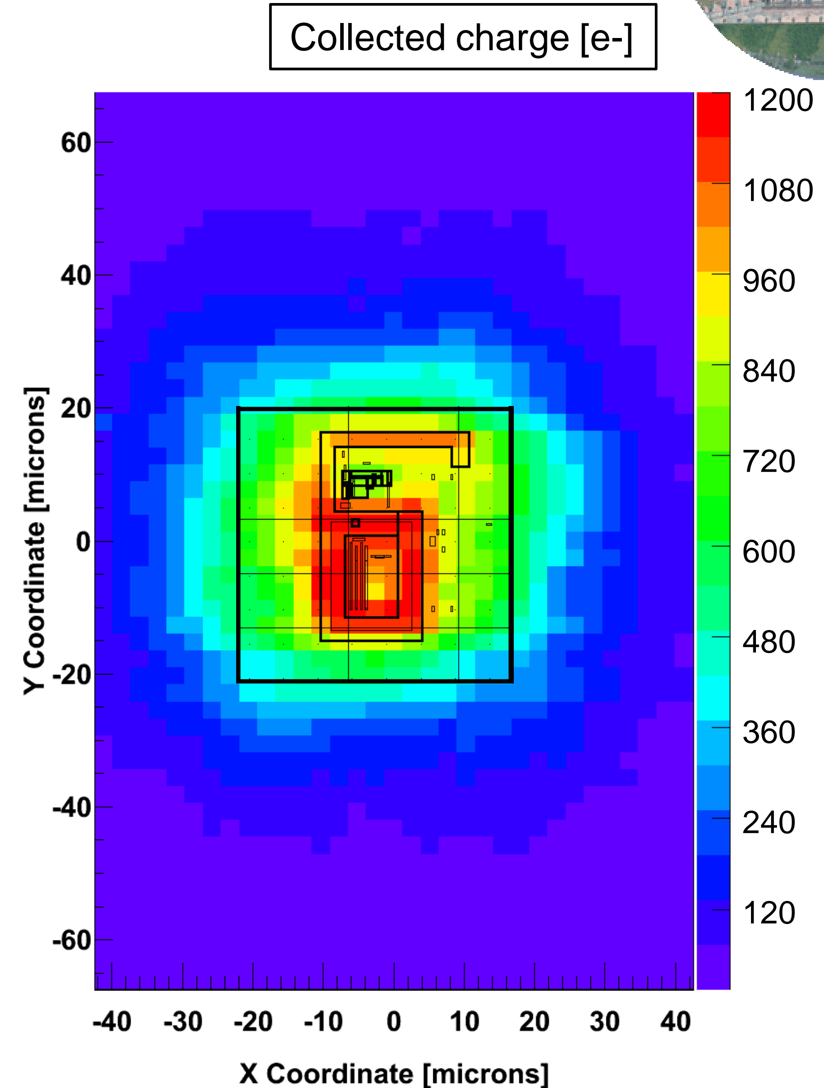
- Charge sensitivity in good agreement with values obtained by means of charge injection

- M1 matrix - 3x3 cluster signal

Laser Measurements

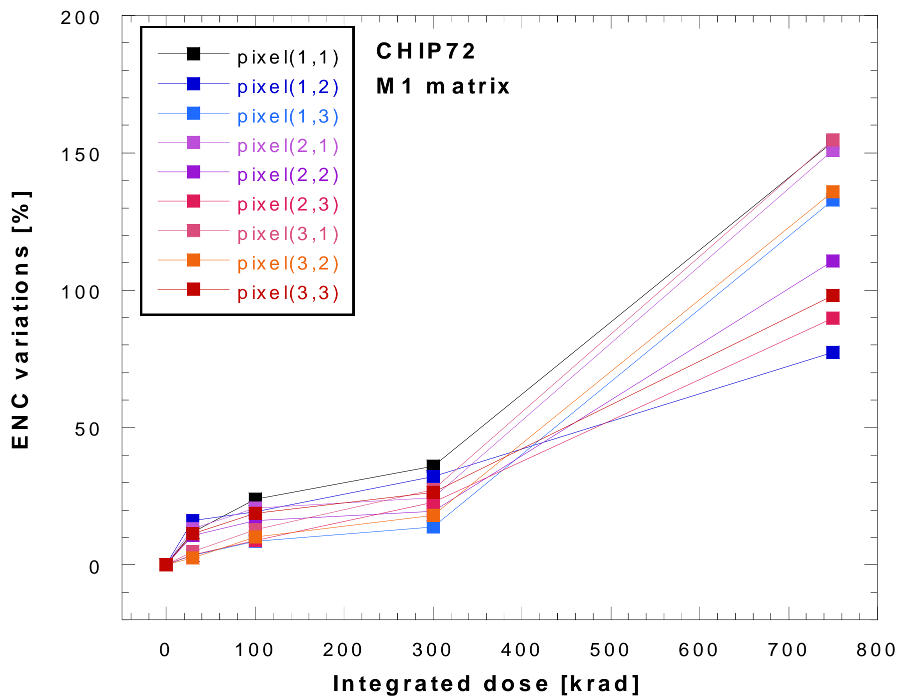
- Normalized collected charge as a function of the IR laser spot position (λ=1064nm)

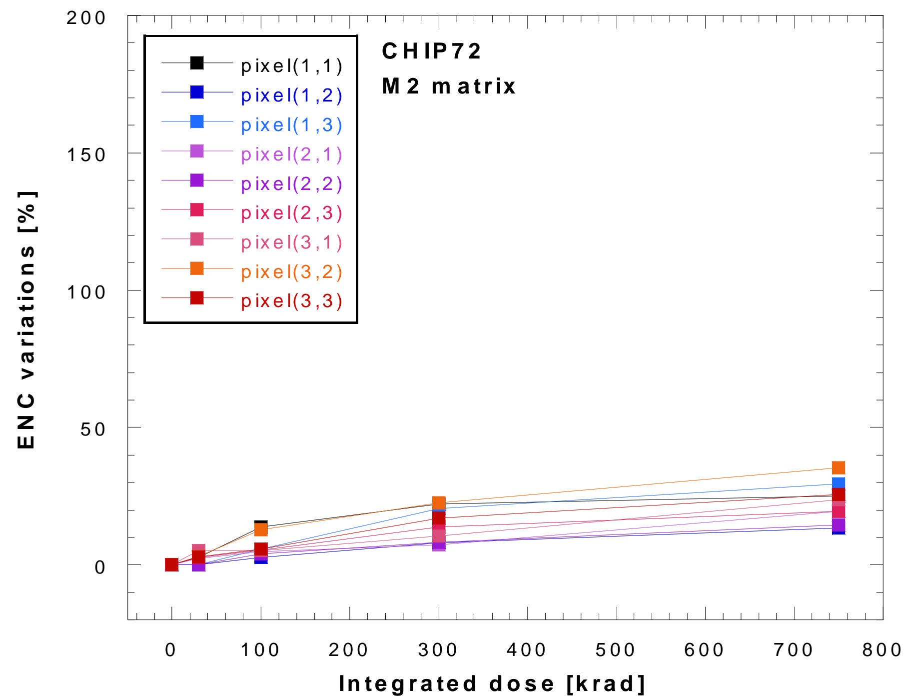




Effects of ionizing radiations on ENC

- The irradiation campaign has been performed with a ^{60}Co source up to a total dose of about 750 krad

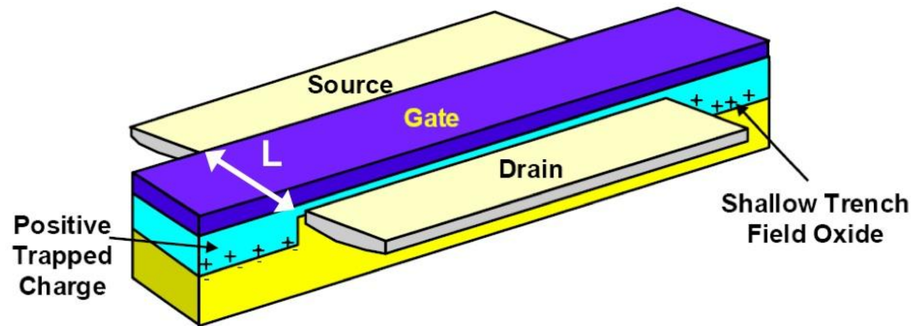


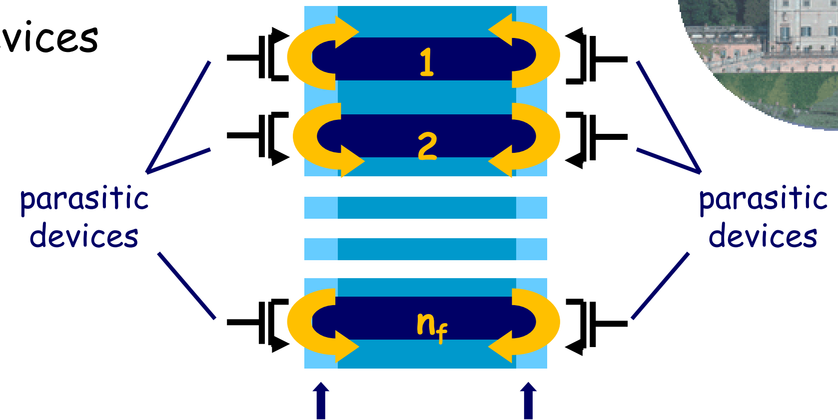


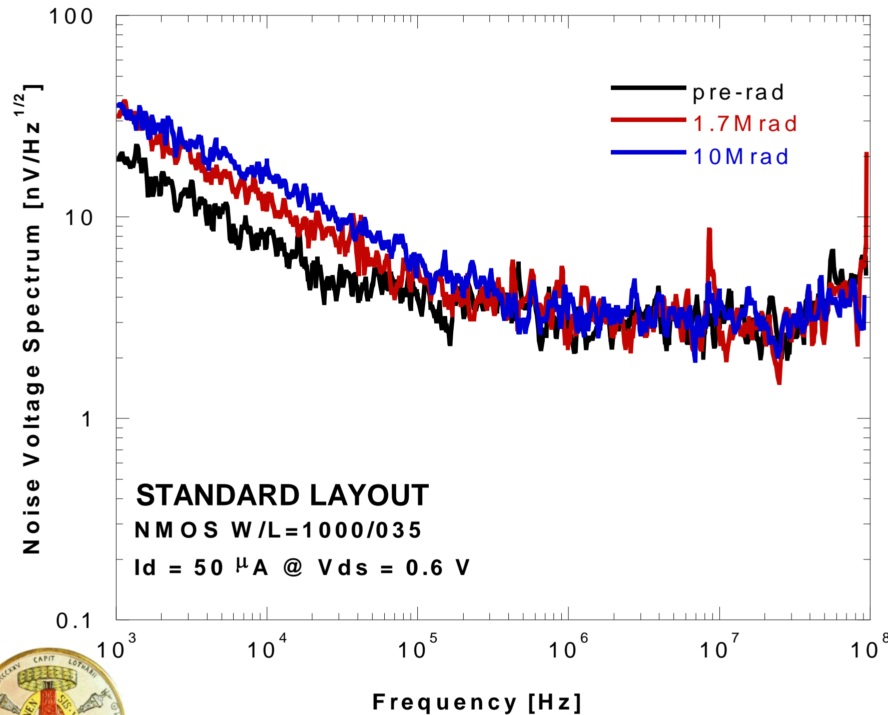
- M1 matrix: PA with standard layout input transistor
- M2 matrix: PA with enclosed layout input transistor

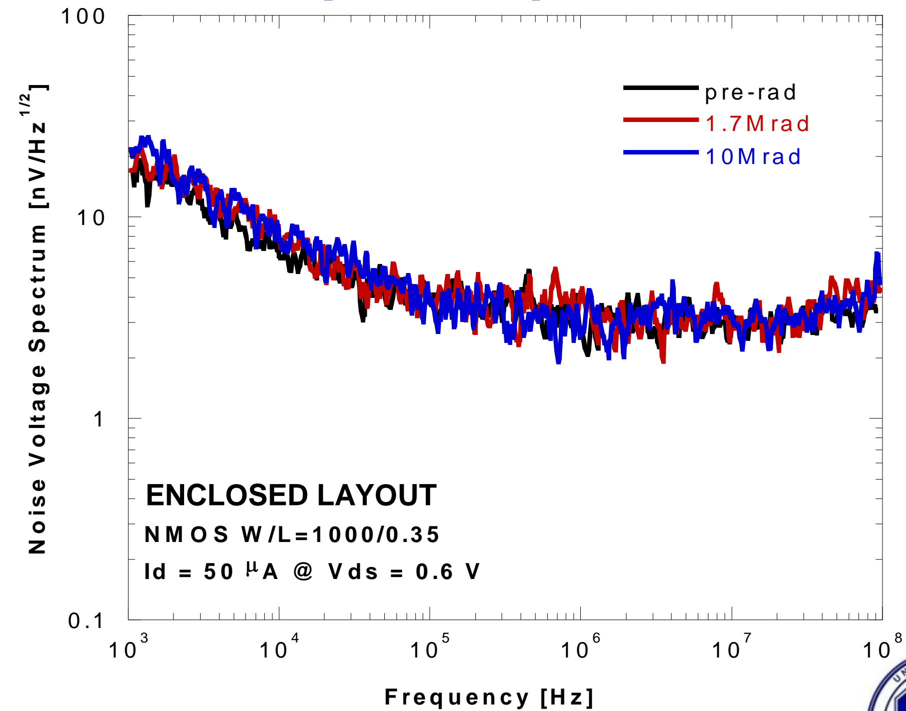
Effects on noise in single devices

- 1/f noise increase due to lateral parasitic devices





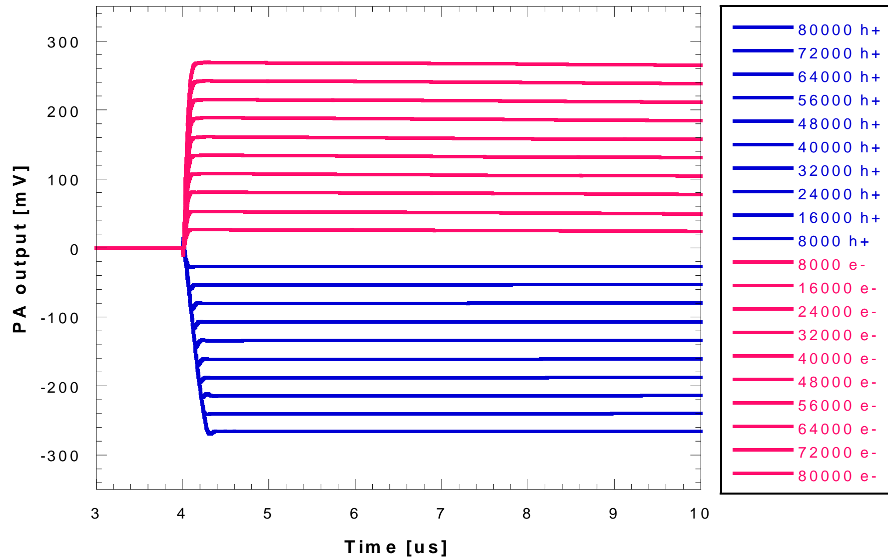


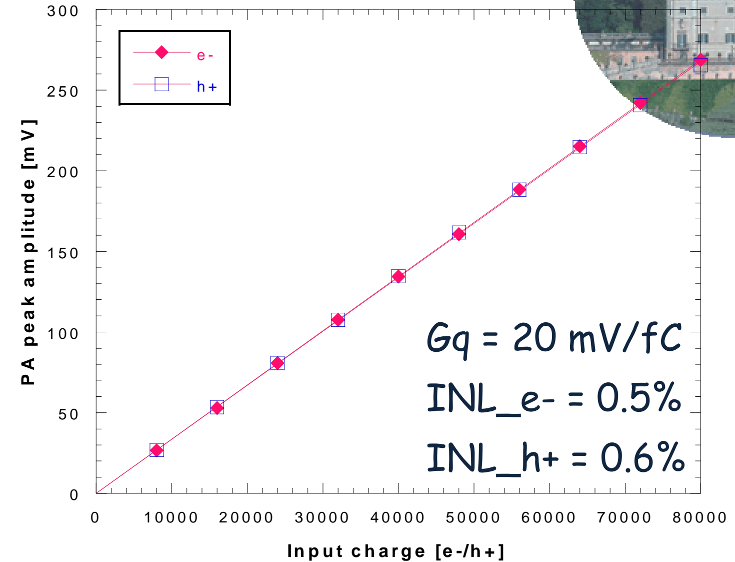


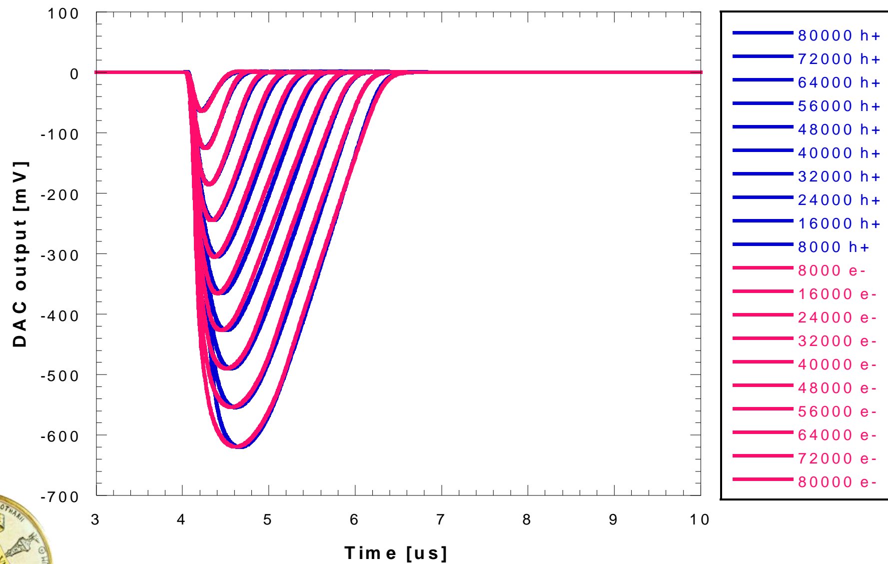
Conclusions and plans for the future

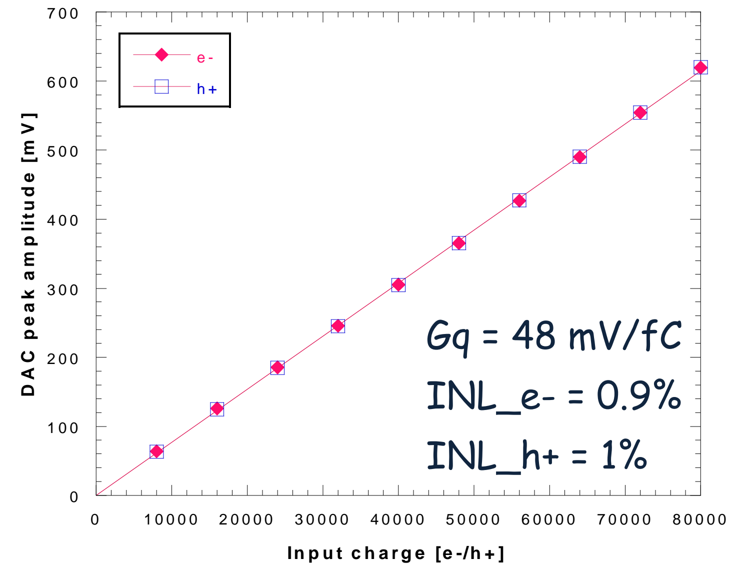
- Two different approaches have been considered for the design of the readout chip in view of applications to the SVT Layer0 of the SuberB factory
- ApselVI and SuperPIX1 will be fabricated in the Tezzaron-Globalfoundries 130 nm 3D CMOS technology (to be submitted Q1 2013)
- Tests on the SDR1 digital circuits pointed out the full functionality of the prototypes designed in the Tezzaron/Globalfoundries 3D technology
- APSEL5T-TC charge collection properties have been characterized by means of radiation sources and IR laser. Radiation hardness tests (γ-rays) have been performed also on single transistors
  - Significant increase in equivalent noise charge
  - ELT are required to avoid excessive 1/f noise increase
- Measurements on 3D prototypes are still in progress

Superpix1 Analog Front-End features

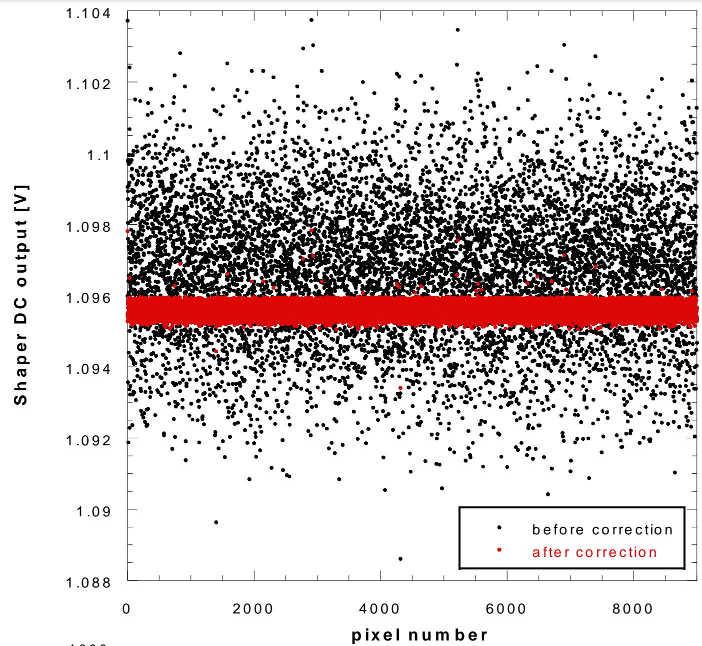


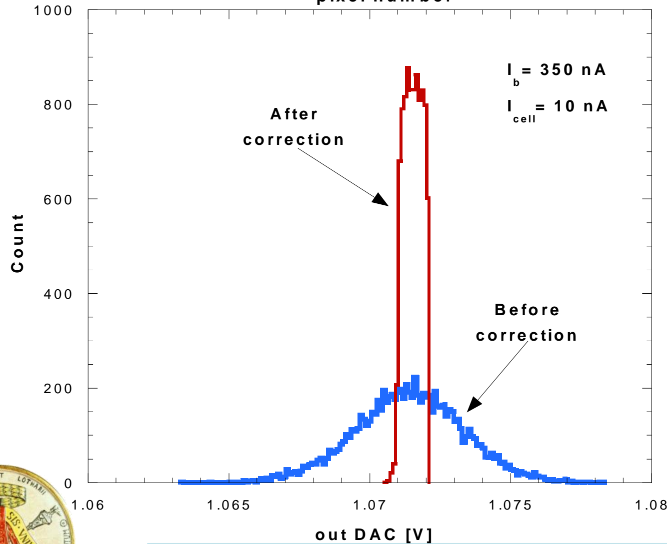


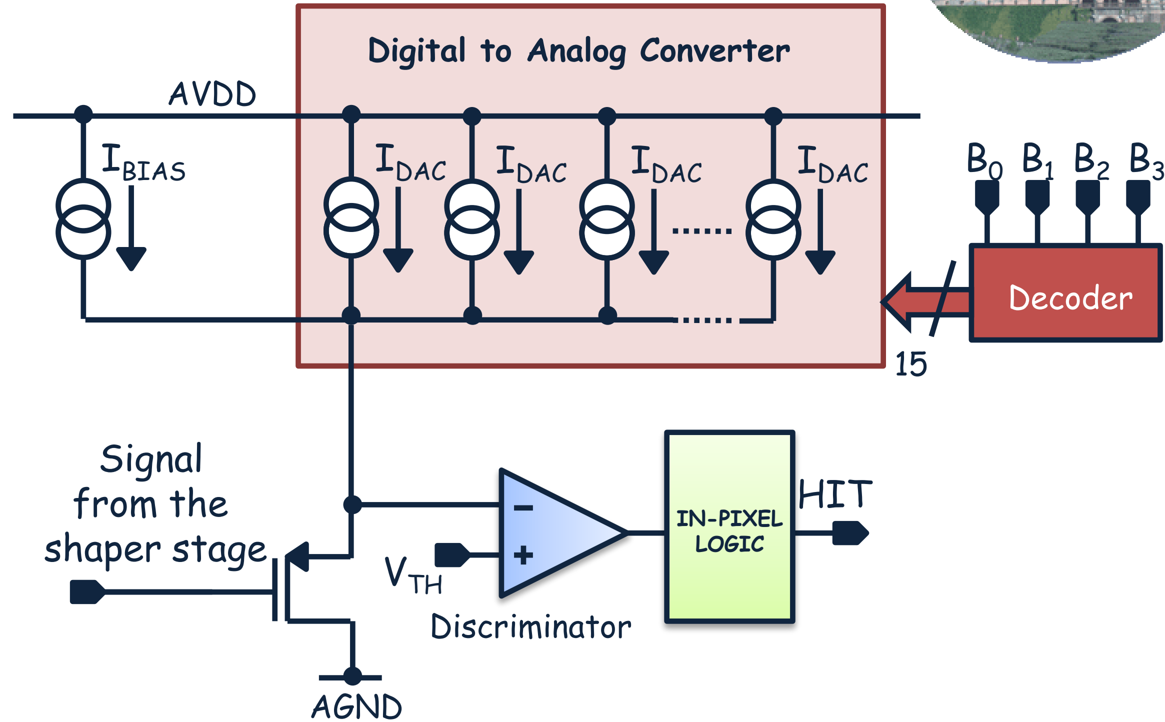




Threshold Correction Scheme







- B0÷B3 bits set by means of a shift register
- Threshold dispersion before/after correction: 560 e-/65e-

Charge Injection Circuit (In the Pixel Cell)

AVDD

R~226.5kΩ

R~226.5kΩ

ΔV

t

Cinj=35fF

HIGH_GAIN

INJ_EN

INJ_CLK

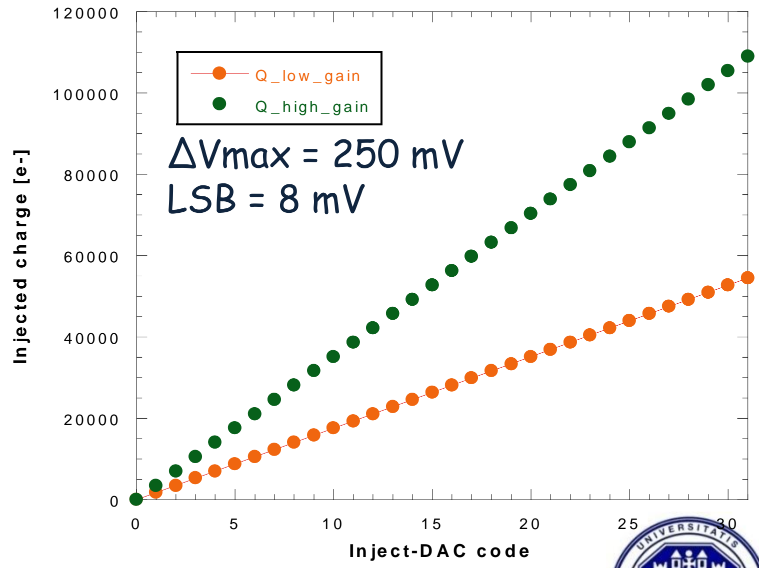
Cinj=35fF

Ipulser
(Imax=1.1 μA)

AGND

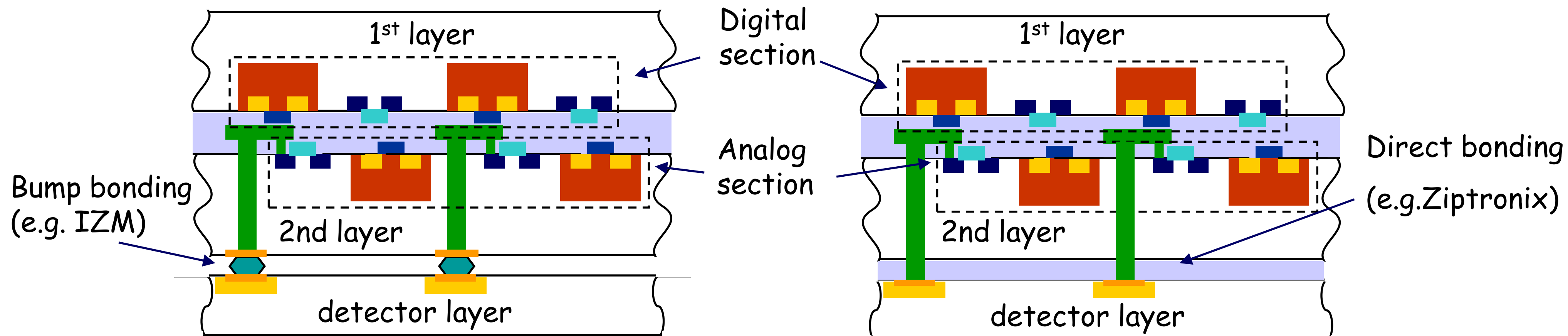
Control circuits
(placed in periphery)
5 bit DAC

From MC simulations:
|DNL|max=0.12 LSB
|INL|max=0.35 LSB



3D Hybrid Pixels

- Development of a 3D front-end chip to be vertically integrated with fully depleted detectors through some more (bump bonding) or less (direct bonding) standard technique

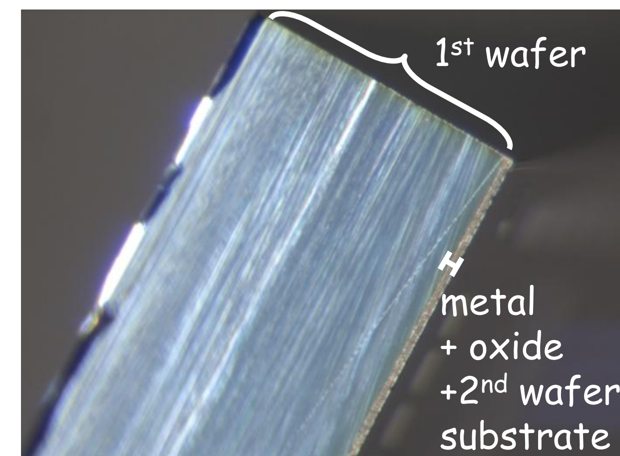


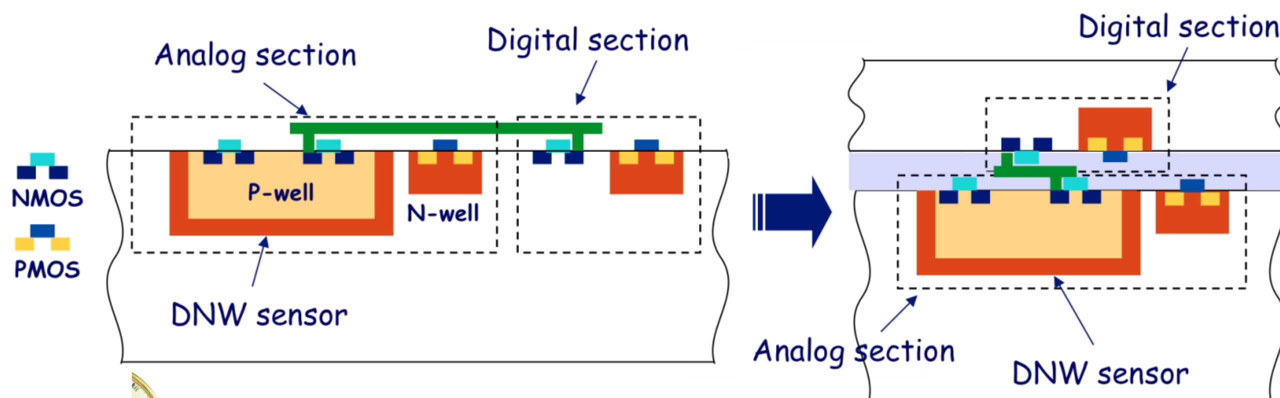
- Larger signal available from the detector (≥ 4000 e^- for 200 μm thickness)
- More advantageous trade-off between S/N and dissipated power

From 2D to 3D DNW MAPS

- Cell functionalities are split onto two different CMOS layers
  → higher functional density at the pixel level
- Sensor and analog front-end can be integrated in a different layer from the digital blocks
  → less digital to analog interference
- PMOS competitive n-wells can be placed on a separate layer from the sensor
  → improved collection efficiency

Photograph of a 3D vertically integrated chip





- The 2nd wafer thickness is about 12 μm
- More room for both analog and digital power and signal routing