ETD - SVT Electronics Update

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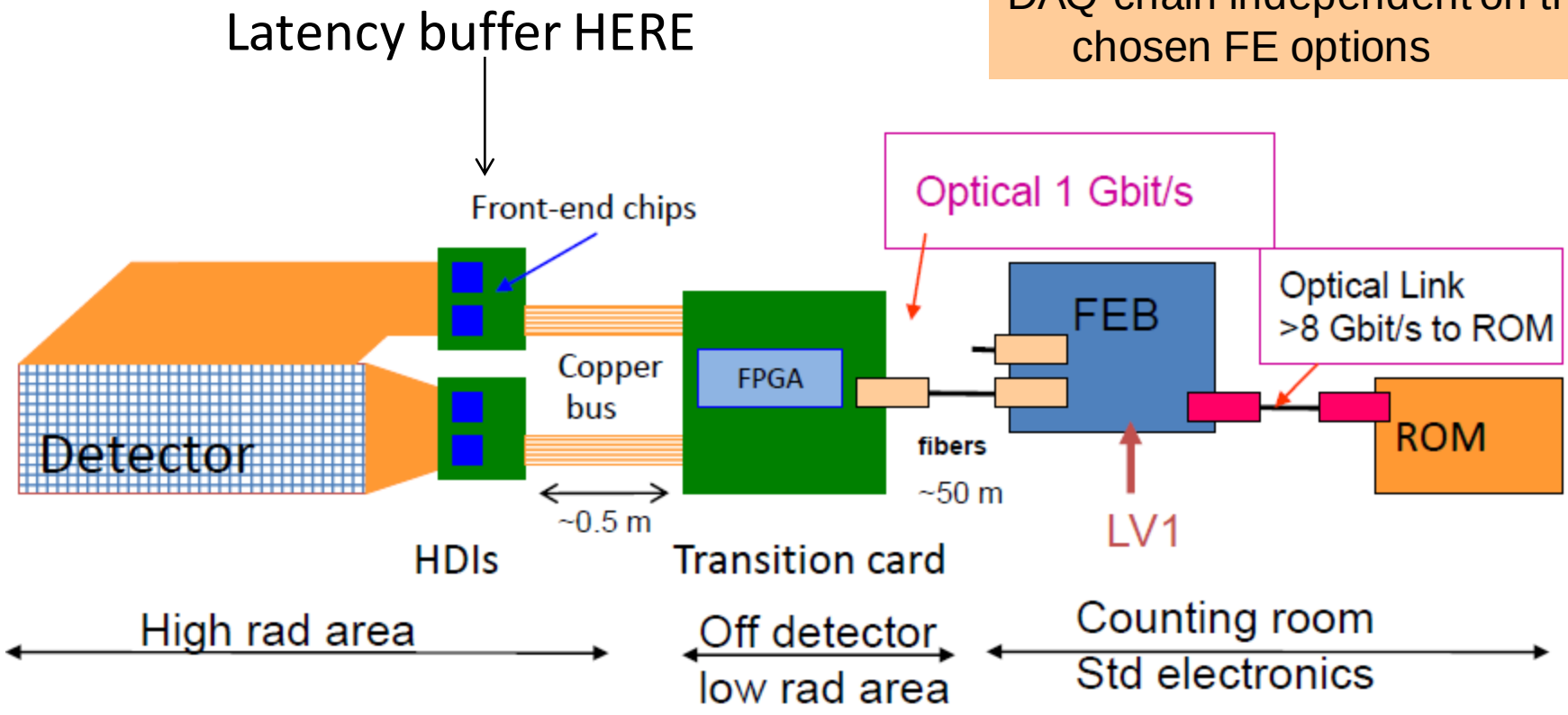
INFN Bologna

6th SuperB Collaboration Meeting, Frascati – December 11th-14th 2012

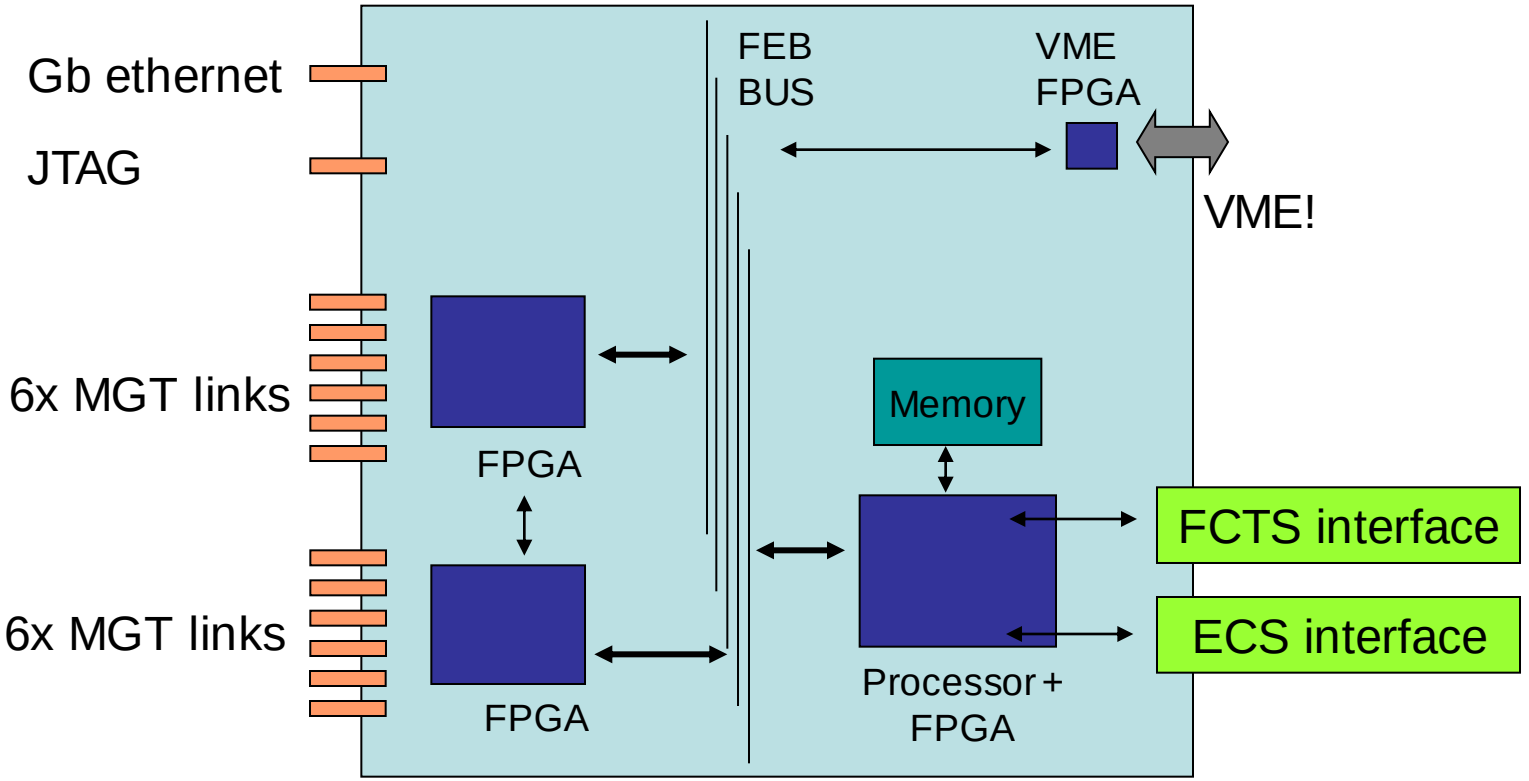
...last one?

SVT reading chain for L0-L5

DAQ chain independent on the chosen FE options



SuperB-FEB Board Scheme



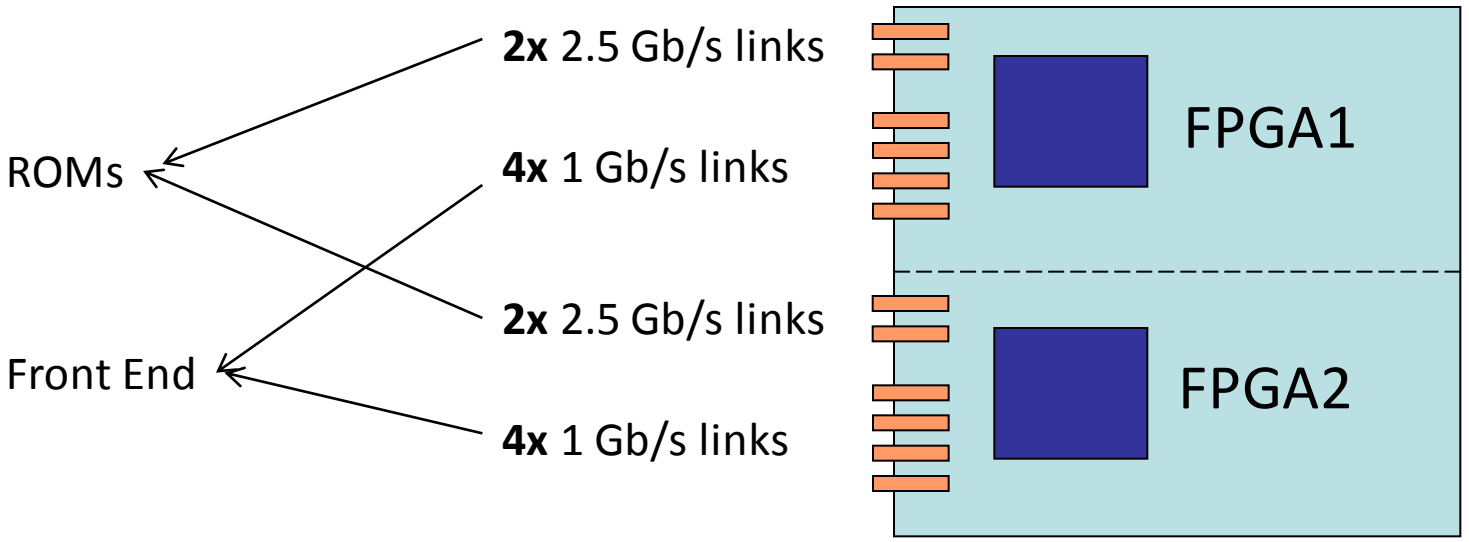
Kintex-7 FPGAs with **Multi-Gb Transceivers** for FE links/DAQ ROMs

- FE interface (clocking/programming/controlling)
- Data Collectors / Data Transmitters
- Event Builders

Zynq All Programmable SoC (ARM Cortex A9 + FPGA fabrics)

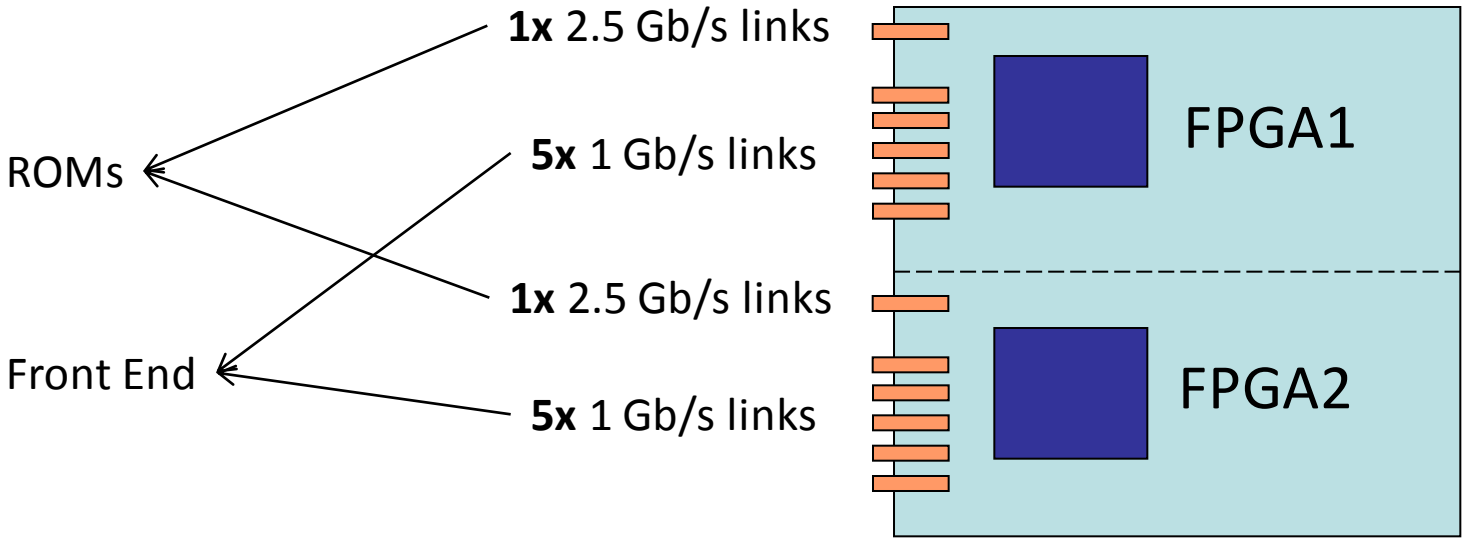
- Control / monitoring / processing / Trigger distribution

FEB boards dual configuration: Layer0



- 4 Links @ 2.5 Gbps to Roms
- 8 Links @ 1 Gbps to Front End Modules

FEB boards dual configuration: Layer1-5



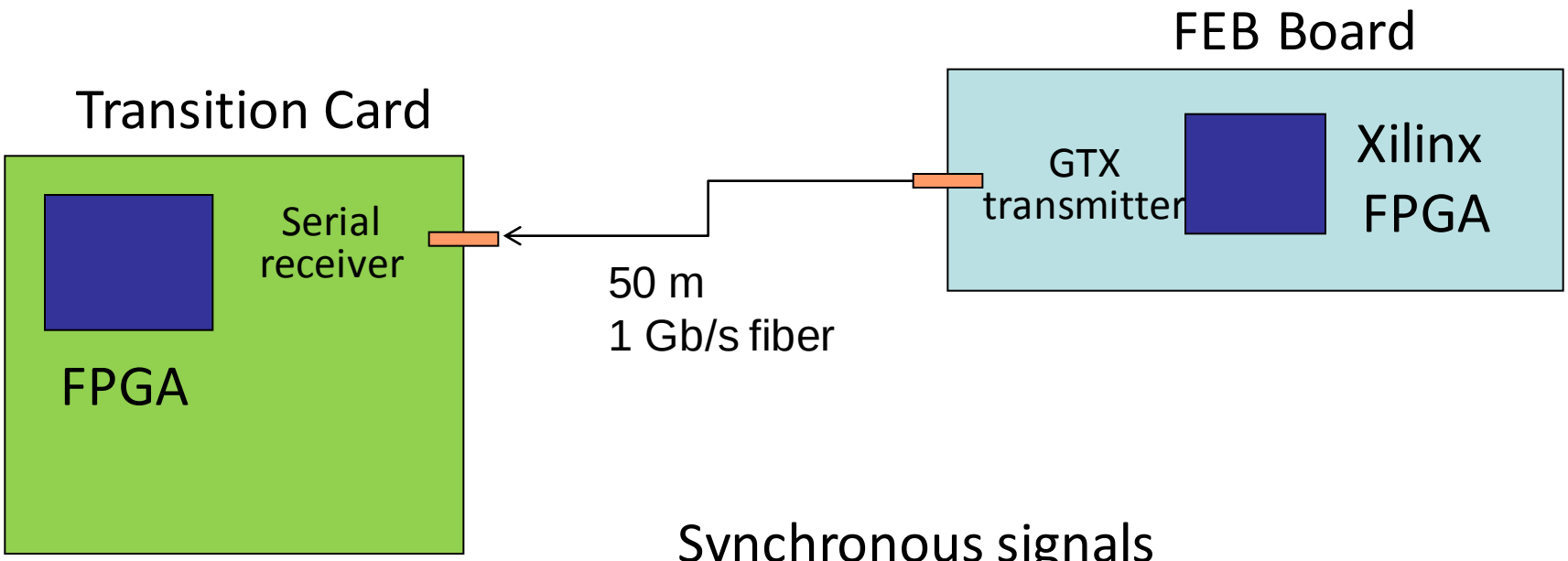
- 2 Links @ 2.5 Gbps to Roms
- 10 Links @ 1 Gbps to Front End Modules

FE boards

Configuration	FEM boards	ROM links per FEM board	TOT ROM links
Layer0	4	4	16
Layer1-5	20	2	40

- TOT **56 Links** @ 2.5 Gbps to ROMs (as reported in TDR)

FE Modules Downlink



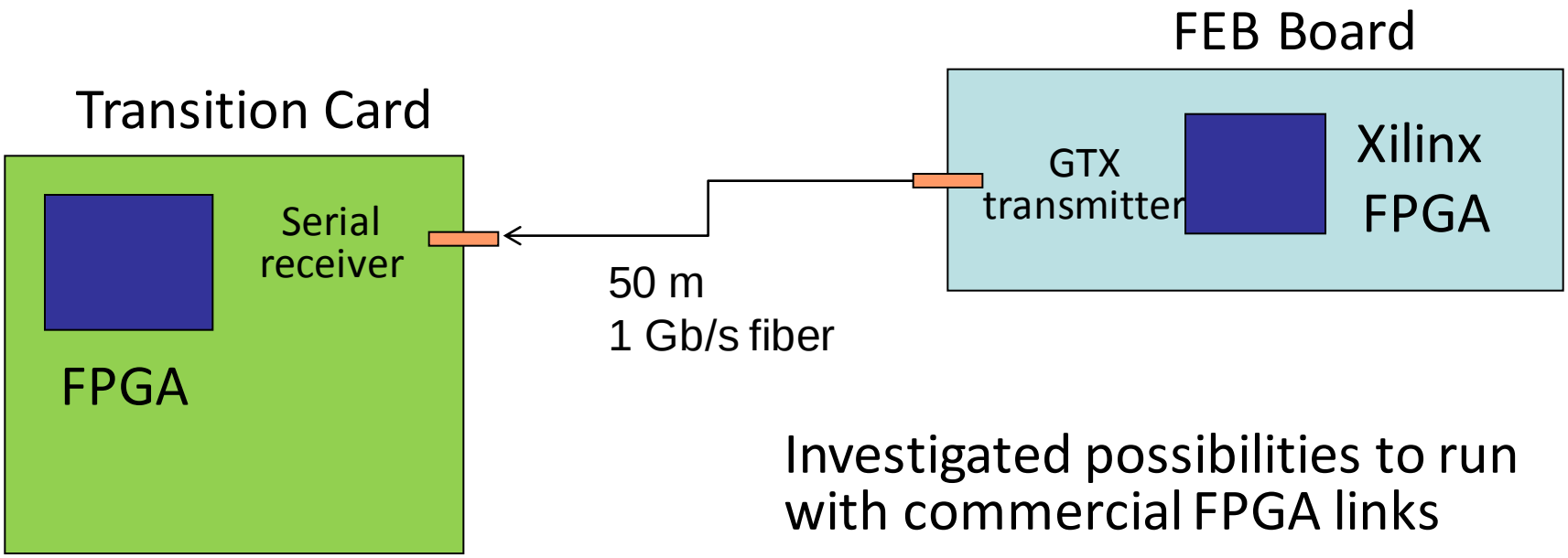
Synchronous signals

- Recovered system clock
- BC clock (Timing)
- Trigger

Slow Control

- FE chips programming
- FE electronics control

FE Modules Downlink



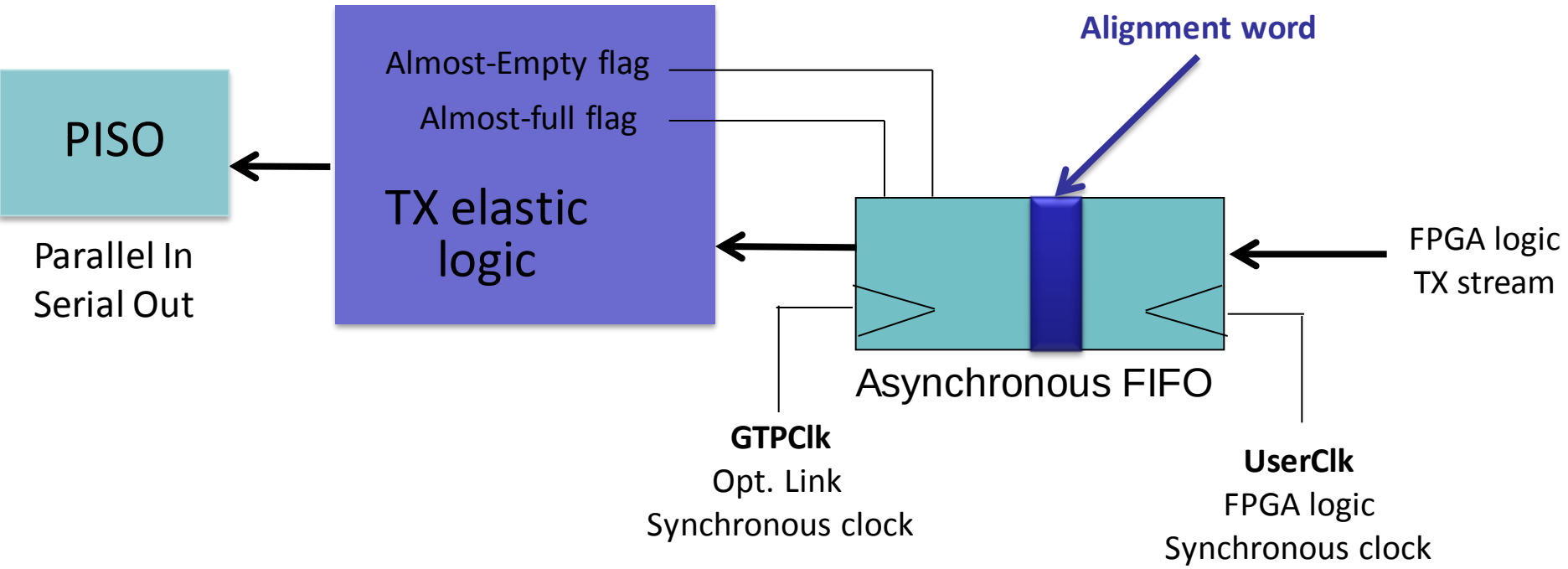
Investigated possibilities to run with commercial FPGA links

Spartan6 GTP link tested in Bologna @ 2.5 Gbps

BC/Trigger Latency between reset cycles is **fixed**

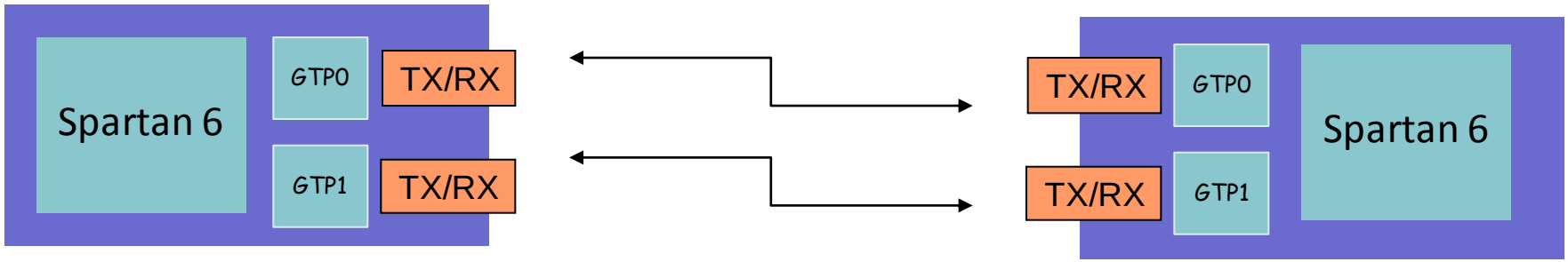
Specific GTP configuration is needed (**NO TX/RX elastic buffer**)

TX Elastic Buffer



- OutClk = InClk (± some ppm)
- **Alignment words MUST be** inserted periodically
- Alignment words can be **skipped** or **repeated** to avoid buffer overflow/underflow
- Intrinsic Async. Transmission → no fixed latency

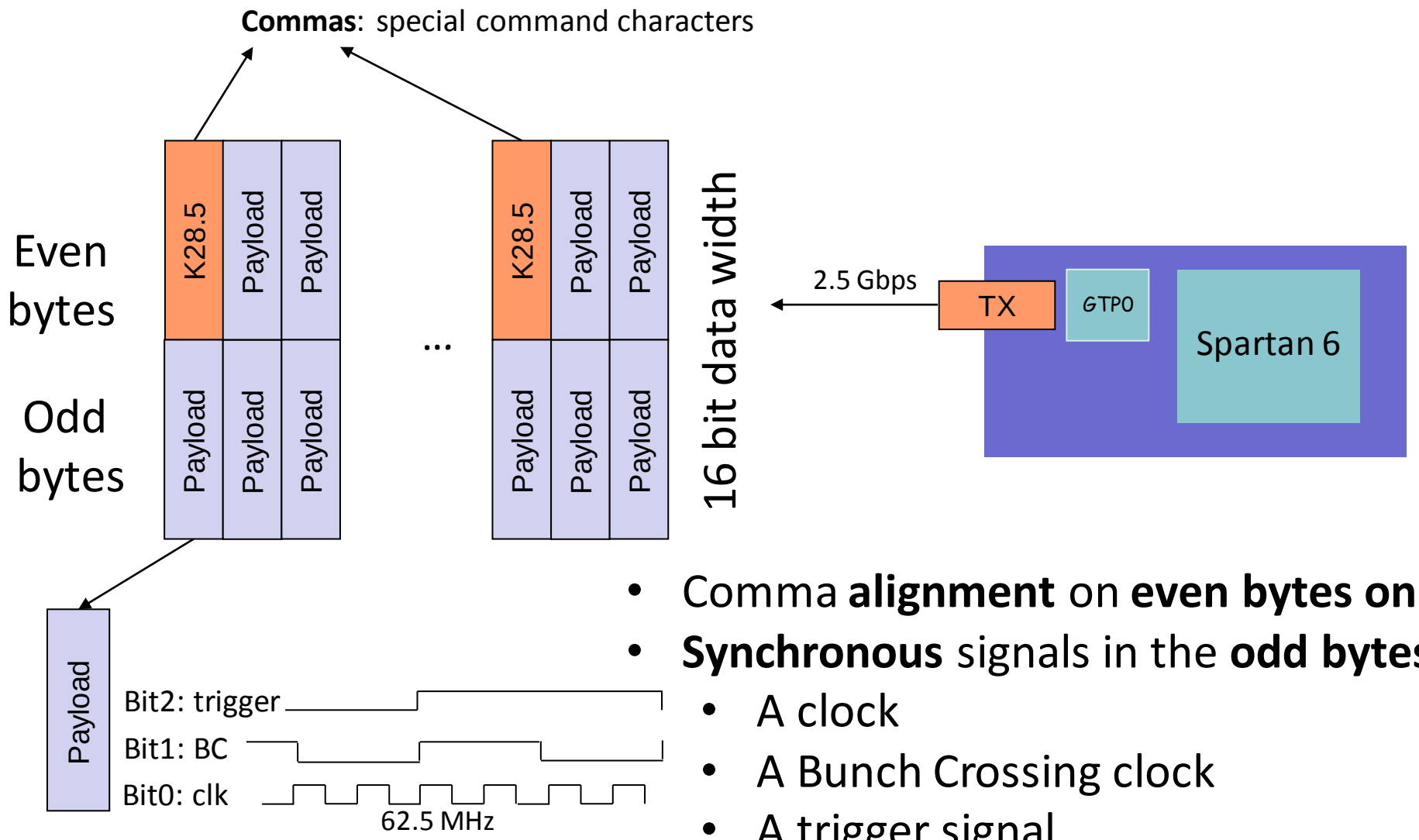
What we did on a couple of custom Spartan6 board: PRELIMINARY "toy play" with GTPs



- Elastic buffer removed
- GTP Built-in procedure for UserClk/GTPClk alignment
- 8b/10b encoding
- 2.5 Gbps links
- **TX side**: All clocks derived from the same **reference clock**
- **RX side**: All clocks derived from the same **recovered clock**

- Measured ΔT at RX side of synchronous, periodic commands (k characters) while **link is always up**.
  - RESULT: latency is fixed (billions of counts) as long as the link keeps up

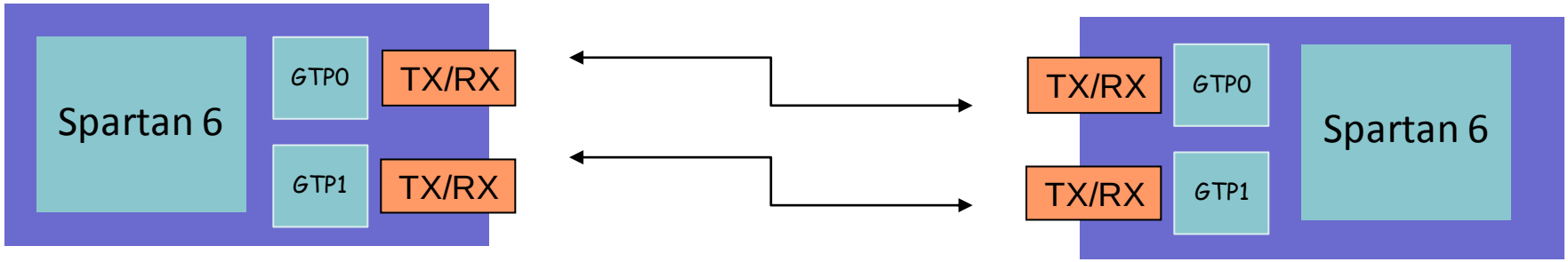
Fixed latency transmissions



- Comma **alignment** on **even bytes only** .
- **Synchronous** signals in the **odd bytes**
  - A clock
  - A Bunch Crossing clock
  - A trigger signal

1.6 Gbps -> 40 MHz clk

Next: Fix latency after GTP reset / power-up

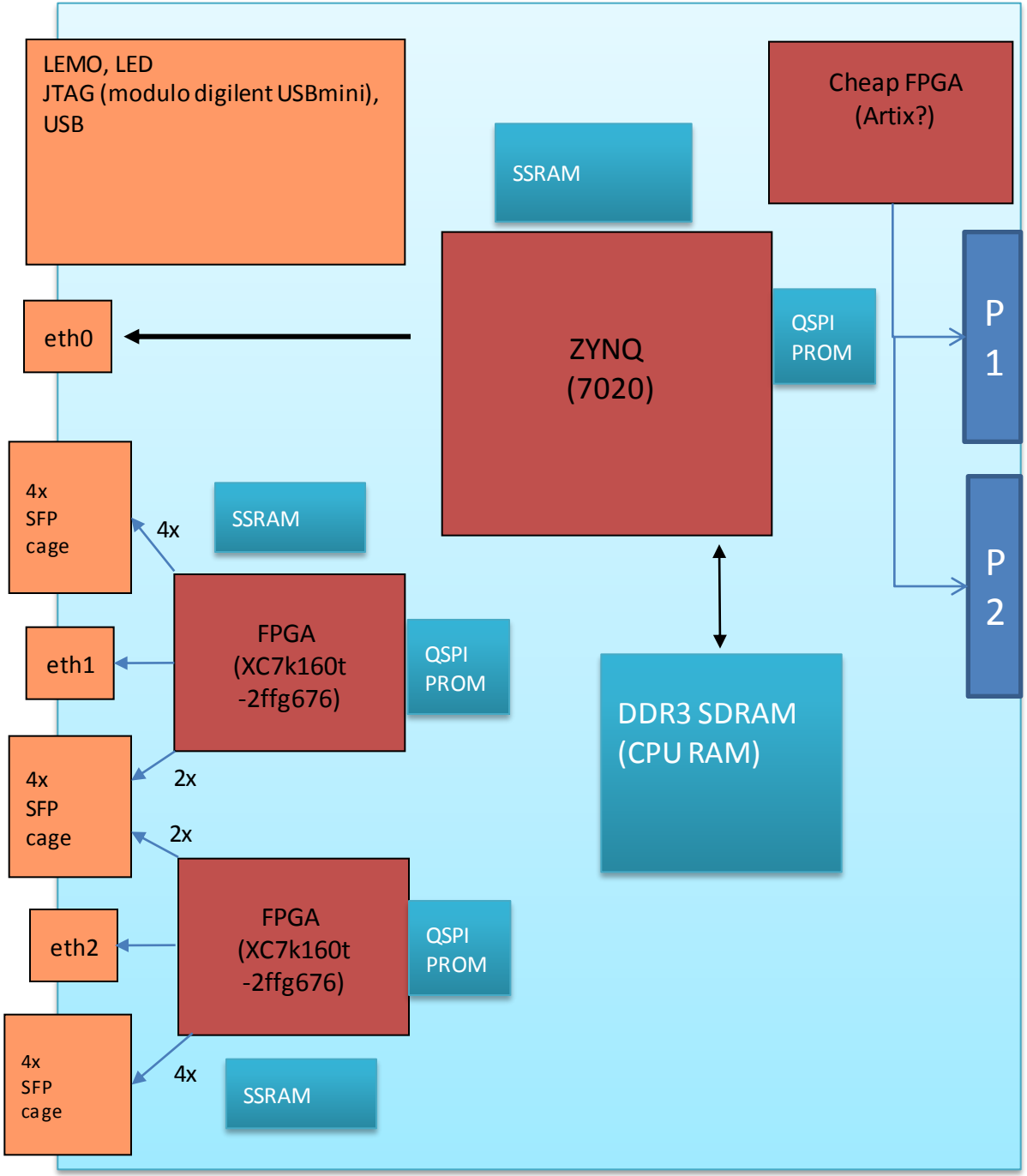


Clock alignment after a Physical Reset:

Fixed power-up latencies are possible. Found several researches about:

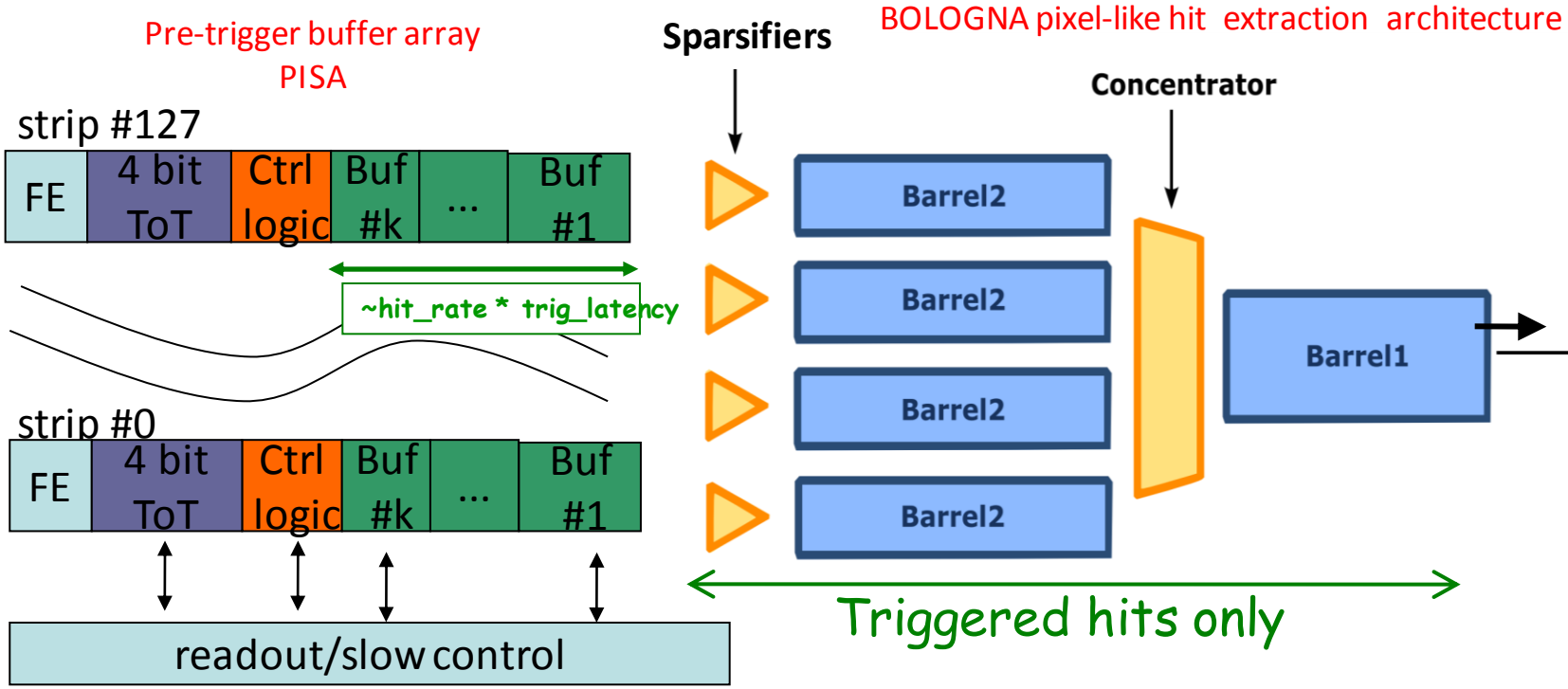
- *Fixed Latency Multy-Gigabit Serial Links with FPGAs. Aloisio, Giordano, Izzo*
- *Phase and latency reproducibility in COTS*. Sophie Baron, TTC for sLHC, CERN

FEB Details


LEMO, LED
JTAG (modulo digilent USBmini),
USB
Cheap FPGA
(Artix?)
SSRAM
ZYNQ
(7020)
QSPI
PROM
eth0
P
1
P
2
VME
4x
SFP
cage
4x
SSRAM
FPGA
(XC7k160t
-2ffg676)
QSPI
PROM
eth1
DDR3 SDRAM
(CPU RAM)
4x
SFP
cage
2x
2x
FPGA
(XC7k160t
-2ffg676)
QSPI
PROM
eth2
4x
SFP
cage
4x
SSRAM

BackUp

Strip readout architecture under development



Triggered event size not known a-priori
(thus readout time as well)

TDR – SVT readout electronics

- Readout chain scheme and reference to the relevant SVT parts
  - (FE and hybrids)
  - (Transition card)
    - Serializers / Links / Trigger / HV
- Design of the Readout Card
  - Input data links/Data compression/Output links
- Fast (Trigger) and slow (configuration) signals handling
- Final Data rates and data volumes

Strip readout chip simulations

Strip FE architecture defined, modeled and simulated.
Digital readout efficiency measured value (simulations)
~100% with buffer depth = 32

2 MHz/strip : Layer 0

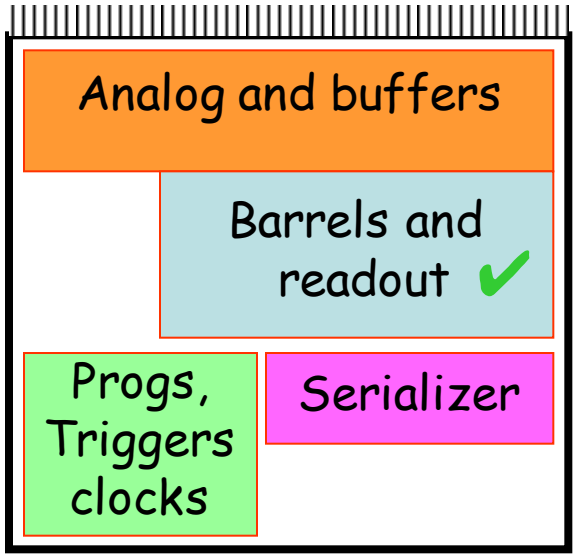
buffer size	16	32	64
buffered hits	3.8 M	12.9 M	12.9 M
of which triggered	23363	76850	23363
output triggered hits	14679	76849	23363
triggered hit lost	8684	1	0
Efficiency (%)	**62.8**	**99.9987**	**100**

Buffer Depth Scan

760 kHz/strip : Layer 1

buffer size	8	16	32
buffered hits	1.4 M	7 M	7 M
of which triggered	8748	28829	28829
output triggered hits	6788	28825	28829
triggered hit lost	1960	4	0
Efficiency (%)	**77.6**	**99.986**	**100**

Digital periferical logic blocks



- Progs, Triggers, clocks:
  - Embedded in the readout architecture and actually part of it. It allows the trigger latency control, clock handling, channel masking, running
- Serializer Interface:
  - Sends out data (16 bits wide) on a programmable number of lines (1, 2, 4, 6)
  - Protocol (8b/10b?) and implementation to be defined.

Clock, Trigger, Registers

- Current set-up is flexible → 7 I/O programming lines
- 6 inputs: Reset, Clock (60MHz), FastClock (180 MHz?),Timestamp, Trigger, RegIn
- 1 Output: RegOut

- NB: SuperB trigger protocol not yet defined
- Contr: no redundancy

- Minimal number of lines:
  - 2 inputs: FastClock (180 MHz?), RegIn
  - 1 output: RegOut

- Requires assumptions on trigger protocol

- Clock, Timestamp and triggers have to be in sync on the whole system!

Two line command implementation

- A fast clock line (180 MHz) and a programming line
- Slow clock (60 MHz) produced internally with known phase
- I2C like commands sent with the programming line to
  - Reset & smart reset the chips
  - Fine-tune the 60 MHz phase
  - Program masks and internal registers
  - Define the timestamp period (slow clock period units)
  - Define the start of the time stamp clock
  - Define the trigger latency
  - Monitor phases of clocks, time-stamps, rates, statuses

  - define the acquisition window in time-stamp units (start and lenght variable) for each FTCS trigger.

FEB Board functionalities

1. FE chip clock, timestamp and trigger signals distribution
   - Check and keep FE chips (>1600) in sync !
2. Configure FE chips (MB of data to upload), provide calibration mechanisms
3. Convert SuperB LVL1 signal to SVT trigger signal (timestamp aware)
4. Acquire FE hits, provide a first data compression
   - TS stripping, hit packing (clusterization?)
5. Send data to ROM
6. HW monitoring of data

ETD knowns and unknowns

- Known: ECS (Experiment Control System) protocol is ethernet
- Known: ROM link is optical. Guaranteed 1 Gbps, aiming at larger bandwidths (**2.5**, 5 or more Gbps).
- Unknown: rad-hard serializer and optical link to be put on detector (assuming fixed latency, 1 Gbps).
- Unknown: Hosting crates (VMEx, ACTA)

Strip front-end chip

- Triggered, 128 channels, 60 MHz clock, 60/120/180 MHz output clock, serialized output.

2 Data word: Time-stamp-like and hit

Hit: 7 bits Channel ID, 4 bits ToT, 1 bit word type,
4 bits to be defined, for a total of **16 bits**

Timestamp: 10 bits Timestamp, 1 bit word type,
5 bits to be defined, for a total of **16 bits**

Guesswork: serialization using a 8b/10b protocol implies a **20 bit output word**

Layer	layer Type	Chip /ROS	Avai chans	back. rate MHz/ cm2 (safety = 5)	Hits in BCO	Occup ancy in BCO	Group ing	Trigge red Gbit/s/ GROS	FE Board s	Event Size (hits)
0	Striplet u	6	768	230	50.2	6.54%	1	1.51	3	8037
0	Striplet v	6	768	230	50.2	6.54%	1	1.51	3	8037
1	Strip z	7	896	10.31	13.6	1.52%	1	0.41	1	1637
1	Strip phi	7	896	14.97	19.8	2.21%	1	0.59	1	2377
2	Strip z	7	896	6.88	12.9	1.44%	1	0.39	1	1550
2	Strip phi	7	896	8.81	16.5	1.85%	1	0.50	1	1985
3	Strip z	10	1280	2.994	12.0	0.94%	1	0.36	1	1438
3	Strip phi	6	768	2.35	9.4	1.22%	1	0.28	1	1129
4a	Strip z	5	640	0.218	1.0	0.15%	2	0.20	1	1038
4a	Strip phi	4	512	0.337	1.5	0.30%	2	0.30	1	1605
4b	Strip z	5	640	0.218	1.0	0.16%	2	0.20	1	1075
4b	Strip phi	4	512	0.337	1.6	0.31%	2	0.31	1	1662
5a	Strip z	5	640	0.114	0.6	0.10%	2	0.13	1	769
5a	Strip phi	4	512	0.159	0.9	0.18%	2	0.18	1	1073
5b	Strip z	5	640	0.114	0.7	0.10%	2	0.13	1	793
5b	Strip phi	4	512	0.159	0.9	0.18%	2	0.18	1	1106

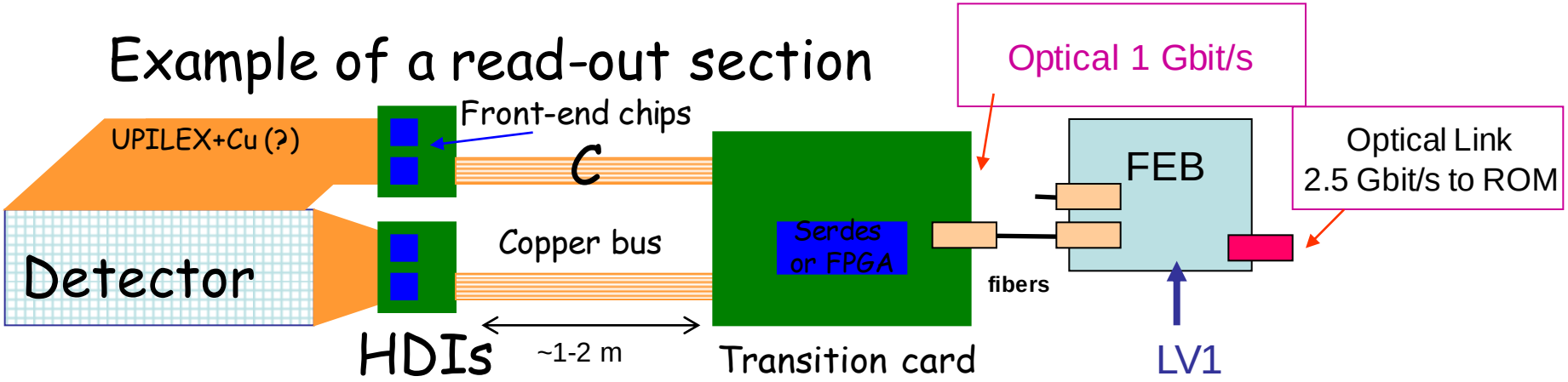
- 172 GROS, 204 1-Gbps links, 20 FEBoards, <88 kB/evento

Maximum data lines per chip

		Max HIT strip rate (kHz)	DAQ Time window (us)	Hits/ chip per Trig.	Words per chip per trigger	Bits per chip per trig.	band width (Mbit /s)	Lines at 60 MHz	Line s at 120 MHz	**Lines at 180 MHz**	Chip/ ROS	Lines/RO S at 180 MHz
L0	U	2000	0.3	76.8	86.8	1736.0	260.4	6	3	**2**	6	**12**
L0	V	2000	0.3	76.8	86.8	1736.0	260.4	6	3	**2**	6	**12**
L1	Z	727	0.3	27.9	37.9	758.3	113.8	3	2	**1**	7	**7**
L1	PHI	1445	0.3	55.5	65.5	1309.8	196.5	4	2	**2**	7	**14**
L2	Z	697	0.3	26.8	36.8	735.3	110.3	3	2	**1**	7	**7**
L2	PHI	960	0.3	36.9	46.9	937.3	140.6	3	2	**1**	7	**7**
L3	Z	676	0.3	26.0	36.0	719.2	107.9	3	2	**1**	10	**10**
L3	PHI	775	0.3	29.8	39.8	795.2	119.3	3	2	**1**	6	**6**
L4	Z	204	1	26.1	36.1	722.2	108.3	3	2	**1**	5	**5**
L4	PHI	195	1	25.0	35.0	699.2	104.9	3	2	**1**	4	**4**
L5	Z	133	1	17.0	27.0	540.5	81.1	2	1	**1**	5	**5**
L5	PHI	135	1	17.3	27.3	545.6	81.8	2	1	**1**	4	**4**

1,2,4 lines **per chip** usable at 120 MHz on all SVT
14 lines **per module** max at 180 MHz (16 bits serializers)

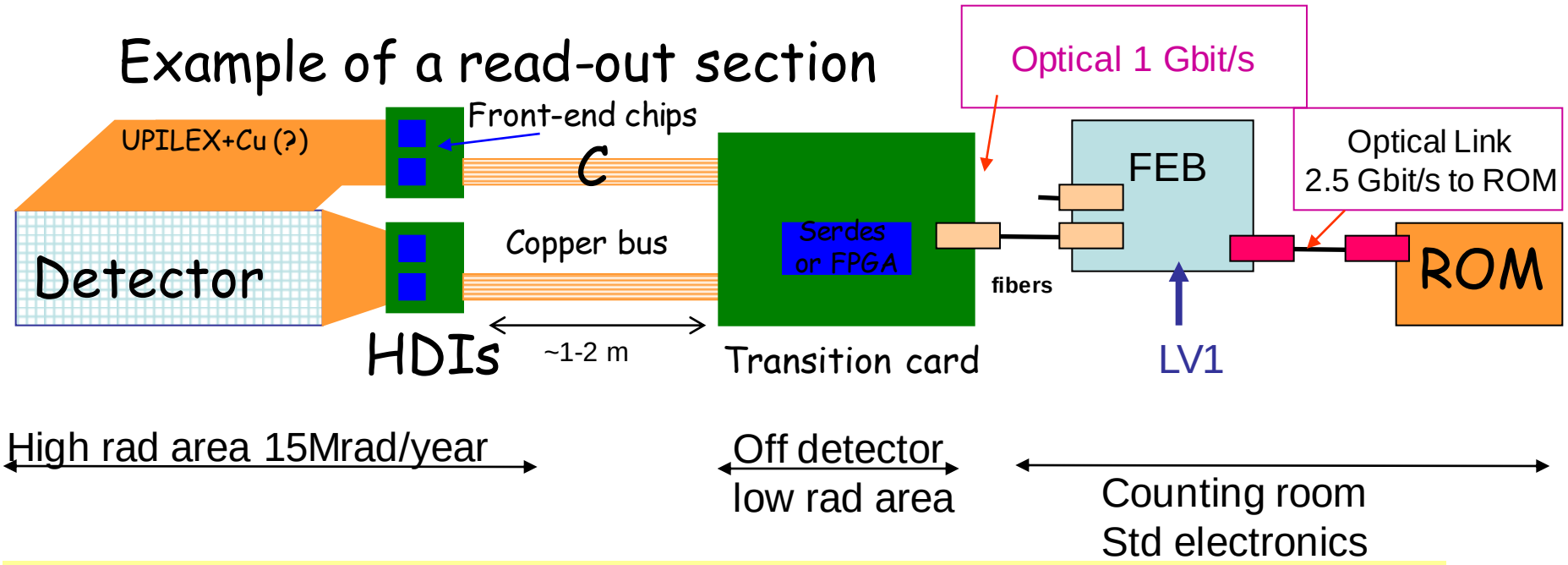
DAQ Activities ongoing



- Studies ongoing for fixed-latency data transmission over optical fibers.
- Latencies have to be **measurable** for: Clock, Timestamp and Trigger
- Test beds for optical links and latencies measurements in place: using xilinx FPGA SerDes
- Front-End board: component selection phase

DAQ reading chain for L0-L5

DAQ chain independent on the chosen FE options



Data Encoder IC .... Specs are under discussion
Rad-hard serializer to be finalized
→ looking into a low power/low speed version
Copper tail: lenght vs data transfer to be studied

FEB Board functionalities

1. FE chip clock, timestamp and trigger signals distribution
   - Check and keep FE chips (>1600) in sync !
2. Configure FE chips (MB of data to upload), provide calibration mechanisms
3. Convert SuperB LVL1 signal to SVT trigger signal (timestamp aware)
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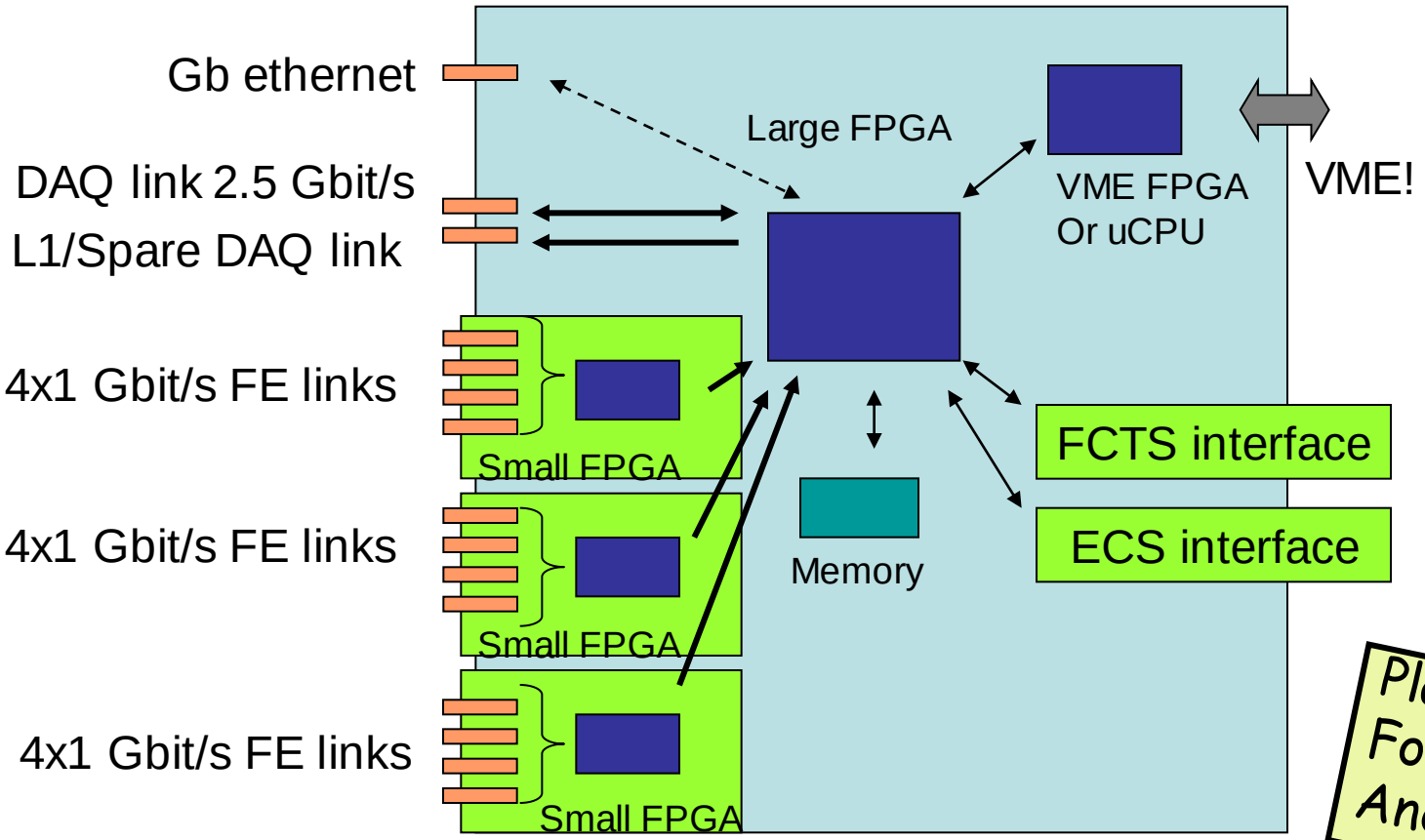
SuperB-FEB Board schematics OLD

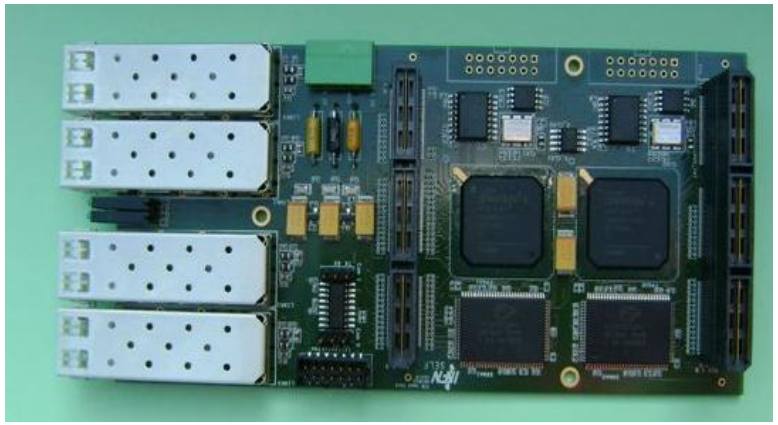


Planning
For changes
And extensions

FCTS protocol to be decided experiment-wide
Large FPGA for data shipping and monitoring
VME FPGA or uCPU might be included in the large FPGA.

Input mezzanines

- Input optical links on mezzanines to easy future upgrades
- 4 1-Gbps optical link mezzanine compatible with EDRO available for tests
- Small FPGA (spartan) and memory on board



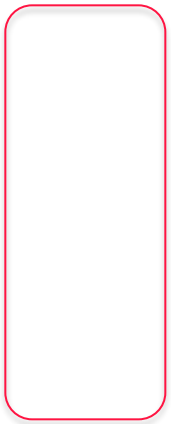
Hit and Trigger generation and read out

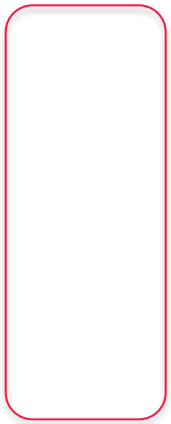
- Bare Assumptions:
  - Readout clock: 60 MHz
  - Time stamp clock: 30 MHz
  - Trigger rate: 150 kHz
  - Fully triggered SVT
  - DAQ Acquisition window: 300 ns (L0-L3), 1 us (L4-L5)
  - Latency <10 us
  - Buffers in chip and in reading chain wide enough for eff>99.8%
  - Optical link 1 Gbit/s ; 2.5 Gbit/s to ROM
  - Background rates from latest BRUNO simulations with safety factors 5

SVT Background rates

Background simulation: R. Cenci, dec 2011; factor >2 increase

- Strip detail implemented in Bruno for a more accurate rate calculation





Data volumes and bandwidths

SVT data volumes and bandwidths are mostly independent on the details of the design, but are defined mainly by background, trigger rates and DAQ time windows.

SVT Data rates, links and boards

MC data from R. Cenci, dec 2011

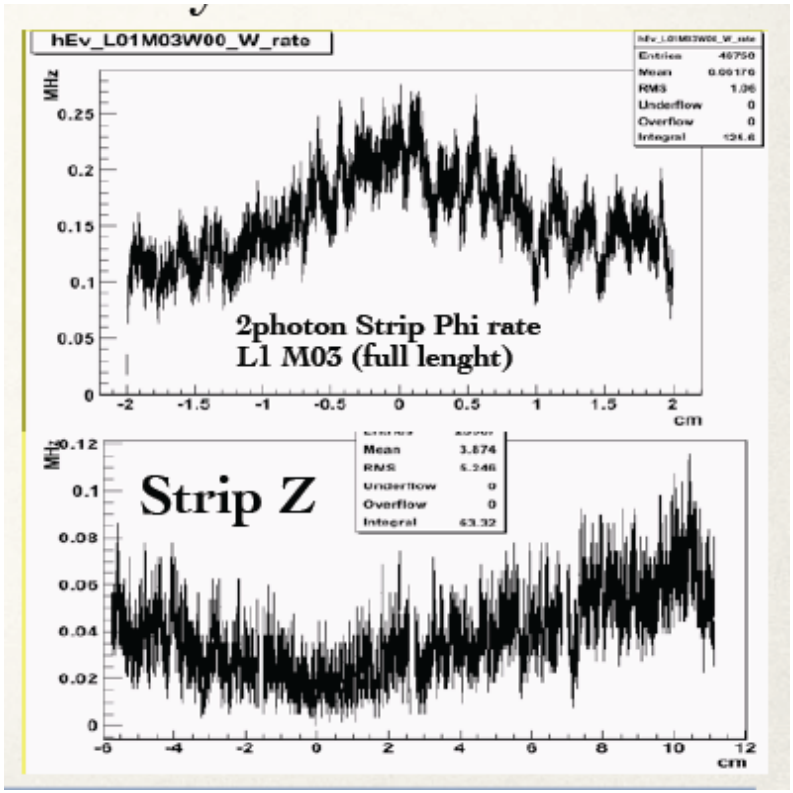
Layer	Modules	HDI	ReadOut Section (ROS)	Grouped ROS	FEBoard	Plain rate Data to ROM/ FEBoard (Gbps)
0 (pixel)	8	16	32	32	4	5.7
1	6	12	24	24	2	6.9
2	6	12	24	24	2	6.3
3	6	12	24	24	2	5.9
4	16	32	64	*32*	4	1.7
5	18	36	72	*36*	4	1.2
Total/mean	60	120	240	172	18	3.5 (strip)

Needs: 172 1-Gbps links, 18 Front-End Boards

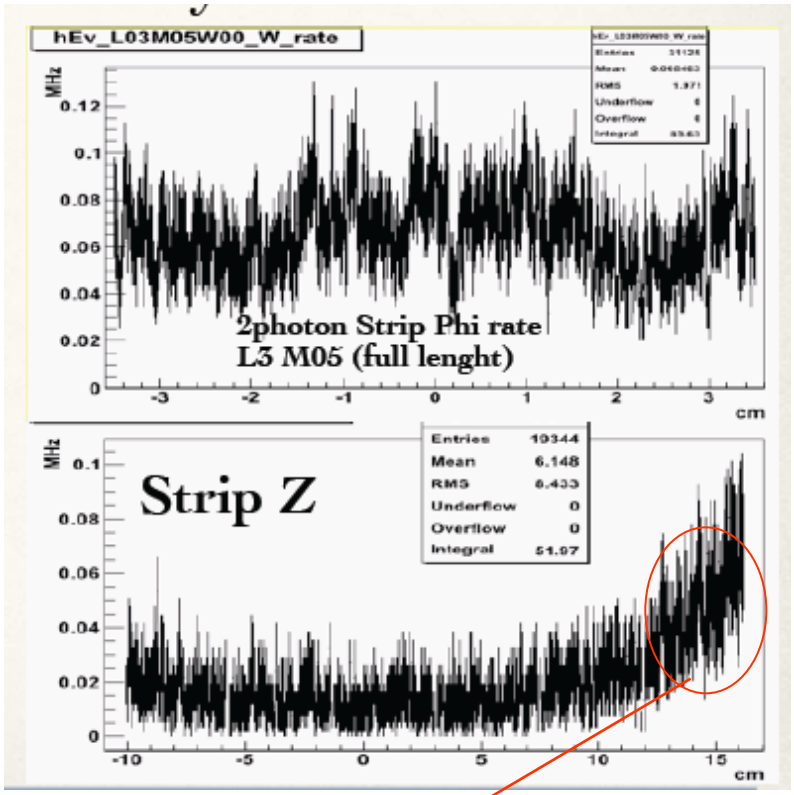
Average event size: 60 kB. 2.5 Gbps links NOT usable.

Needed a factor 2-3 data compression.

Layer 1



Layer 3



Il pairing riduce le hits
e quindi i rates

Be aware of Safety Factors around

- Trigger rate: 150 kHz	SF: 1.5
- Hit width (14 vs 12)	SF: 1.2
- DAQ Acquisition window	SF: 1.5
- Optical link 1 Gbit/s	SF: 1.2
- Background rates	SF: 5
- Ignored clusterization (pixels)	SF: 1.2-1.5 (?)
- Pairing and Gangling (strips)	SF: 1-1.5 (?)

$$TotalSF = \prod SF_i > 20$$

SVT Data rates, links and boards

Layer	Modules	HDI	ReadOut Section (ROS)	Grouped ROS	FEBoard	Plain rate Data to ROM/ FEBoard (Gbps)
0 (pixel)	8	16	32	32	*12*	1.9
1	6	12	24	24	*6*	2.3
2	6	12	24	24	*6*	2.1
3	6	12	24	24	*6*	1.9
4	16	32	64	32	4	1.7
5	18	36	72	36	4	1.2
Total/mean	60	120	240	172	*38*	1.9 (strip)

Needs: 172 1-Gbps links, *38 Front-End Boards & 38 ROMs*
Average event size: 60 kB. 2.5 Gbps links usable.

DAQ Summary

Data chain outlined; FEB functionalities clear

Major (ETD common) unknowns:
- 1 Gbps optical link types (bidirectional?)
- Serdes/FPGA
- Crate type

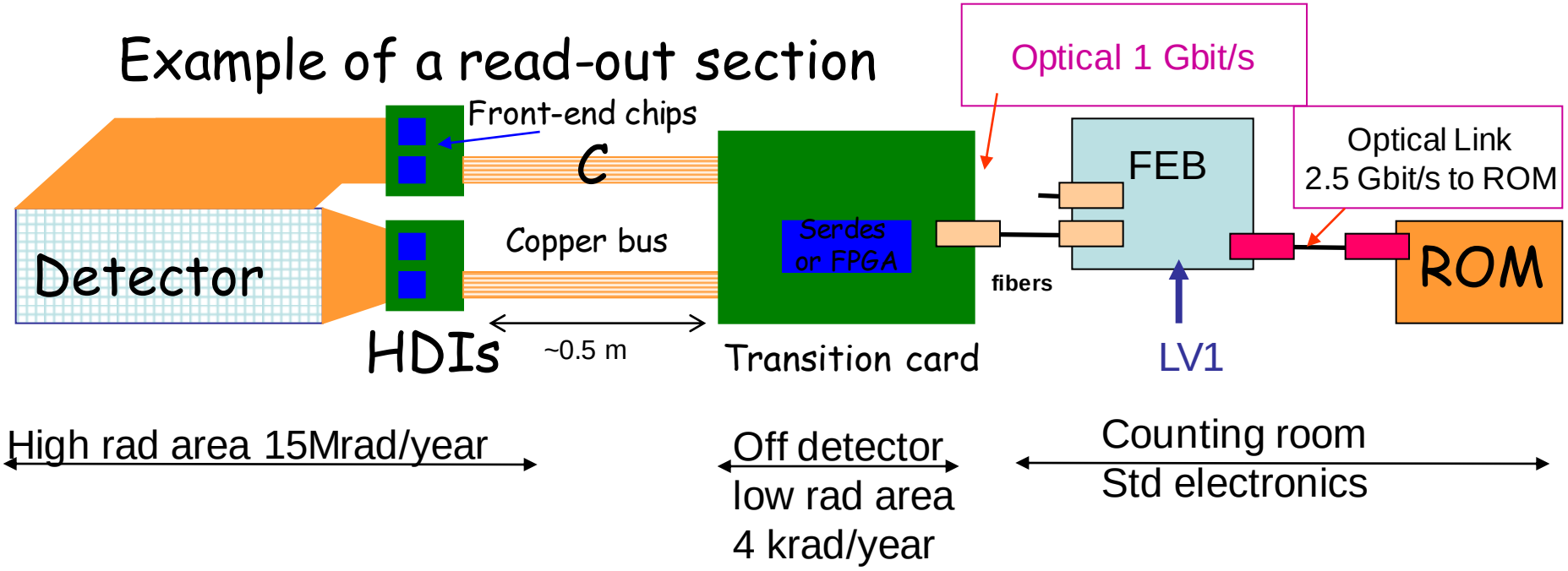
SVT data volumes and bandwidths are mostly independent on the details of the design.
MC (Bkg) simulation still not 100% reliable.

Safety factors all around. Probably still too large.
→100% uncertainty on the number of FEB board!

No showstopper seen in the "upper" part: FEB & ROMs.

SVT reading chain for L0-L5 OLD

DAQ chain independent on the chosen FE options



Studies ongoing for fixed-latency data transmission over optical fibers.
Latencies have to be **measurable** for: Clock, Timestamp and Trigger
Test beds for optical links and latencies measurements in place: using xilinx FPGA SerDes
Front-End board: component selection phase