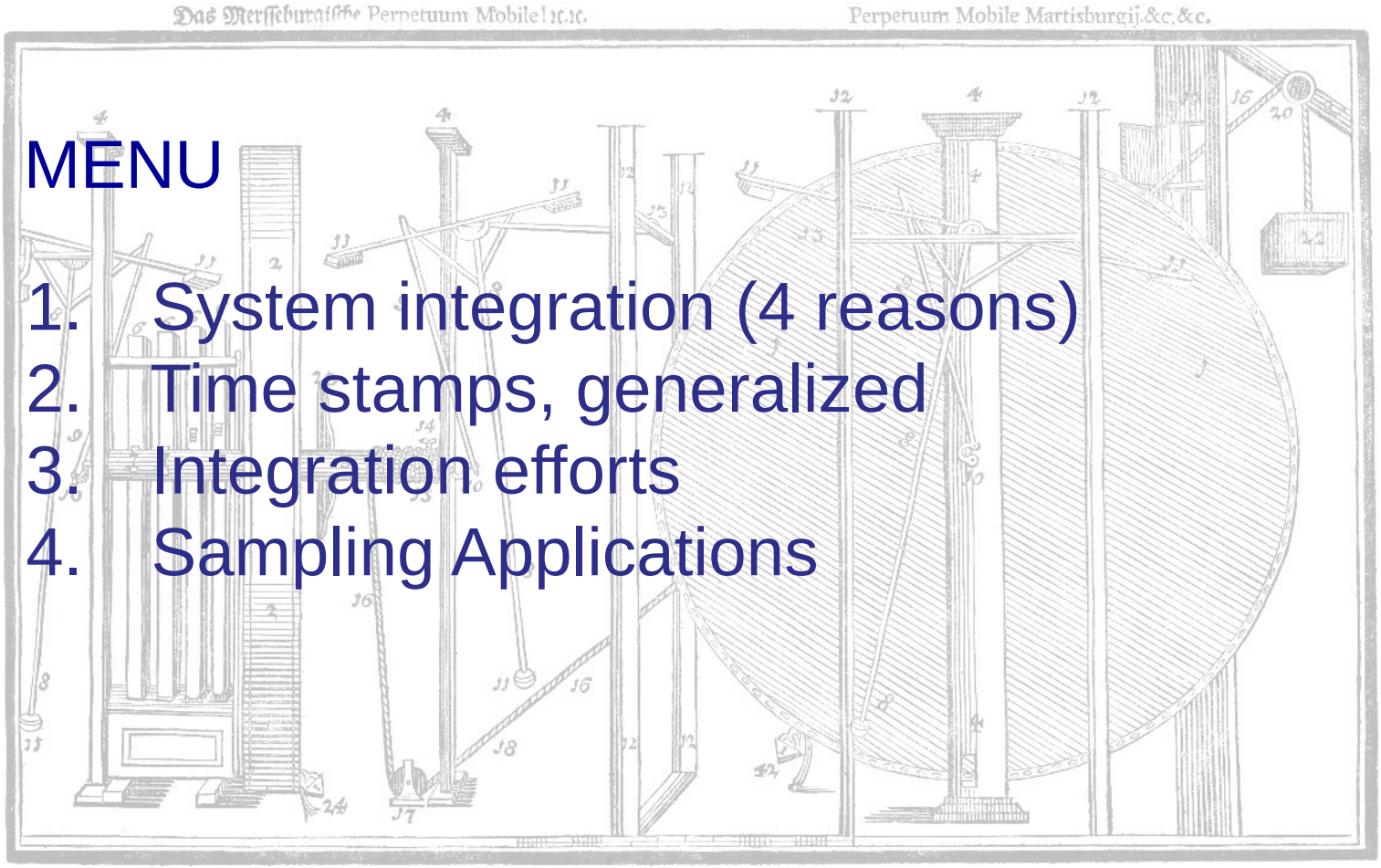
System design for nuclear structure experiments

H.Simon / GSI Darmstadt

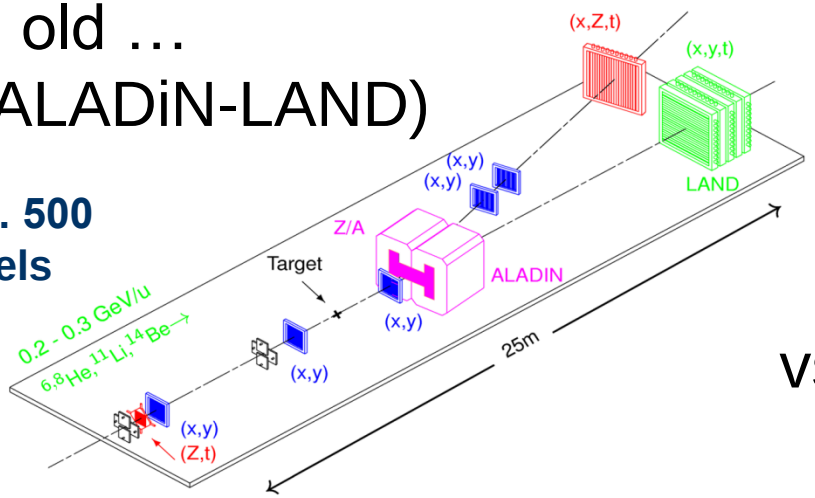


MENU

1. System integration (4 reasons)
2. Time stamps, generalized
3. Integration efforts
4. Sampling Applications

Reason 1: From past to future …

old …
(ALADiN-LAND)

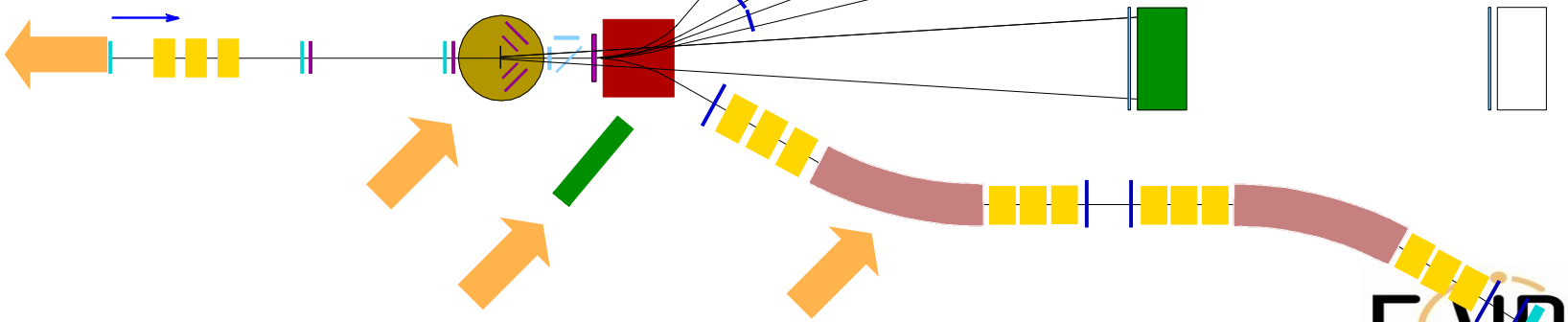


’95 ca. 500 channels

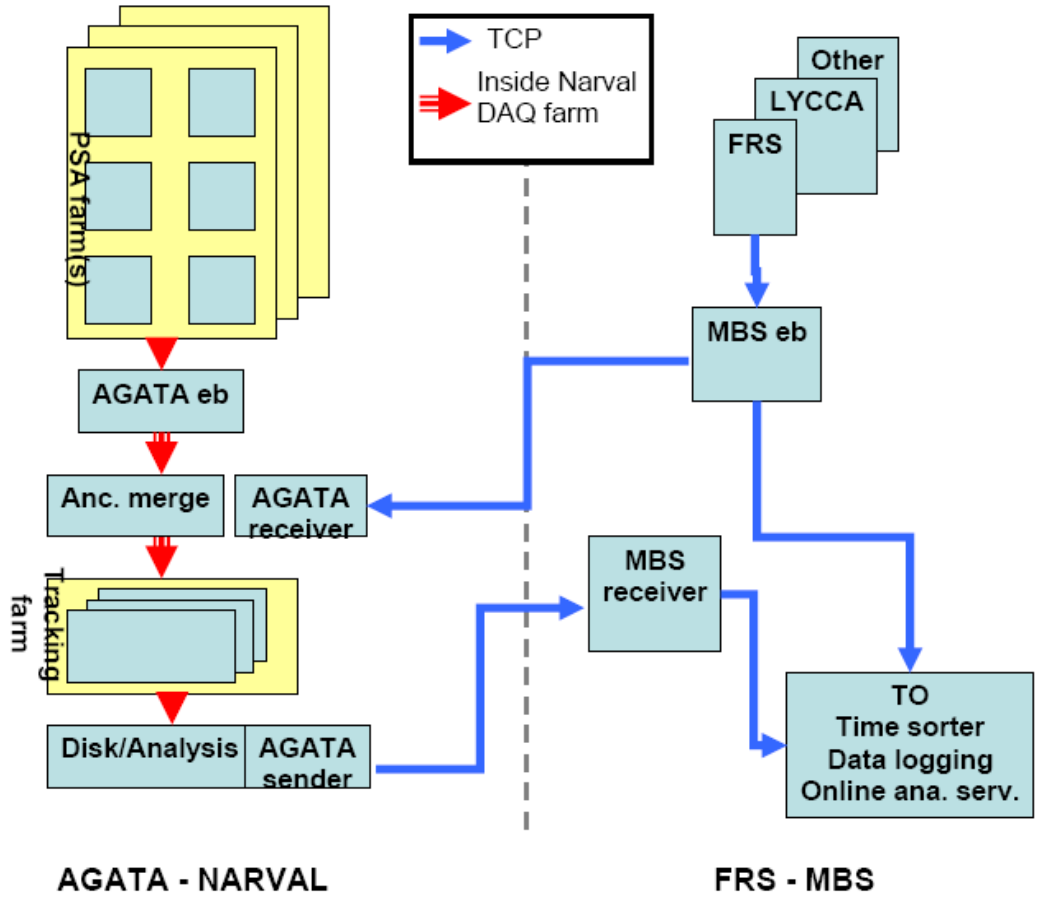
vs.

new
(R³B)

’15 ca. 50’000 channels



Reason 2: External detector systems:
AGATA coupling – data flow merging/coupling



Two parallel data flows

AGATA needs Tracking information for Doppler correction

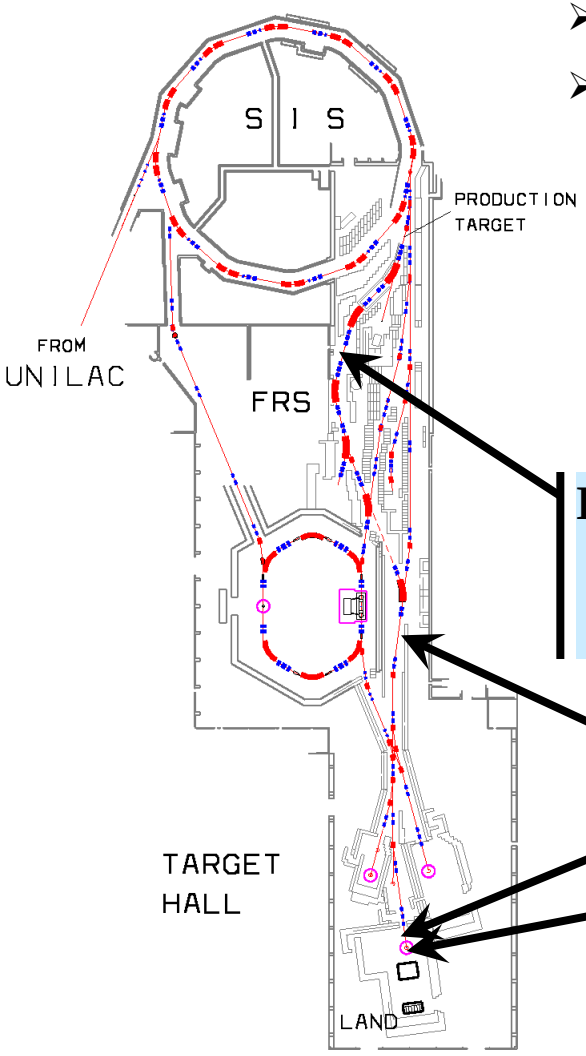
FRS needs Gamma data to optimize beam

Common time stamps

Reason 3:
Continous beam ID is integral part of experiments

Example: ^{132}Sn PDR studies

- Primary: 3*10^{8} ^{238}U/spill @550Mev/u
- Secondary (mixed): 50 ions ^{132}Sn/spill

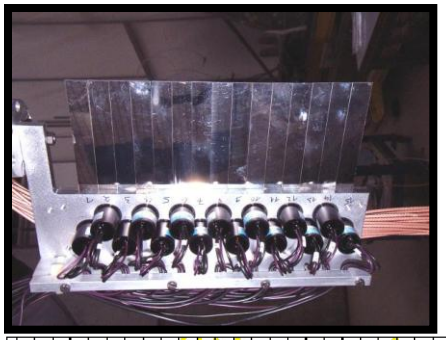


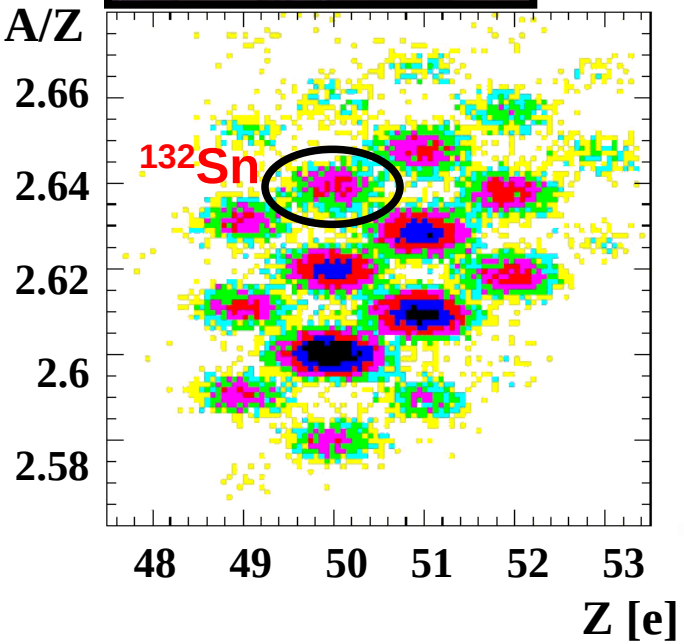
$$\frac{A}{Z} = \frac{m_u c}{e} \frac{B\rho}{\beta\gamma}$$

Bρ – from position at middle focal plane of the FRS

β – from TOF

Z – from ΔE





Reason 4:

Delayed coincidences → Decay studies

Implantation ID DAQ (Spectrometer)

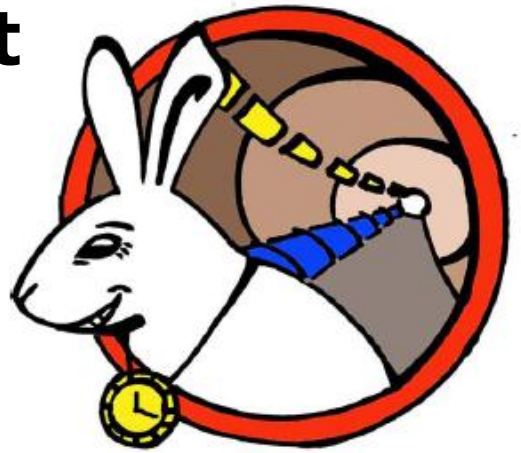
Decay DAQ(s) (independend)

- high rates ➔ dead time free

- overlapping decays & decay channels ➔ dead time free

Time Stamped Events: White Rabbit

T. Włostowski/CERN



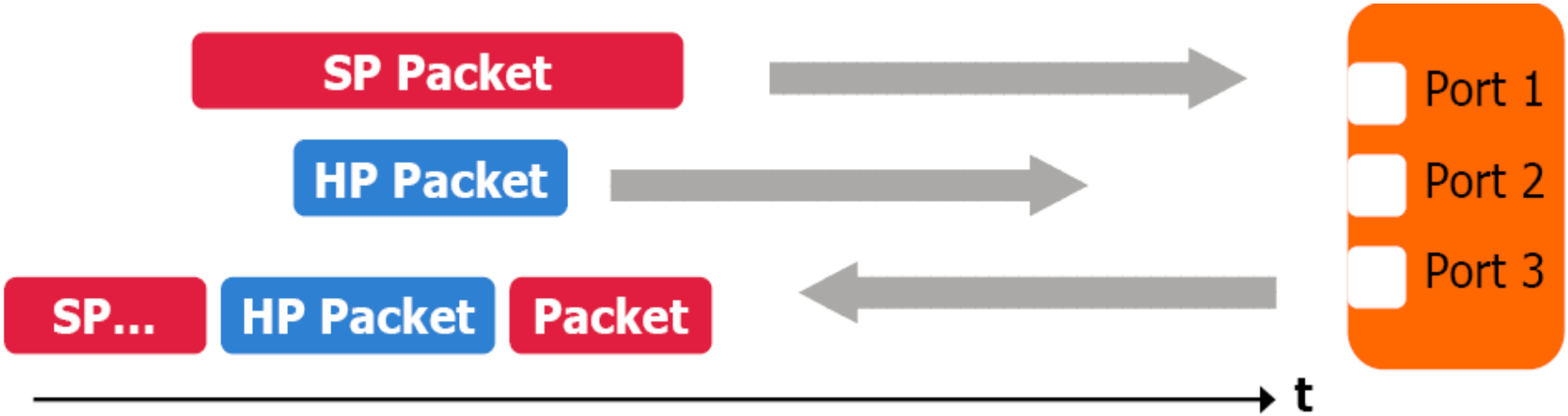
- Extension to Ethernet providing

1. A common clock via synchronous ethernet + compensation from PHY clock (PTPv2@125MHz IEEE1588 + compensation) 10MHz with ~1ns precision and ~100ps accuracy

2. A real time Protocol with guaranted latency

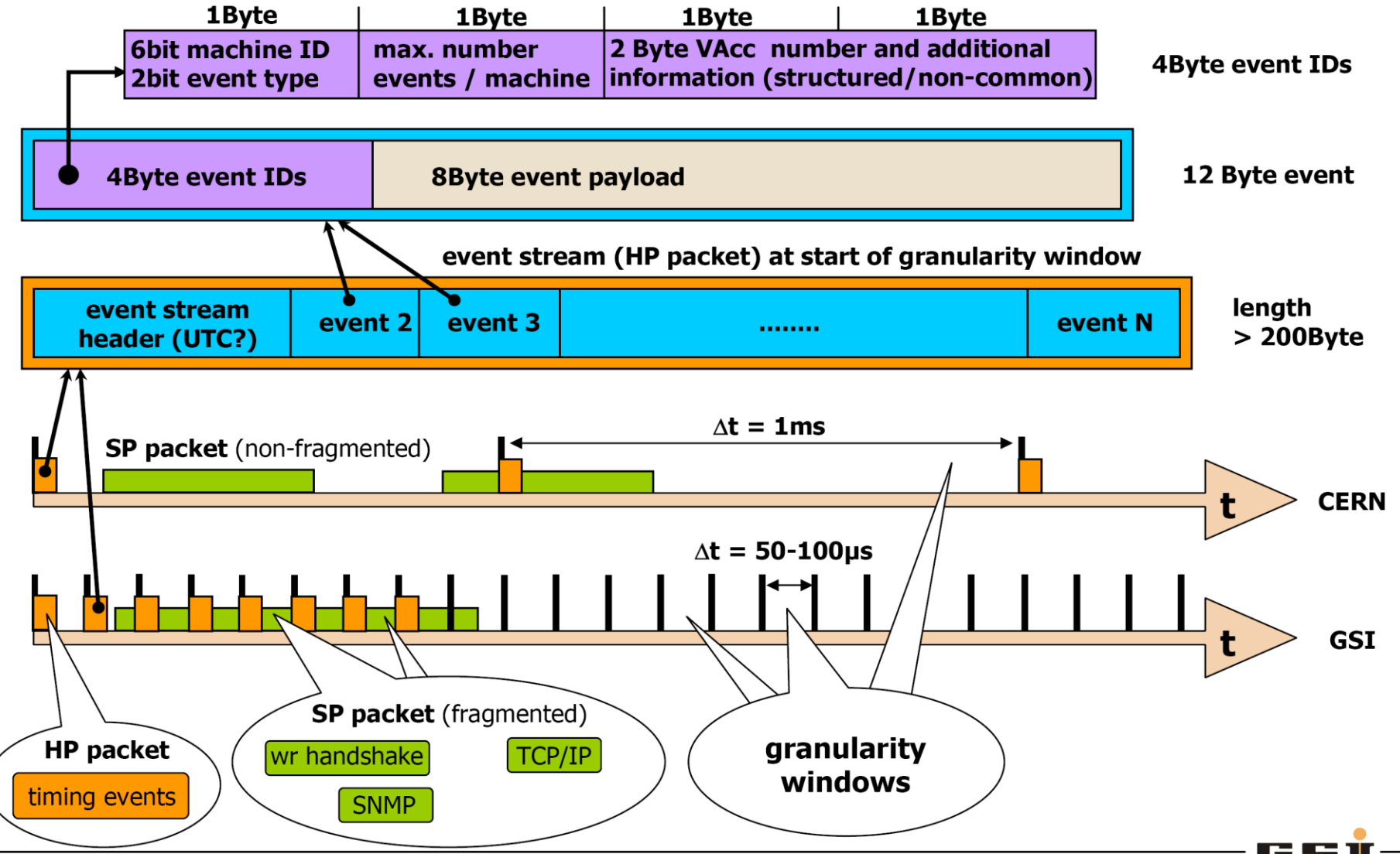
Fixed latency communication can be used to label local events

- Functionality of the White Rabbit switch



SP packets are fragmented in the switch if they collide with HP packets

timing event messages / content granularity windows



First prototype (D. Beck/Acc. Division)

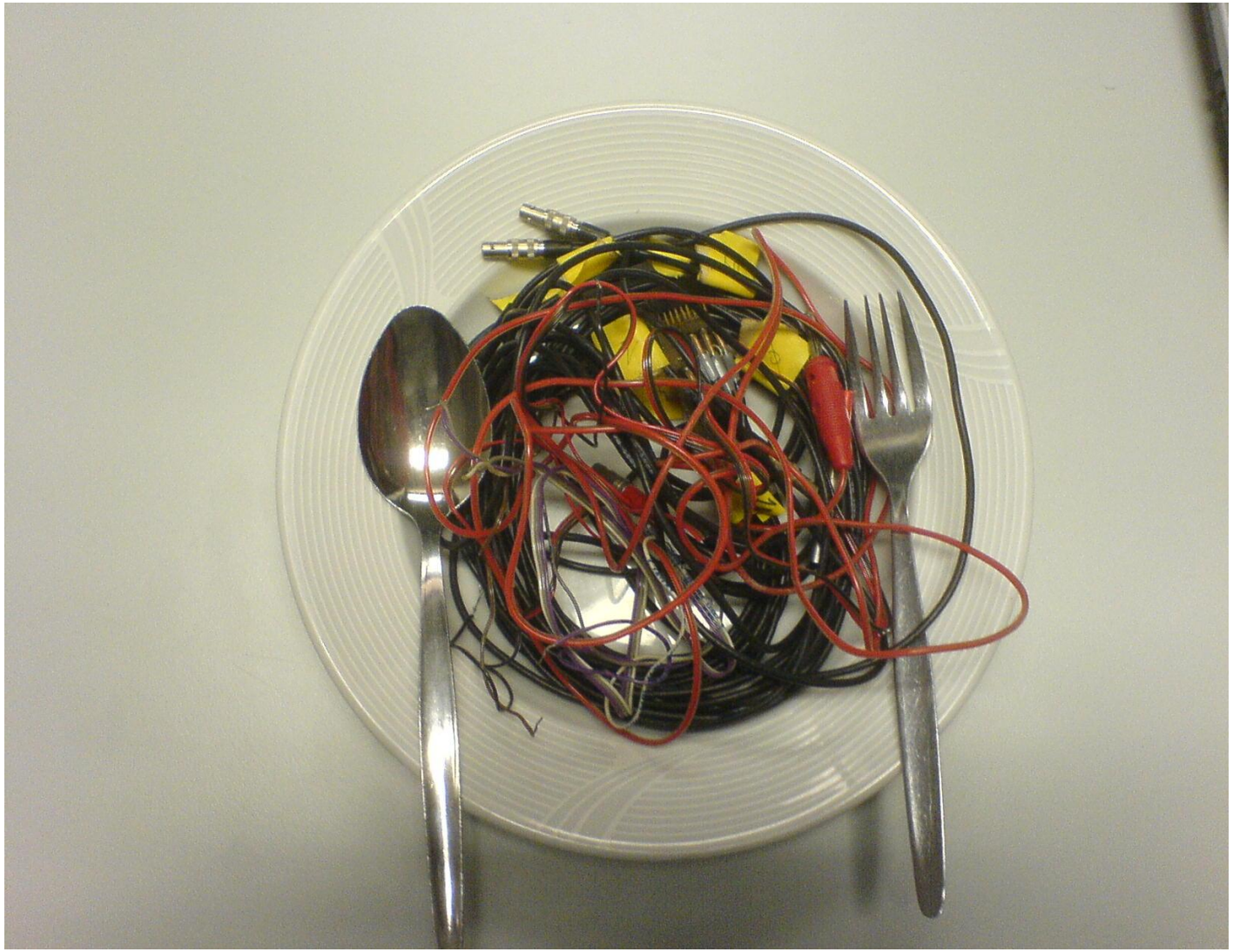
WR switch + 2 nodes running	09/2011
Fibre length compensation running	10/2011
User interface	ongoing

User implementation for time stamp injection needed
Piggy-back with lemo inputs exists
Code improvements to get user friendly operation !

Use case: Lightweight interfacing between systems

- data link / controls link
- time distribution system
- region of interest (aka trigger)

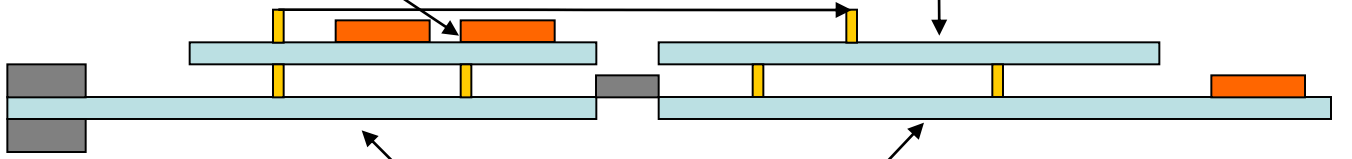
Getting rid of even more cables …
→ Integrated Electronics

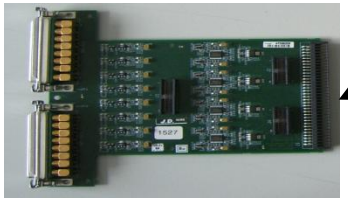


Fully Integrated System: (orig. for FOPI)
Precision timing, energy, trigger, monitor

TRIPLEX (new)

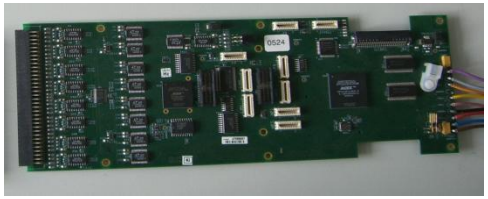
piggyback – QDC (mod.)



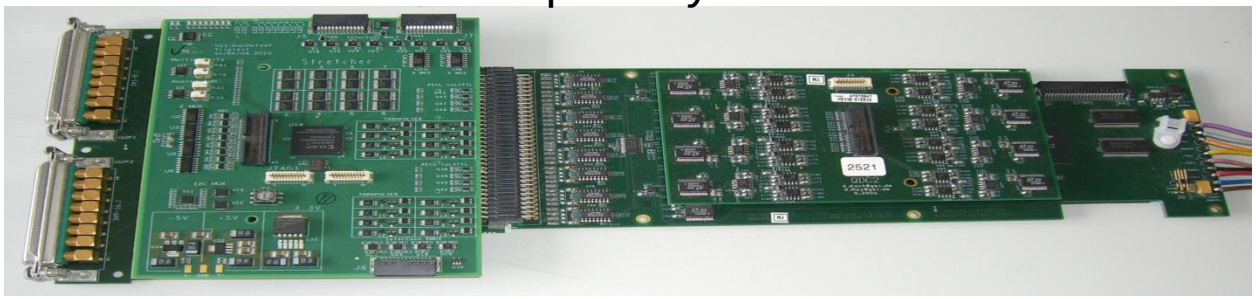


LAND FEE (new)

tacquila board
(mod., 17 ch.)

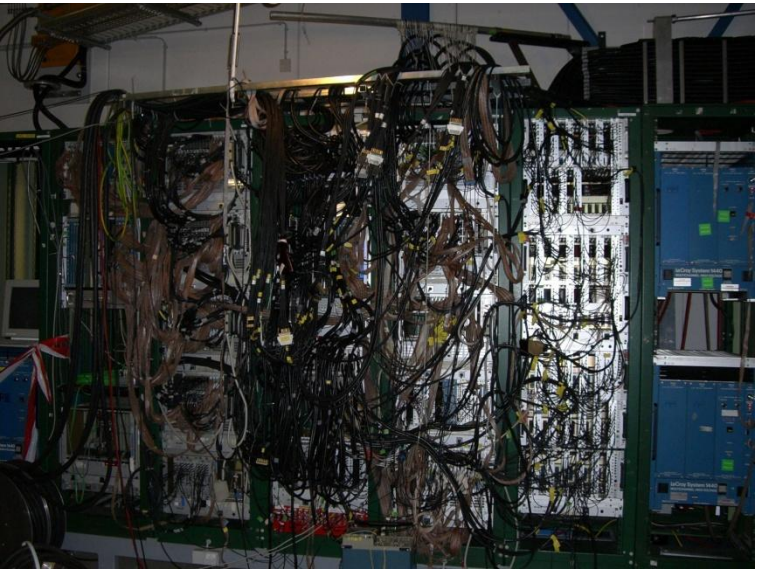


complete system



K. Koch
C. Caesar

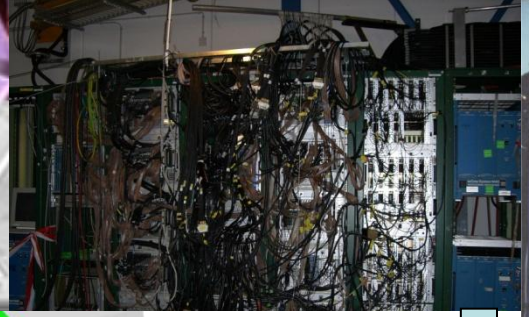
Replacing LAND electronics

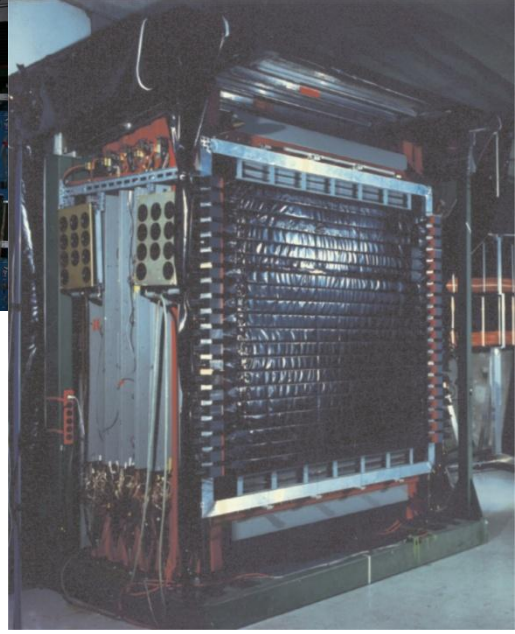


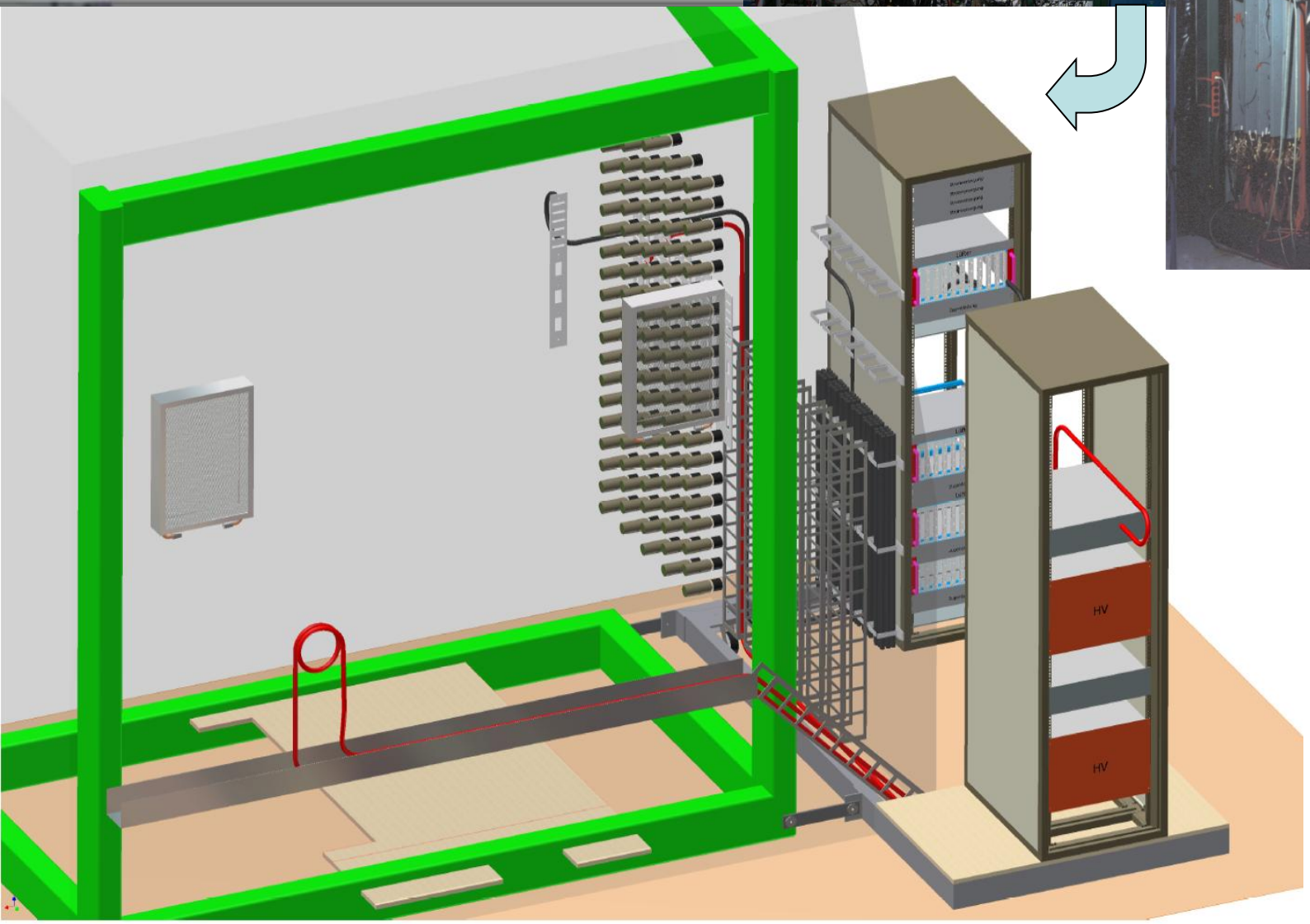
3x

160 channels

Eventually:
LAND gets mobile…







First exp.
05/2011

Power consumtion ~ 1W/ch. ➔ <1kW total

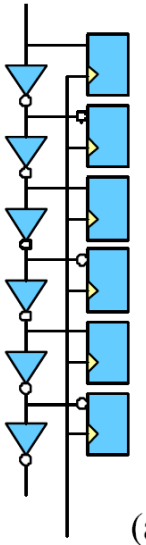
Avoid (Delay Line) Cabling !

Further steps: FPGA TDC; replacing TAC27 ASICS
➔ multihit/deadtime-free readout

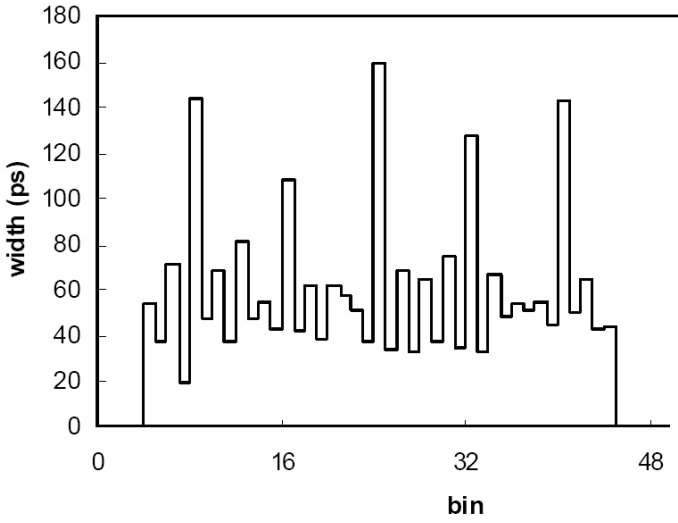
The 10-ps Wave Union TDC:
Improving FPGA TDC Resolution beyond Its Cell Delay

Jinyuan Wu and Zonghan Shi

IEEE Nuclear Science Symposium Conference Record, 2008. NSS '08.



(a)



GSI implementation
E. Bayer, M. Traxler, N. Kurz

TABLE I
PARAMETERS OF SEVERAL TDC SCHEMES

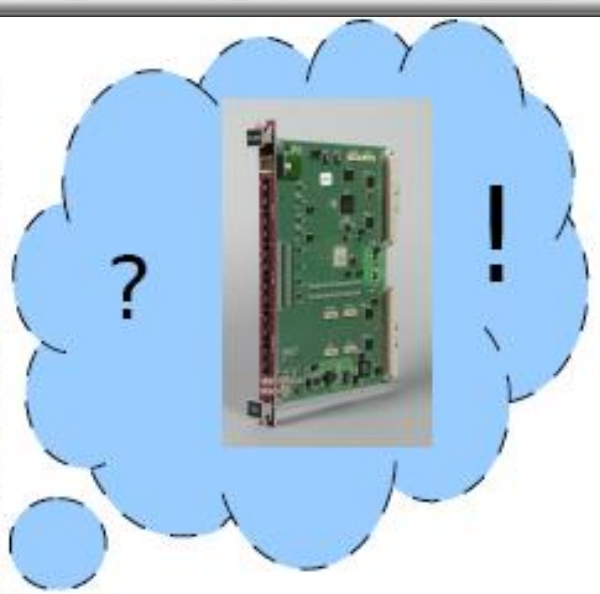
Device: EP2C8T144C6, Price: $28 (April 2008),
Operating Frequency: 400MHz, Total Logic Elements: 8256

	Max bin width	Av bin width	ΔT RMS error	Dead Time	Delay Chain Length	Logic Element Usage
Un-calibrated TDC	165ps	60ps	58ps	2.5ns	64	1621 (20%)
Plain TDC	165ps	60ps	40ps	2.5ns		
Wave Union TDC A	65ps	30ps	25ps	5ns		
Wave Union TDC B			10ps	45ns		6851 (83%) 8 CH

Altera Cyclone II device (EP2C8T144C6)

Flexible Trigger electronics

H.T. Johansson/CTH



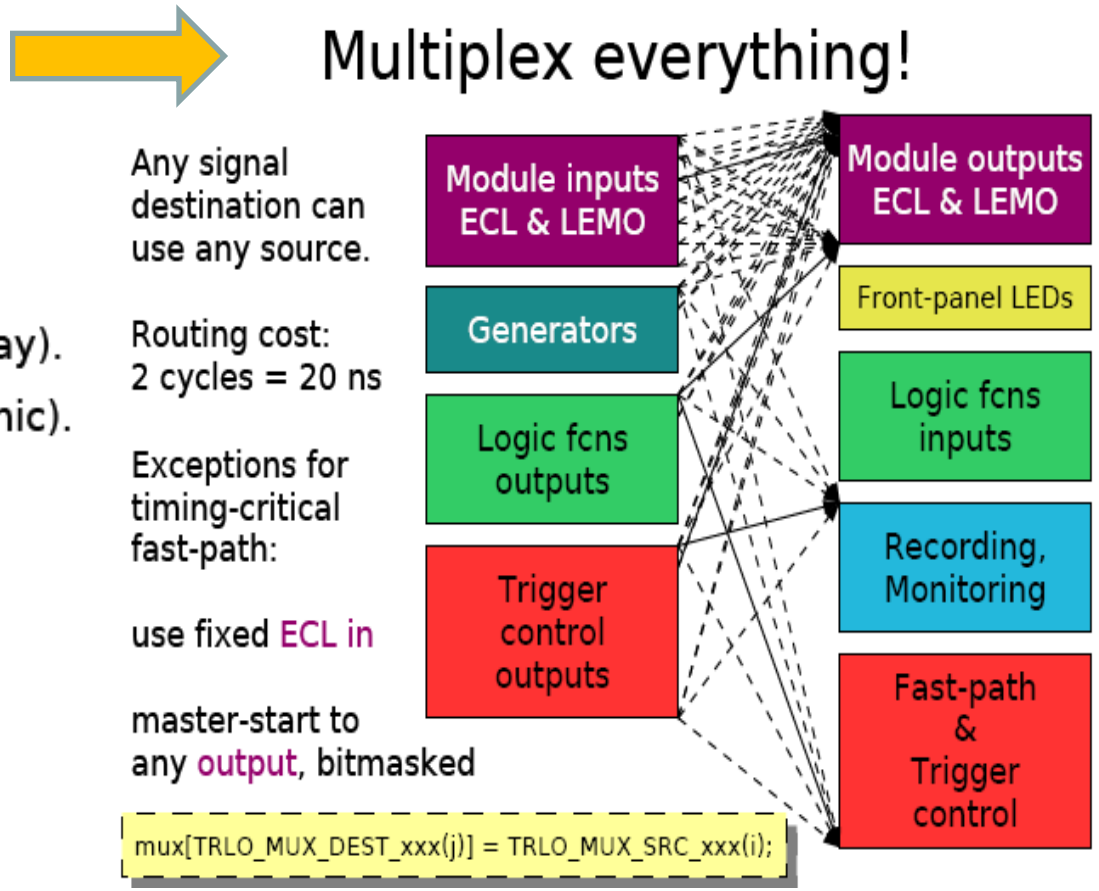
VULOM
(VME universal logic module)

by J. Hoffmann, GSI

Original TRLO firmware
by J. Frühauf, GSI

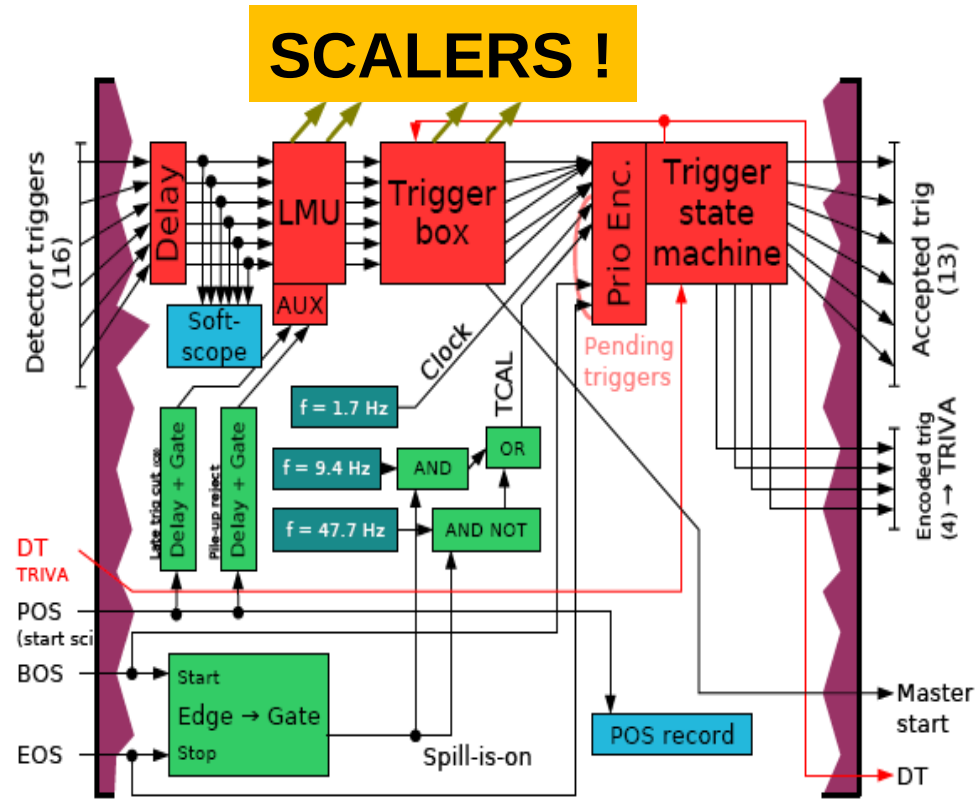
Building blocks configurable by user C-code

- Pulsers (programmable frequency).
- PRNG (pseudo-random sequence).
- LMU (not the same as in fast-path).
- Downscale.
- Delay and stretch (a.k.a. gate-and-delay).
- Edge-to-gate conversion (e.g. spill mimic).
- Fan-in (masked all-or).
- Coincidence.

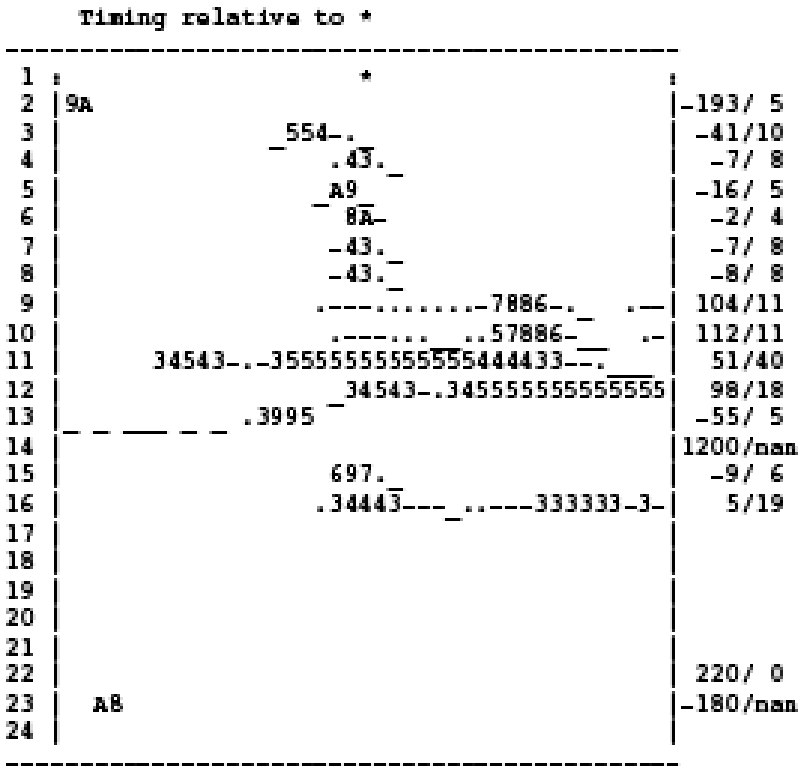


H.T. Johansson/CTH

Layout and features for hands-off operation

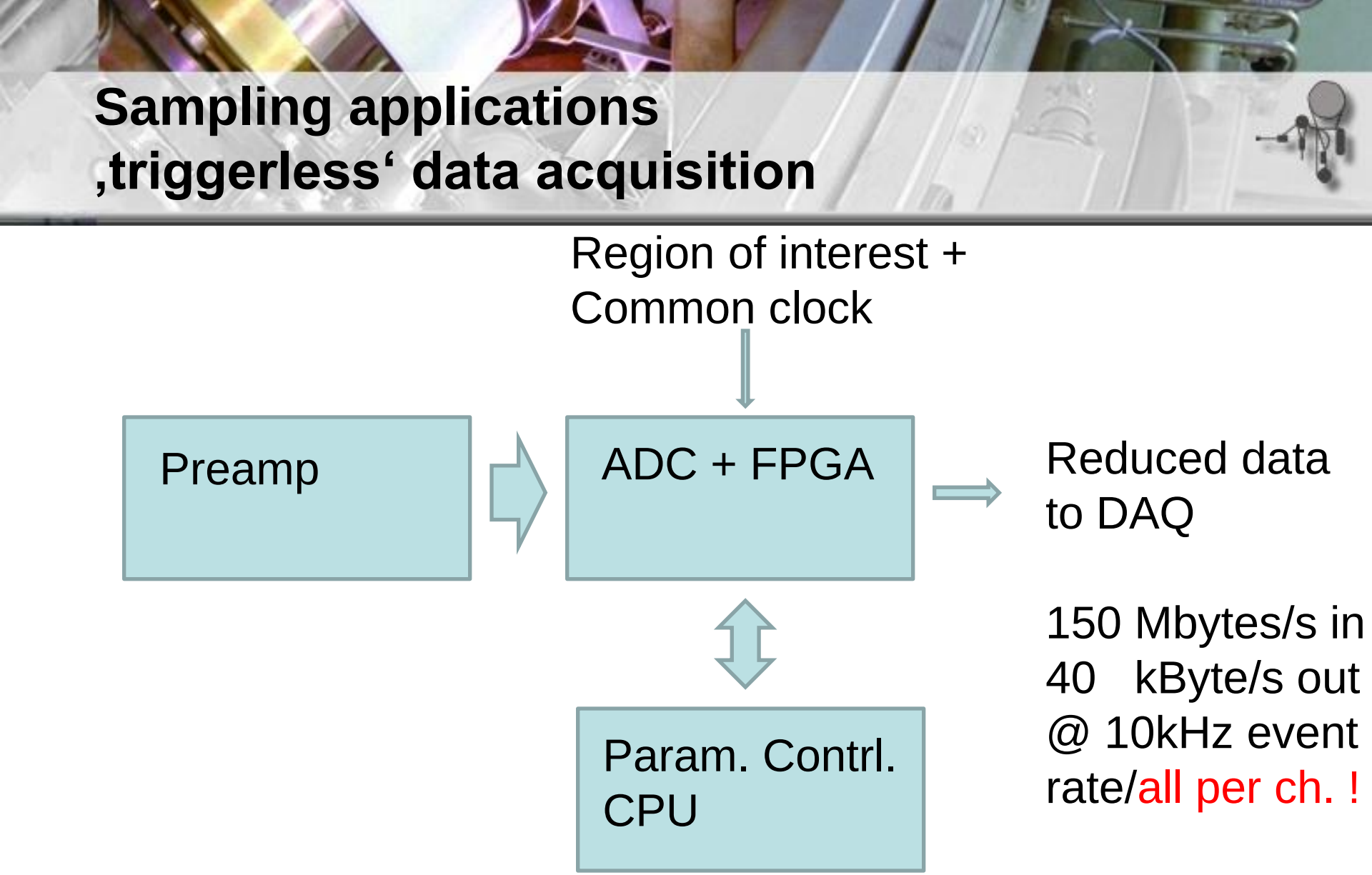


- Trigger alignment via built in diagnostics

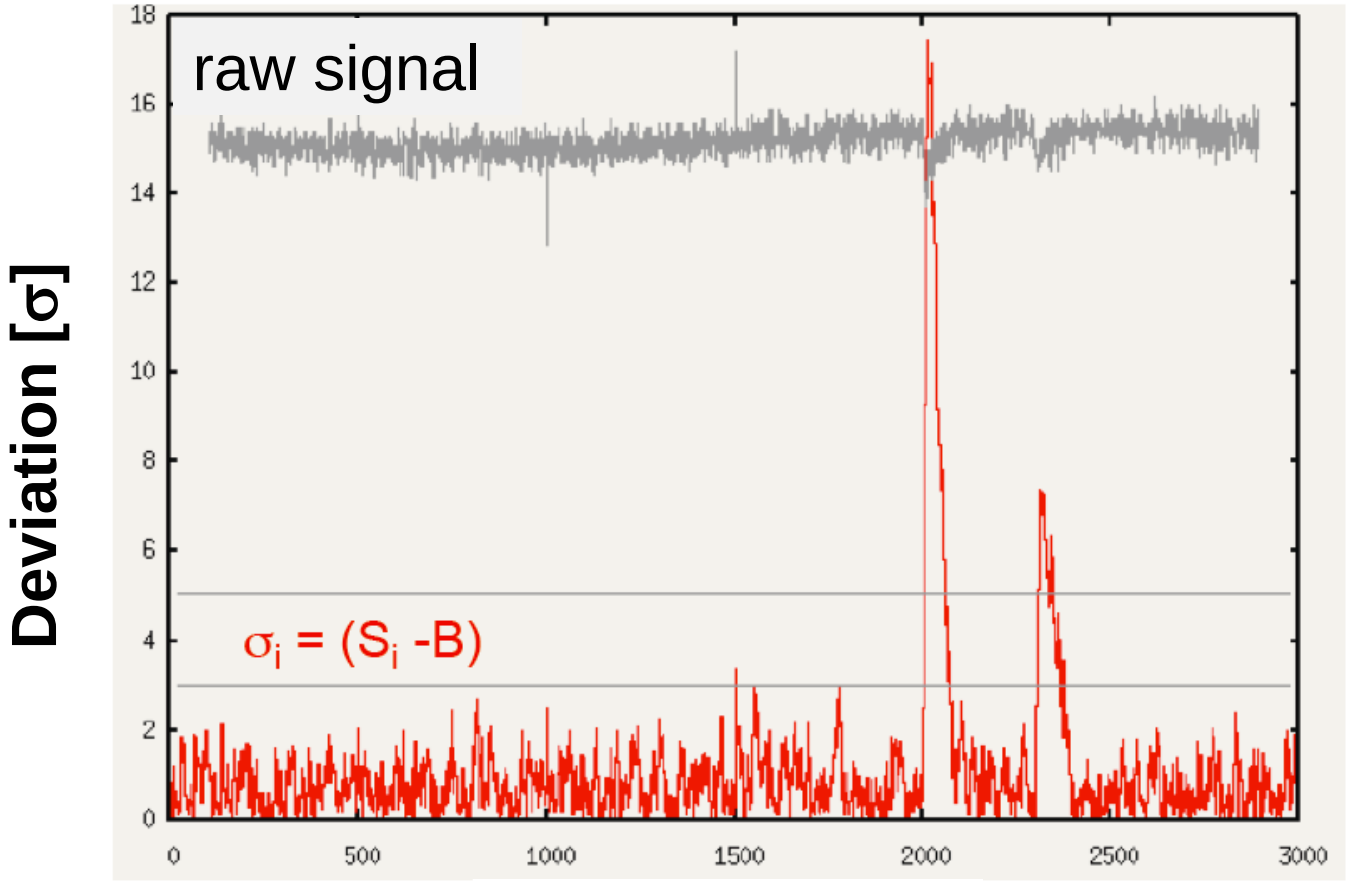


H.T. Johansson/CTH

Sampling applications
‚triggerless' data acquisition

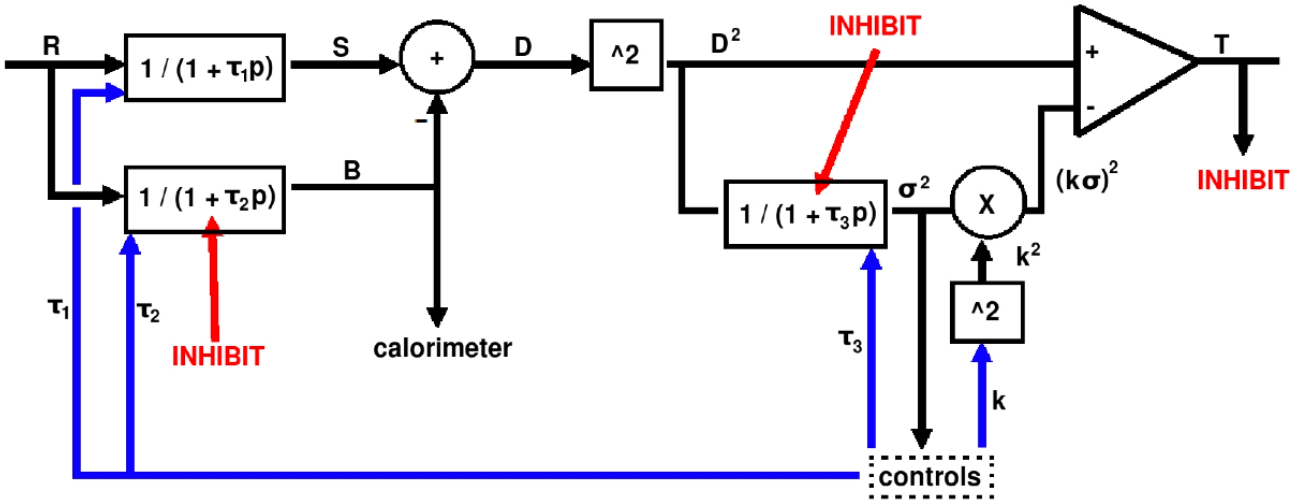


Feature extraction: Probabilistictrigger decision



Quelle: J.H. Jungmann, private communication

Baseline follower



3 fold low-pass filter

- **R**aw, **S**ignal, **B**aseline → **D**ifference → **D²** (Energy)
- **calorimeter,** σ^2 → histograming ➔ controls
- Inhibit → **Bimodal** filter

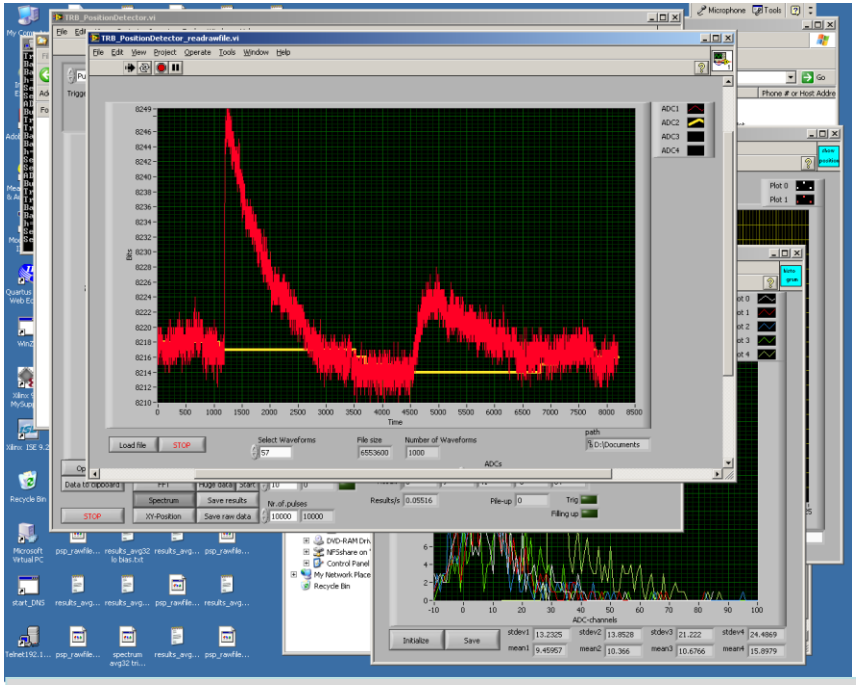
- controls ➔ filter parameters

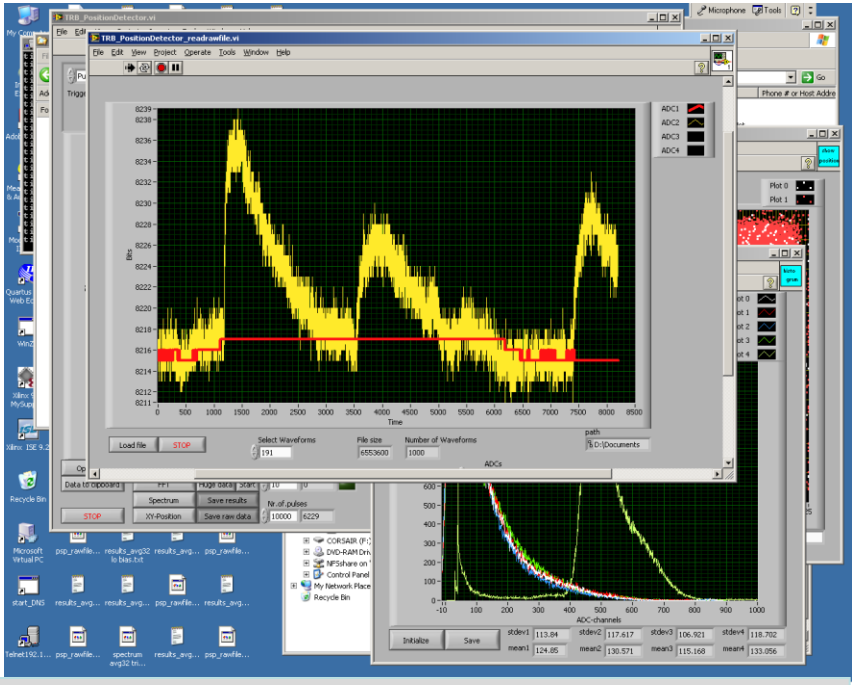
Heinrich Wörtche

Benefit: kσ Trigger i.e. most precise & "quantitative" treshold

Unwanted features can be removed ➔Spikes

Example Si PSP Baseline



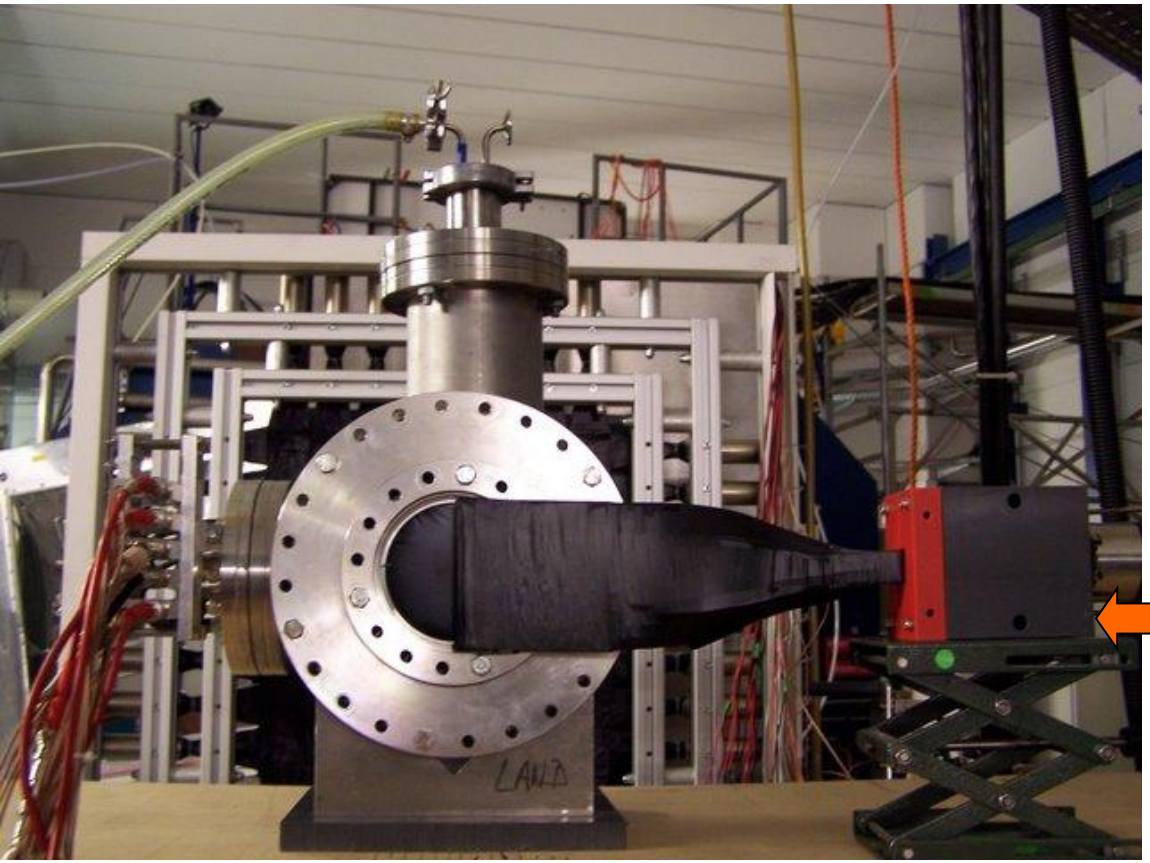


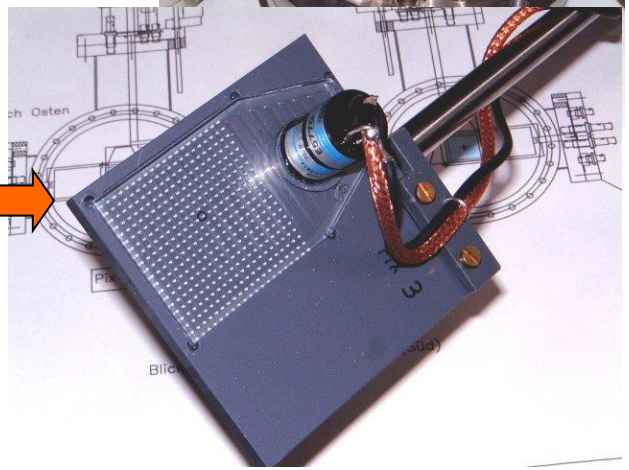
Baseline follower works (Bimodal Filter)

➔ Online monitoring of channels ➔ ‘slow’ CPU process

➔ Treatment of double hits via pile up correction !

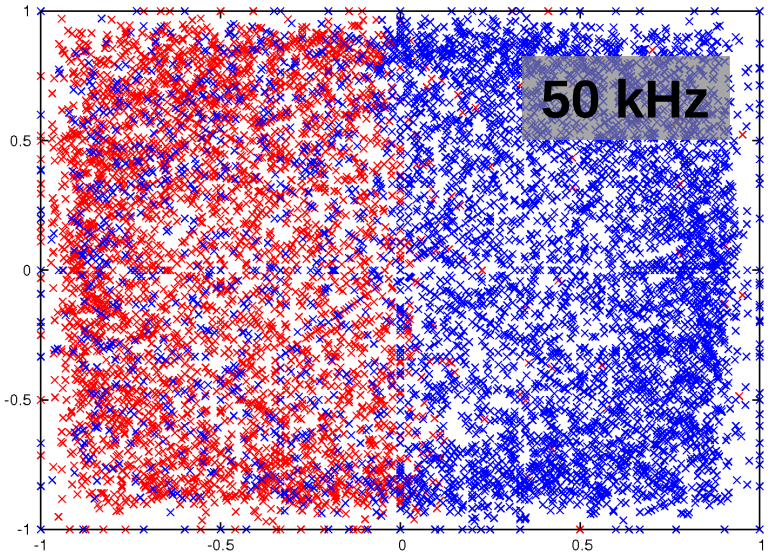
Tracking Si-Det (PSP)
^{12}C: 550-700 MeV/u ; 2-50 kEv/s

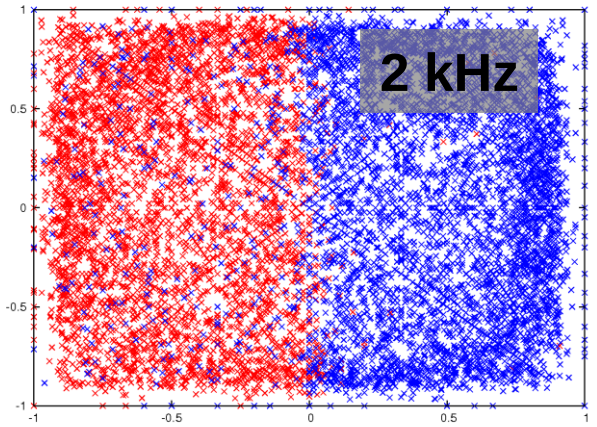


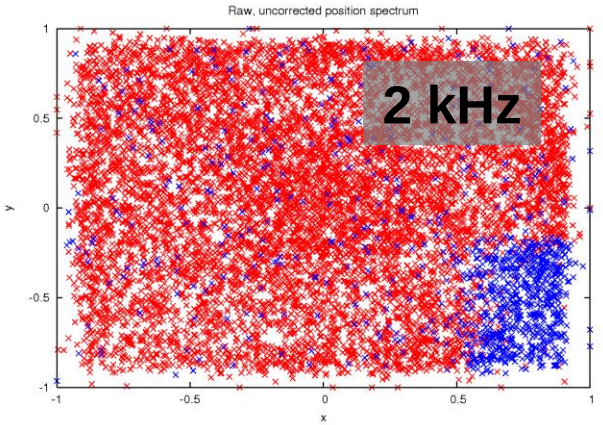


Pim Lubberdink

Online Position and amplitude reconstruction







minimal distortions

Computation in FPGA:

i. @ full rate (i.e. 50+ kHz, theoretical limit: ADC speed !)
ii. no correction yet

→ development of a “slow process”

Commercial VME module implementation vs. home made design

- Open Firmware (SIS3302, SIS3320)

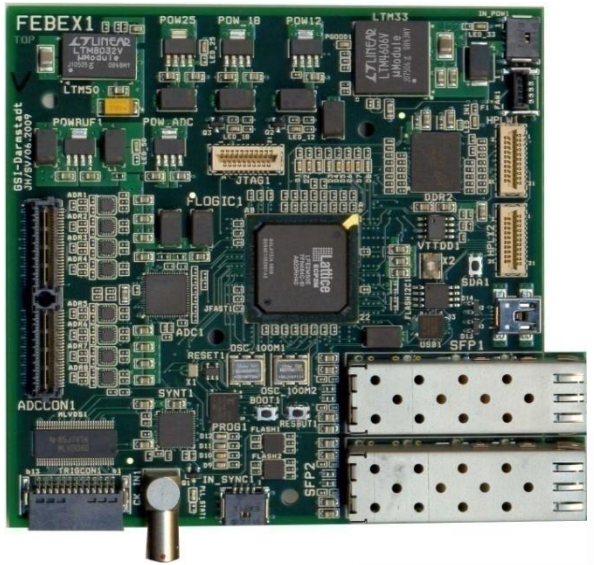
➔ Agreement 20090507
KVI/GSI/Struck (P.Schakel/V.Stoica/H.S.)

- MBS integration (N.Kurz)

➔ Agreement 20100927 (Struck/GSI)

- Package for distribution available

➔CAEN promised to look into options to open firmware



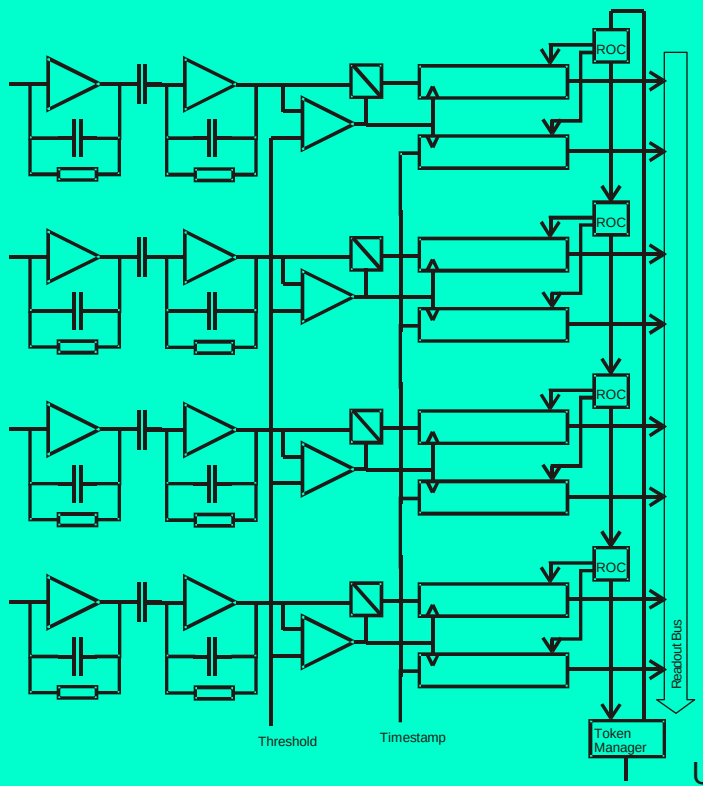
ASICS: e.g. Token Ring Scheme (NXYTER)

➔"deadtime free"/no trigger out

Ch. Schmidt (GSI)

ASIC Labor Heidelberg

Sparse & derandomized readout



- Periodic readout at 32MHz
- Token asynchronously passes from channel to channel in search of data
- Within one readout cycle token could pass through all channels
- If token encounters occupied channels, data readout is initiated.
- After readout the token passes to the next channel.

➔**32 MHz/128 Ch ≈ 250 kHz**

ENOB 10.4

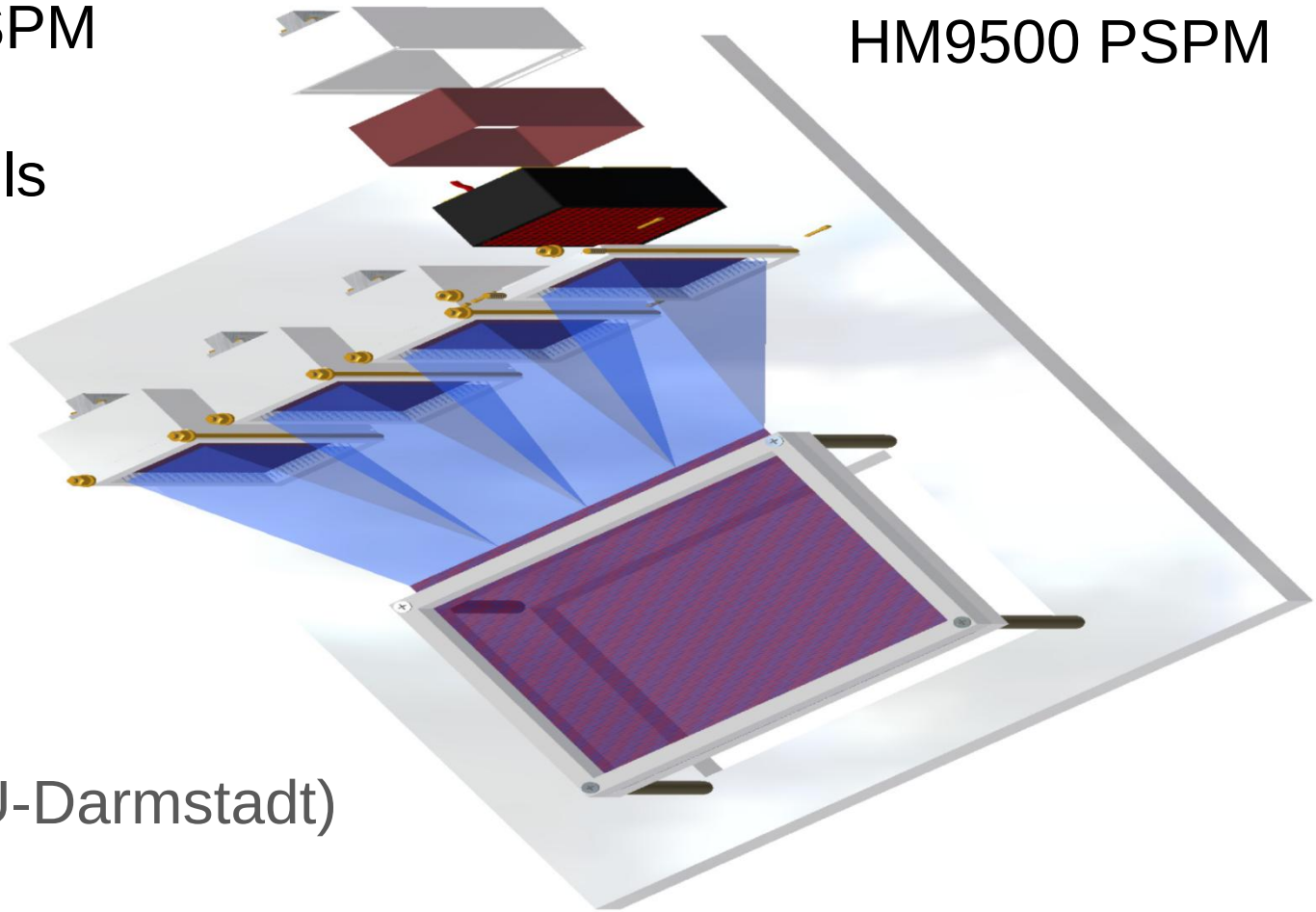
Ulrich Trunk

Physikalisches Institut der Universität Heidelberg

FAIR

Tracking using a 250µm fiber detector

256 Anodes/PSPM
1 fiber/Anode
➔1024 channels



HM9500 PSPM

Spaghetti
fiber detector

P. Schrock (TU-Darmstadt)
04/2012

The ASIC Problem: CBM RIČH adaption

Nuclear Instruments and Methods in Physics Research A 639 (2011) 307–310

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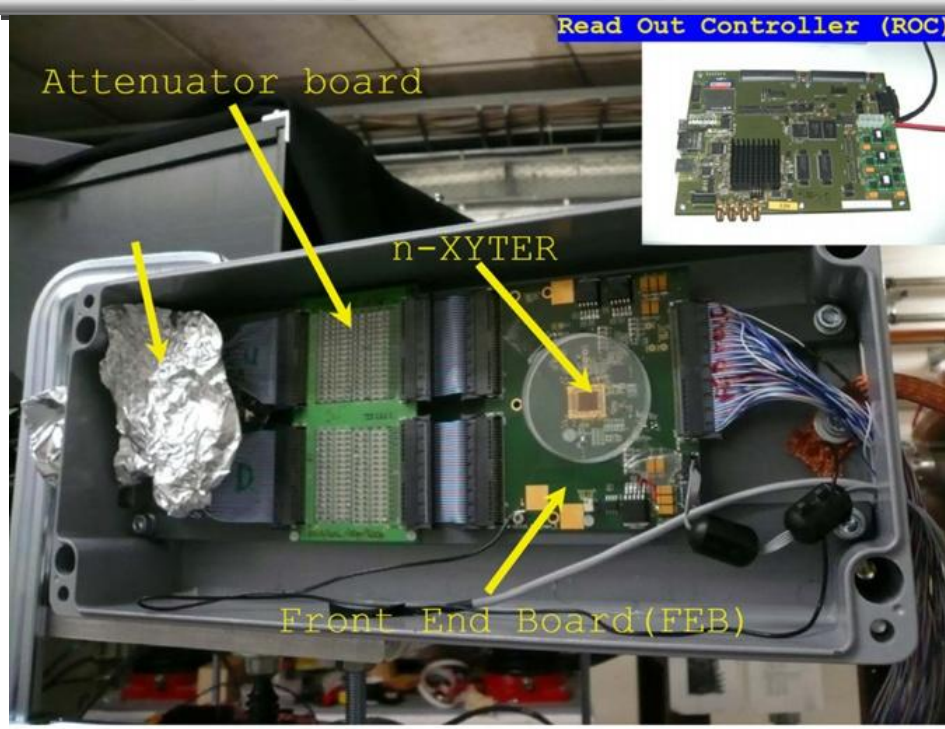
journal homepage: www.elsevier.com/locate/nima

Results from first beam tests for the development of a RICH detector for CBM

J. Eschke [a,*], C. Höhne [a,b]

[a] GSI Darmstadt, Germany
[b] University Gießen, Germany

NIM A 639 (2011) 307–310



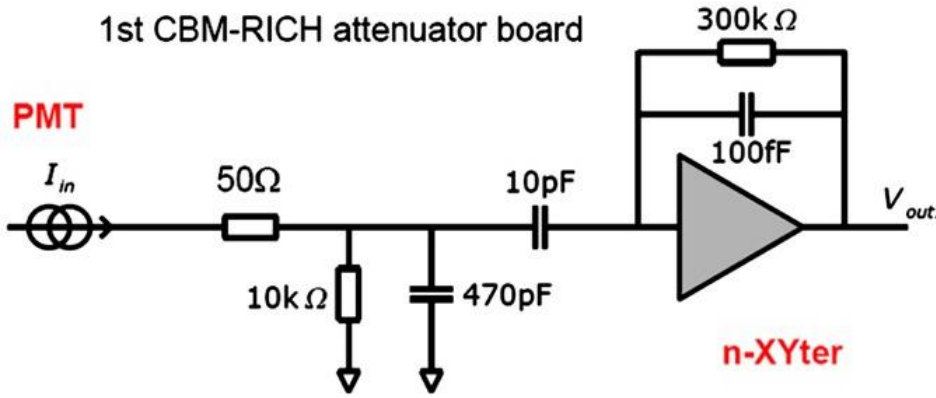


Fig. 3. Photograph of the FEE chain with Charge Attenuator Board, Front End Board with n-XYTER chip and Read Out Controller (ROC) used for the test beam datataking. The Charge Attenuator Board has been designed, simulated and tested for the attenuation of MAPMT signals with a divisionfactor 1 /47.

Providing building blocks and links …

- Integration of foreign/distributed systems
  - GET, AGATA, …, decay studies
- and ‚Triggerless' / dead time free sys.
- Online pulse shape processing (pile up treatment)
- Compact systems
  - Integration / tac-asic-free fpga-based multihit-tdc
- Time distribution and stamping
  - (BuTiS field test – precision time stamps)
  - White Rabbit prototypes