Quality control for the ATLAS ITk Pixel Flex PCB

G. Chiodini([1])(*), M.R. Coluccia([1]), S. Maggiore([1]), F. Martina([1])(**), A. Miccoli([1]), A. Pellegrino([1])([3]), S. Spagnolo([1])([2]) and C. Veri([1])

([1]) *INFN, Sezione di Lecce, Italy*
([2]) *Dip. di Matematica e Fisica "Ennio De Giorgi", Università del Salento - Lecce, Italy*
([3]) *Nikhef, SciencePark 105,1098 XG Amsterdam, the Netherlands*

Summary. — The ITk hybrid pixel detector features thousands of planar and 3D sensor modules adopting high-reliability flexible printed circuits (the *flexes*). Given the harsh environment of HL-LHC, rigorous quality control is essential. This work outlines the procedures standardised by the collaboration to validate the flexes, including the visual inspection, metrology, and electrical testing, ensuring defect detection prior to module assembly and thus maximizing production yield.

1. – Introduction

The ITk hybrid pixel detector [1] consists of multi-chip modules comprising approximately 10,000 planar sensors and 400 triplet 3D sensors, equipped with front-end chips developed within the RD53 collaboration.

To ensure optimal performance and long-term reliability in the harsh environment of the HL-LHC [2], rigorous quality certification is mandatory for all the embedded components [3][4]. In particular, this involves the test of the flexible printed circuit board (hereafter referred to as the *flex*), as it provides the electrical interconnection between the ASICs and the external systems.

The flexes are manufactured and populated adopting the highest reliability industrial standards. However, a standardised post-production quality control (QC) protocol allows to detect defects before the module assembly, maximizing the yield. This involves a detailed visual inspection, metrology cross-checks, and exhaustive electrical tests, which are carried out both prior to and following the soldering of the SMD components [5]. About 10% of the flexes will be certified at the INFN Section in Lecce.

(*) gabriele.chiodini@le.infn.it
(**) francesco.martina@le.infn.it

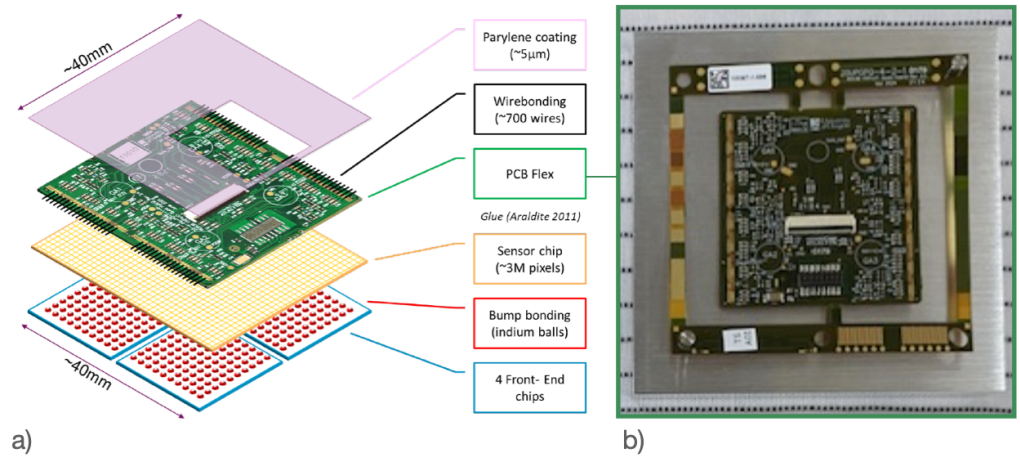

Fig. 1. – a) Assembly of an ATLAS ITk pixel module. b) Detail of the flex PCB.

2. – The Flexible PCB

Fig. 1a shows the components of a quad pixel module and how they are assembled. Four front-end ASICs are bump bonded to a planar pixel sensor and a flex circuit (in fig. 1b) is glued on top of the sensor back-plane. The front-end chips are wire-bonded to the flex by aluminum wires of 25 μm of diameter.

The key specifications that the flexes must meet are listed below:

- The dimensions and reference hole positions must comply with design tolerances.
- The wire-bonding pads must be free of scratches or lithographic over-etching.
- The power dissipated by the supply planes must be less than 10% of the overall module power consumption.
- The leakage current of the high voltage (HV) rails and relative bypass capacitor must be negligible.
- The transmission lines must have a characteristic impedance of 100 $\pm$ 10 Ω.

The bare flexes are produced by three different manufacturers: NCAB (SE), TECNOMEC (IT), and YAMASCHITA (JPN) on a panel including four units. The panels are subjected to a preliminary inspection. Those passing the control successfully are later populated by one the companies: NORBIT (NOR), G-O (UK), and HR (JPN).

After the soldering, the flexes are separated from the panels by cutting the supporting tabs (a total of 12 incisions). This is performed at the flex QC sites, under microscope supervision, by adopting a surgical scalpel with a round blade, which is often replaced for an optimal result. A disposable square frame is kept on the single flex PCB (visible in fig. 1b) to provide mechanical support in the successive processes. It is later removed by cutting its tabs right before the module gluing.

3. – Visual Inspection

The flexes are carefully inspected under a microscope both before and after component population. High-resolution images of the SMD layer are acquired and stored in a database. In contrast, data from the back layer are recorded only if severe degradation is reported, as this layer is less frequently affected by issues. At INFN Lecce, an automated acquisition procedure is used to perform an XY scan, capturing a total of 26 images per flex. These images are then stitched together using a set of scripts to produce a single wide-field image (approximately 9 MB in size).

Afterward, an evaluation form is filled with scores ranging from 1 to 3 (good, usable, to be rejected), which are related to each of the desired features. In particular, the main defects that need to be identified are listed here:

- Over-etched wire-bonding pads
- Coating scratches
- Solder-Mask defects
- Non-Conformal fiducial marks
- Silkscreen resolution
- Component misalignment
- Solder spill
- Solder flux spill
- Stain
- Watermarks

So far, visual inspection is supervised by an operator and takes approximately 10 minutes per flex. AI-driven software for defect identification has been explored by the collaboration. However, these solutions are not yet sufficiently mature to meet the stringent requirements of the application. This is not surprising due to the vast repertoire of possible issues and the variability in imaging conditions, such as microscope performance or illumination, which can significantly affect their appearance.

Finally, this activity has contributed to optimise the technological process and to improve soldering quality, thanks to active report exchanges with manufacturers and multiple iterations of prototype productions.

4. – Low and High Voltage Tests

In order to minimise the material budget for cabling and related power loss, a serial supply chain is adopted throughout the ITk detectors. In such a way, multiple pixel modules can be powered in series by a constant current source, while a parallel structure is adopted only for the high-voltage biasing. Thus, it is essential to ensure that powering rails present a limited voltage drop and the high-voltage rail and its bypassing capacitors are not affected by excessive leakage. Finally, the characteristics of the embedded temperature sensor are monitored, as it represents a critical component for local monitoring and the prevention of thermal runaway.

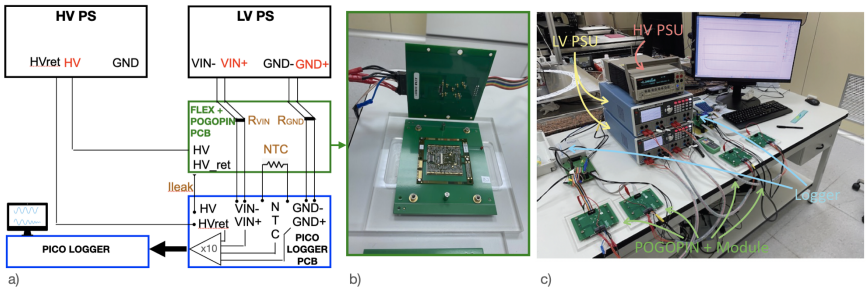

Fig. 2. – a) Architecture of the HV-LV test-bench. b) A flex placed on the ground plane PCB, just before applying the pogo pin card. c) The setup allowing concurrent testing of four modules.

In order to perform the electrical validation, test points are available on the flexes. They are contacted by a set of cards designed by the collaboration, a pogo pin card, signal conditioning and readout electronics, based on the PicoLog commercial device.

During the electrical QC tests, named HV-LV tests, the flex is sandwiched between a ground plane and the pogo pin card. The pogo pin card is then plugged in the flex power connector (see Fig. 2b) and its pins are contacted with the flex test pads. This operation is mechanically guided by precision pillars placed on the ground plane and dowel holes on the flex and pogo pin card. An interfacing circuit amplifies and measures voltages and currents from the pogo pin card, which are then acquired by the PicoLog device and stored on a computer.

The architecture of the test-bench is reported in Fig. 2a and it has been recently upgraded to support the concurrent analysis of 4 flexes (see Fig. 2c). The following quantities are registered for each module and averaged in 20 minutes, to ensure the stability of results.

1. Electrical resistance of the power supply rails (VCC and GND).
2. Leakage current of the high-voltage rail and related bypass capacitor at -975 V.
3. Electrical resistance of the NTC temperature sensor.

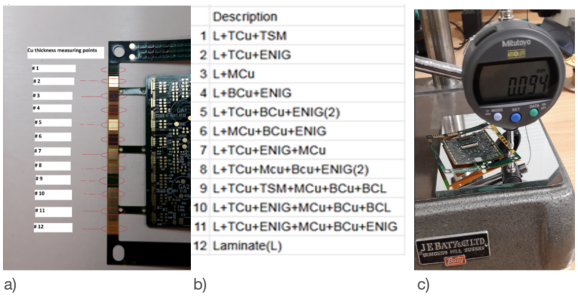

Fig. 3. – a) Stack-up testing layout. b) Flex stack-up. c) Caliper-based measurement setup.

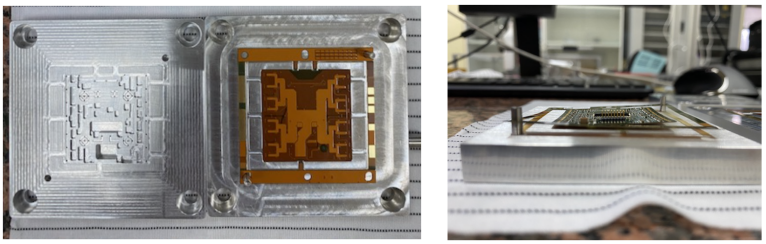

Fig. 4. – a) Validation jig. b) Check of the dowel hole positions.

5. – Metrology

Different mechanical metrology measurements are carried out on the bare and populated flexes. We report here only the most relevant ones.

The stack-up validation is performed by using a precision caliper (see Fig. 3c) which measures the PCB thickness at different regions. The evaluation of the single layer thickness is achieved by subtraction, exploiting specific layout features (Fig. 3a) which are etched on the flex frame for the goals. In Fig. 3b the design flex TECNOMEC stack-up is reported. The 10% of the flexes of each batch is checked with this procedure before the component population.

Another relevant check consists in Go-No-Go jigs milled into the aluminum, which reflects the 3D profile of the full PCB and soldered components. This is specifically aimed to verify the correct position and height of components (Fig. 4a) and to validate the flex dowel holes (see Fig. 4b).

6. – Conclusions

The quality certification of both bare and populated flexes has proven to be essential for maximising the production yield of the ATLAS ITk pixel modules and preventing schedule delays. Thanks to validated and standardised procedures, complete certification of a flex can be performed in approximately 35 minutes at the INFN facility in Lecce, with an average throughput of 40 flexes analyzed per week. To date, the collaboration has produced 318 pre-production flexes for the pixel inner system, along with 795 pre-production and 970 production flexes for the outer system.

REFERENCES

[1] *Technical Design Report for the ATLAS Inner Tracker Pixel Detector.* CERN-LHCC-2017-021, ATLAS-TDR-030.
[2] *The High Luminosity LHC Project.* Available at https://hilumilhc.web.cern.ch/ (2022/09/15).
[3] *Technical Specification for ITk Pixel Modules.* (AT2-IP-ES-0009).
[4] *Production Flow and QA/QC of Module Flex PCB.* (AT2-IP-QA-014).
[5] *QA/QC procedures for the ITk Pixel Flex PCB.* (AT2-IP-AP-0009).