Cleopatra: a recycling integrator ASIC for the readout of hydrogenated amorphous silicon detectors in radiotherapy dosimetry

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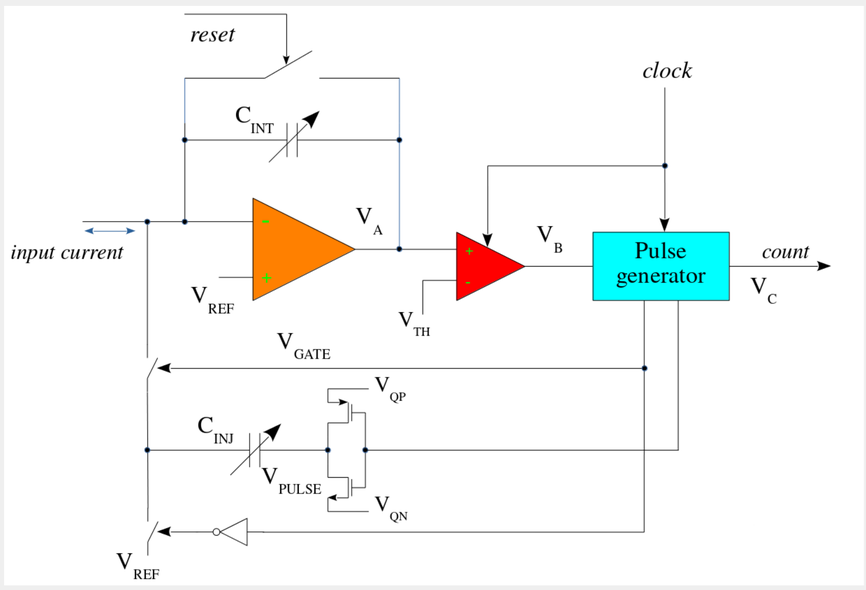
Abstract

The Cleopatra ASIC is a 12-channel prototype designed within the HASPIDE project for the readout of hydrogenated amorphous silicon sensors in real-time dosimetry for radiation diagnostic and therapy. In particular, IORT and FLASH radiotherapy use high particle fluxes and require a high dynamic input range. The analog front-end is a current-to-frequency converter based on the recycling integrator principle, to cover a dynamic range of four orders of magnitude with high linearity. Three different input amplifier configurations have been implemented to check the trade-off between detector capacitance and maximum output frequency. Cleopatra has been designed in CMOS 28 nm technology and successfully tested in the laboratory. The prototype is now being tested under radiation with an array of sensors.
A new version of the ASIC is being designed, featuring 32 input channels.

Readout architecture

- Each analog channel includes a Charge Sensitive Amplifier, a comparator with a programmable threshold, a charge injection circuit and a test-pulse control logic
- The input current is integrated over C_{INT}, thus obtaining a voltage ramp at the amplifier output V_A
- When the ramp crosses a threshold, a fixed amount of charge Q_{INJ}, generated by sending the voltage pulse $V_{QP} - V_{QN}$ to the capacitor C_{INJ}, is subtracted from the amplifier input
- The frequency of the output periodic digital signal is proportional to its input current:

$$f_{out} = \frac{I_{input}}{Q_{INJ}} = \frac{I_{input}}{C_{INJ}(V_{QP} - V_{QN})}$$

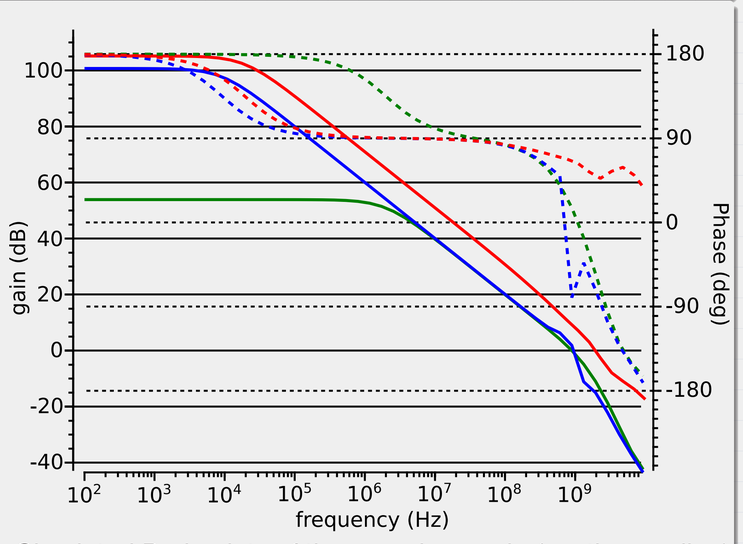


Schematic diagram of the channel readout

Input amplifier

Three different operational amplifiers have been designed:

- a two-stage cascoded amplifier with feed-forward compensation (FF)
- a telescopic current mirror configuration (TS)
- a current mirror with gain boost (GB)



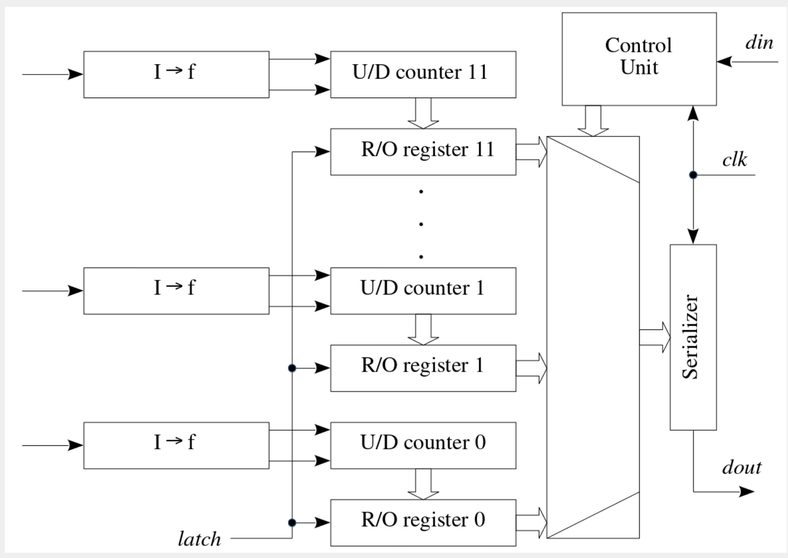
Simulated Bode plots of the open-loop gain (continuous line) and phase (dashed line) of the three amplifier versions in typical case: FF (red), TS (green), and GB (blue).

Digital interface

The readout can operate with either positive or negative input signals. The signal polarity can be selected through a static polarity selection bit.

Each current-to-frequency converter is coupled to a 24-bit up/down counter, which in turn is connected to a 24-bit register. An externally provided load signal, common to all registers, stores the value of the counters, thus providing a snapshot of the measured charge by all channels at a given time.

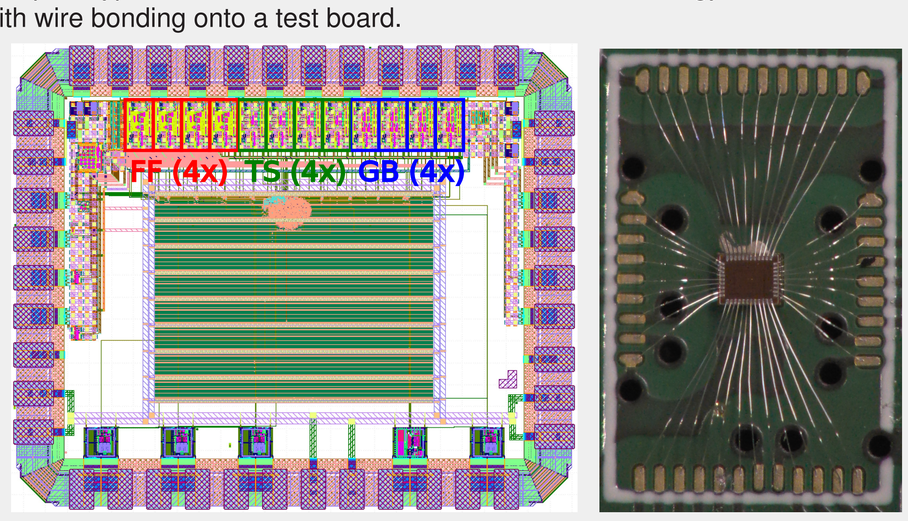
The output data is sent through a serializer connected to an SLVS driver.



Digital interface

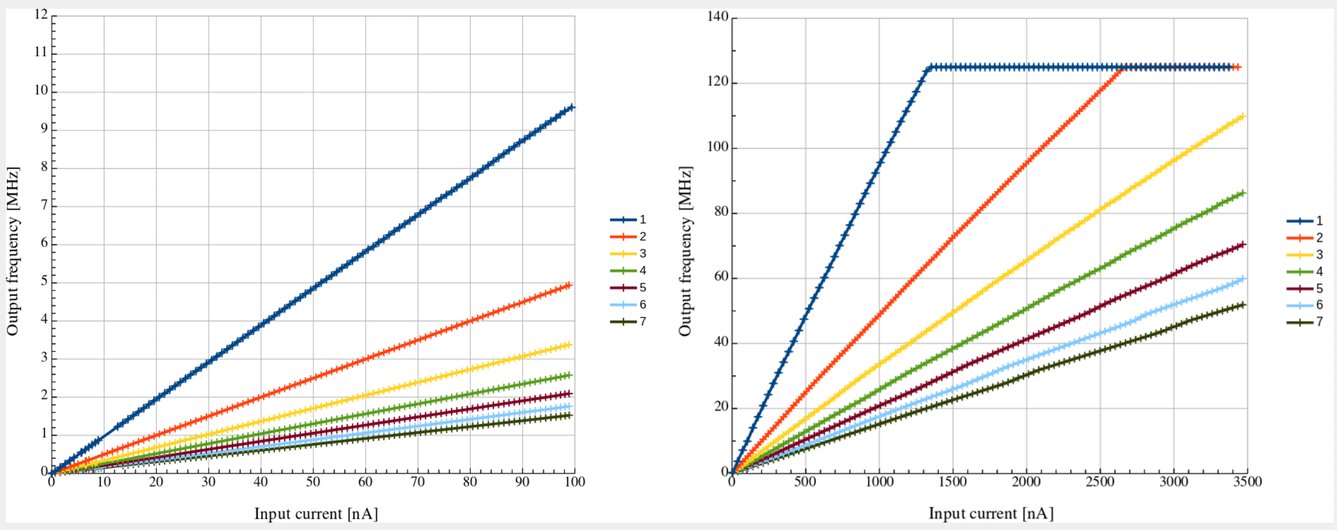
Cleopatra prototype

The prototype has been fabricated in 28 nm CMOS technology and assembled with wire bonding onto a test board.



Layout and photograph of the Cleopatra chip

Test results



Output frequency vs. input current, for different values of the injection capacitance

The ASIC has been tested standalone by provinding a precise voltage with a Source Measurement Unit (SMU) and measuring the current with the same instrument.

A 10 MΩ resistor mounted on the test PCB in series to the input provides a high impedance source. The digital interface is controlled by an FPGA-based evaluation board connected to a computer via ethernet interface. Due to limitations of the FPGA test board, the test has been performed only up to a clock frequency of 500 MHz.

- Left: the response of a typical channel to an input current ranging between 1 nA and 100 nA for 7 injection capacitance configurations, corresponding to capacitors ranging from 20 fF to 140 fF. The non-linearity is below ±0.5% for currents above a few nanoamperes
- Right: the response of a typical channel to an input current ranging up to a 3.5 A. A non-linearity below ±2% has been measured in this range. As shown, the circuit saturates at 125 MHz, i.e. the frequency at which the maximum input current occurs

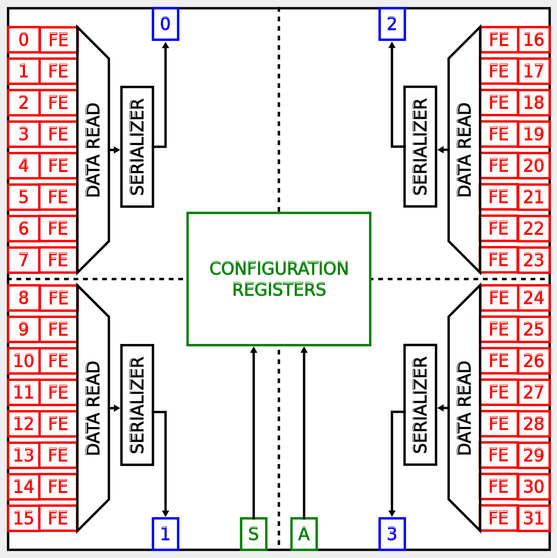
Floorplan of the final version

The final version is being designed. Its main features are:

- 32 input channels on the left and right sides (in red)
- 4 serial data outputs, one for each quadrant (in blue)
- a serial input S for chip selection, configuration and commands (in green)
- a static chip address A to select the single chip in a board containing multiple chips (in green)

The digital part of the chip is being designed using Verilog behavioural description and Cadence Genus compiler.
As for the first prototype, the supply voltages are: 0.9 V for chip core and 1.5 V for the pads.
The chip area is 2 mm × 2.25 mm.

The tape-out of the final ASIC is forecast in April 2025.



Floorplan of the ASIC final version

Conclusion

The first version of the Cleopatra test chip has been fabricated in 28 nm CMOS, and successfully tested in the laboratory.
The final version is being designed.
Meanwhile, the first prototype is being assembled with sensors, for testing under a radiation beam.

References

- G. Mazza *et al.*, "A front-end circuit in 28 nm CMOS for hydrogenated amorphous silicon detectors in clinical dosimetry," in *Int. Conf. on Modern Circuits and Systems Technologies (MOCAST)*, Sofia, Bulgaria, 2024.
- G. Mazza *et al.*, "Cleopatra: a 12-channel recycling integrator ASIC for the readout of hydrogenated amorphous silicon detectors in radiotherapy dosimetry," JINST **20** (2025), C01034.

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