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TID mechanisms on nanoscale CMOS technologies

In High-Energy physics applications, electronic devices will experience ever-increasing radiation doses. The forthcoming increase of the luminosity of the Large Hadron Collider (LHC) at CERN will require electronics to be able to withstand ultrahigh total ionizing dose (TID) levels up to 1 Grad(SiO2). For this reason, research on the TID response of modern technologies at ultrahigh doses has been receiving increasing attention in recent years in the HEP community. This paper reviews recent studies on TID effects on two modern commercial technologies: 28nm planar CMOS and 16nm FinFET technology. DC measurements provide insights into degradation mechanisms affecting oxide structures, including gate oxide, shallow trench isolation (STI), and spacers. The influence of transistor geometry and bias conditions during irradiation is analyzed, with emphasis on the mechanisms driving parameter degradation. Similarities and differences between the two technologies are highlighted.

Keywords: radiation effects; Total Ionizing Dose (TID); Metal–oxide semiconductor (MOS) transistors; FinFET

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