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High speed serial links and radiation tolerant serdes devices for TTC distribution and DAQ in future HEP experiments

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The increase of the luminosity in the upgrade of the Large Hadron Collider at CERN required the complete redesign of the Front-End electronics in most of the detectors of all the experiments. The first challenge was the increase of the data rates due to higher trigger rate and to the need of data from the Silicon Trackers for the generation of the level 1 trigger. The second challenge was the increase of the Total Ionizing Dose (up to 1Grad in the inner layers of the Silicon Trackers). New protocols for the distribution of the Timing, Trigger and Control (TTC) signals and for the data readout have been developed and implemented in radiation-tolerant IP-cores embedded in Front-End circuits. The technology scaling and the introduction of new design methodologies was the key for the success in the production of IP-cores that could fit the tight requirements w.r.t. performances and radiation tolerance. INFN designers have been deeply involved in these developments in the framework of different R&D projects supported by the Gr.5. A short survey of these projects is presented with a more detailed focus on the most recent results.

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