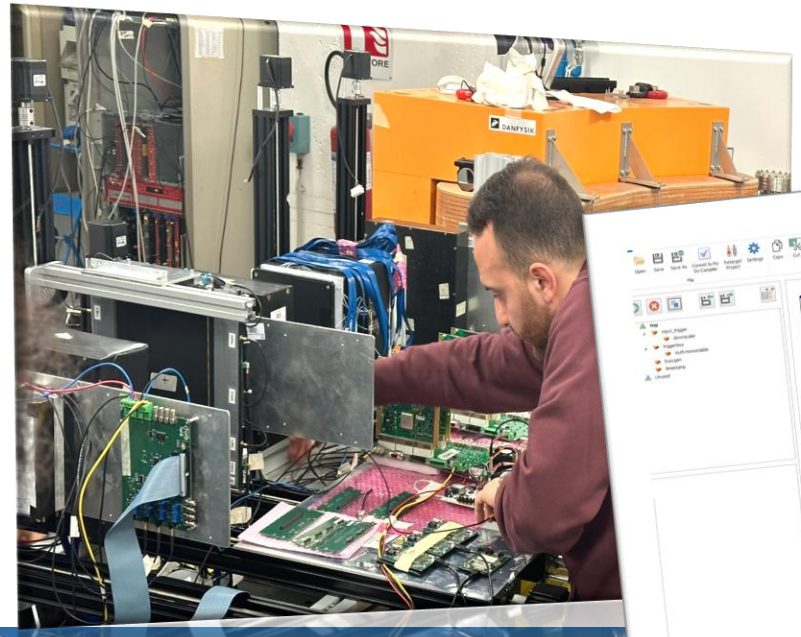
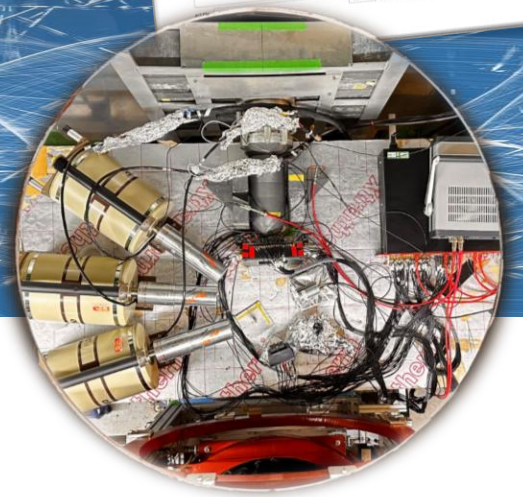
SCI-COMPILER

Sci-Compiler: A Flexible Tool for Designing Complex Multi-Channel Readout Systems



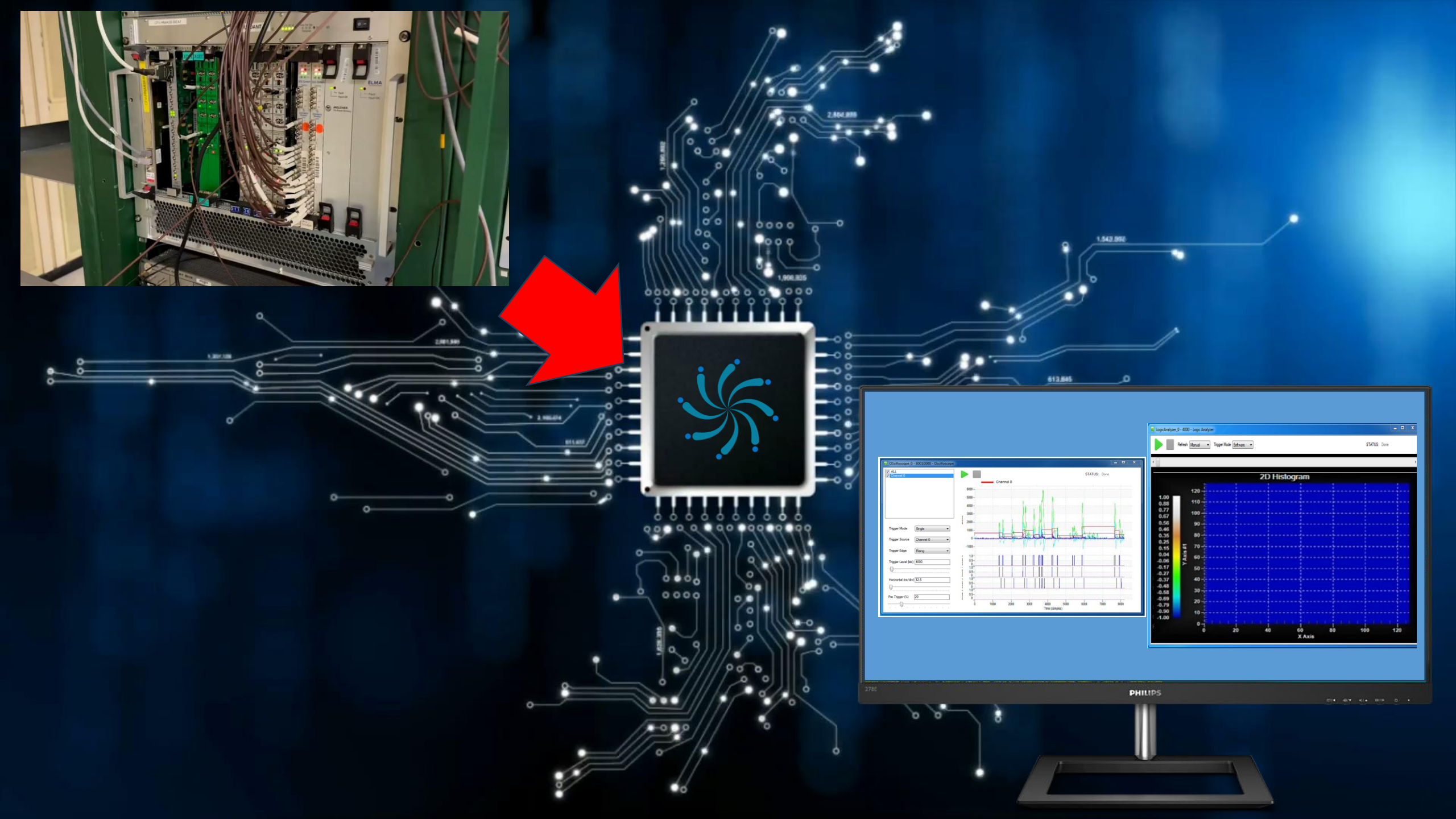


A. Abba
F. Caponio
S. Carsi
D. Bianchi
V. Arosio
M. Petruzzo
C. Tintori
L. Colombini
M. Bianchini
V. Bottiglieri
Y. Venturini
A. Cusimano

designed for CAEN digital acquisition systems

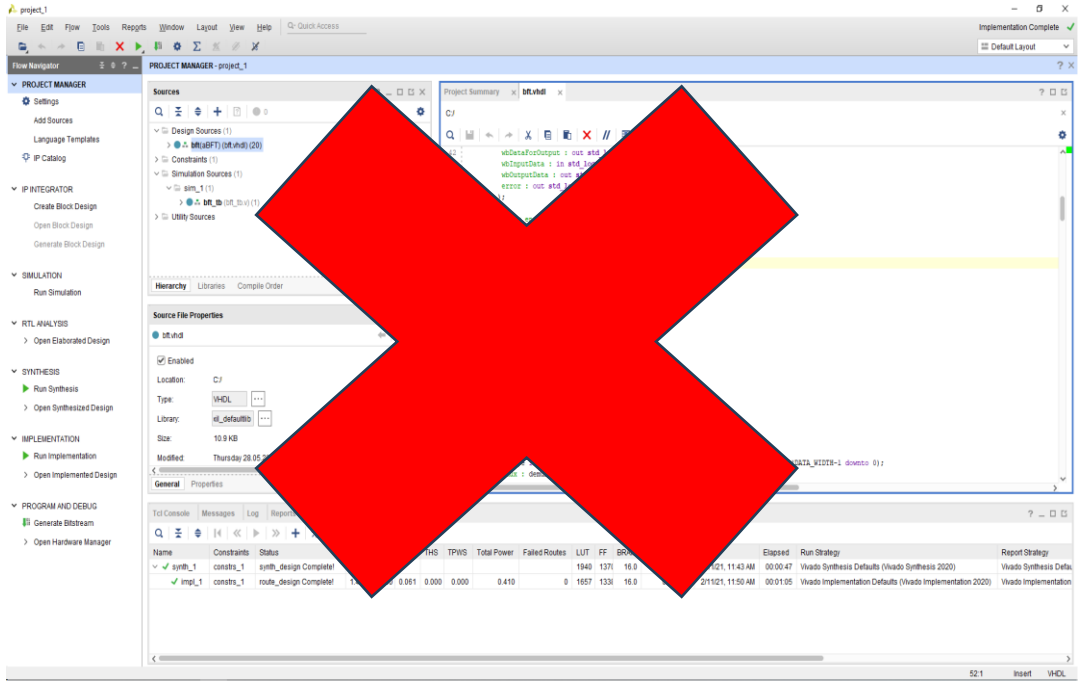
CAEN
Tools for Discovery

Nuclear Instruments

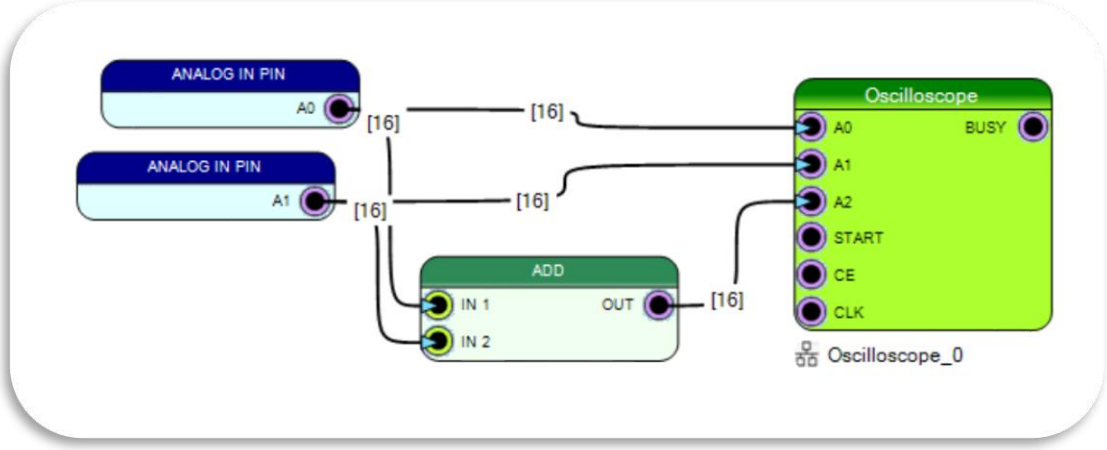

ELMA
PHILIPS
2D Histogram
X Axis
Y Axis #1

From Concept to Creation: SciCompiler Brings Your Ideas to Life

Design as easily as sketching your ideas – no need to learn complex languages like VHDL or Verilog; SciCompiler takes care of it for you.

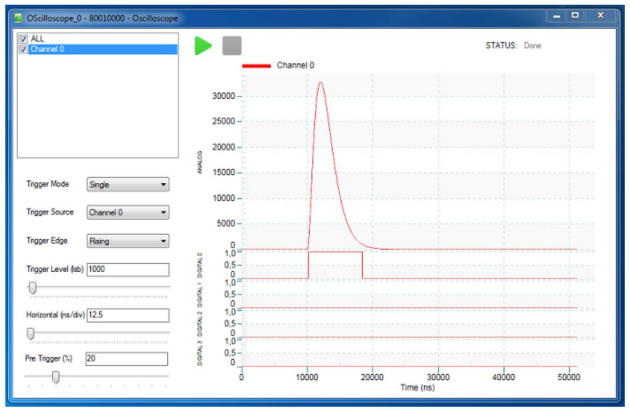


Develop with block diagram



SCI-COMPILER

Sci-Compiler generate for you firmware and software



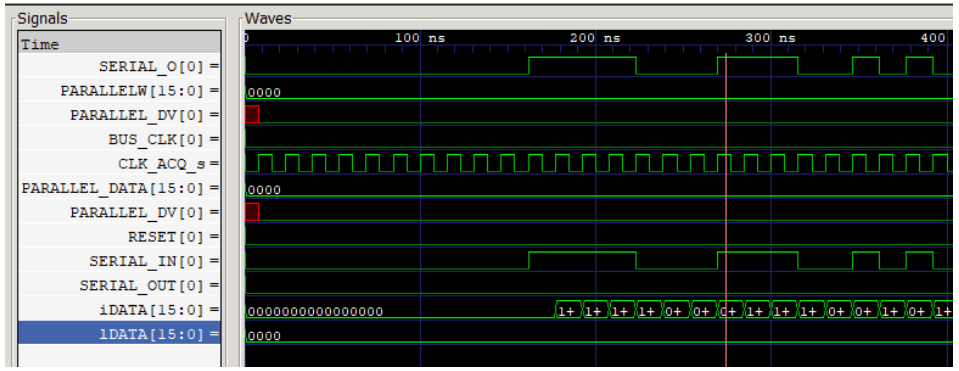
READOUT UI

```
architecture Behavioral of SERIAL_TO_PARALLEL_FIXED is
    SERIAL_OUT(0) <= iDATA(0);

    deserializer_process: process(CLK,RESET)
    begin
        if RESET(0) = '1' then
            iDATA <= (others => '0');
            lDATA <= (others => '0');
        else
            if rising_edge(CLK(0)) then
                if CE(0) = '1' then
                    iDATA(busWidth-1) <=    SERIAL_IN(0);
                    for I in 1 to busWidth-1 loop
                        iDATA(I-1) <= iDATA(I);
                    end loop;
                end if;

                if STREAM_START(0) = '1' then
                    counter <= busWidth;
                    PARALLEL_DV <= "0";
                    running <= '1';
                else
                    if running = '1' then
                        if counter = 0 then
                            PARALLEL_DV <= "1";
                            running <= '0';
                            if MSBFirst = "0" then
                                lDATA <= iDATA;
                            else
```

FIRMWARE

SCI-COMPILER

SIMULATE

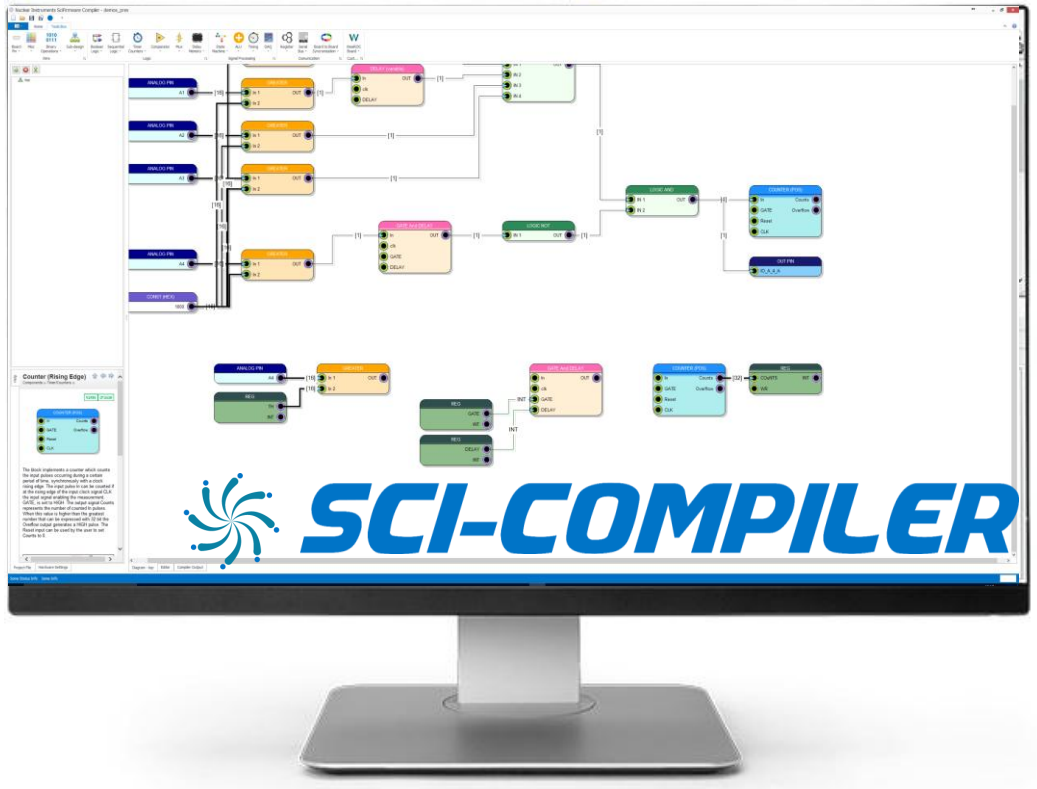


```
int main()
{
    SCISDK_OSCILLOSCOPE *osc_data;

    sdk.AddNewDevice("usb:0006", "dt1
    sdk.StrobeRegister("Registers/res

    sdk.SetParameter("Oscilloscope_0/decim
    sdk.SetParameter("Oscilloscope_0/trigger", "ext"
    sdk.SetParameter("Oscilloscope_0/acq_mode", "b
    sdk.SetParameter("Oscilloscope_0/data_processing", "decode");

    sdk.ExecuteCommand("Oscilloscope_0", "start");

    sdk.AllocateBuffer("Oscilloscope_0", "decoded_buffer", (void **) &osc_data);

    for (int i = 0; i < 10; i++) {
        sdk.ReadData("Oscilloscope_0", osc_data);
        dump_to_file(osc_data);
    }

    return 0;
```

SDK Software Development Kit

WINDOWS AND LINUX SDK

NI/CAEN Solution: OpenFPGA digitizers + SciCompiler firmware generator



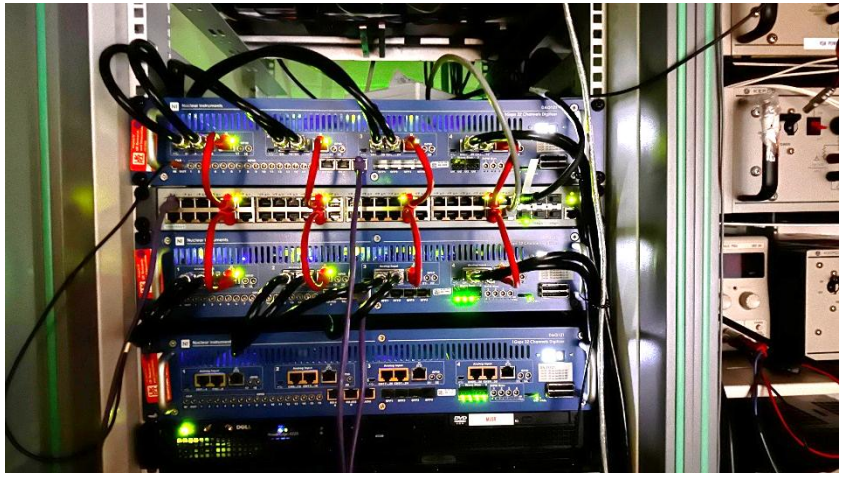
DAQ 121 / DAQ 122

12/14 bit – 1 Gsps

32 channels

Large Scale Experiments read-out system based on Sci-Compiler devices

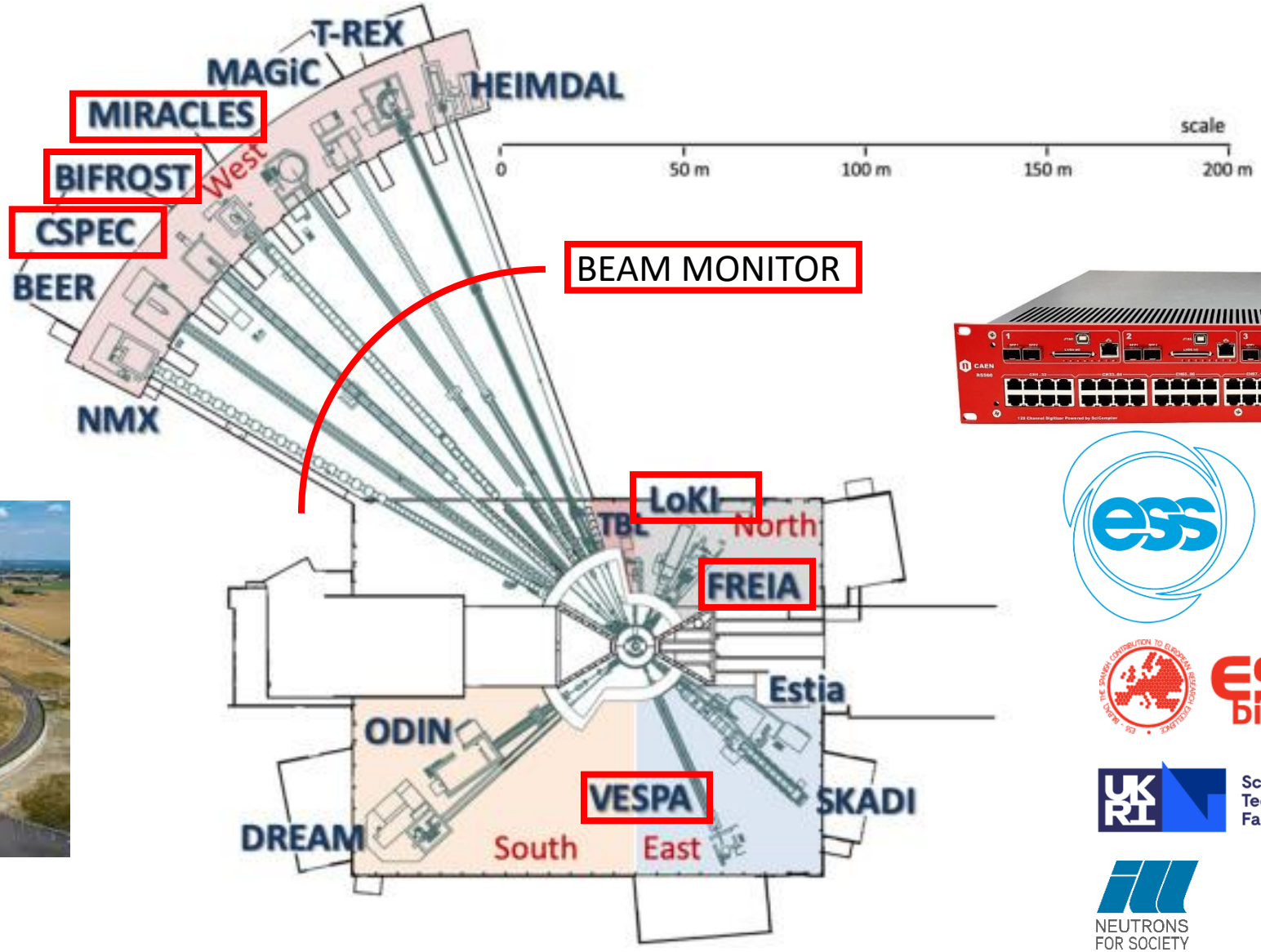
LOKI SANS @ ESS, developed by UKRI – ISIS – R5560



ISIS HiFI – DAQ 121

ISIS SuperMUSR – DAQ 121

(ESS) LOKI, BIFROST, MIRACLES, CSPEC, VESPA more than 10K channels



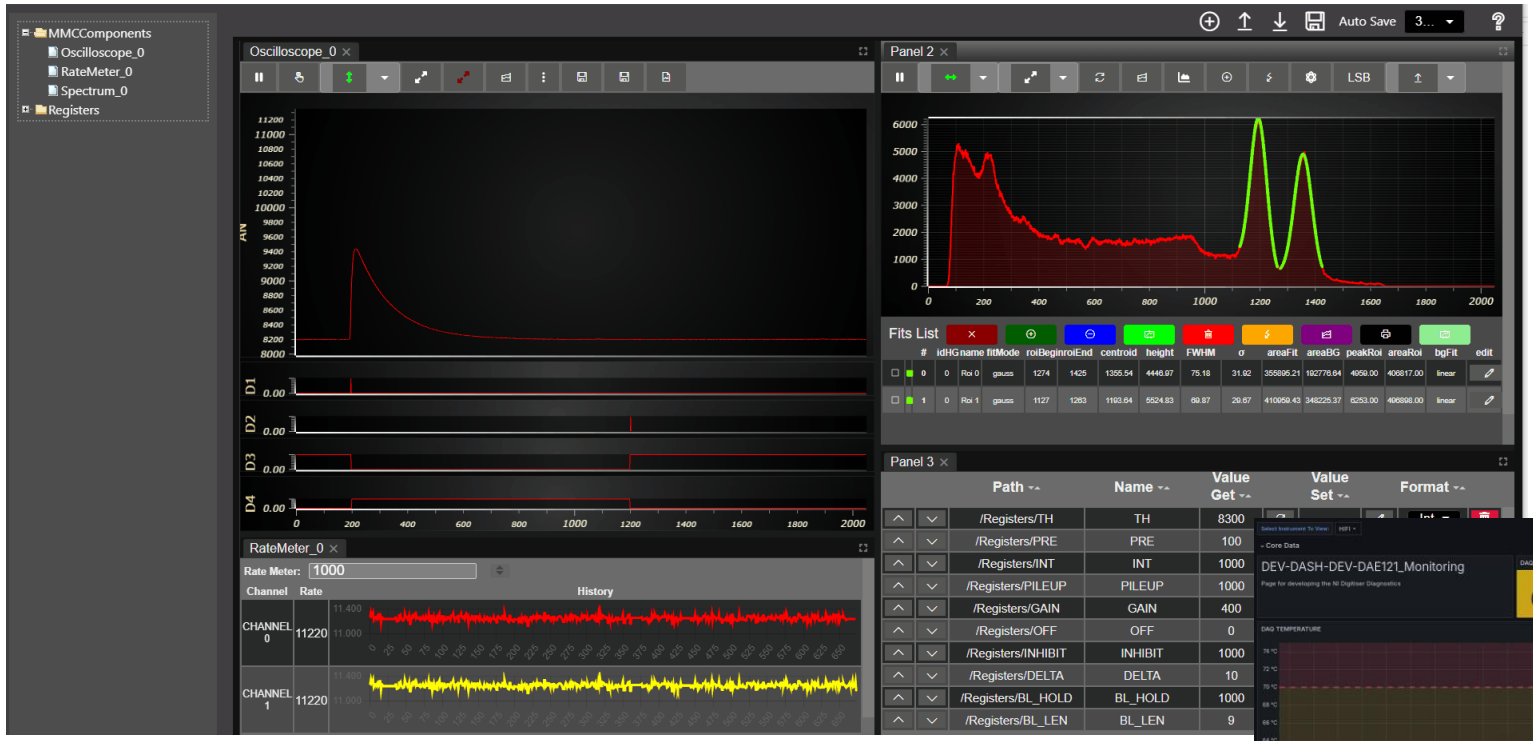
EUROPEAN SPALLATION SOURCE

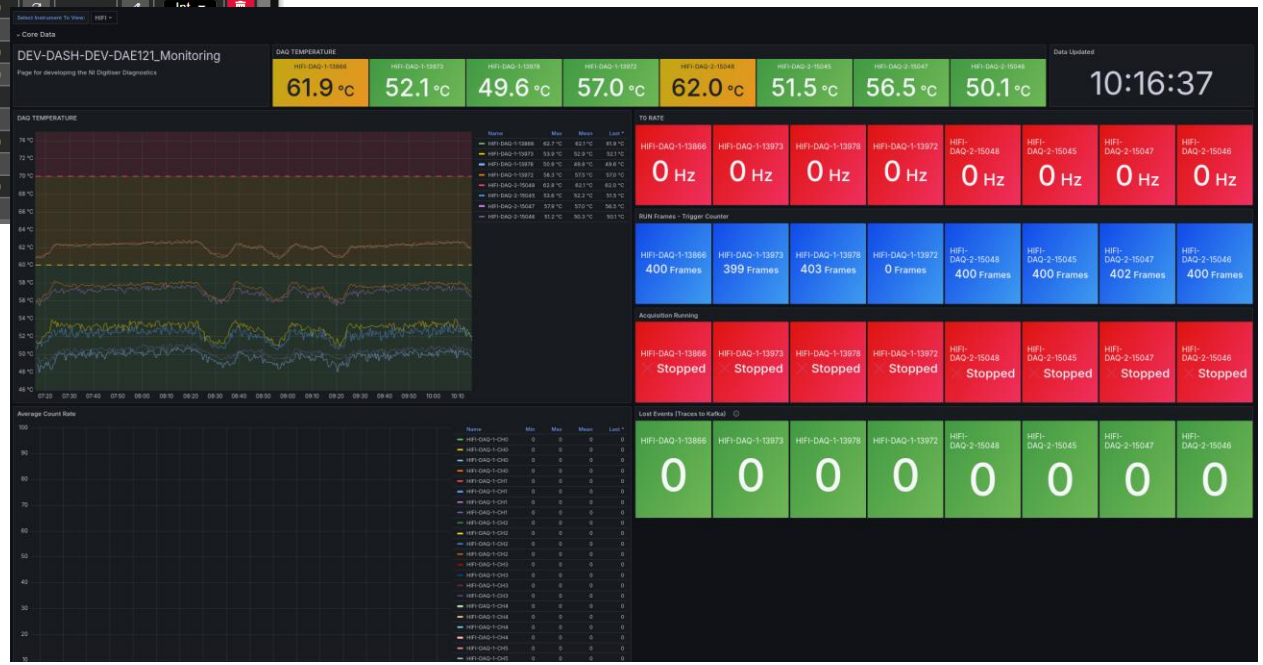
ESS bilbao

Science and Technology Facilities Council

NEUTRONS FOR SOCIETY

Real-time monitor and SCADA integration



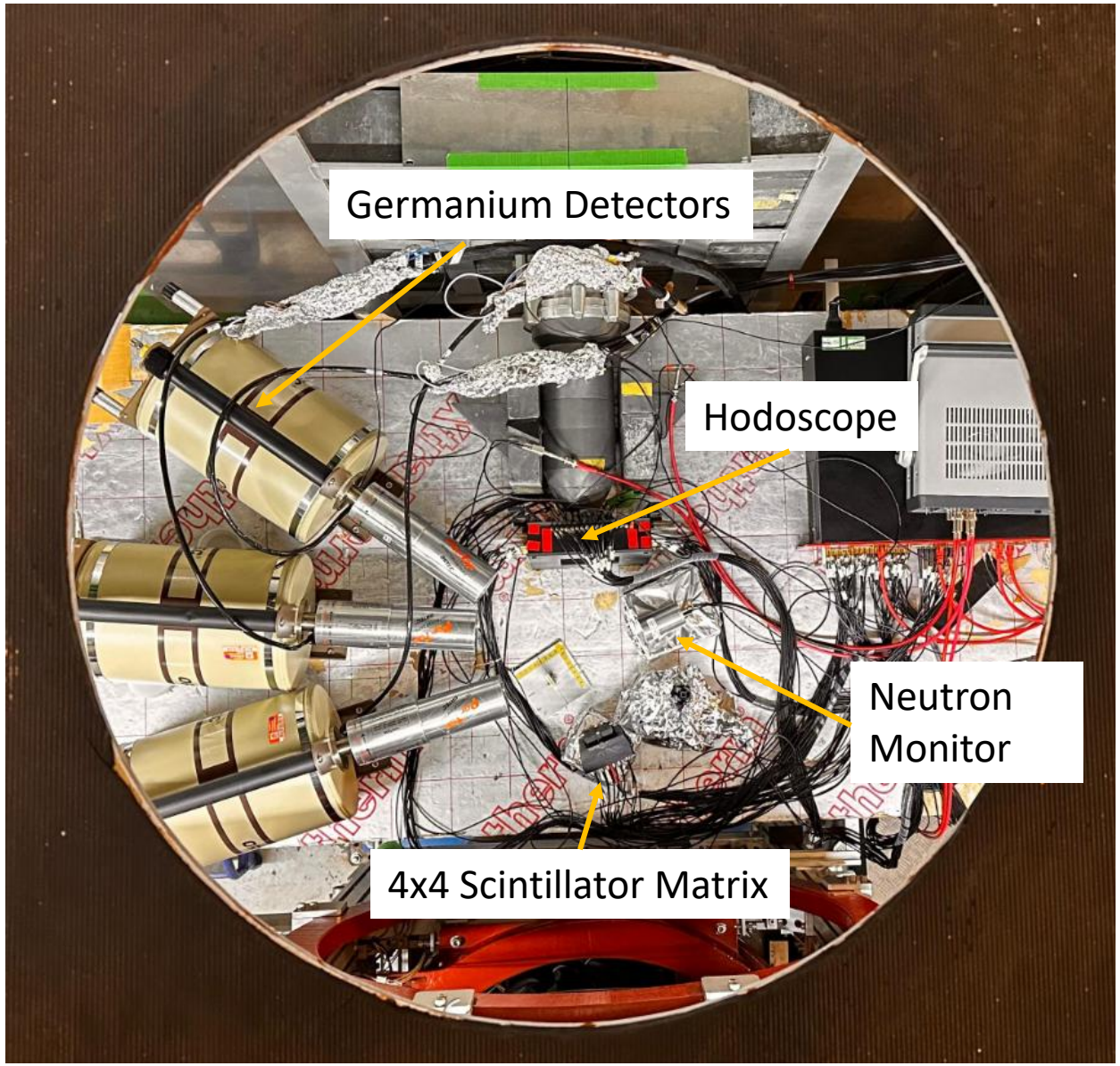


- On-board signal probe with web interface
- Influx DB connector (GRAFANA MONITOR)
- On-board EPICS server
- On-board UPCUA server

ISIS Fiber Hodoscope CHNET MAXI

Massimiliano Clemenza - UNIMIB

- 32X + 32Y scintillating fiber
- 9 Germanium detector readout with online spectrum calculation
- 4x4 Scintillator matrix readout
- 2 neutron monitor with PSD real-time processing
- Readout using R5560SE digitizer
- Installed and test on CRONOS ISIS detector



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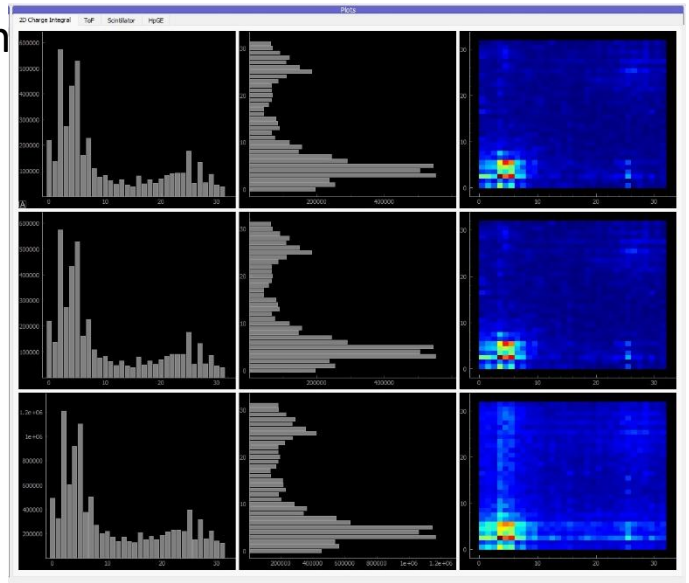
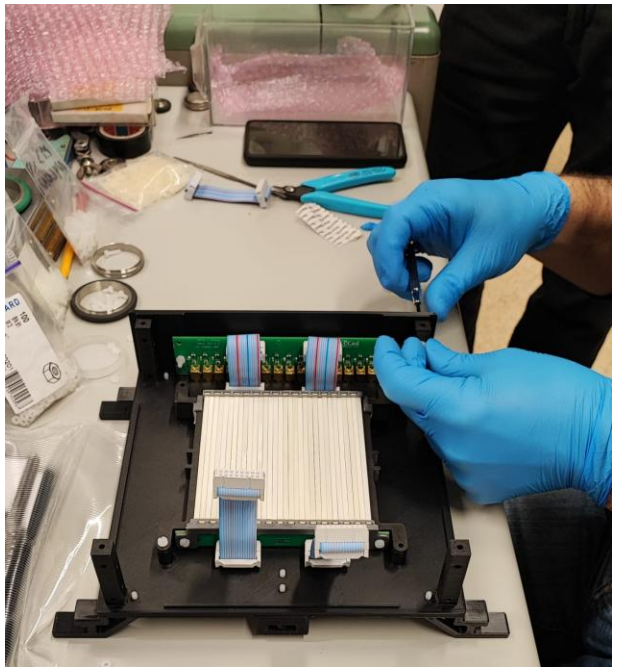
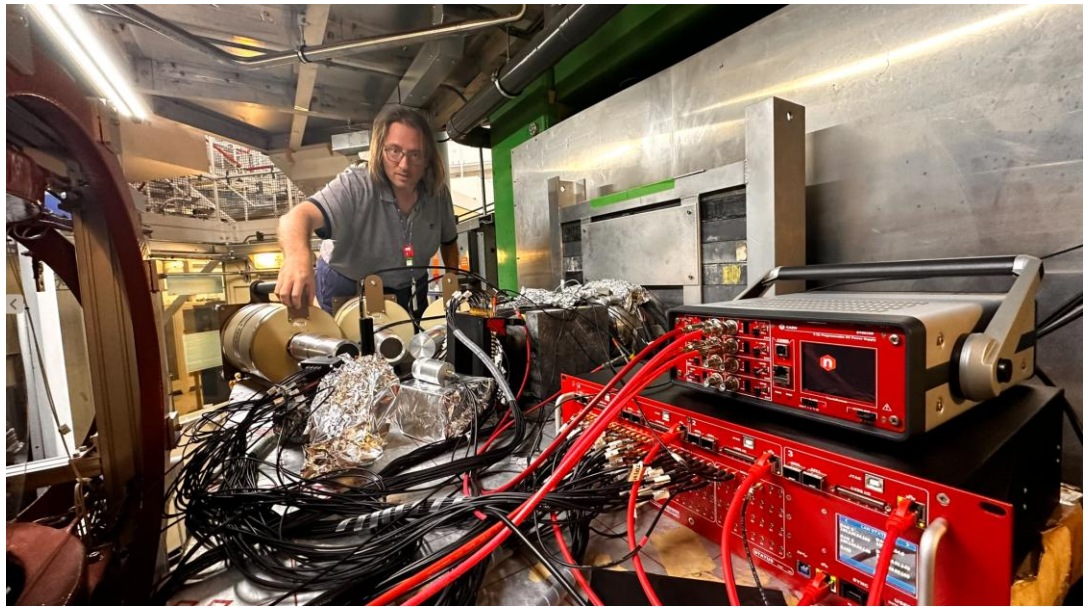
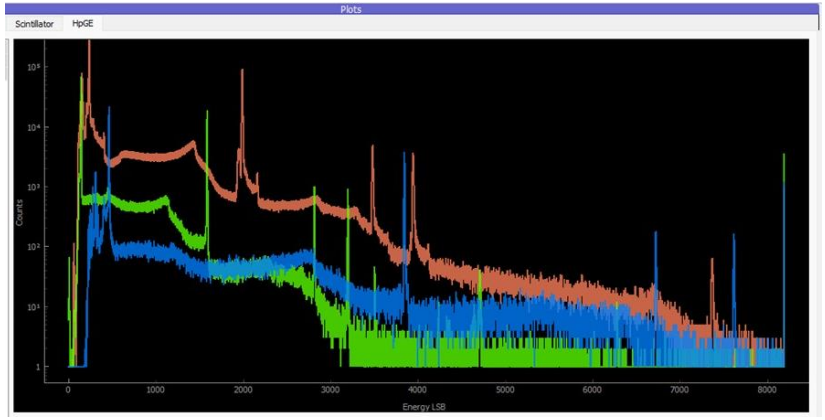
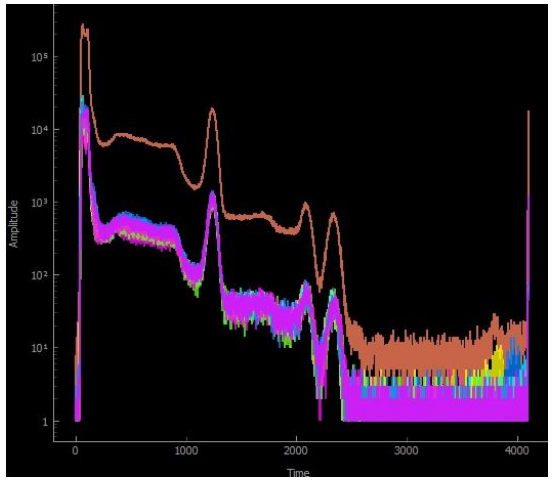




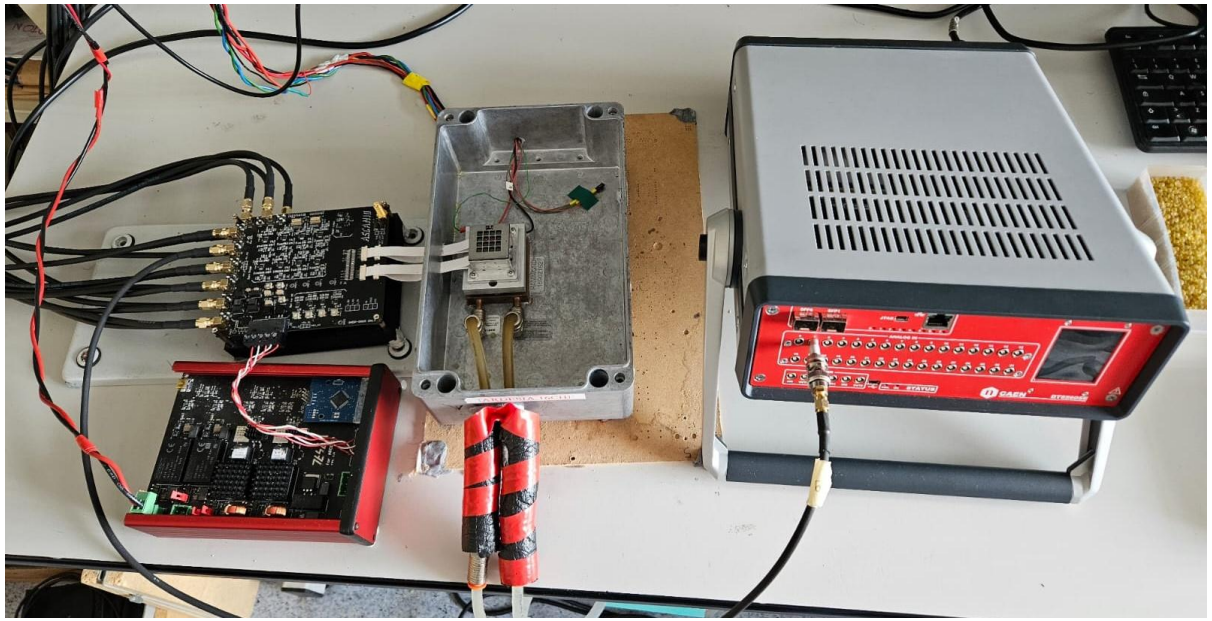


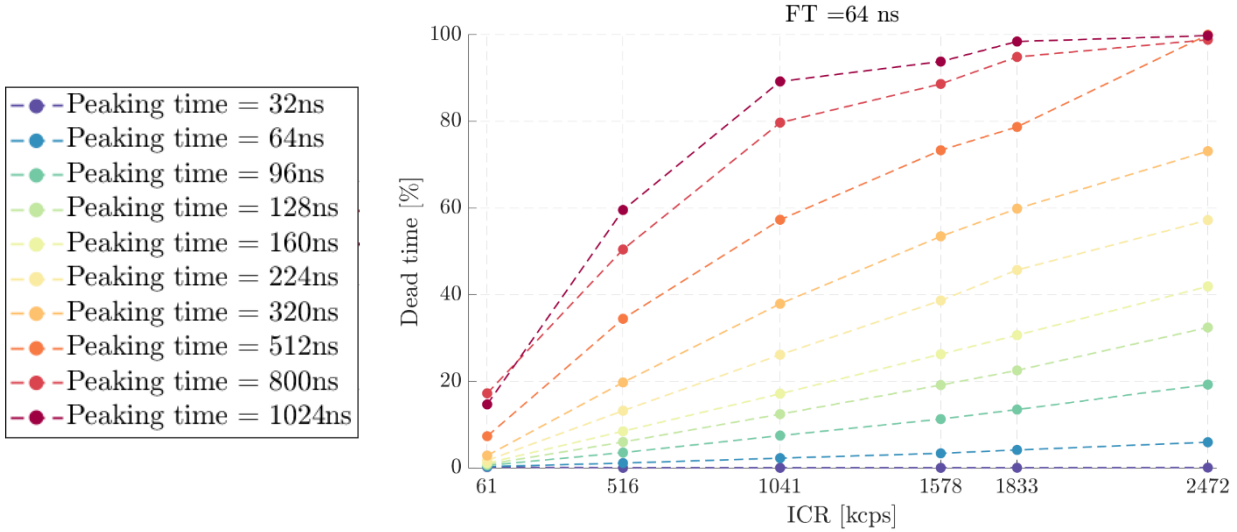


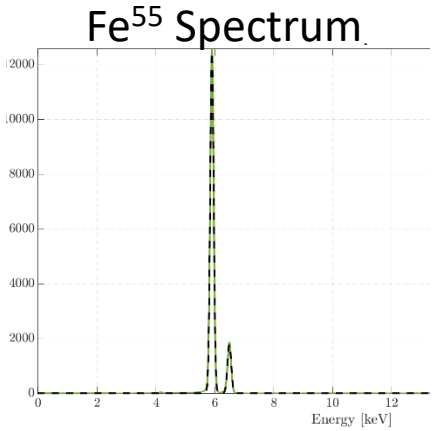


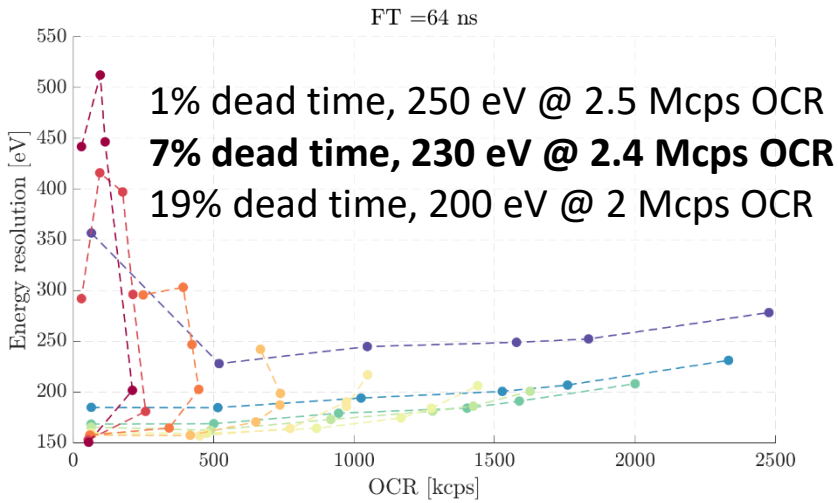
Ardesia 16 channels SDD read-out

- SDD (Silicon Drift Detector) matrix 4x4 detector
- Front end: 4 channel Cube ASIC designed at PoliMI
- Achieving high throughput with minimal dead time
- Good energy resolution.









POLITECNICO MILANO 1863

DEIB

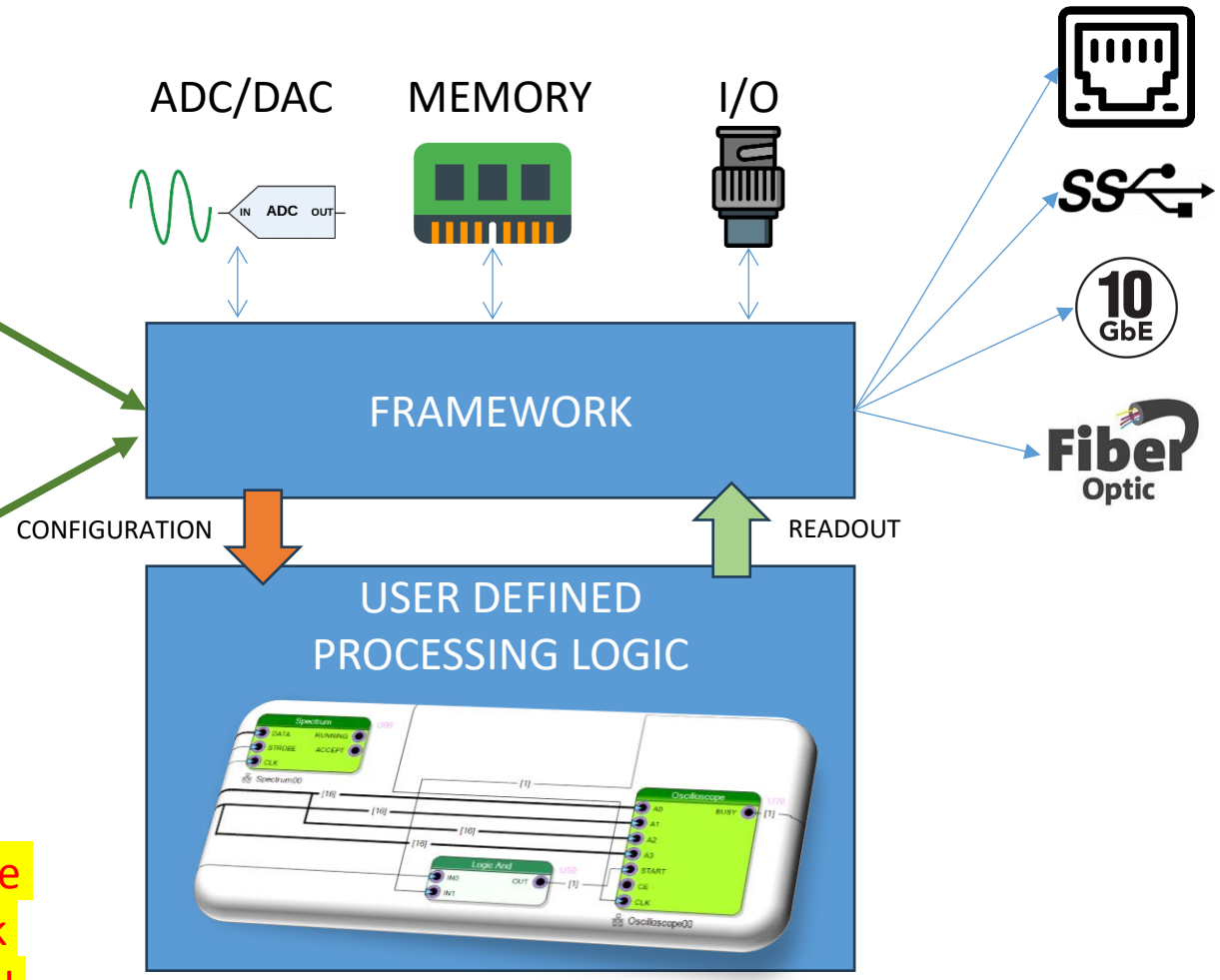
Open-FPGA Board architecture

Primary function of a firmware:

Control the board acquisition process

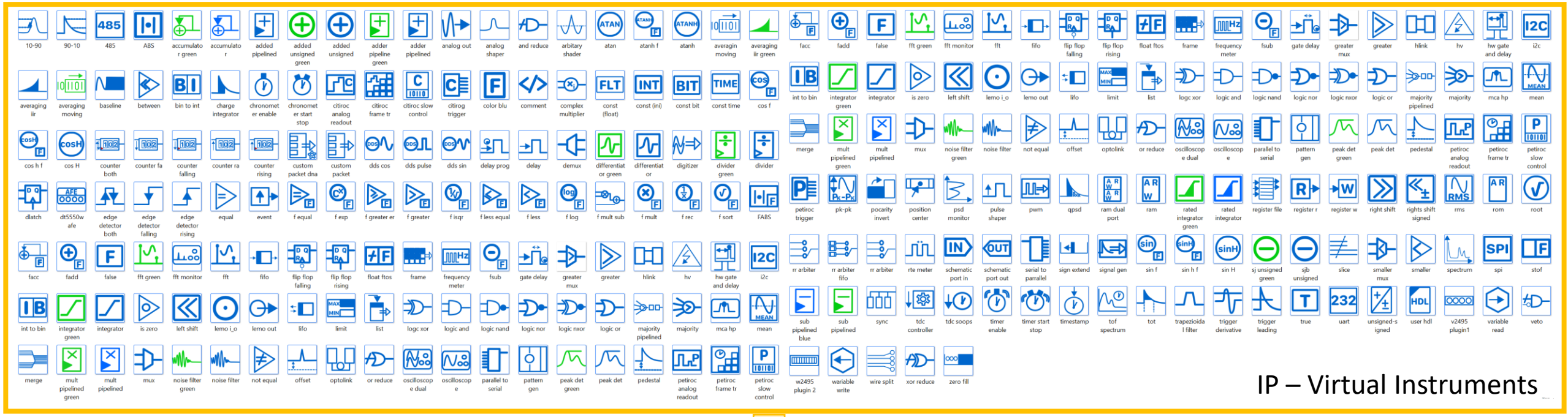
Processing data

Transfer data to and from readout PC/Server

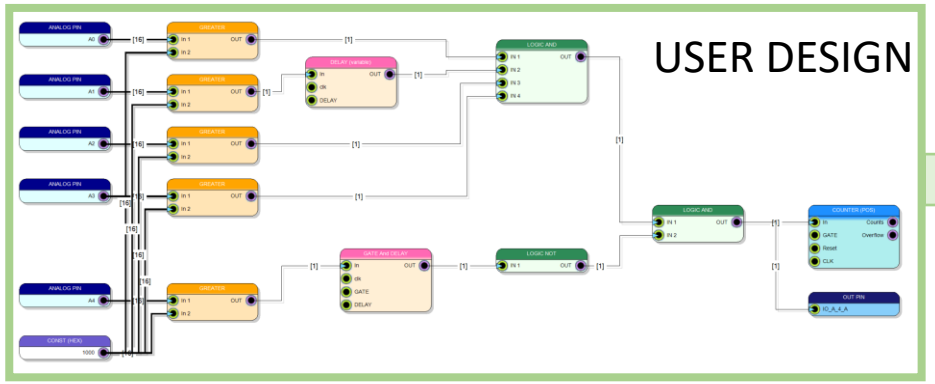


Sci-Compiler lets the developer think only about the core algorithm — everything else, from framework to readout, is handled automatically with high-level abstraction blocks.

SciCompiler: ip integrator software

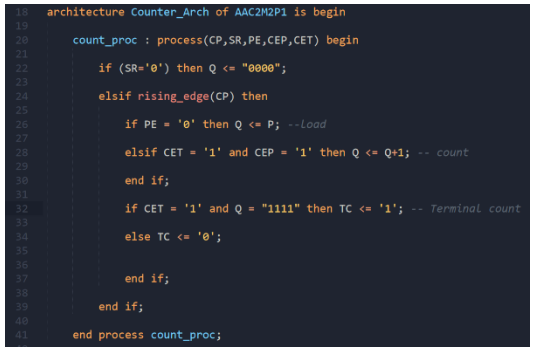


IP – Virtual Instruments



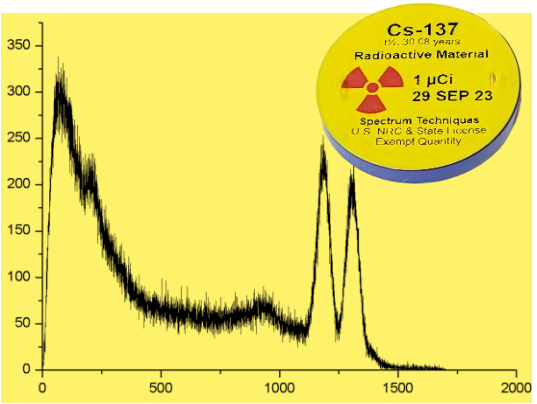
USER DESIGN

BUILDER ENGINE

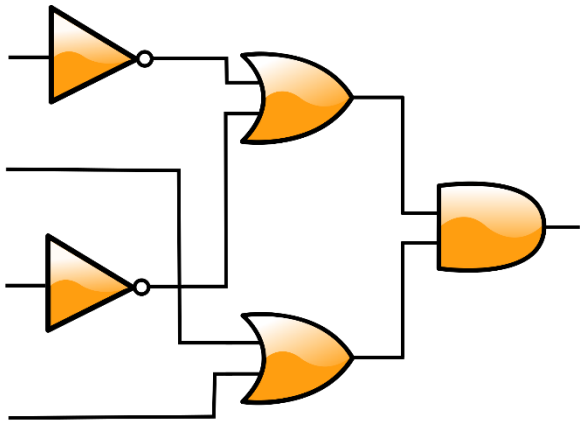


```
architecture Counter_Arch of AAC2M2P1 is begin

    count_proc : process(CP,SR,PE,CEP,CET) begin

        if (SR='0') then Q <= "0000";

        elsif rising_edge(CP) then

            if PE = '0' then Q <= P; --Load

            elsif CET = '1' and CEP = '1' then Q <= Q+1; -- count

            end if;

            if CET = '1' and Q = "1111" then TC <= '1'; -- Terminal count

            else TC <= '0';


            end if;

        end if;

    end process count_proc;
```

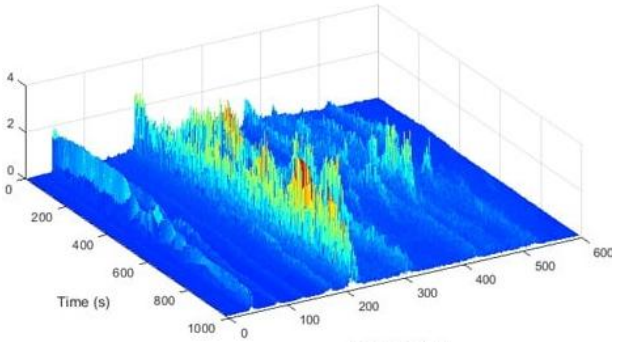
Examples of what you can do with Sci-Compiler



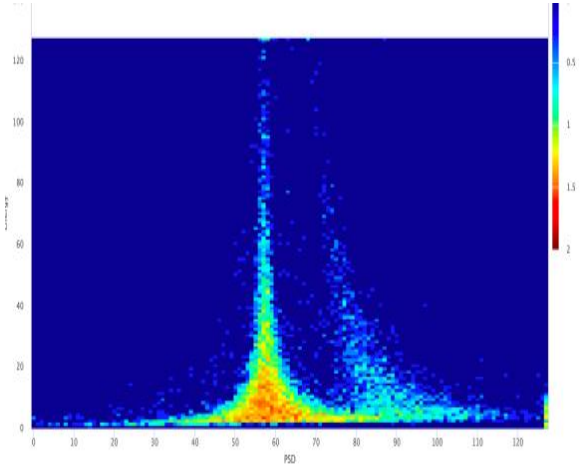
PHA



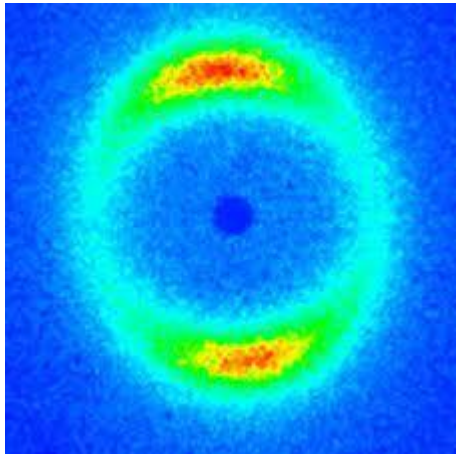
COMPLEX TRIGGER LOGIC



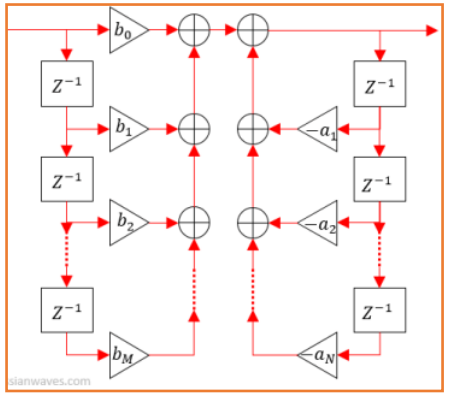
REALTIME FFT



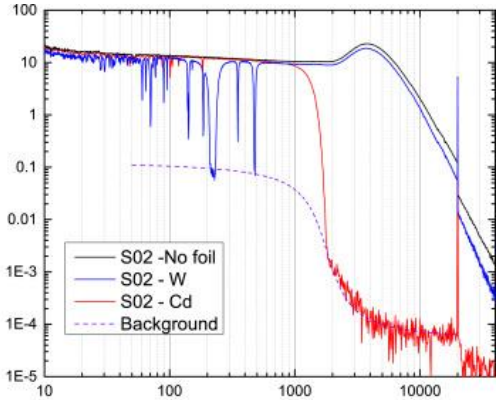
PSD



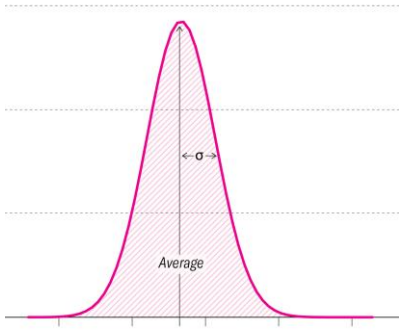
NEUTRON IMAGING



REALTIME IIR-FIR FILTER

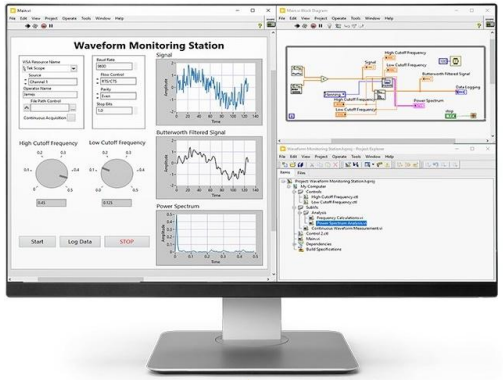


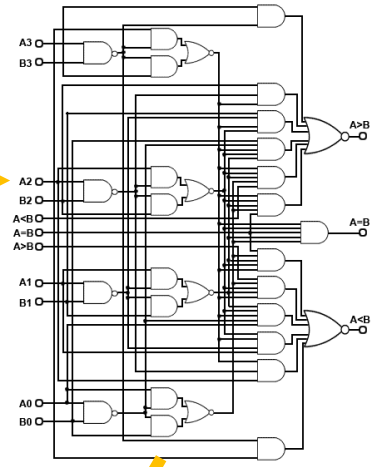
SUB-ns TOF TDC



REALTIME STATISTICS

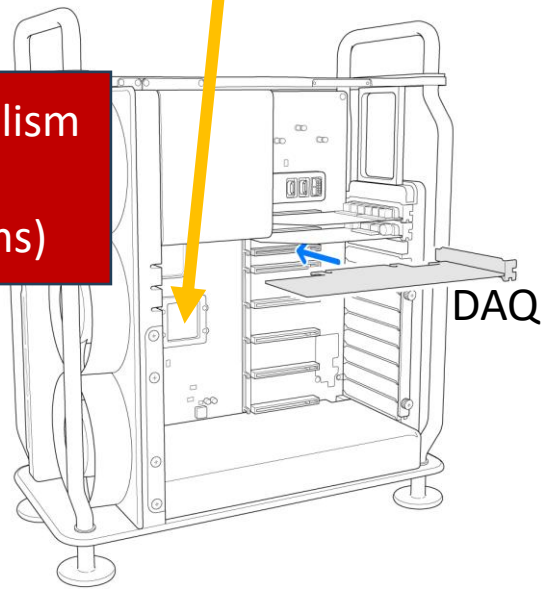
Sci-Compiler generates firmware

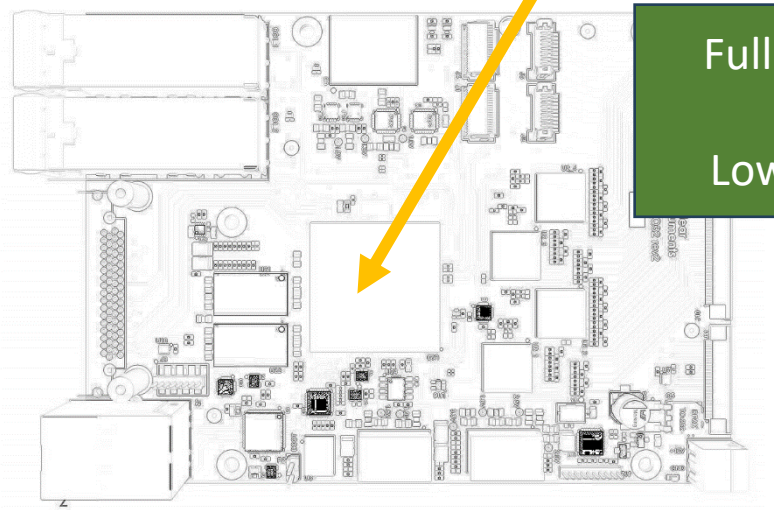




Limited parallelism

High delay (ms)





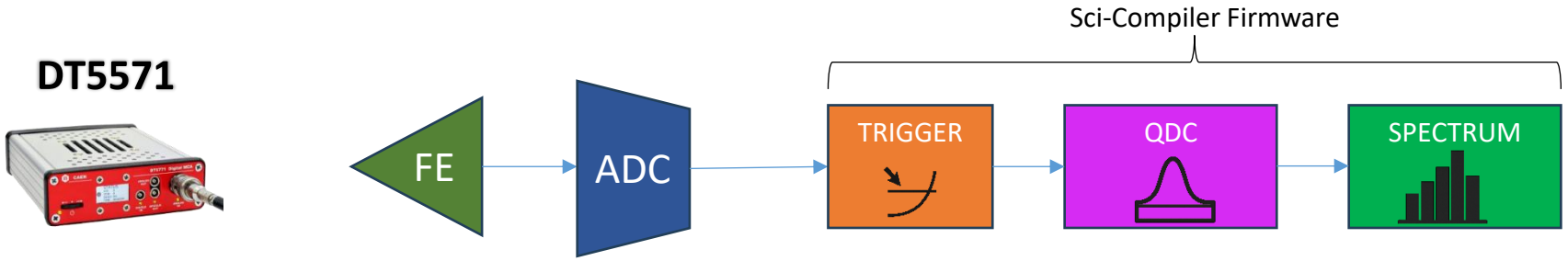
Full parallelism

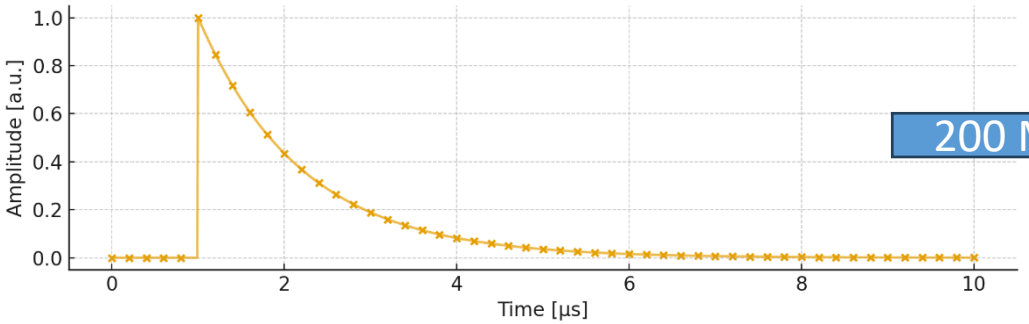
Low delay (ns)

Other VPL (like Labview) generate code for CPU running inside DAQ computer

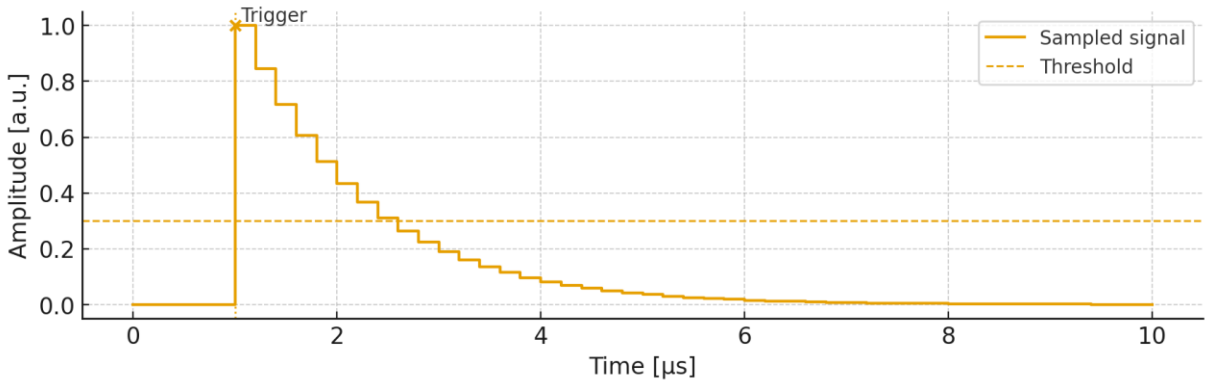
Generate FPGA firmware that «runs» directly inside the DAQ

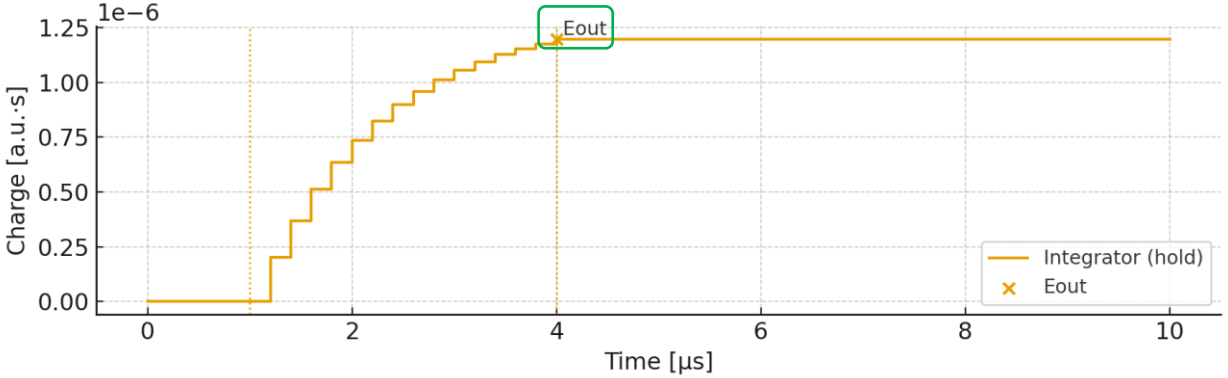
High Speed Digitizer



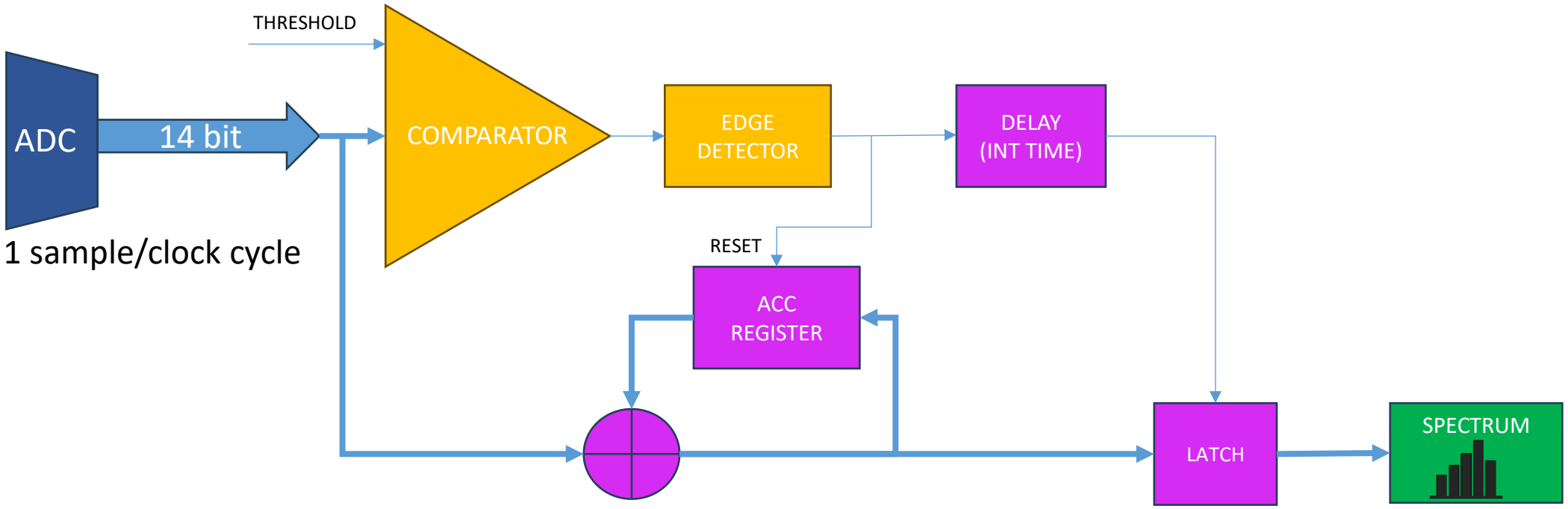


200 Msps





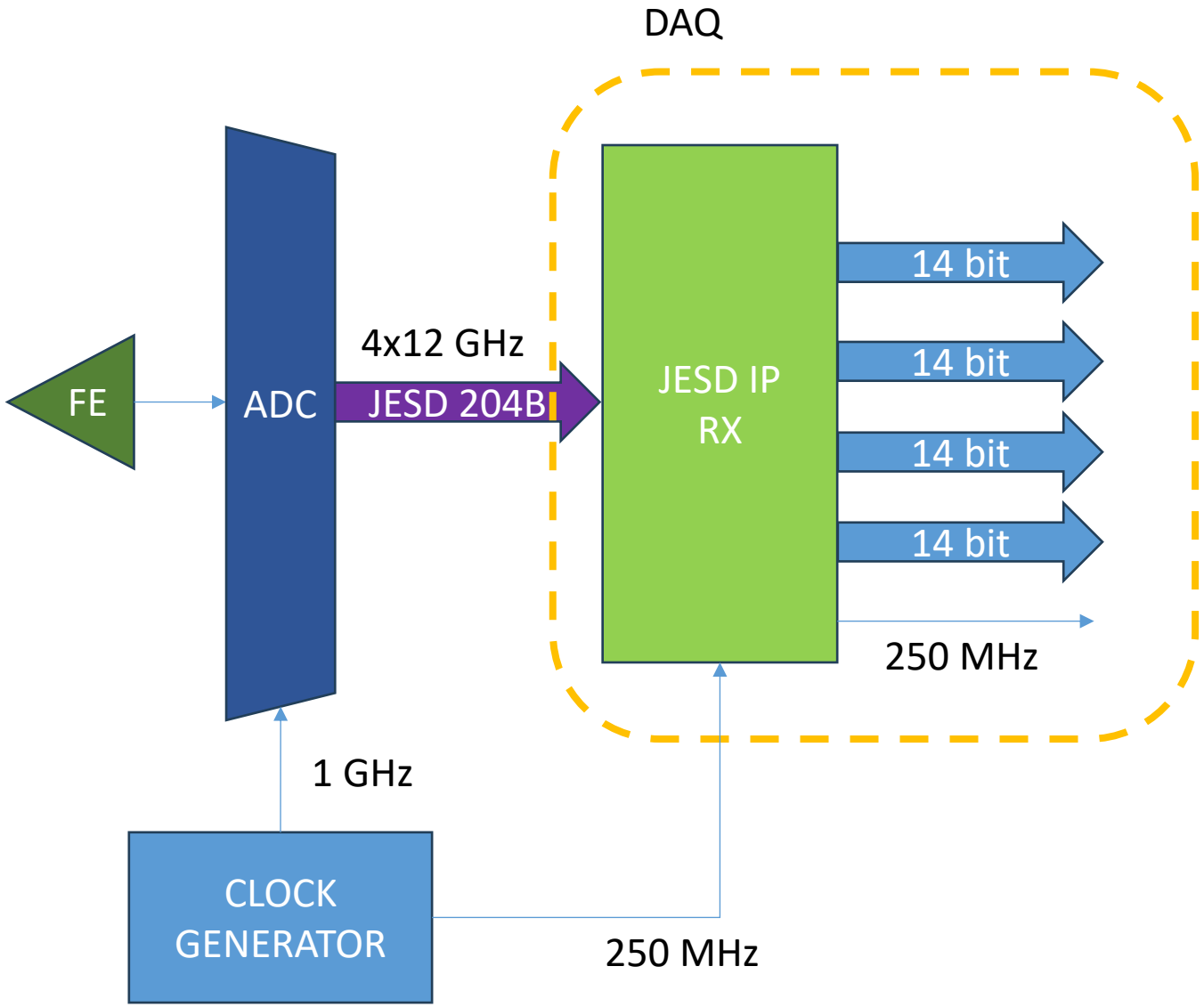
High Speed Digitizer



High Speed Digitizer

Nuclear Instruments
DAQ 121 - DAQ 122
1 Gsps, 32 channel, 12/14 bit

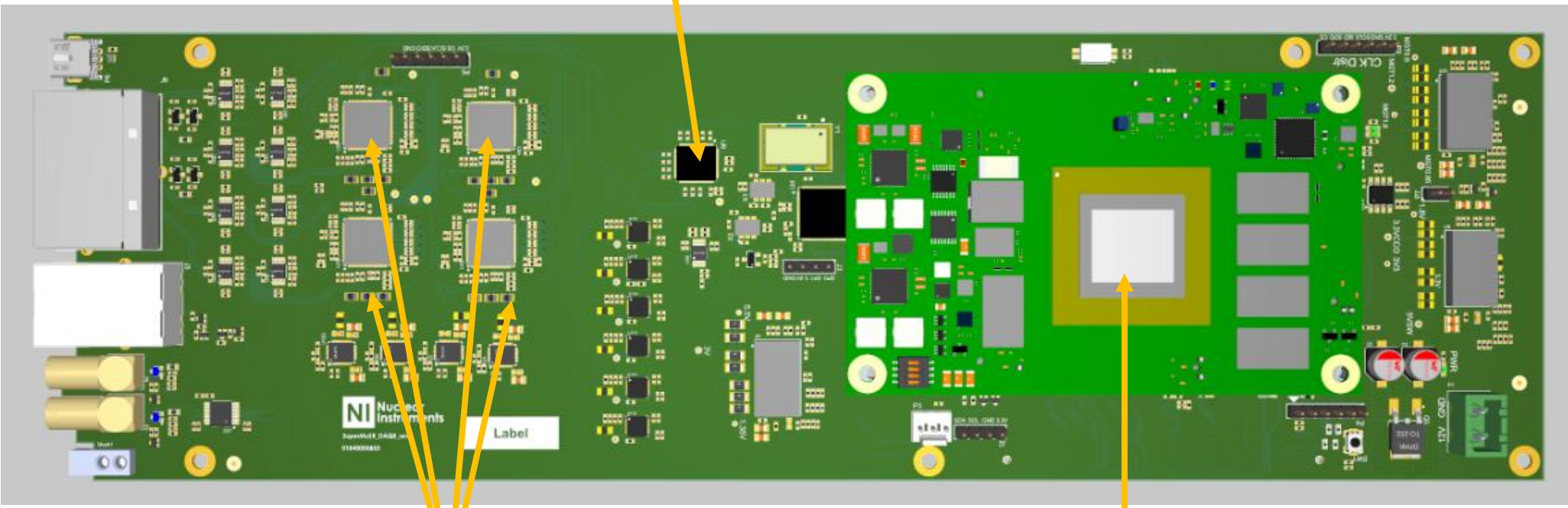
CAEN V2730 - 500 Msps, 32 channel, 14 bit
CAEN V2751 - 1 Gsps, 16 channel, 14 bit



High Speed Digitizer

8 Channels module

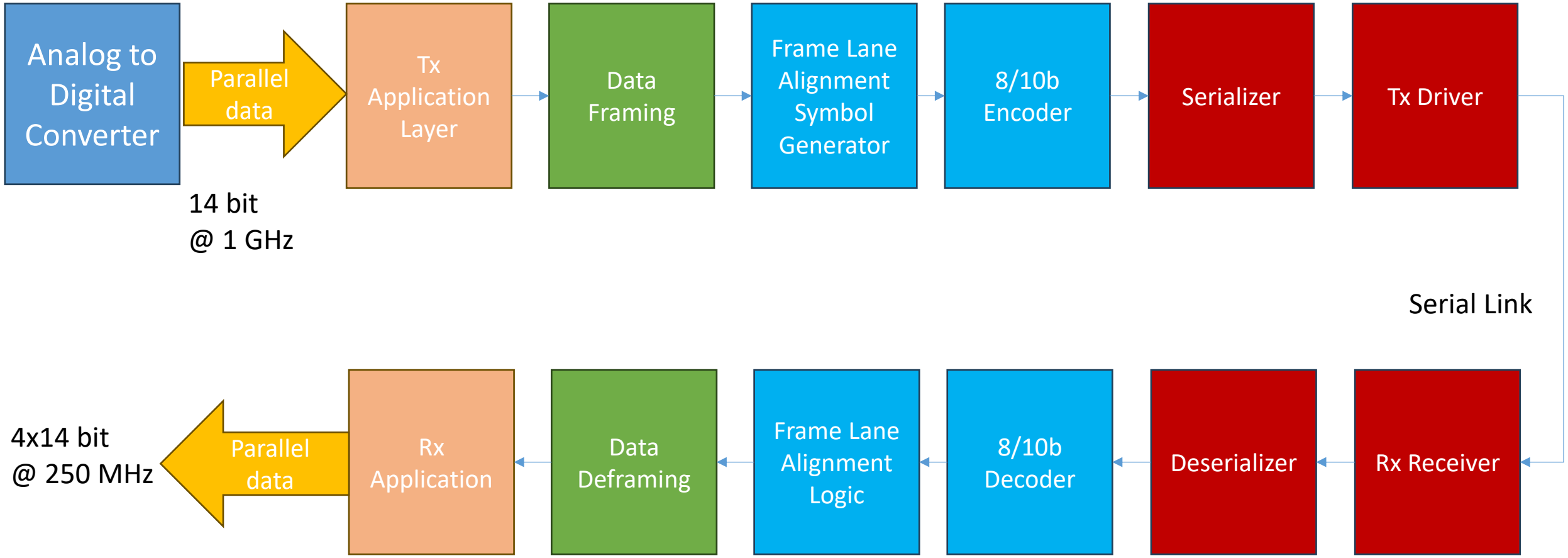
Clock Generator/Distributor



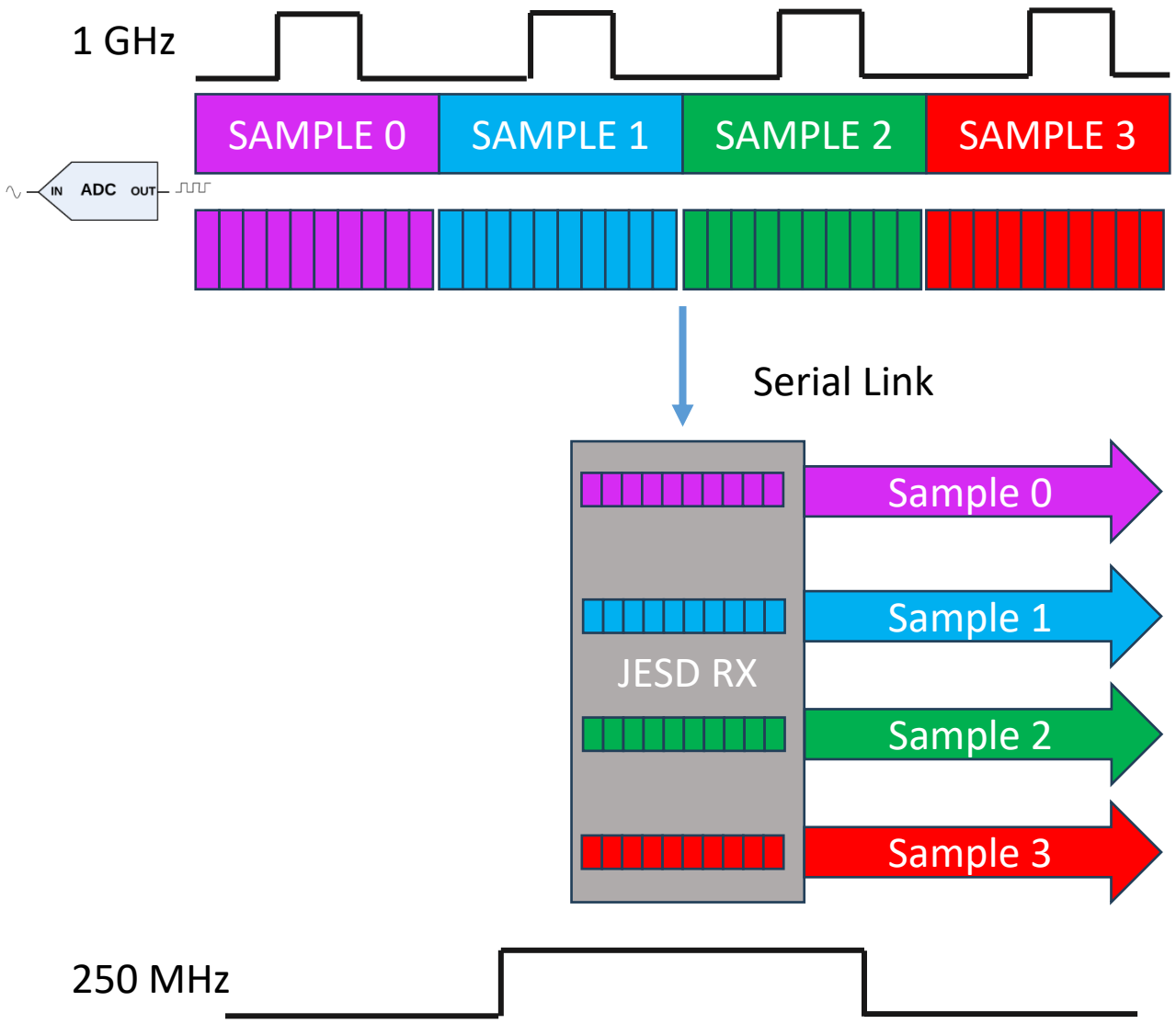
FPGA (Zynq Ultrascale+ SoC)

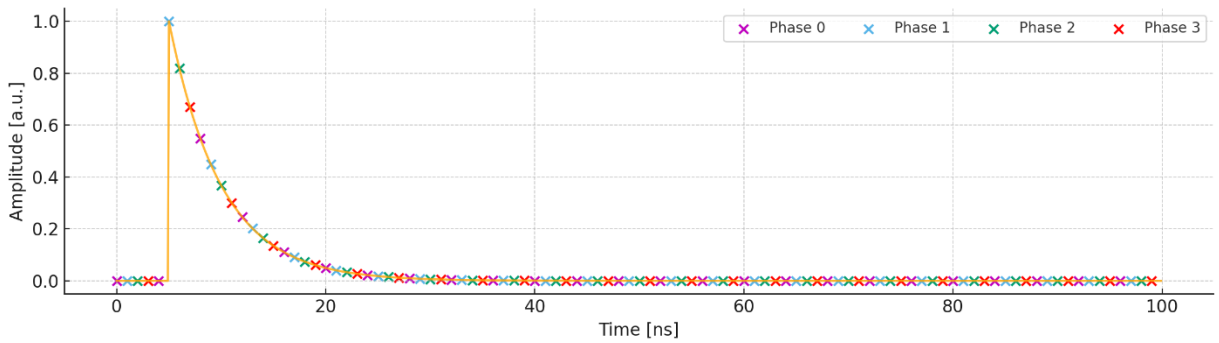
ADC 1 Gsps – 14 bit

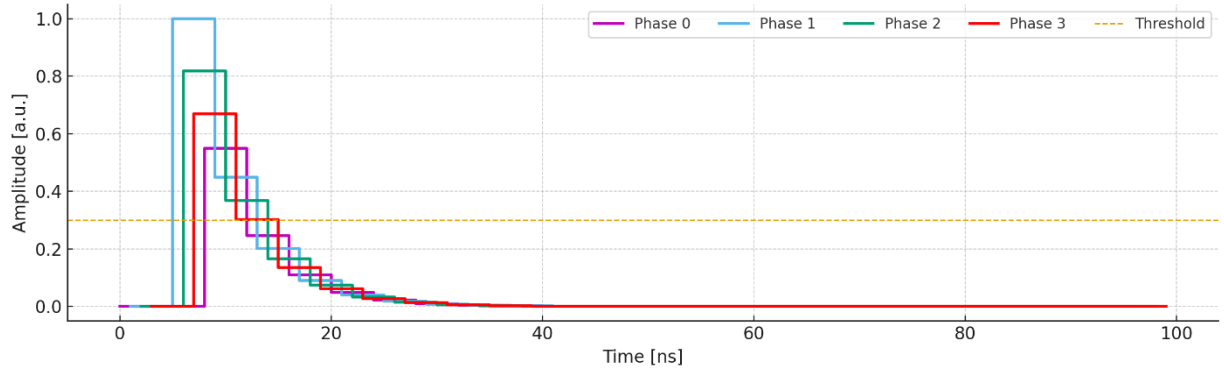
High Speed Digitizer: Serial data link JED204.B



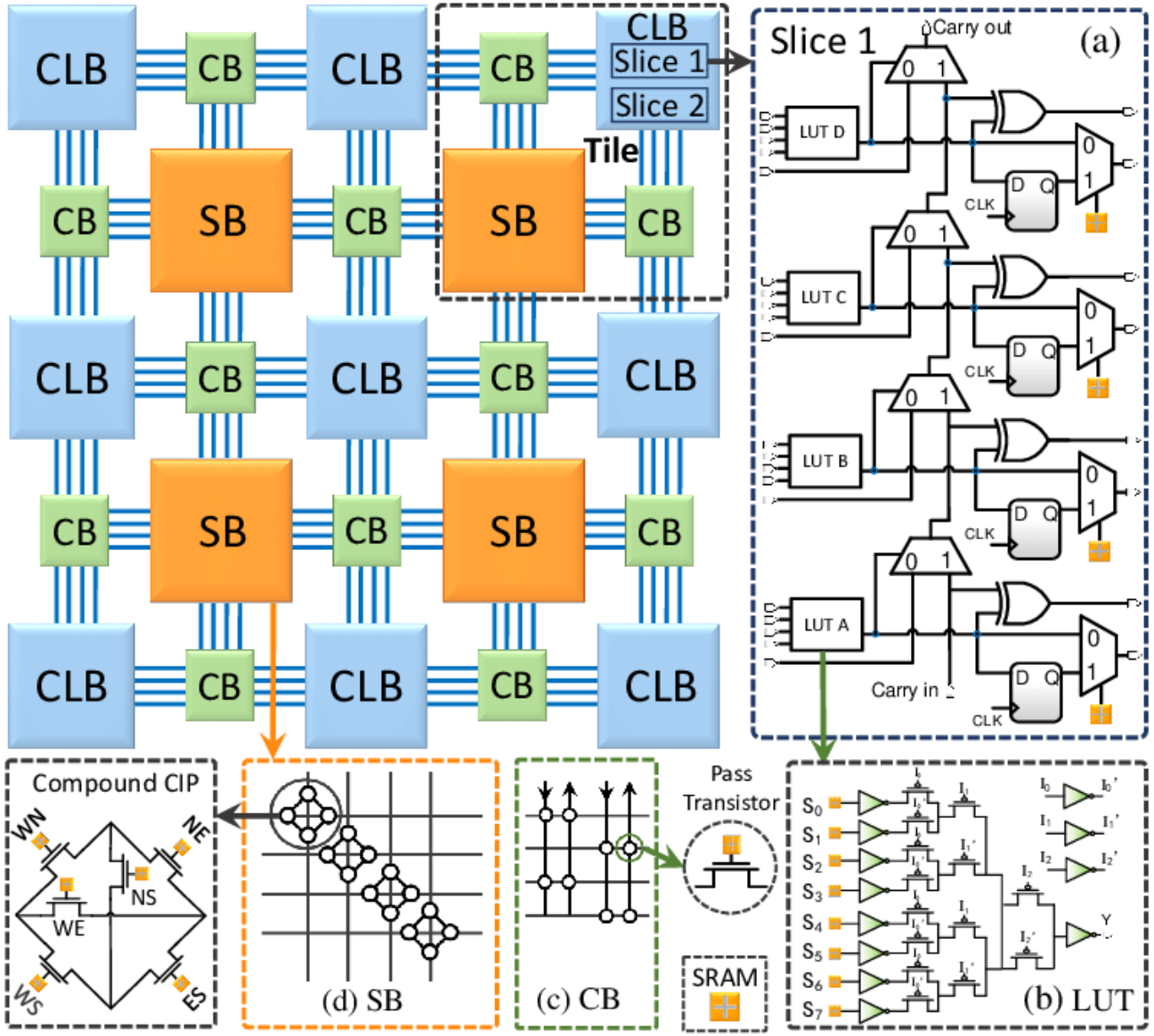
High Speed Digitizer: Parallel data decoding







High Speed Digitizer: FPGA clock speed limit

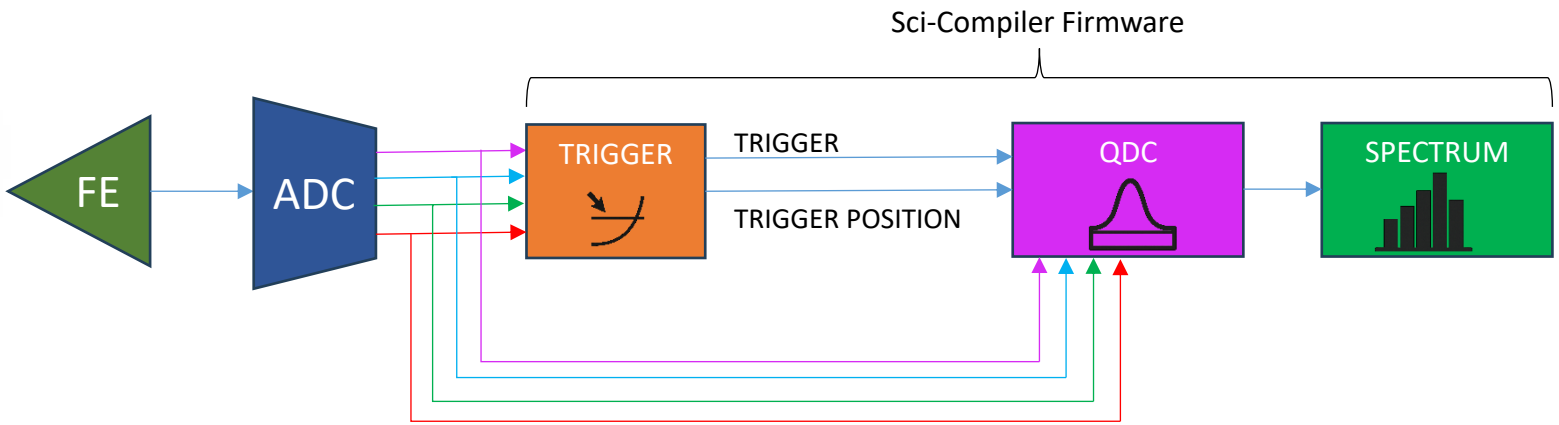


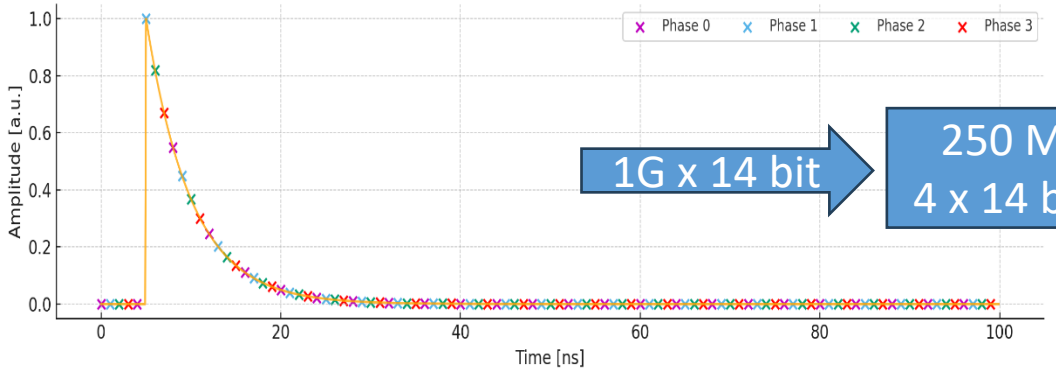
- Programmable FPGA architecture limits maximum clock speed
- Modern FPGA optimized designed may operate in the range 250 – 400 MHz
- Congestion in the device reduce maximum speed
- Safe margin must be considered for “open hardware” configurable application

High Speed Digitizer: Parallel QDC implementation

NI-DAQ 122

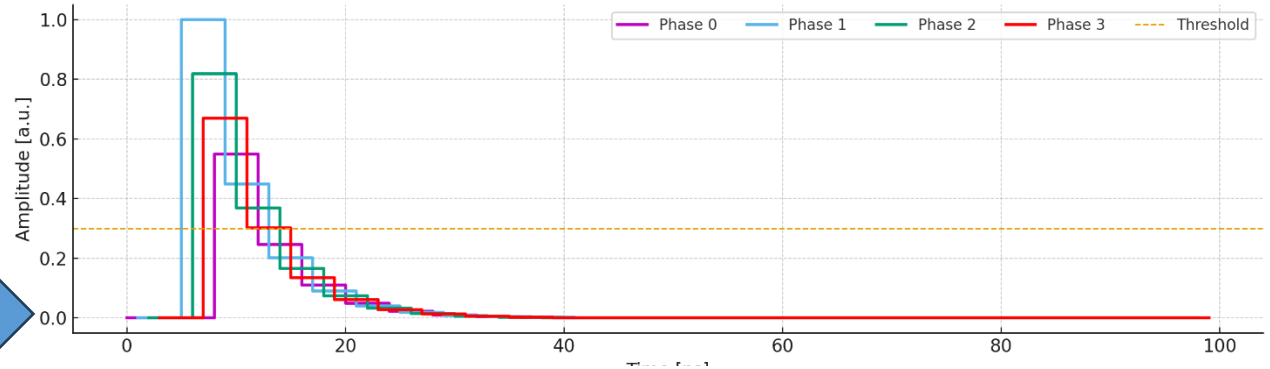
CAEN DT2730

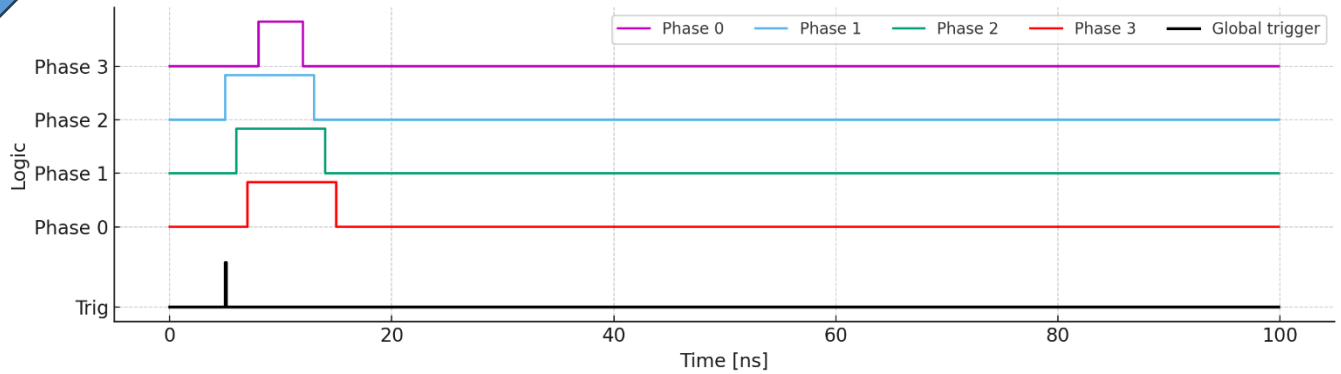




1G x 14 bit

250 M
4 x 14 bit

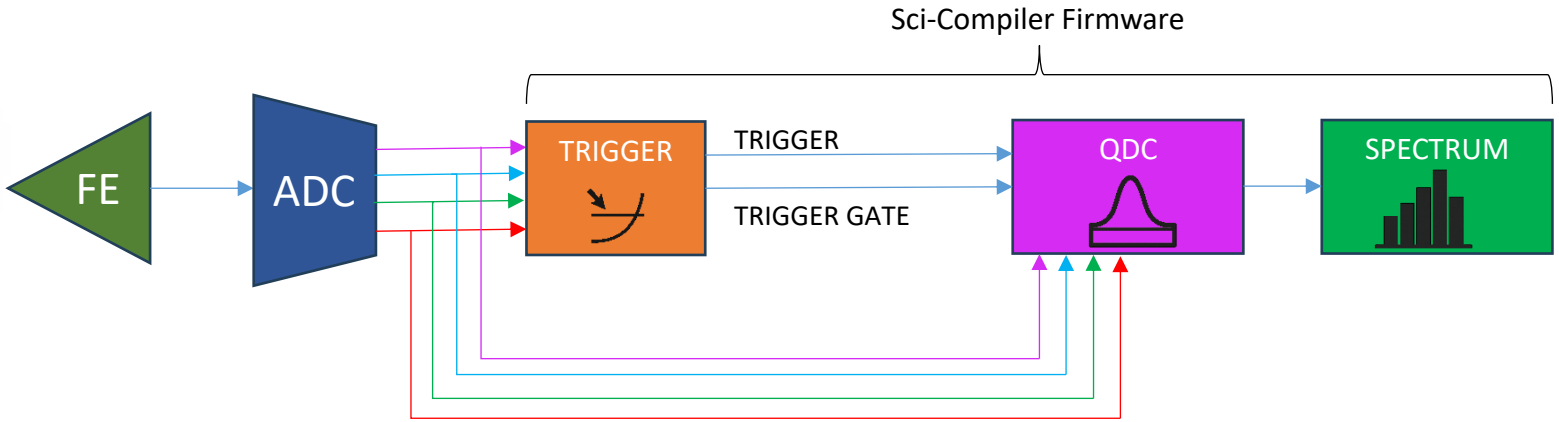


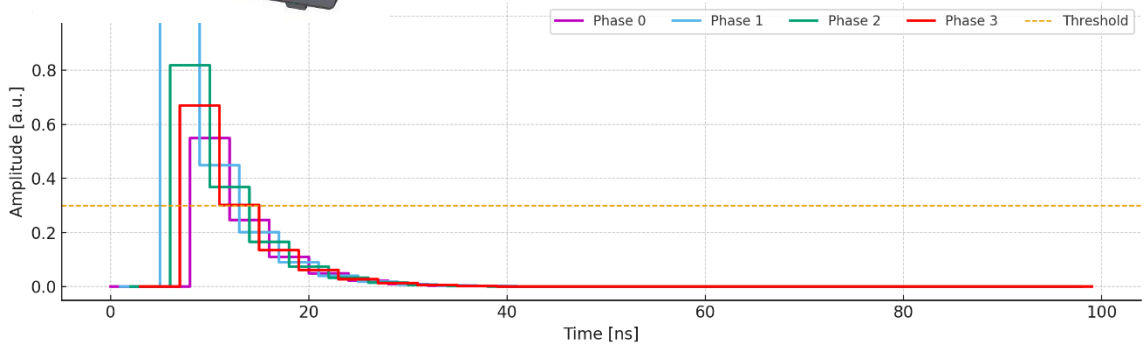


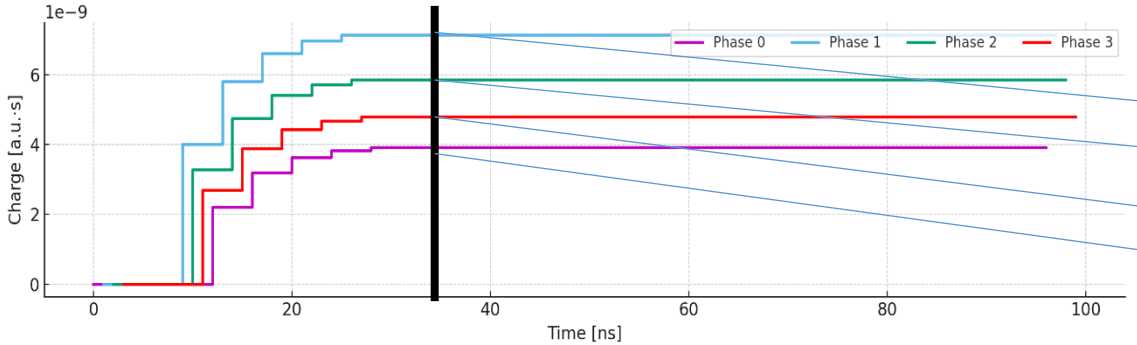
High Speed Digitizer: Parallel QDC implementation

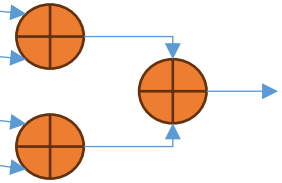
NI-DAQ 122

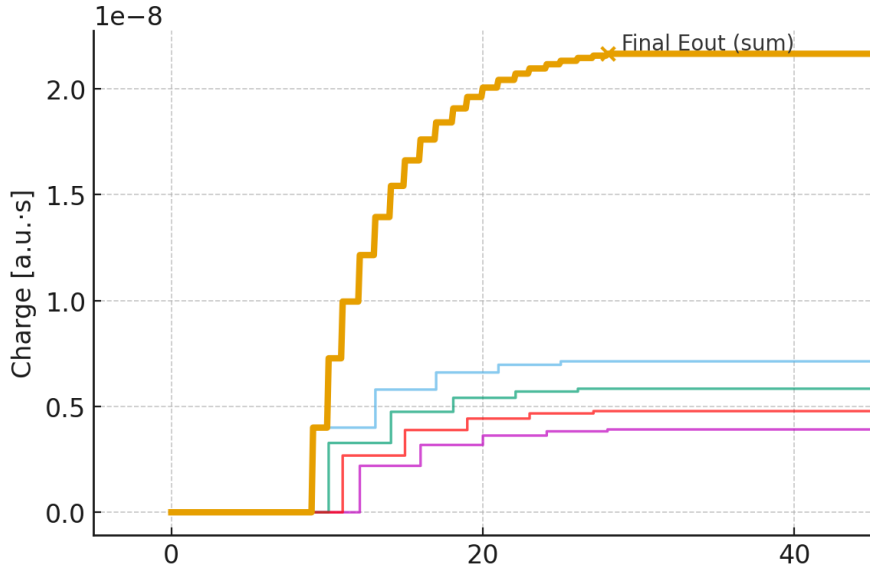
CAEN DT2730



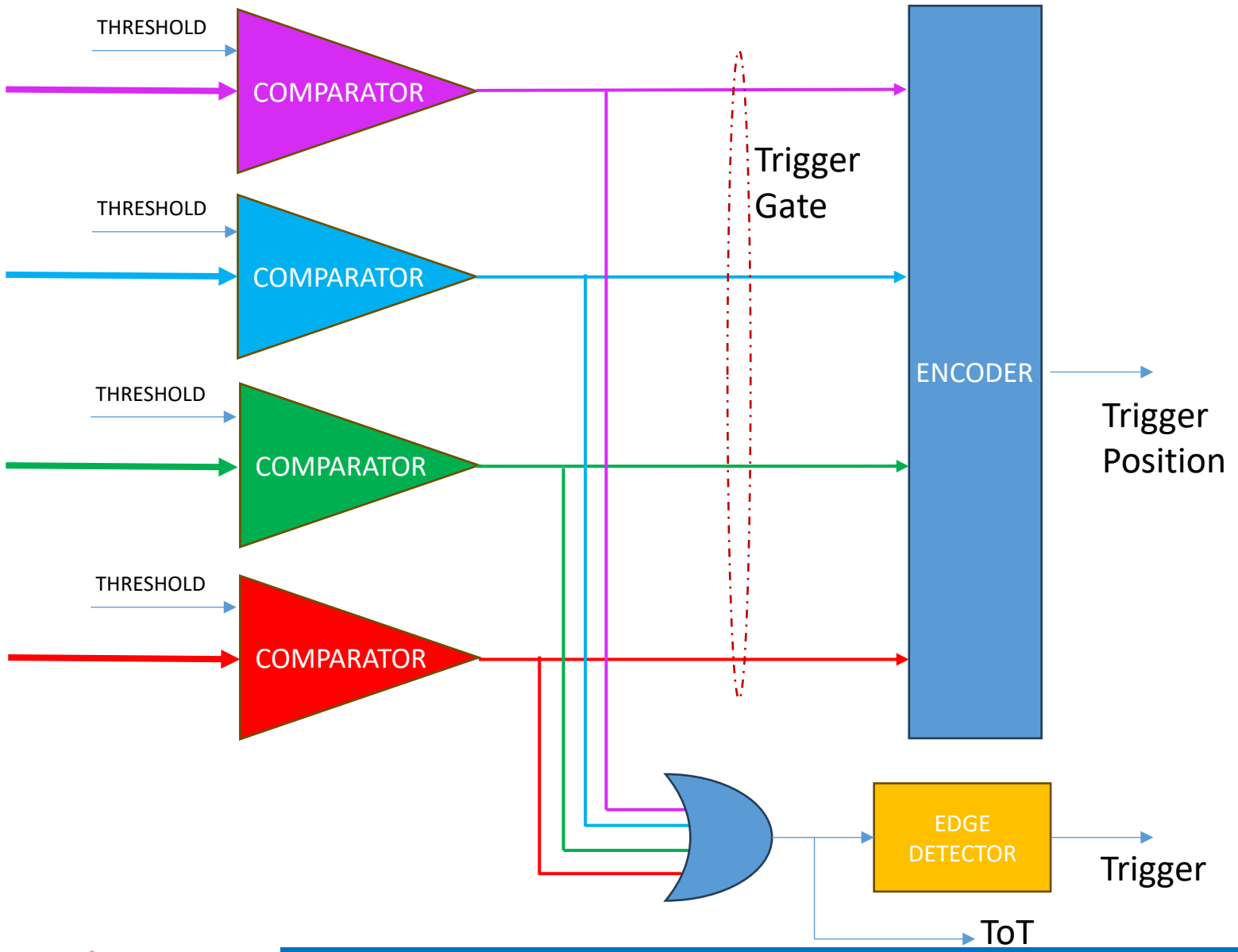




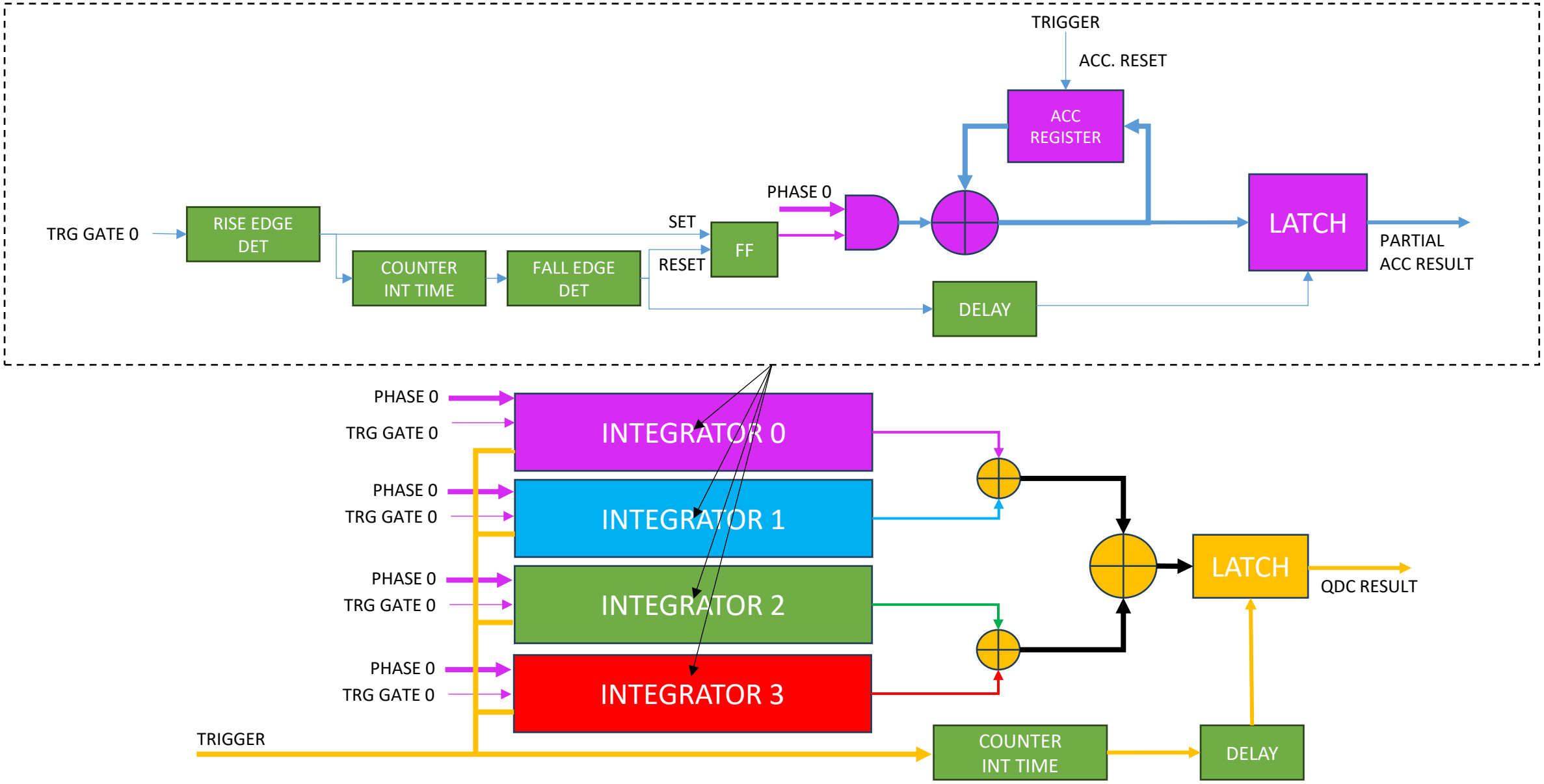




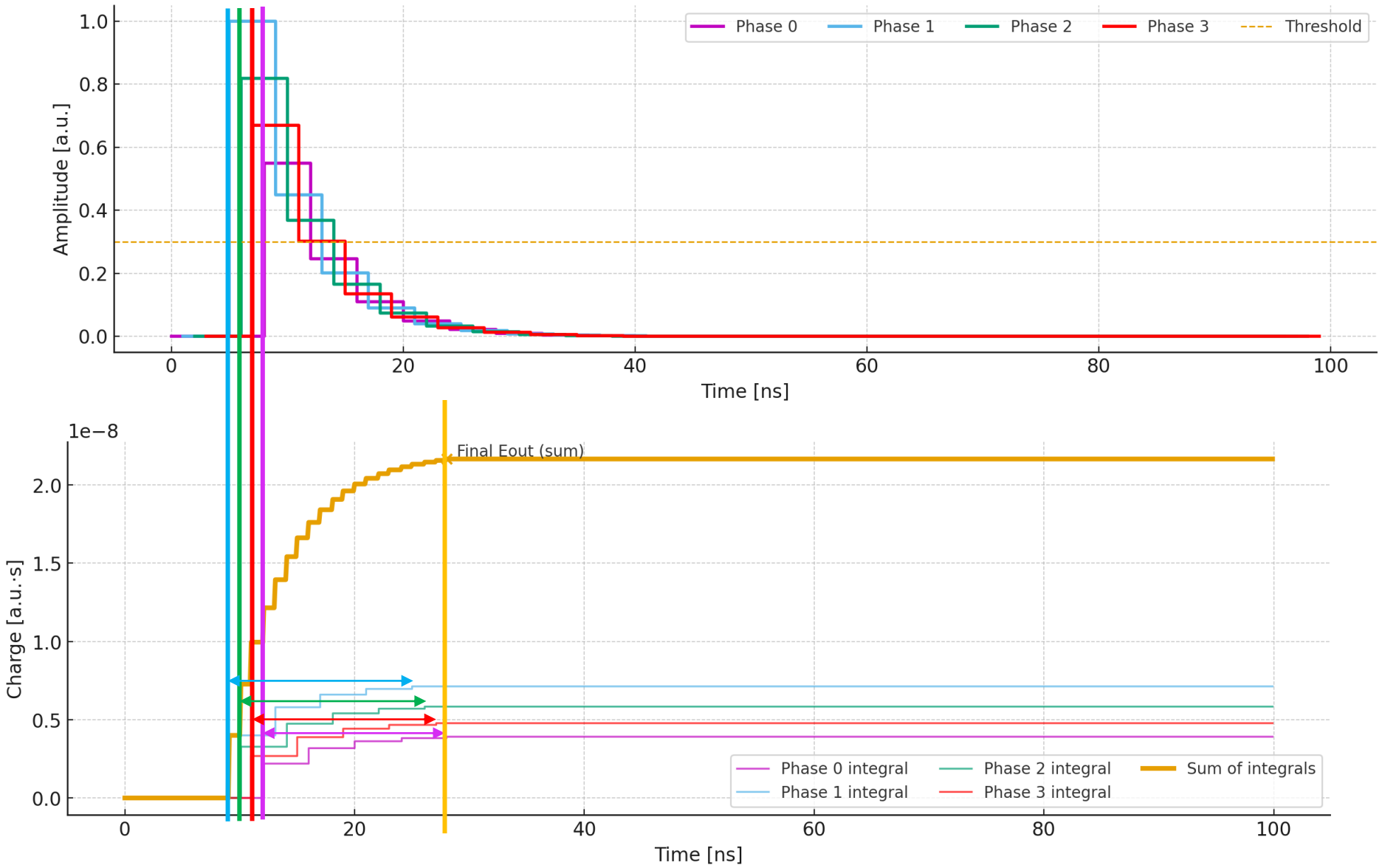
High Speed Digitizer: Parallel QDC implementation



High Speed Digitizer: Parallel QDC implementation



High Speed Digitizer: Parallel QDC implementation



High Speed Digitizer: Parallel trapezoidal implementation

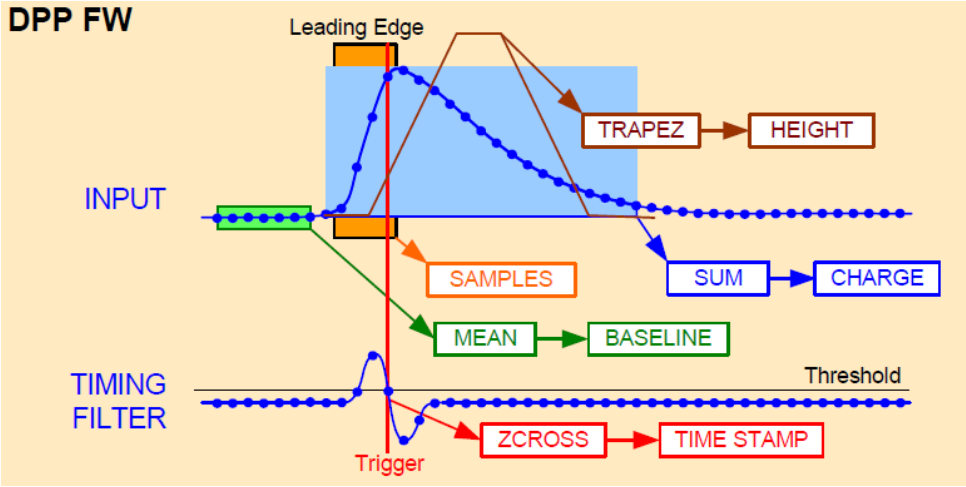
PRE → ADC → FAST SHAPER → ZERO CROSS

ADC → SLOW SHAPER → BASELINE RESTORER

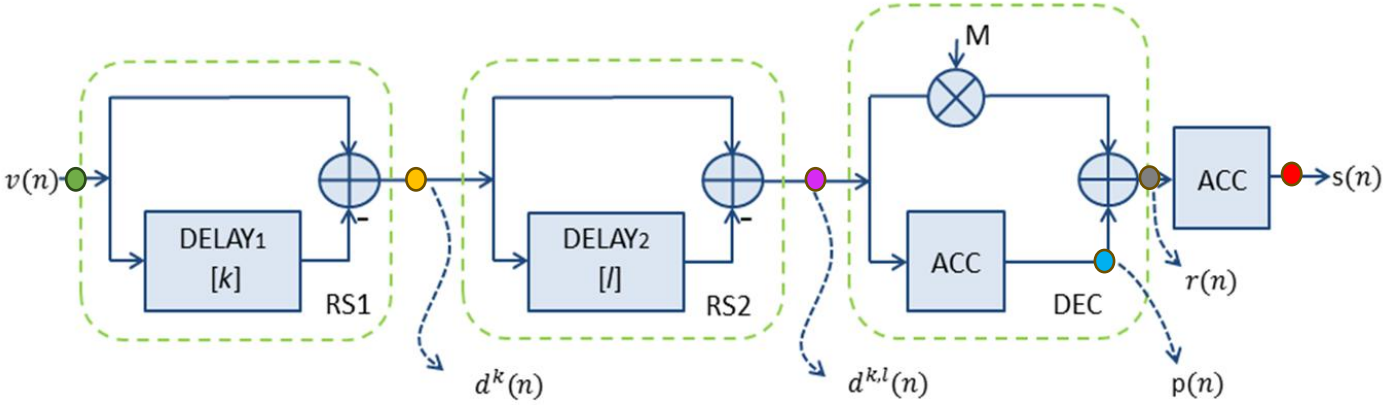
ZERO CROSS → BASELINE RESTORER

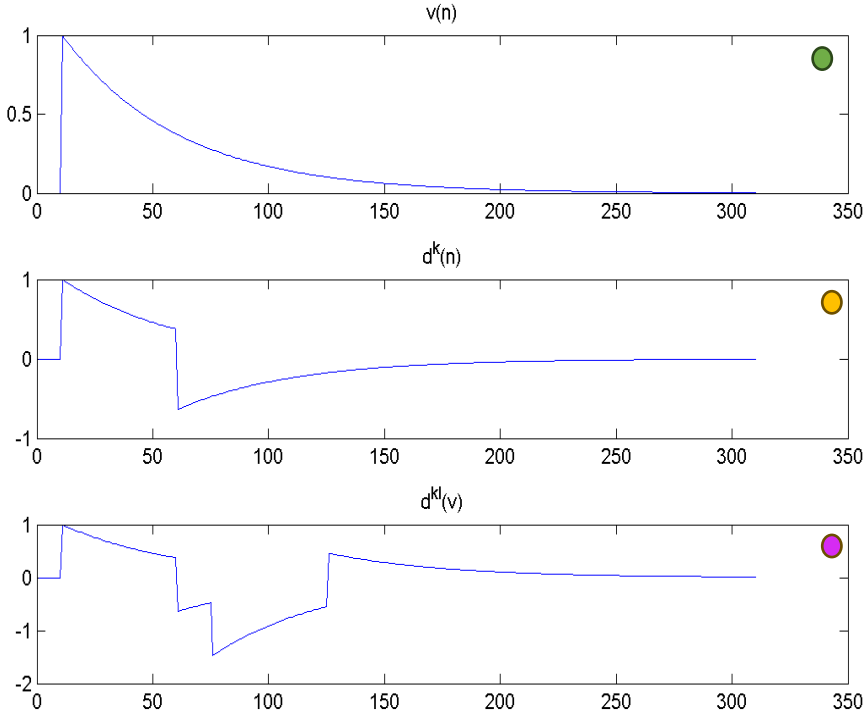
BASELINE RESTORER → - ; SLOW SHAPER → -

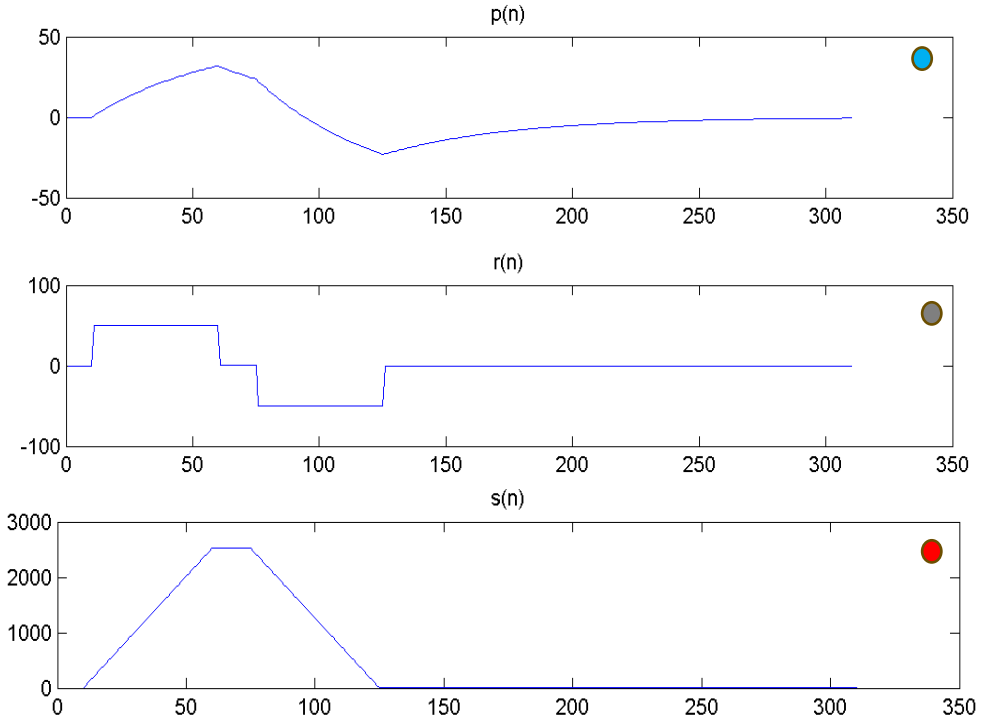
- → ENERGY SAMPLING → SPECTRUM



High Speed Digitizer: Parallel trapezoidal implementation

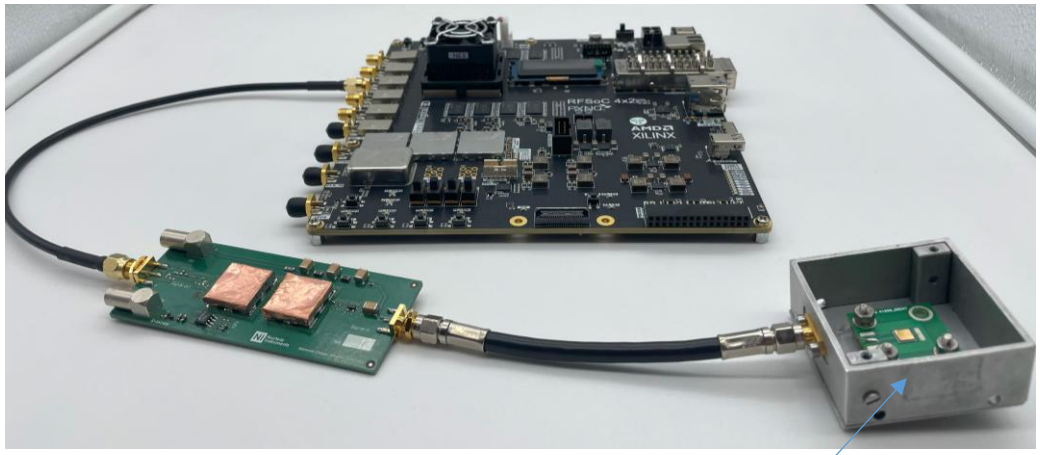




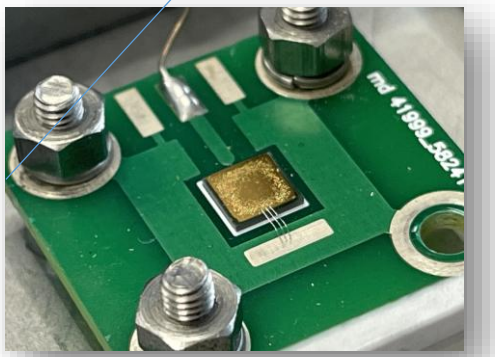


High Speed Digitizer: Parallel trapezoidal implementation

DT9000 → 5 Gsps
upcoming digitizer family



Diamond Detector



High-Energy Physics
•Particle tracking in collider experiments
•Radiation-hard sensors for extreme environments.

Nuclear Physics & Fusion
•Neutron detection and spectroscopy.
•Monitoring of intense radiation fields in fusion reactors.

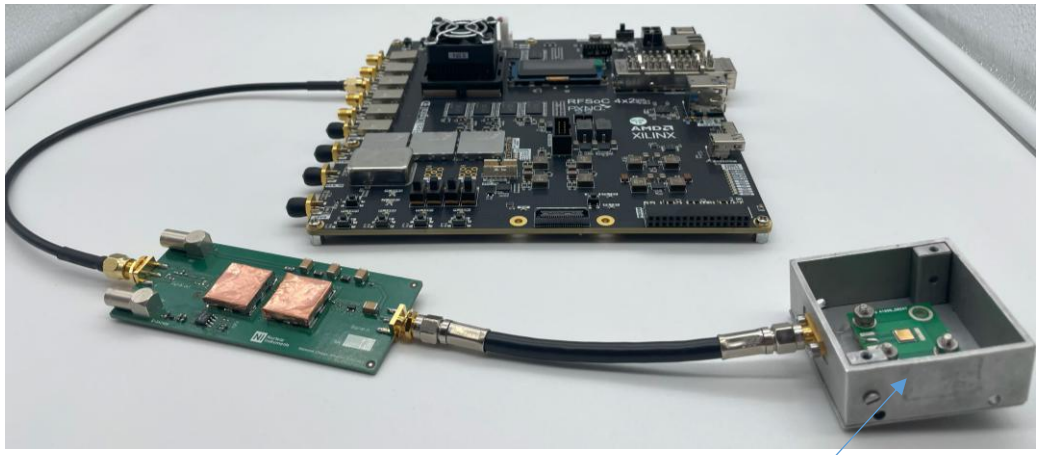
Medical Physics
•Dosimetry for radiotherapy and proton therapy (high precision and radiation hardness).
•Real-time monitoring of therapeutic beams.

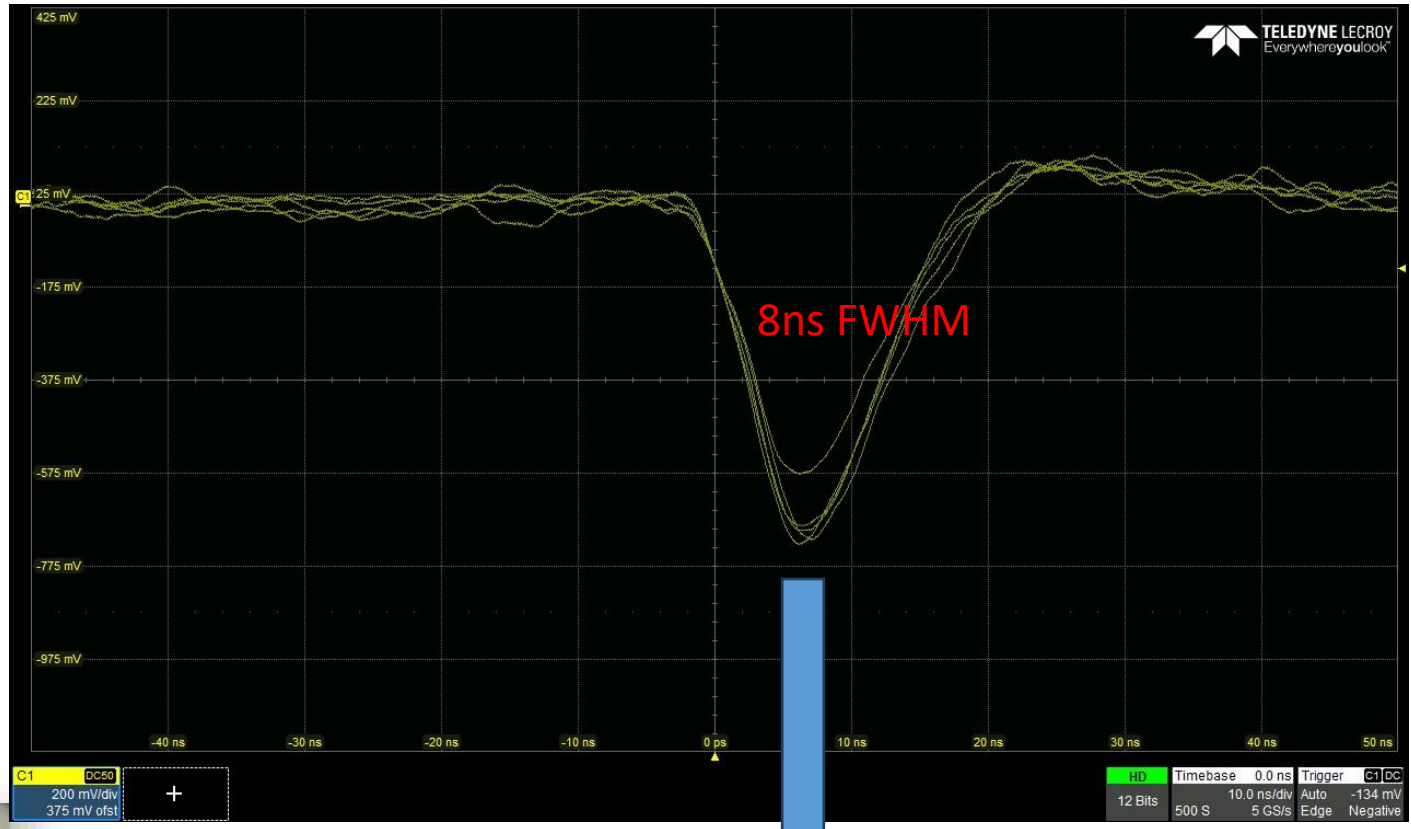
Space & Astrophysics
•Radiation monitoring in satellites and space missions.
•Detection of cosmic rays and solar particle events.

Industrial & Security Applications
•Beam diagnostics in accelerators and synchrotrons.
•Non-destructive testing using radiation.
•Radiation monitoring in nuclear facilities.

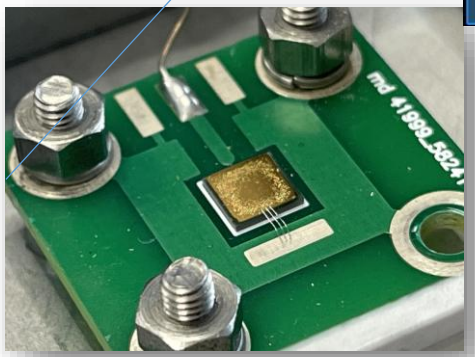
High Speed Digitizer: Parallel trapezoidal implementation

DT9000 → 5 Gsps upcoming digitizer family





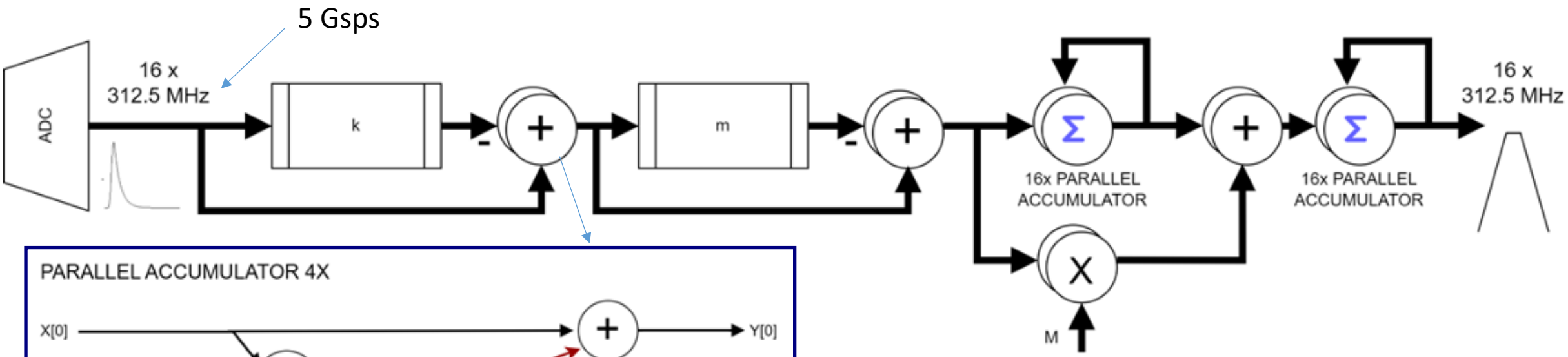
Diamond Detector

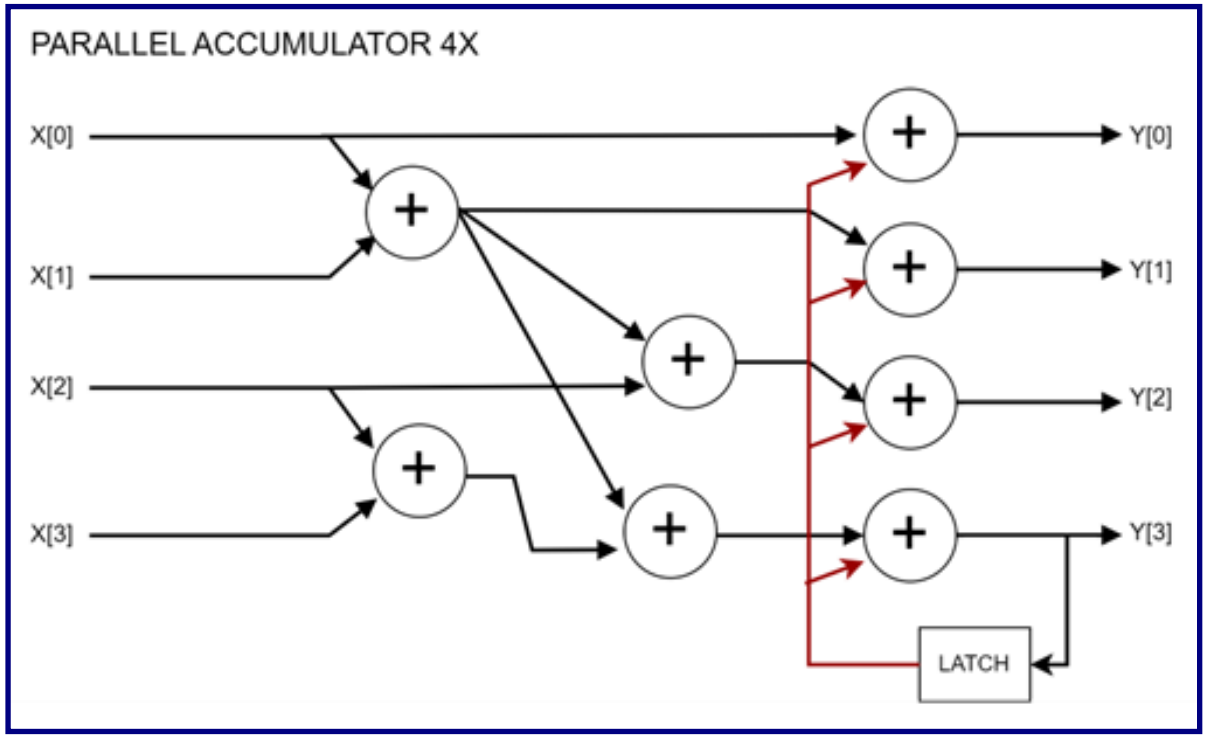


Ultra Fast signal response

Fast digitizer and new processing algorithms

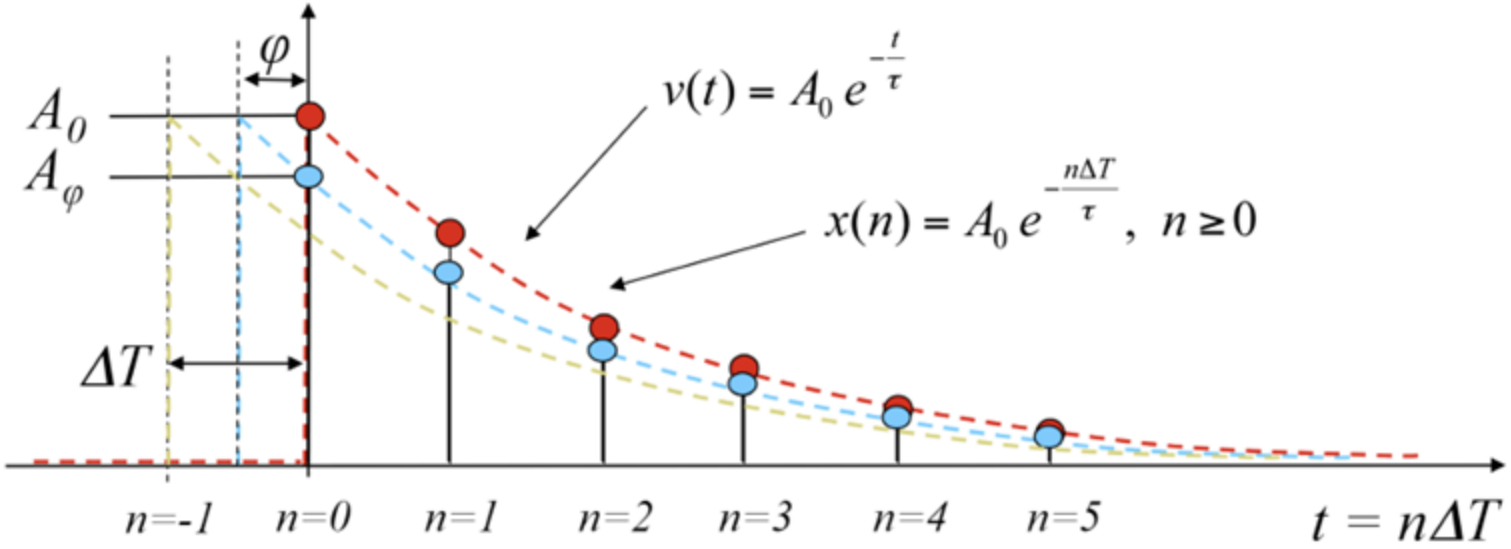
High Speed Digitizer: Parallel trapezoidal implementation



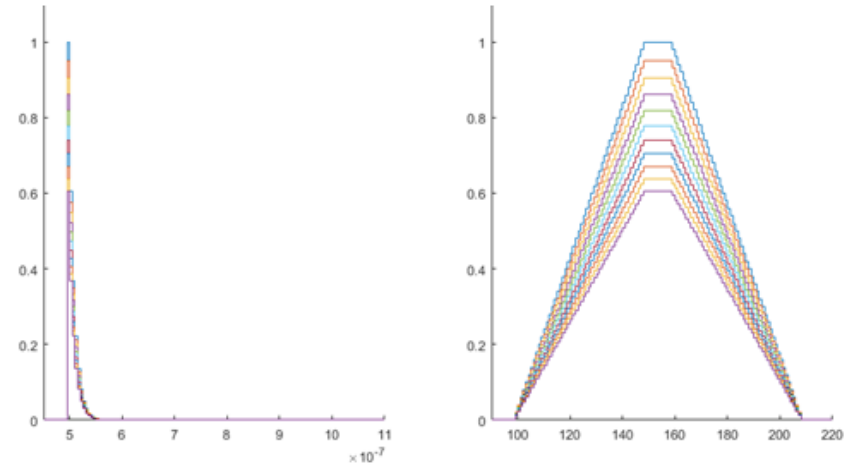


$$Y_0(n) = Y_0(n-1) + X_0(n); \quad Y_1(n) = Y_1(n-1) + s_0(n);$$
$$Y_2(n) = Y_2(n-1) + s_1(n); \quad Y_3(n) = Y_3(n-1) + s_4(n);$$
$$s_1(n) = X_0(n) + X_1(n); \quad s_2(n) = s_1(n) + X_2(n);$$
$$s_3(n) = X_2(n) + X_3(n); \quad s_4 = s_1(n) + s_3(n)$$

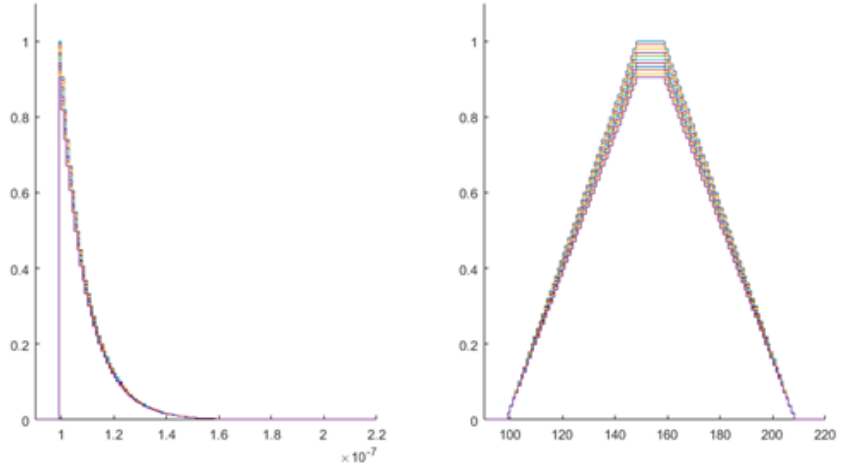
High Speed Digitizer: Parallel trapezoidal implementation



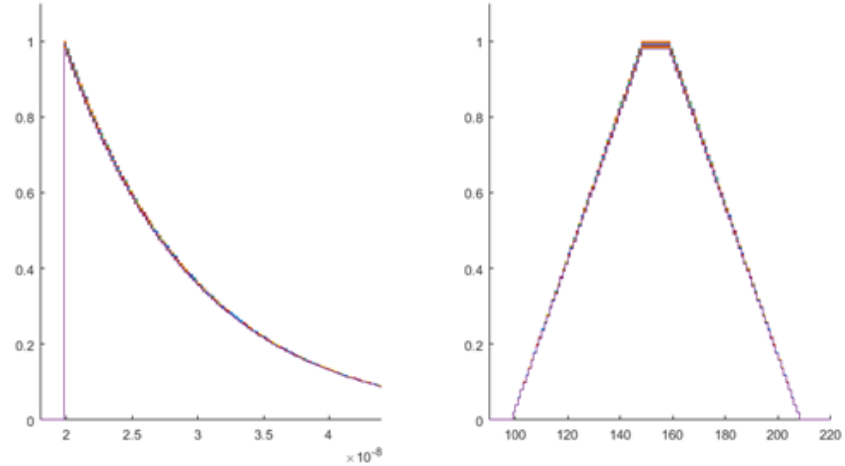
200MHz Sampling Clock



1GHz Sampling Clock

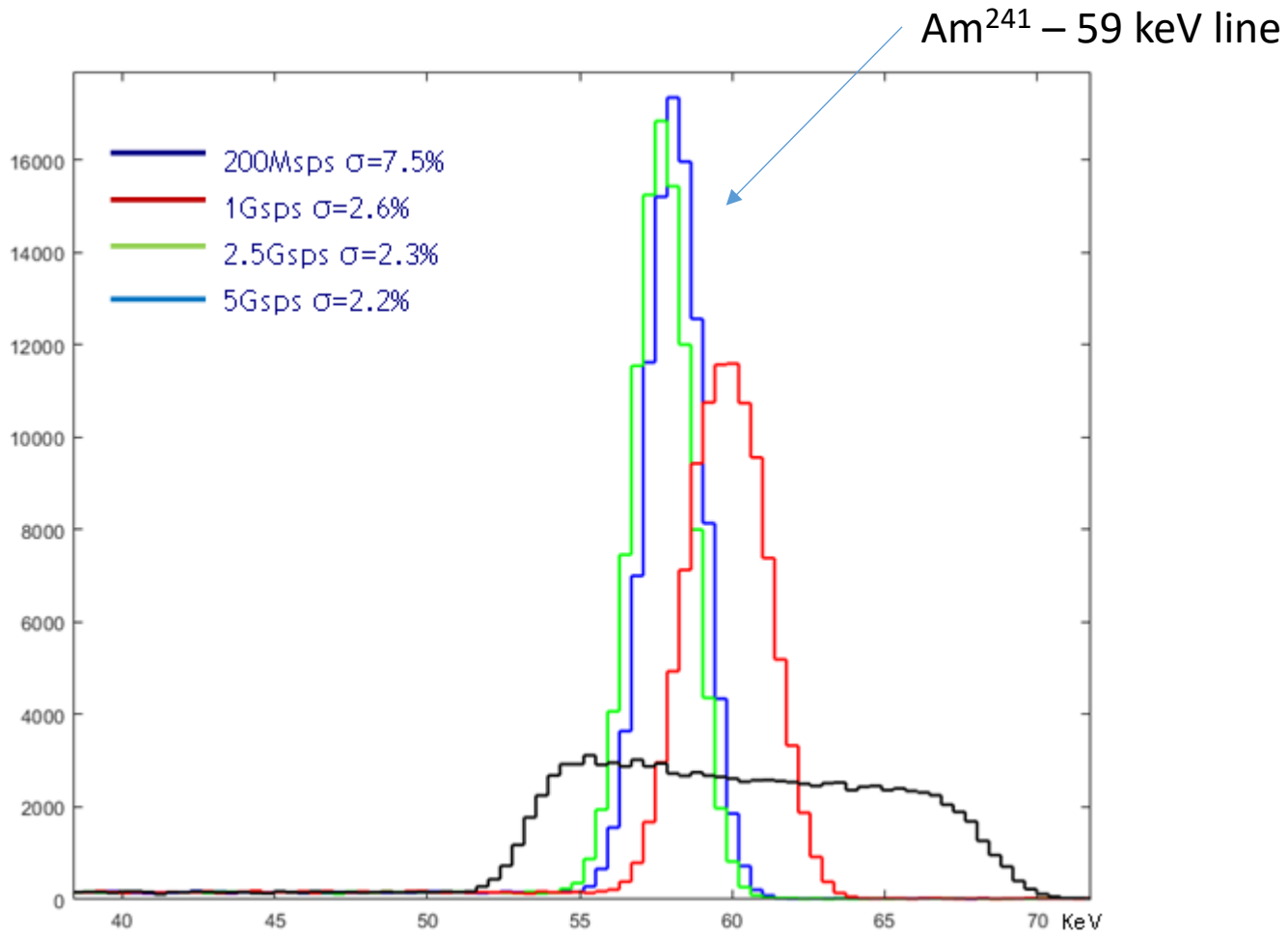


5GHz Sampling Clock

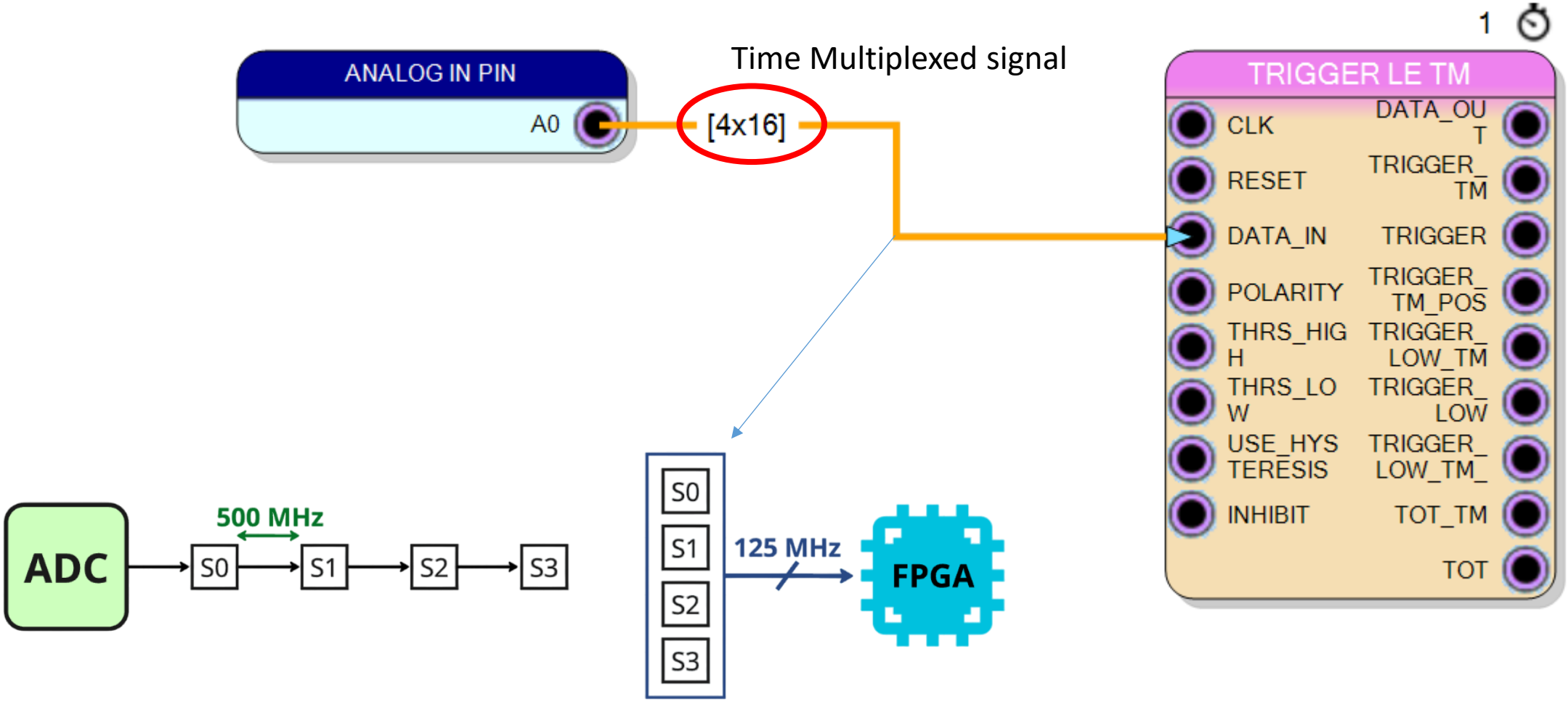


High Speed Digitizer: Parallel trapezoidal implementation

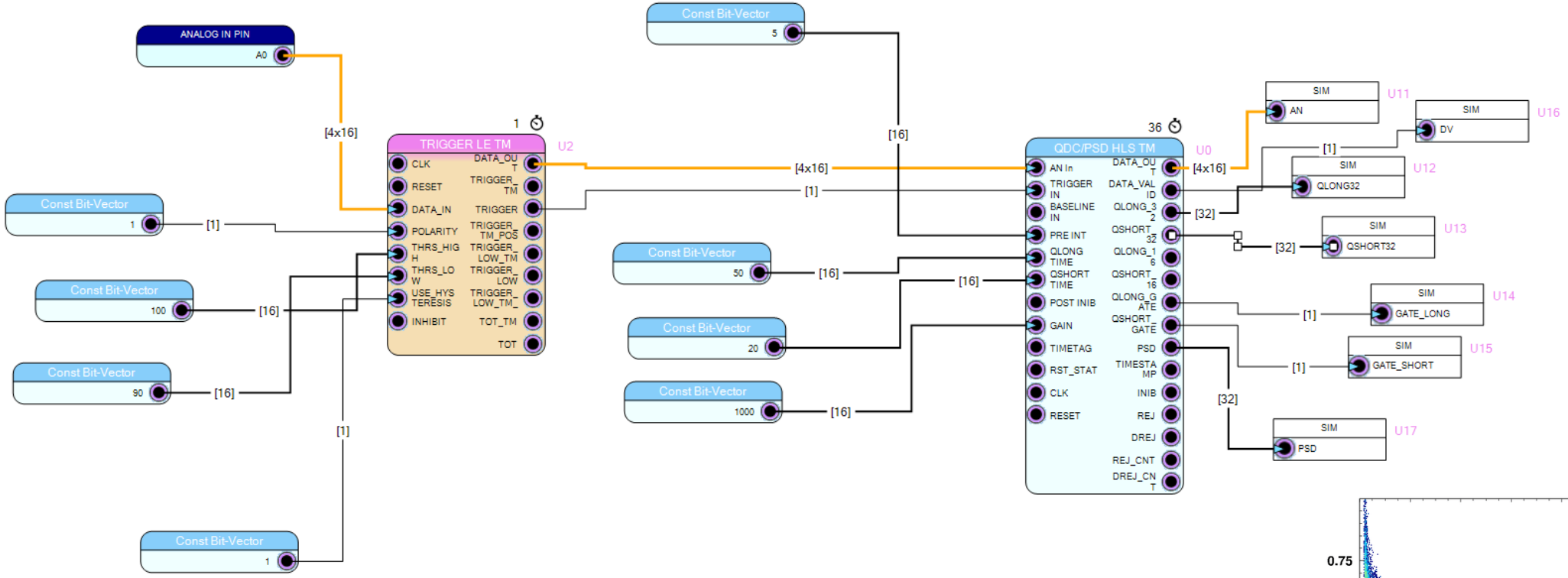
Resolution comparison at different sampling rate and constant shaping time for 20ns decay signal from diamond detector

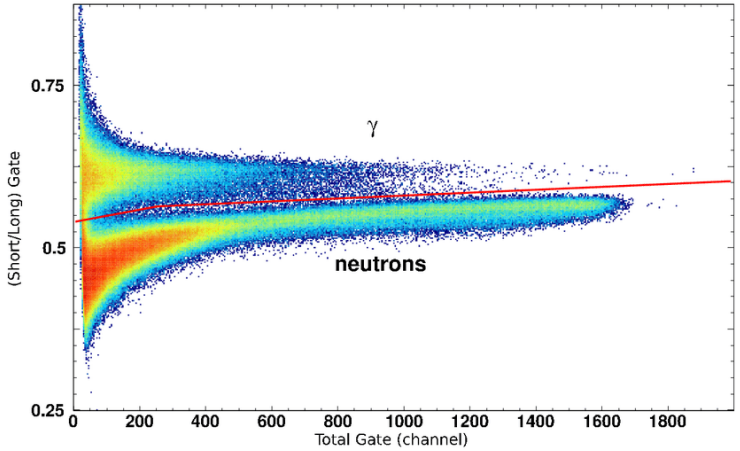


Sci-Compiler TM signals

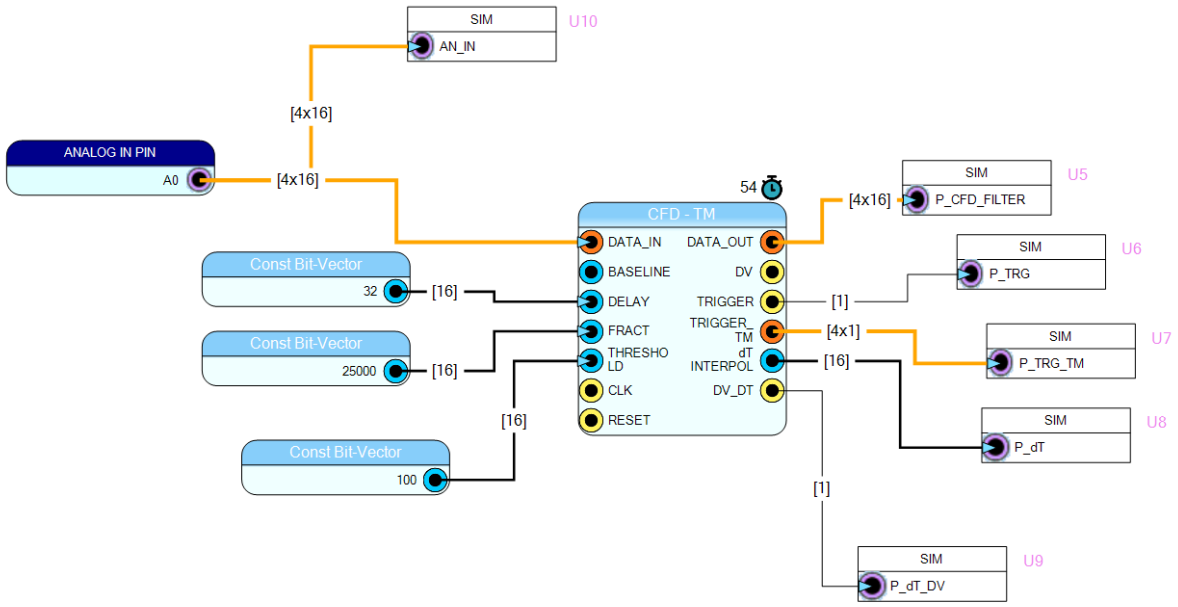


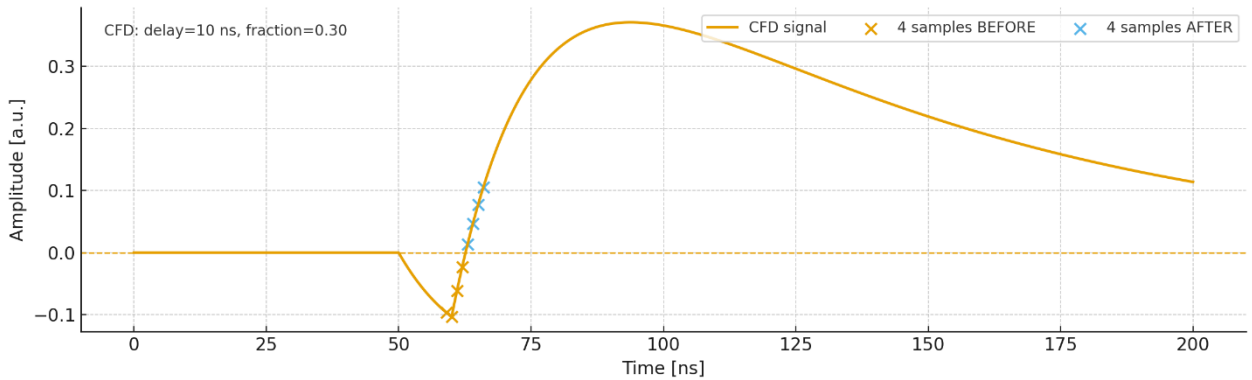
Sci-Compiler TM signals



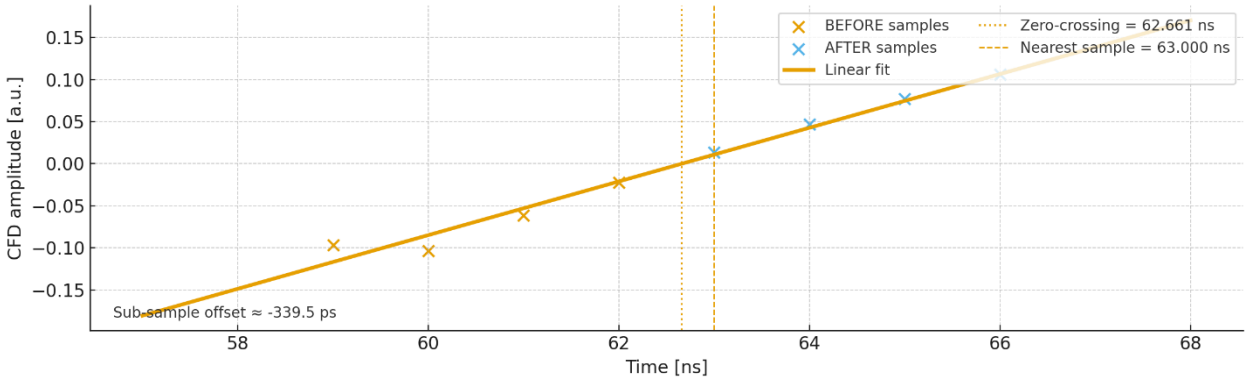


Sci-Compiler TM signals



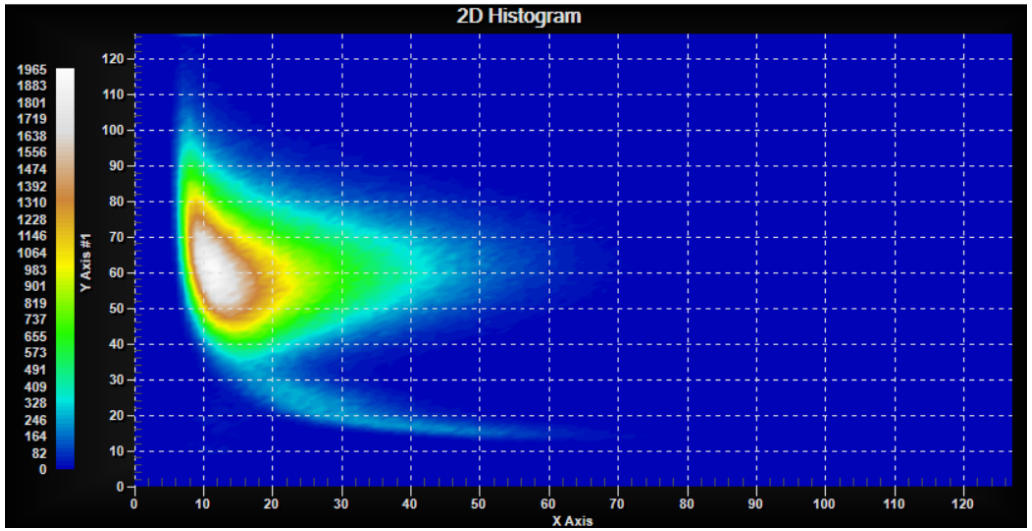


Sub-sample interpolator



(ISIS) Realtime PSD on GS20 scintillator and Nanoparticles detectors

- DAQ 121, 1 GSPS 12 bits Advanced DSP
- Innovative Neutron detectors test beam with good gamma/neutron separation
- Reatime PSD SciCompiler Firmware



Science and Technology Facilities Council

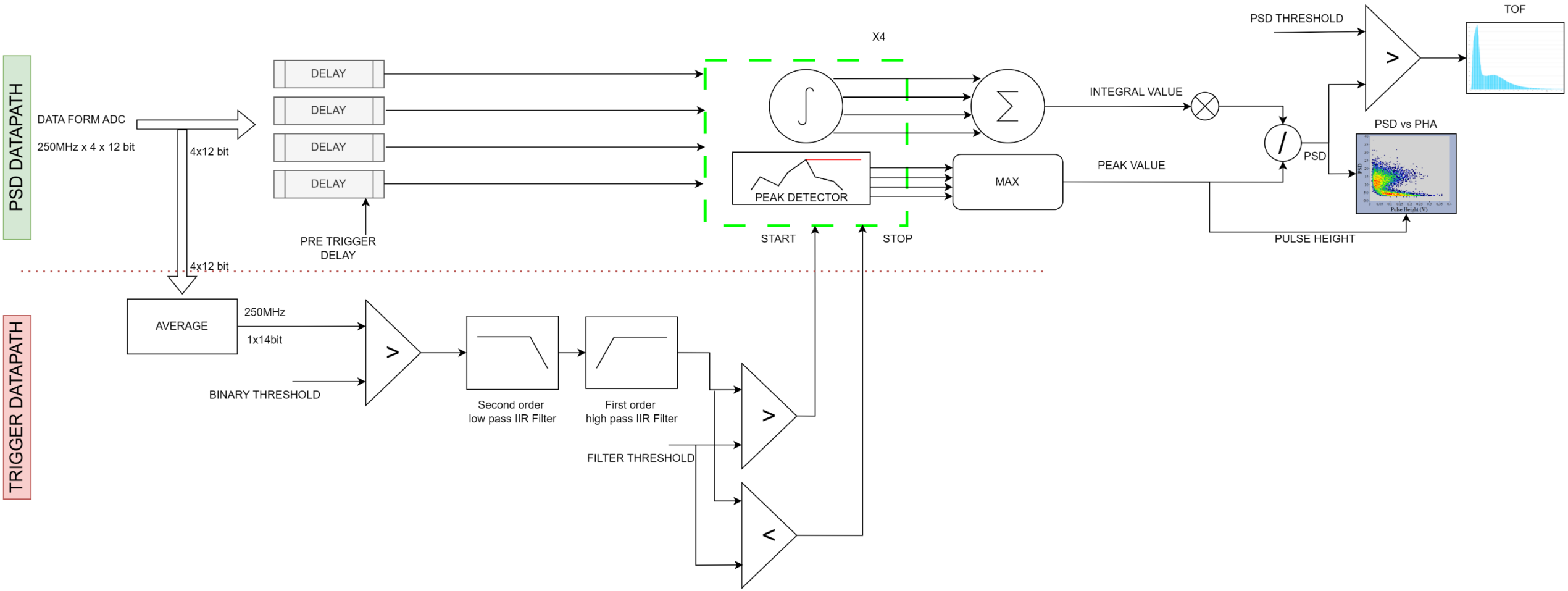
Years of ISIS Neutro and Muon Source

University of BRISTOL

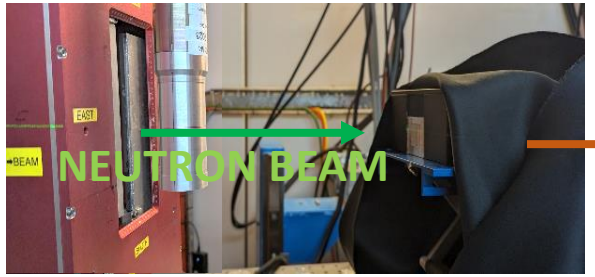
EMAM

Nuclear Instruments

(ISIS) Realtime PSD on GS20 scintillator and Nanoparticles detectors



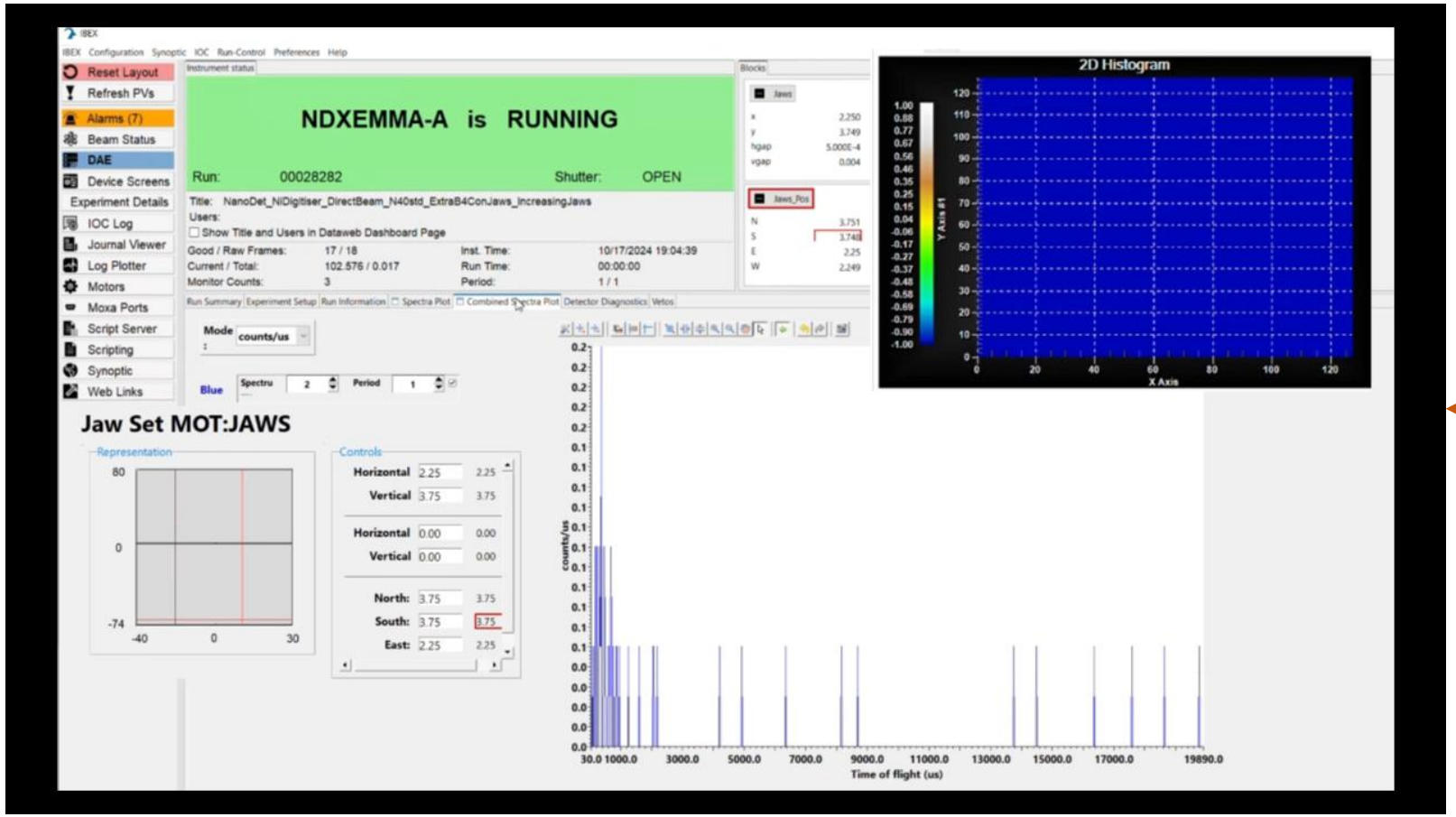
(ISIS) Realtime PSD on GS20 scintillator and Nanoparticles detectors



DAQ 121 Real Time Processor

220 ns Latency
Up to 50 Mcps

ISIS DAE



RFX Neutron Monitor

Scientific goals

- Neutron measurement → direct indicator of fusion reaction rate and fusion power
- Requires accurate **neutron/gamma discrimination (PSD)**

Geometry and installation

- 3 scintillator-based detectors installed below the vacuum vessel.
- Modular shielding: **borated polyethylene (outer layer)** + **lead (inner layer)**.

Scintillators

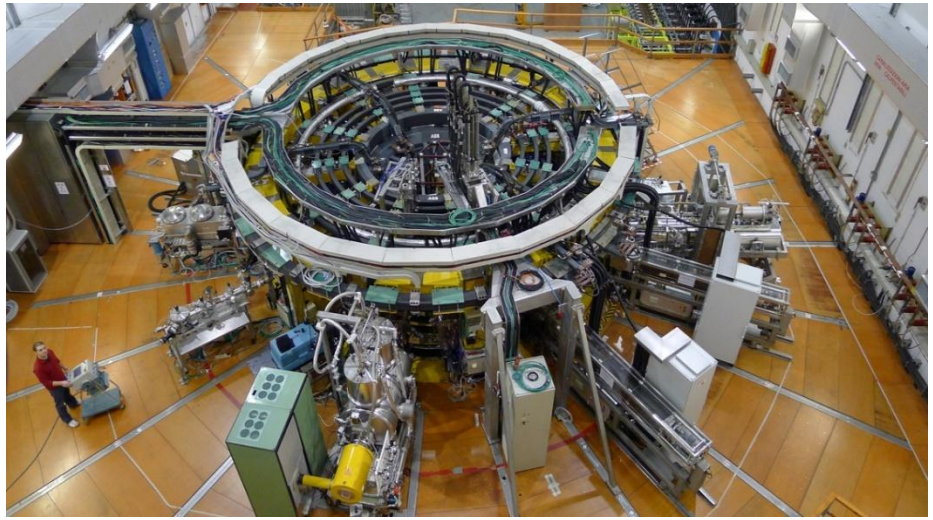
1. **EJ276D** (25×25×100 mm, plastic):
   Fast response, excellent n/γ discrimination.
   Efficient for fast neutrons, but **no spectral information** (H-scattering).
2. **$LaCl_3$** (Ø1” × 1”):
   Provides spectral information (discrete energy peak).
   Fast signals (~50 ns), but **poor n/γ discrimination** → requires advanced algorithms.

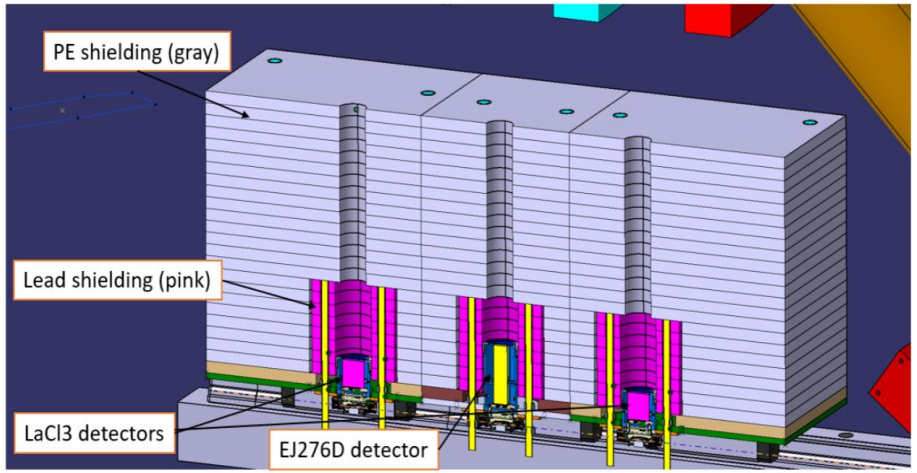
Readout

All crystals coupled to **SiPMs**.

Experimental requirements

Typical discharge: 1 s duration.
Average count rate ~1 kHz, with short spikes (100 µs – 1 ms).
Detectors must follow rapid neutron bursts from **magnetic reconnection events**.





RFX Neutron Monitor

Detector system

- Three scintillator crystals
- Each read by **SiPM arrays (4×4)**
- Arrays divided into **4 groups with 2 SiPM**, summed analogically
- Signals sampled by **NI DAQ121**

Acquisition

- Full waveform readout (128 samples @ 1 ns).

Standard PSD methods

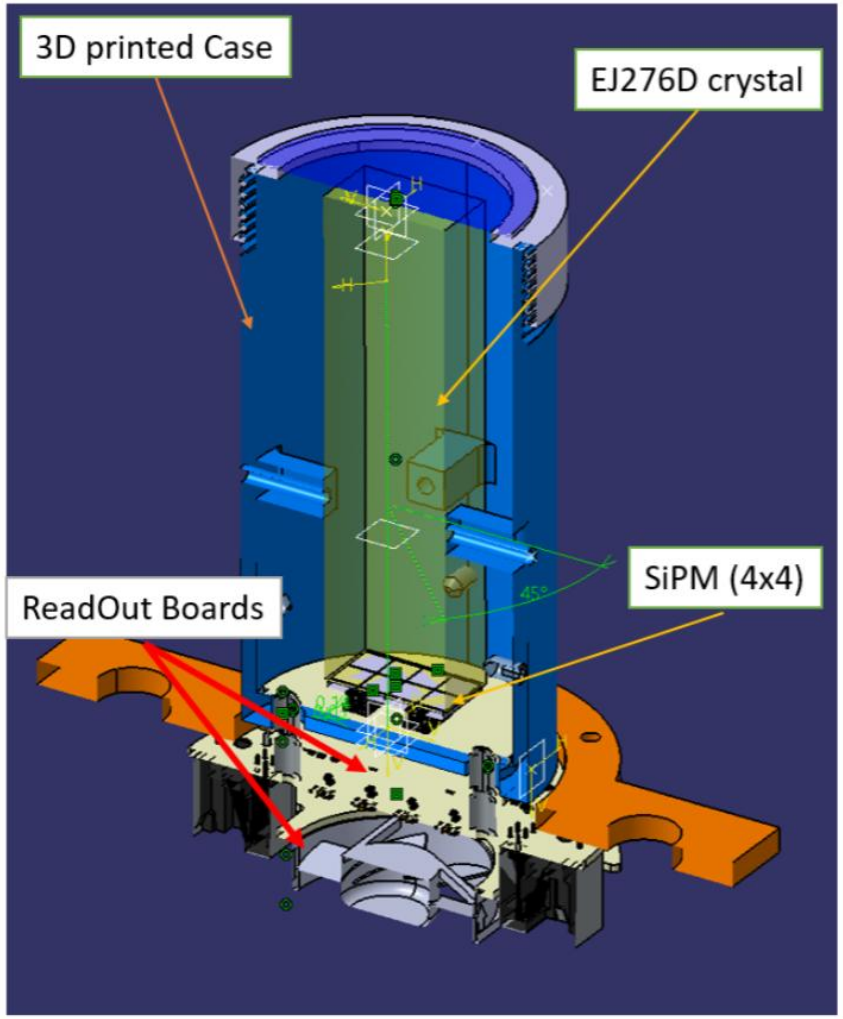
- Traditional n/γ PSD algorithms tested → ineffective for $LaCl_3$.

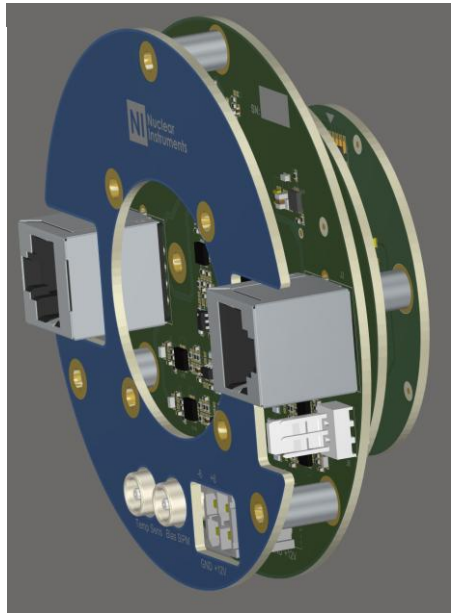
FFT-based method

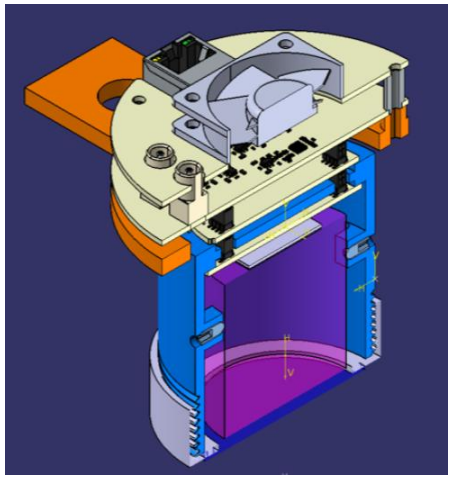
- Compute FFT for each event.
- Evaluate ratio:

$$\Sigma|allharmonics|/\Sigma|aboveN-thharmonic|$$

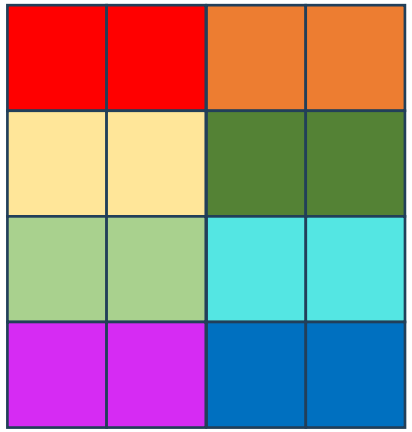
- Provides reasonable separation

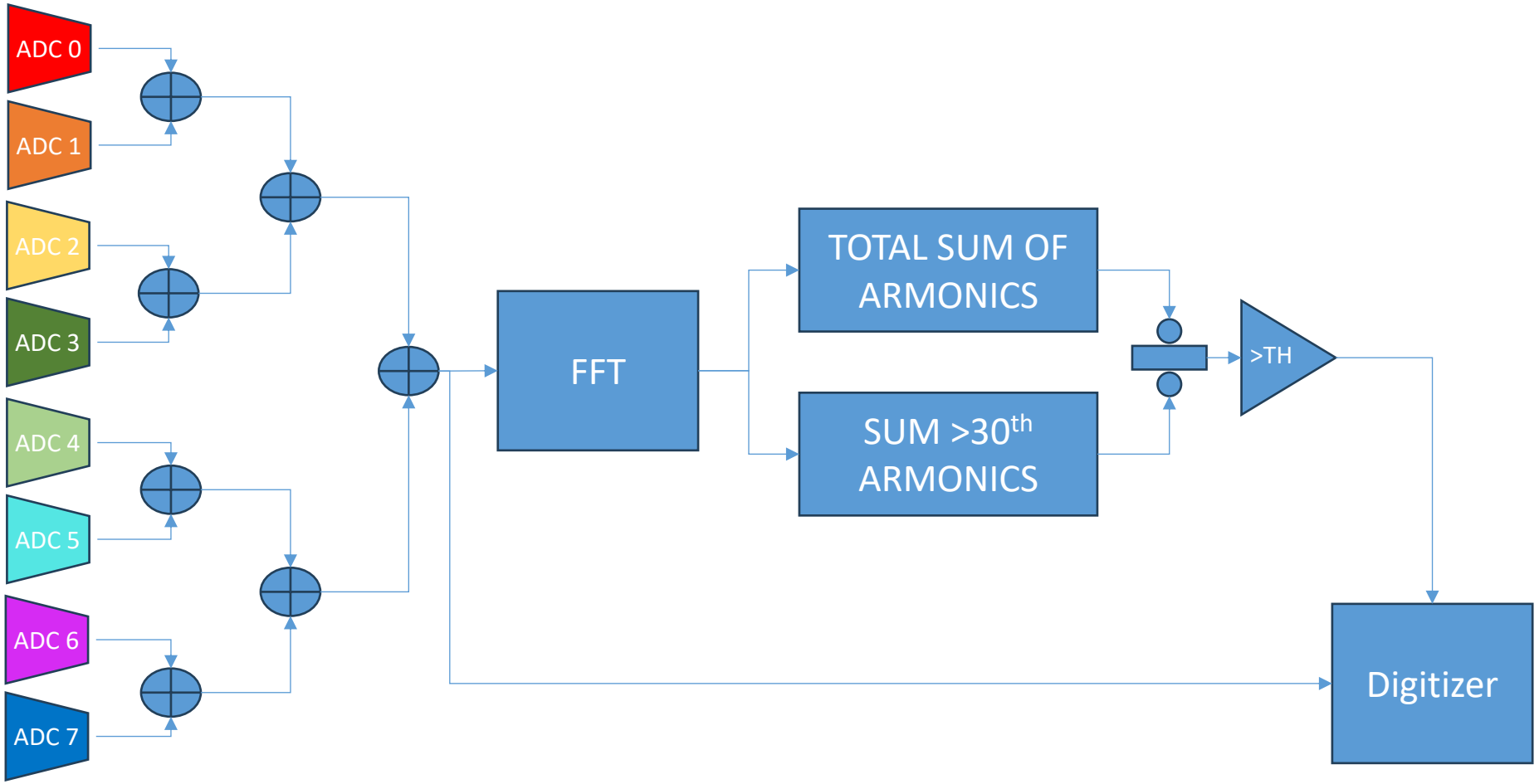






RFX Neutron Monitor: Firmware

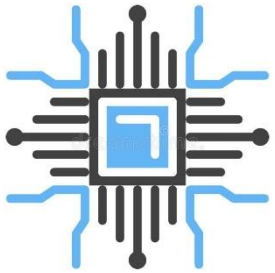




Integrated development system

SCI-COMPILER

Simulate & Generate Firmware

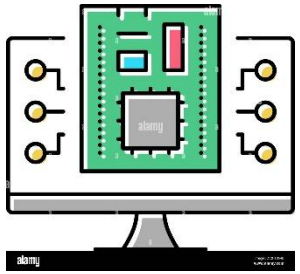


RESOURCE EXPLORER

Visual Firmware Debug

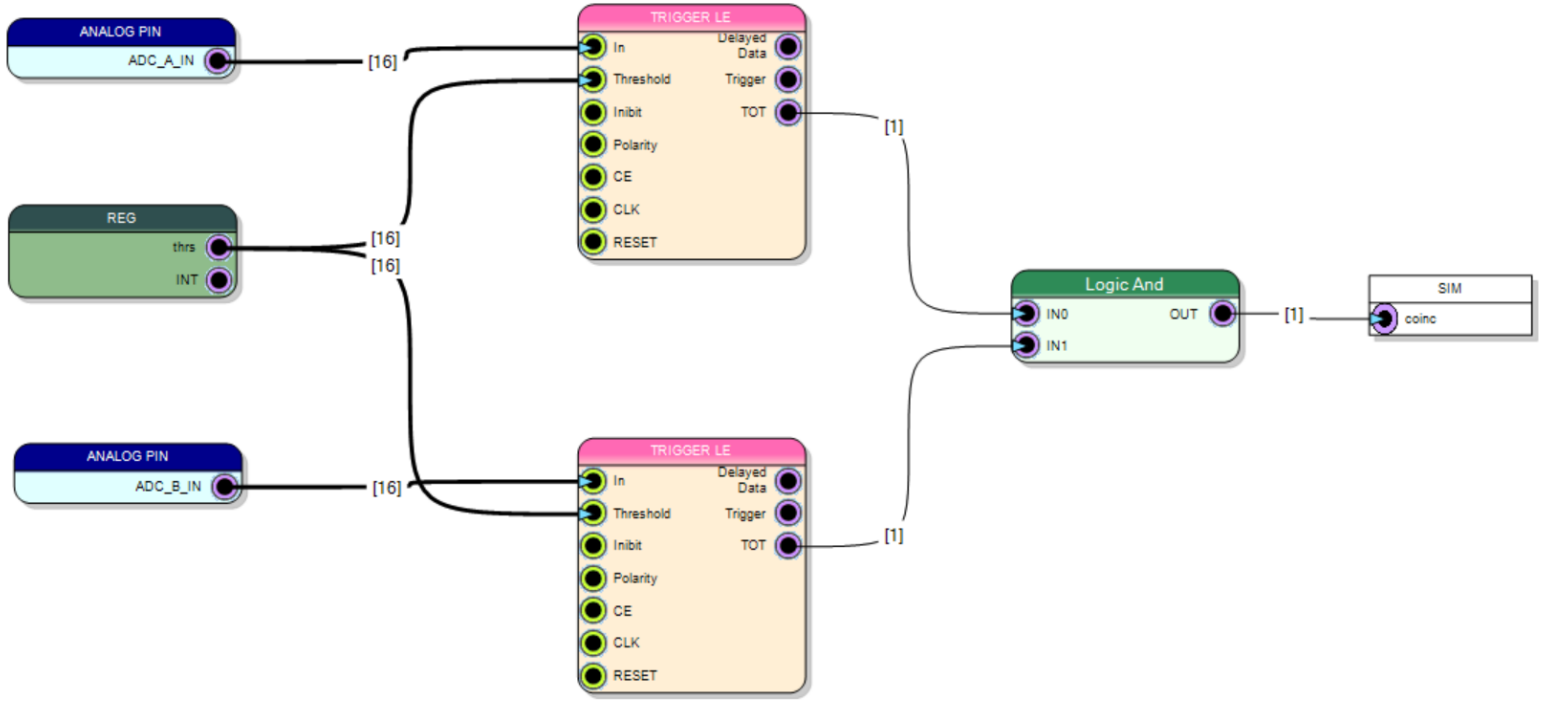
SCI-SDK

Data Readout

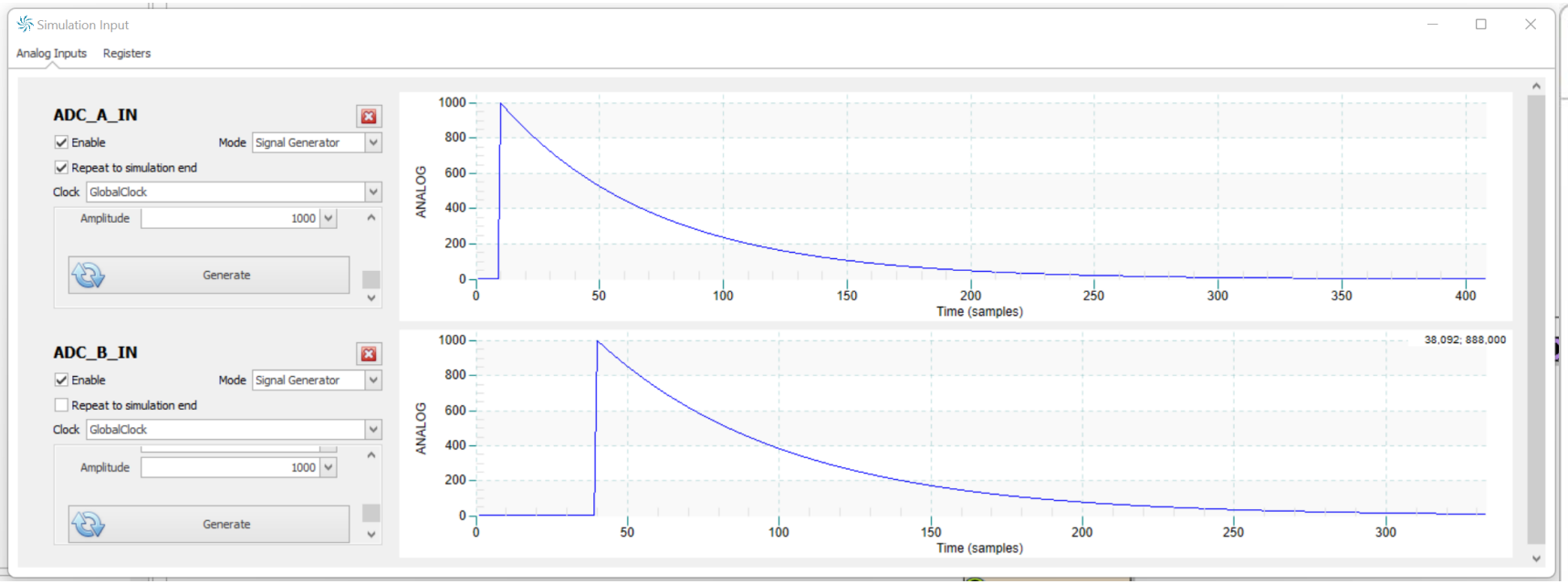


Integrated simulation

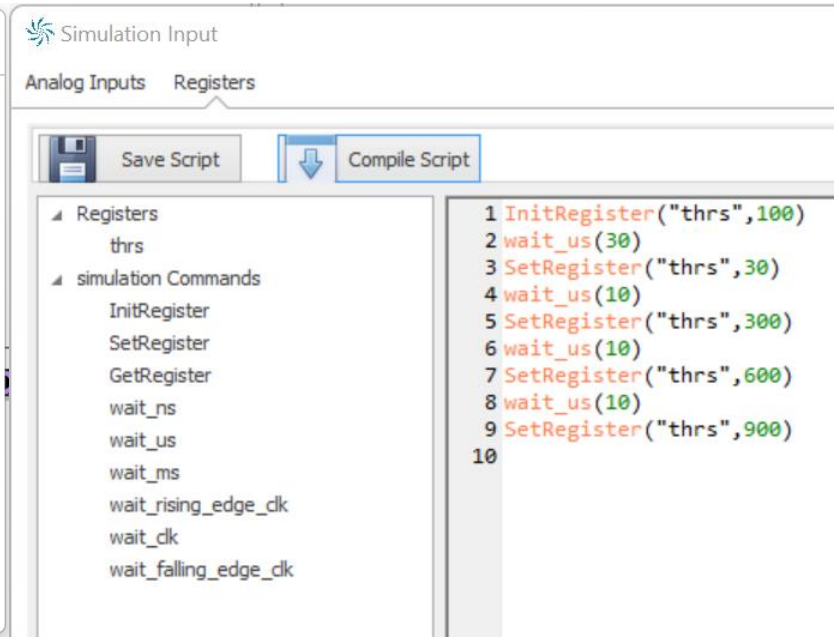
- Save your time → Compile can require hours, simulation few seconds
- Simpler debug → You can inspect any net and signal
- Better test coverage → You can insert critical signal to check how firmware perform



Integrated simulation

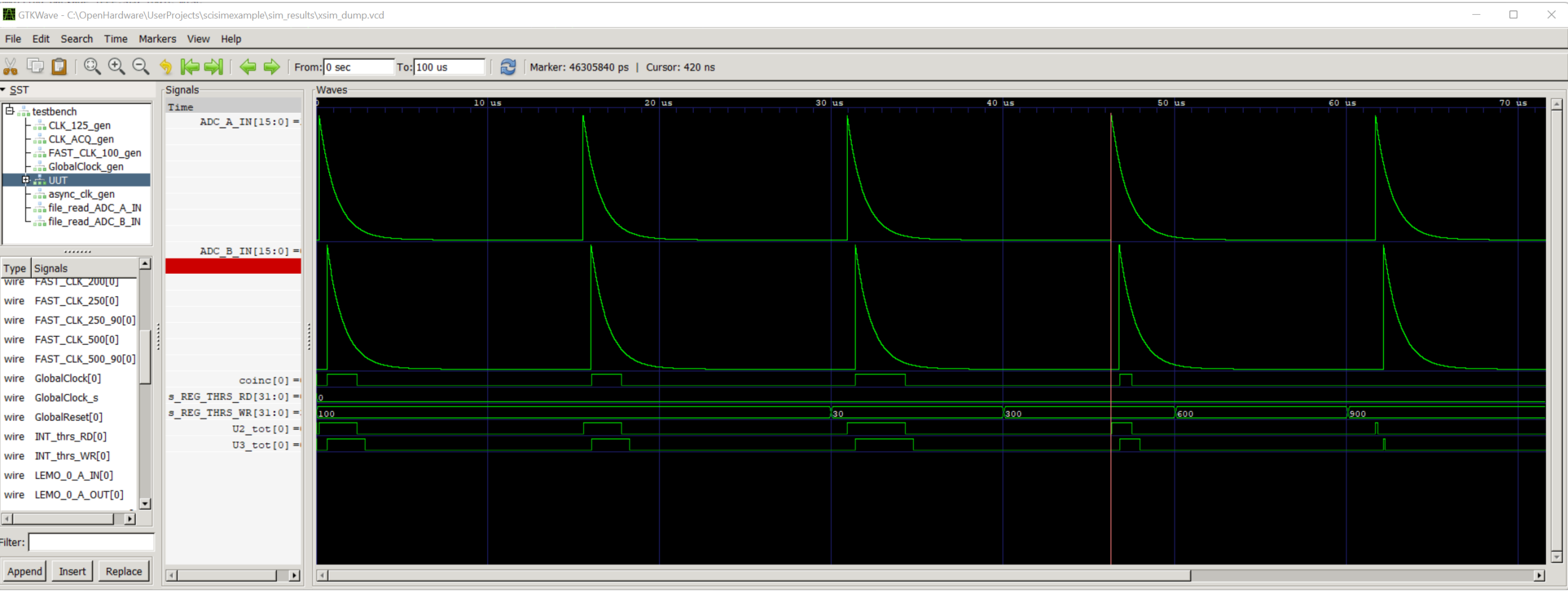


Generate analog signal to replace ADC data stream

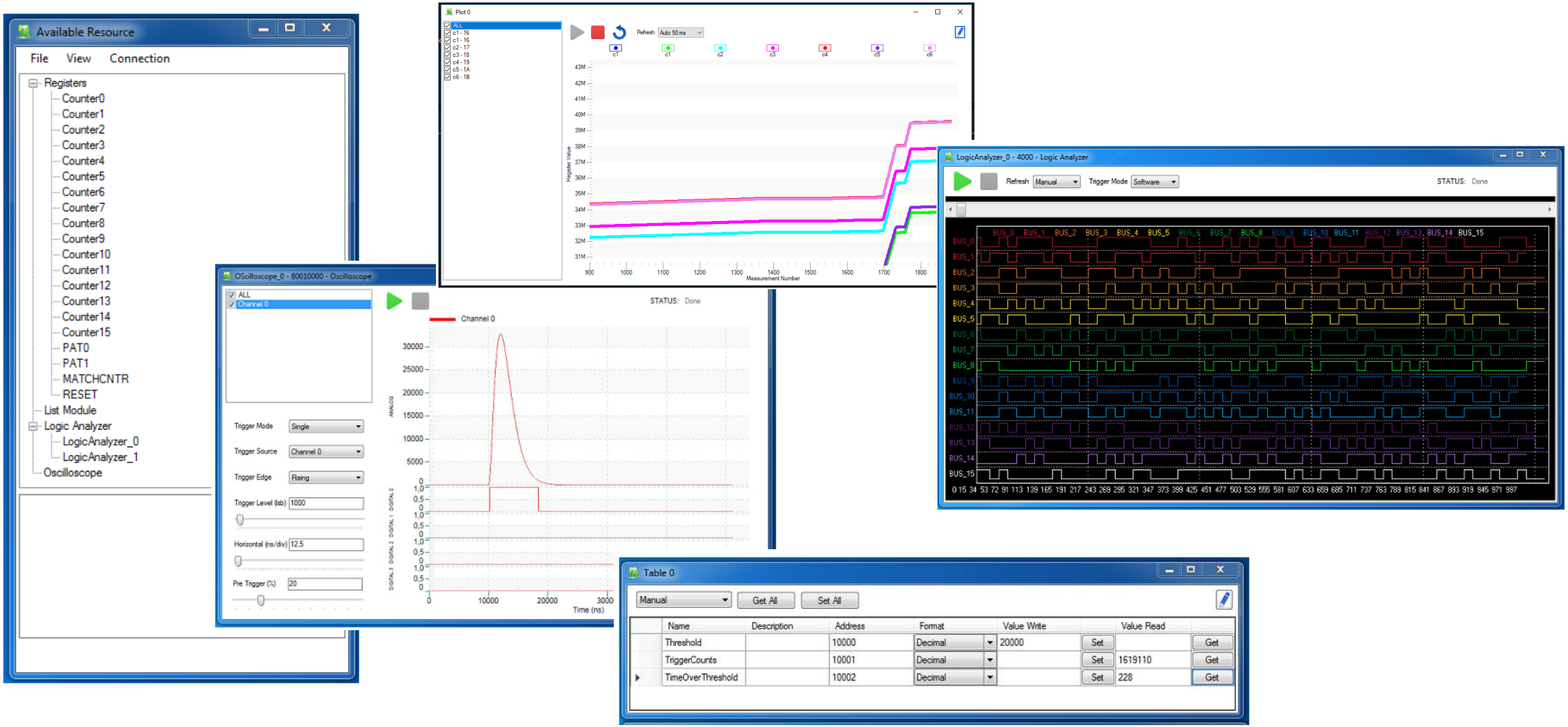


Write script to simulate Register RW

Integrated simulation



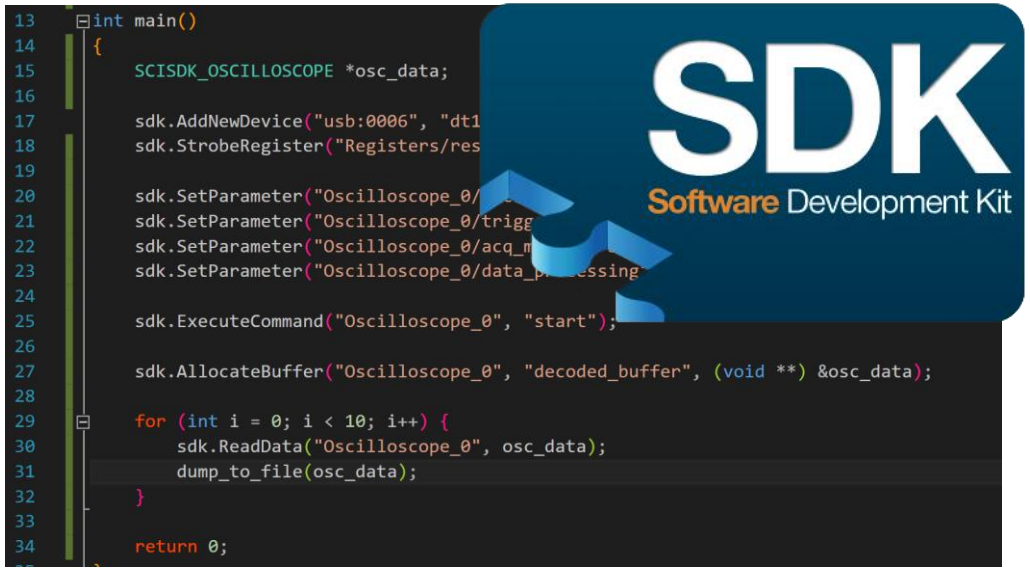
Resource Explorer: Debugging tool



SCI-SDK: Multi-platform device indipendent readout library

Available open source on GitHUB

https://github.com/NuclearInstruments/SCISDK



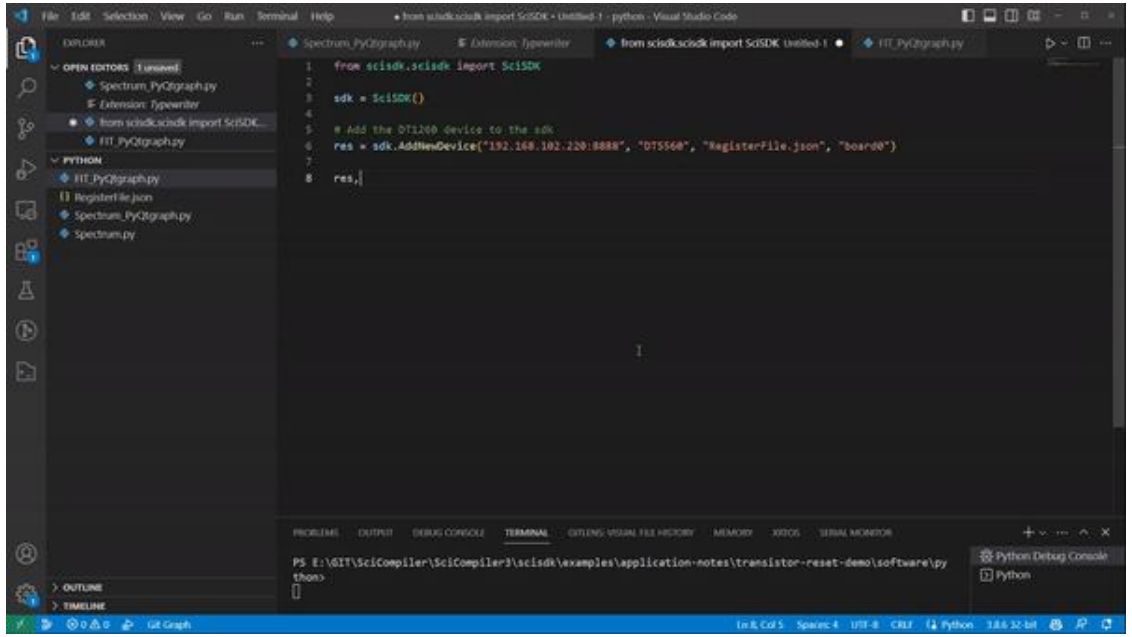
Works on: Windows, Linux
Compatible with Raspberry PI

Available on: PIP, NPM, and APT (for Ubuntu) and ANT (java)

Works inside Jupyter Lab, pre installed on new instruments

Documentation and examples available here:
https://nuclearinstruments.github.io/SCISDK/

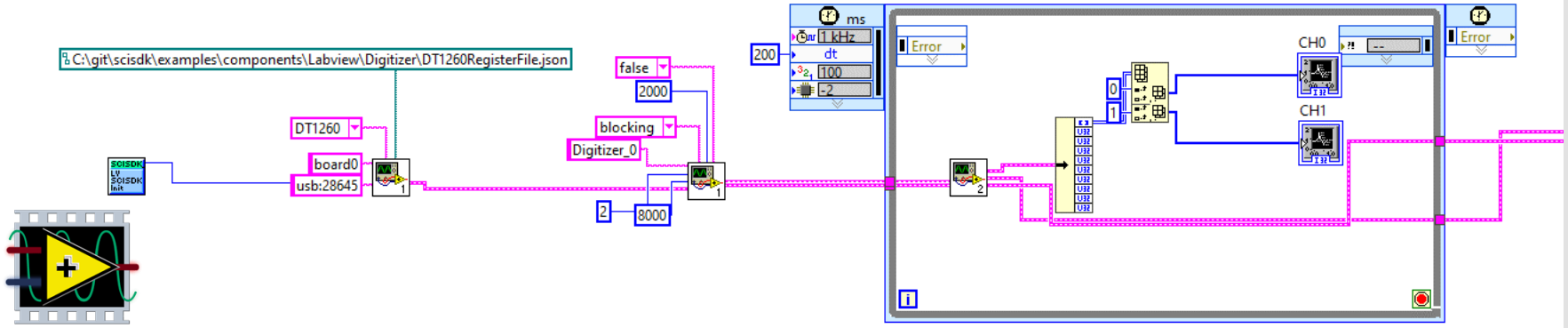
SCI-SDK: Multi-platform device indipendent readout library



python™

Just enter in your terminal to start using SciSDK

pip install scisdk



LabVIEW

SCI-SDK: Multi-platform device indipendent readout library

Board0

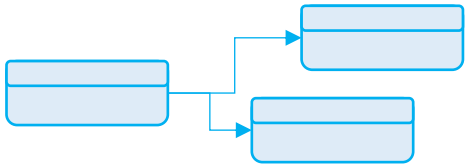
Board1

Board2

SCI-SDK

```
sdk.ReadData("board0:/Oscilloscope_0")
sdk.ReadData("board1:/Spectrum_0")
```

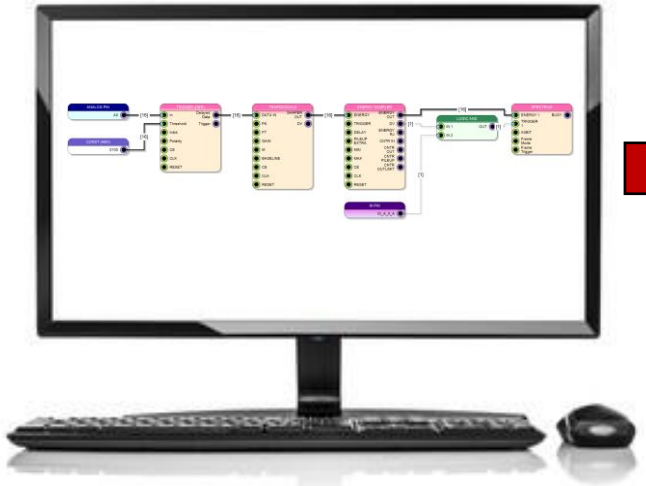
Remote Compile Service based on My SCI-Compiler Cloud

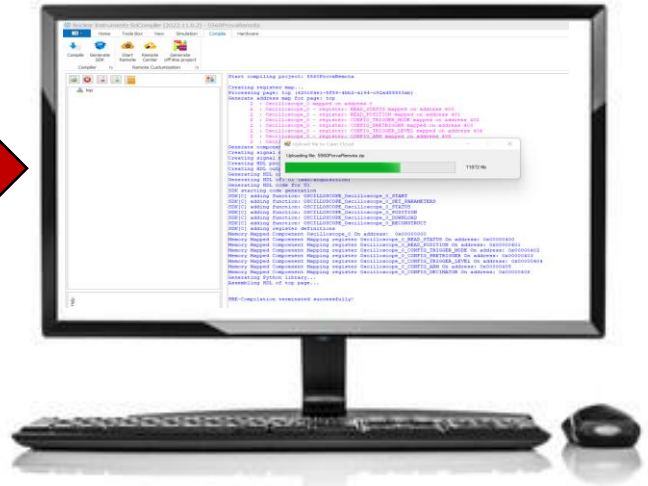


Design entry with SciCompiler

Upload project on the cloud

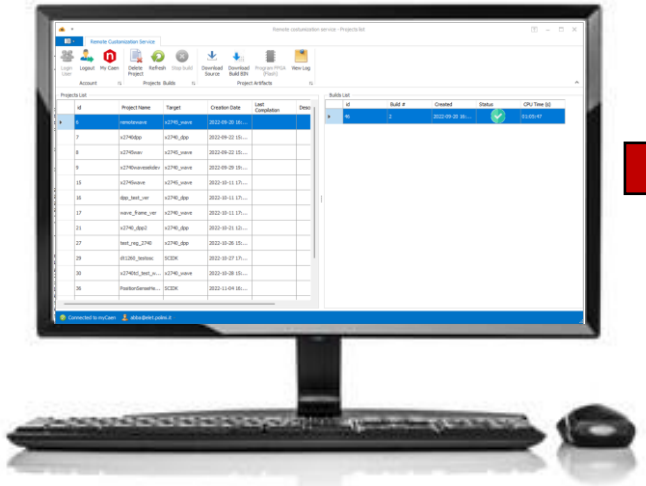
Remote Compile on MyCaen

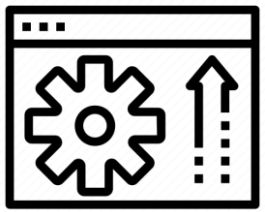




Remote Compile Service based on My SCI-Compiler Cloud

Download the firmware compiled





Install the firmware on the device

Nuclear Instruments

DAQ121 – 1 Gsps 32 channels – 12 bit
DAQ122 – 1 Gsps 32 channels – 14 bit

(COMPATIBLE WITH ESS & ISIS READOUT)