

ALCOR: a mixed-signal SiPM readout ASIC for Cherenkov and cryogenic detectors



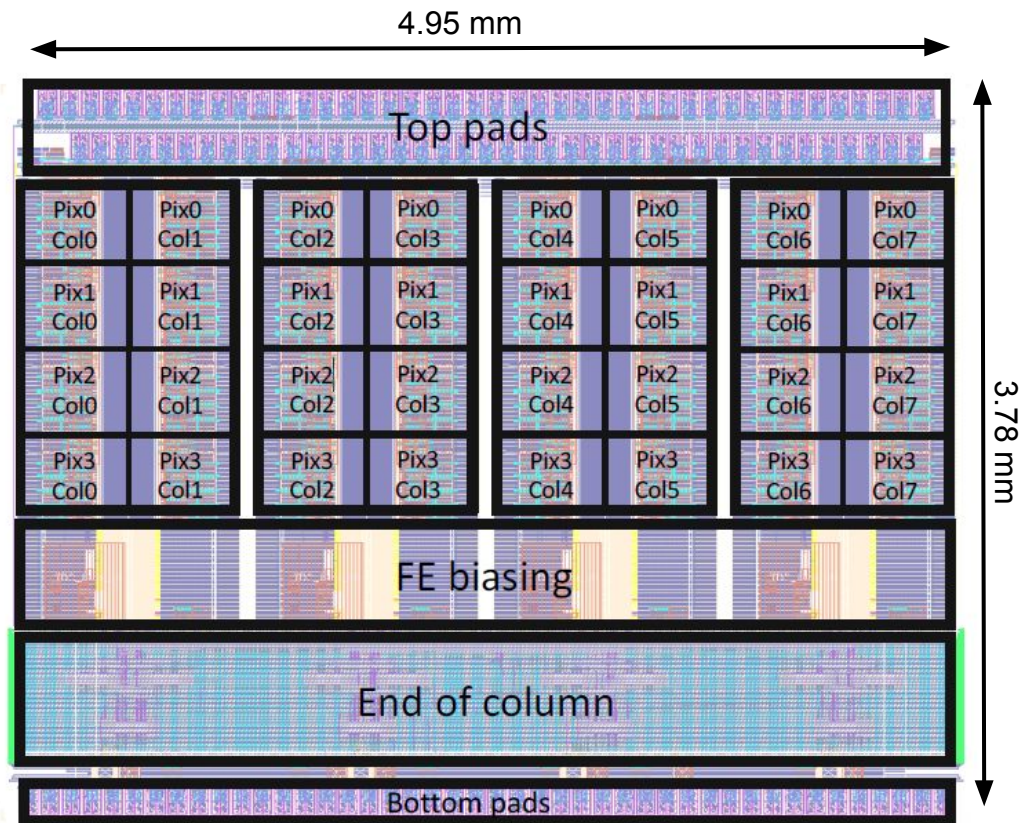
Fabio Cossio on behalf of the ALCOR group - INFN Torino

IFD 2025 - INFN Workshop on Future Detectors
Sestri Levante, 18 March 2025

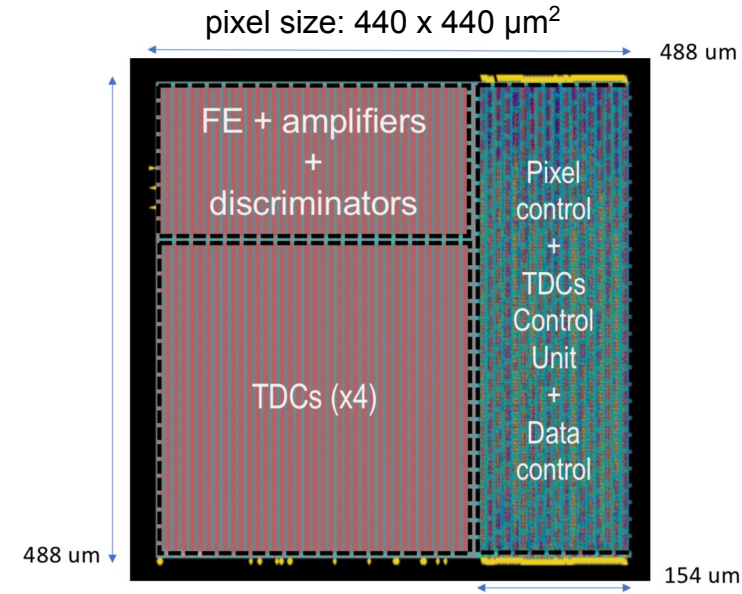
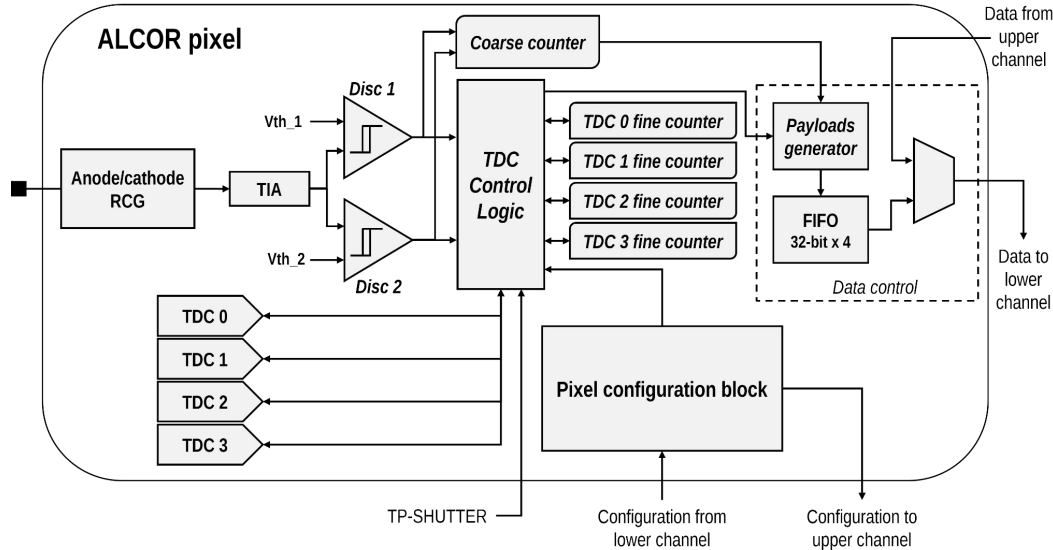
ALCOR (A Low Power Chip for Optical Sensor Readout)

Mixed-signal ASIC for SiPM readout with **single-photon sensitivity**

- **32-pixel** matrix (8x4) providing signal **amplification, conditioning** and **digitization**
- Time measurement: **ToA + ToT** or **Slew-Rate** information for **time walk correction**
- **Triggerless** readout scheme with **fully digital output**: 32-bit event word, 4 LVDS 320 MHz DDR Tx links
- Power consumption **~10-12 mW/channel**
- 0.11 μm CMOS technology



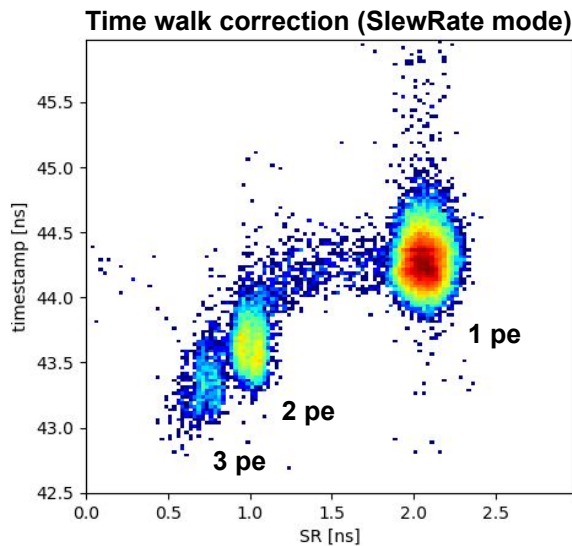
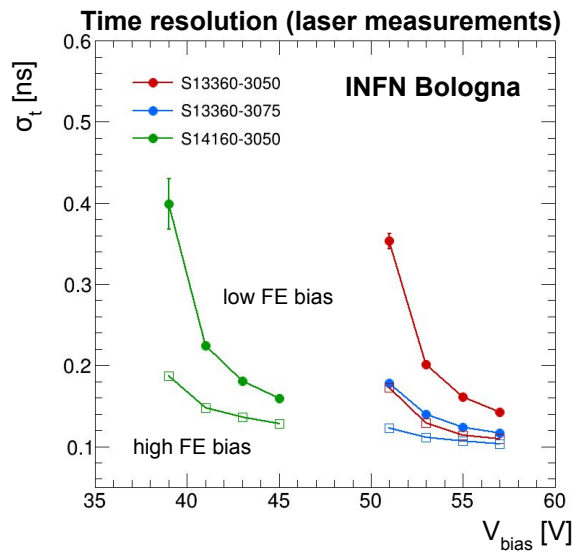
Pixel architecture



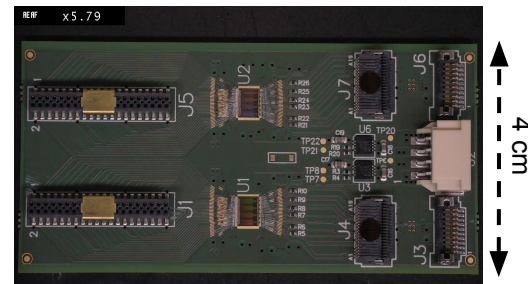
- **Dual-polarity RCG input stage** current conveyor ($Z_{in} = 10\text{-}20 \Omega$) + **TIA** with 4 gain settings
- **2 leading edge discriminators** with independent (and per pixel) threshold settings (6-bit DAC)
- **4 TDCs** based on **analogue interpolation** with **25-50 ps** time-bin (at 320 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration, operating mode and data transmission
- **TP-Shutter** to inhibit events digitization (synchronous now, asynchronous with ns time window in next version)

Results highlights

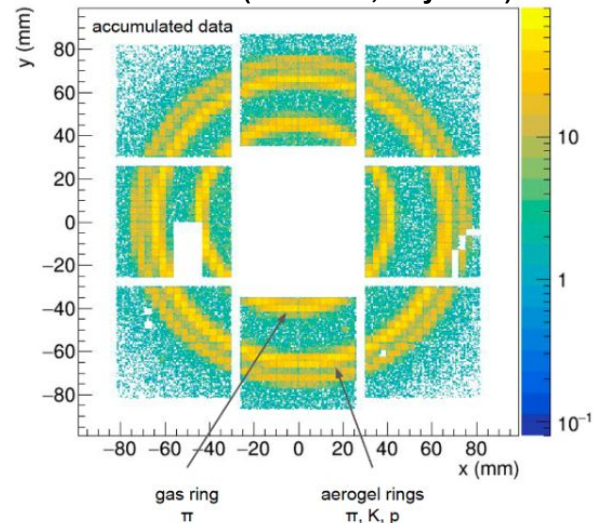
- First version developed for the readout of SiPMs at **cryogenic temperatures**, in the framework of **DarkSide** (ALCOR v1, 2020)
- Adopted for the readout of SiPM sensors of the **ePIC dRICH** detector at EIC and extensively used within the dRICH Collaboration since 2021 (ALCOR v2, 2023)



dRICH ALCOR-FE-DUAL



Beam test with prototype dRICH and PDUs (CERN-PS, May 2024)



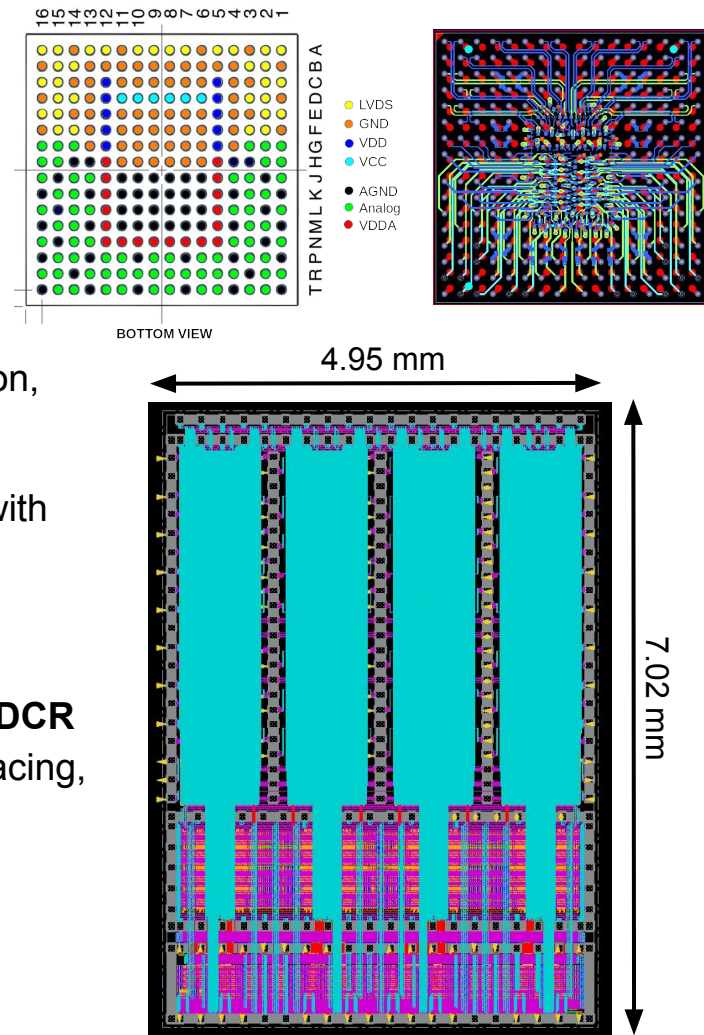
32 FE-DUAL (64 ALCOR, **2048 channels**)
 SiPM: HPK **S13360-3050** and **S13360-3075**
 ($3 \times 3 \text{ mm}^2$, $T = -30/-40^\circ\text{C}$)

ALCOR for ePIC

ALCOR v3: 64-channel ASIC (8x8 matrix) inside **BGA package**
(256 balls, 17x17 mm², 1 mm pitch)

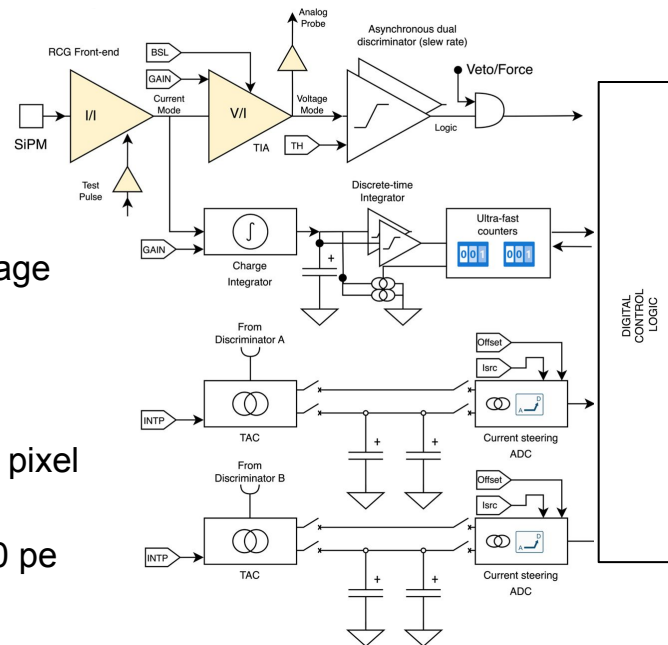
- Amplifier with **increased bandwidth** to improve time resolution, approaching 100 ps at low V_{bias}
- **Hysteresis discriminator** to avoid re-triggering on slow tail with very low thresholds
- New clock frequency: **394.08 MHz** (4x EIC clock frequency)
- **Digital shutter** to inhibit pixel digital logic to **cut out-of-time DCR signals** and reduce data throughput (~10.2 ns EIC bunch spacing, **2-3 ns** time window → 3x-5x data reduction before ALCOR digitization)

Tape-out on 31st March 2025



- Electronics operating from **T = 300 K** to **T = 77 K**
- ToA with a resolution of **100-150 ps** with a threshold of 0.5 pe
- **Photon counting** in each event window (dynamic range **> 100 pe**)
- Limited number of cables entering the cryostat

- **1024 channels** (32x32 pixel matrix, area $\approx 20 \times 20 \text{ mm}^2$), BGA package
- ALCOR FE with improved response at **cryogenic temperatures**
- Operation at **87 K** \rightarrow **P < 15 mW/ch**, **power gating**
- Programmable **data-link sharing** among pixel columns
- **Time:** TAC + SAR ADC \rightarrow faster conversion capability and reduced pixel dead time (backward compatible with ALCOR Wilkinson ADC)
- **Charge:** discrete-time charge integrator with 0.25 pe resolution, 500 pe dynamic range, up to 50 simultaneous pe



1024-channel demonstrator tape-out scheduled for the end of 2025