A 12 bit, sub-100 ps LSB Time-to-Digital Converter for ToA measurements in digital SiPMs

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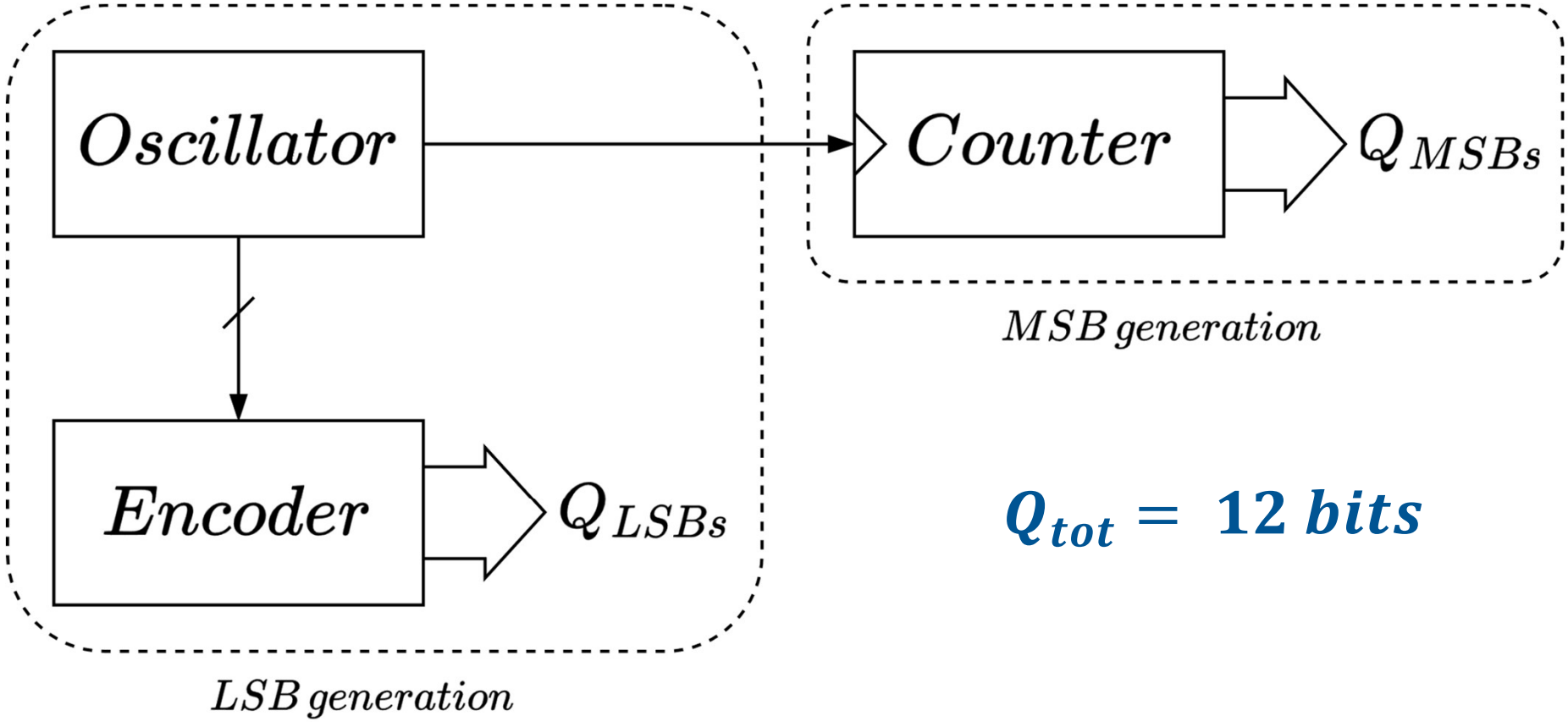
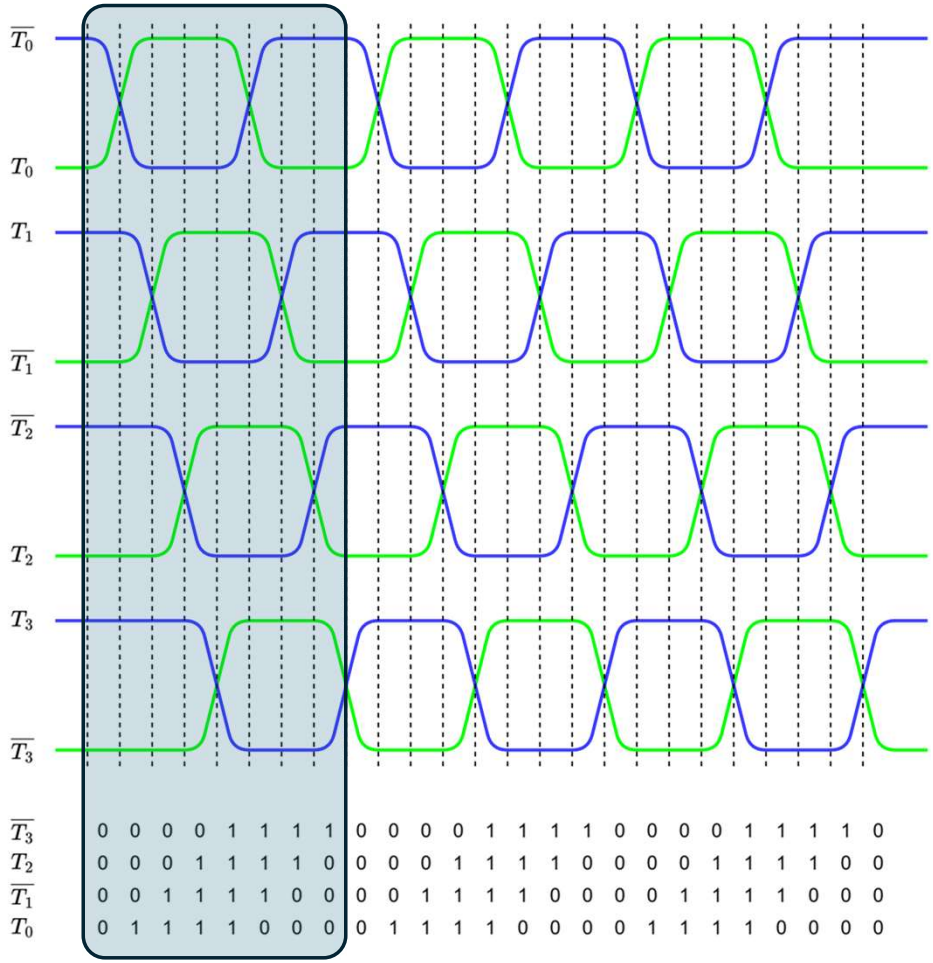
Architecture: Interpolation TDC



$$Q_{tot} = 12\ bits$$

Output Decoding

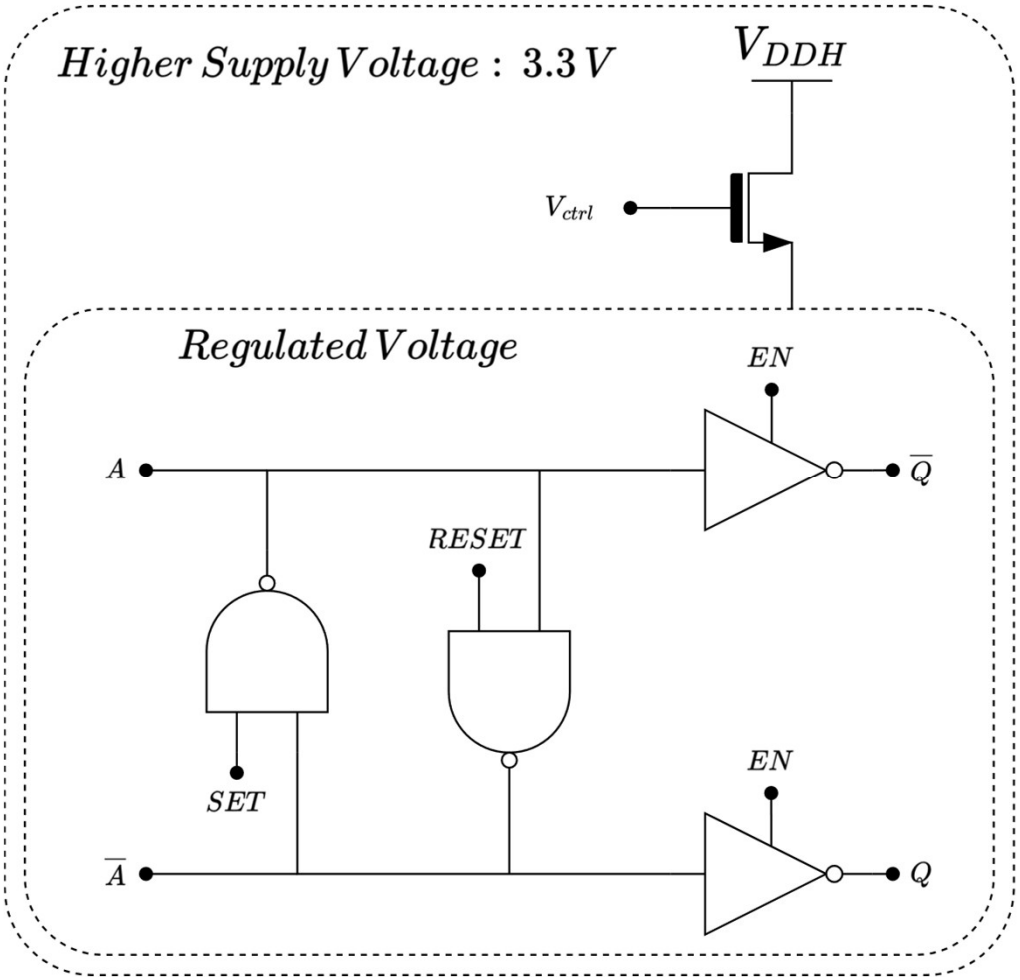


$$LSB: \frac{1}{8} th\ period$$

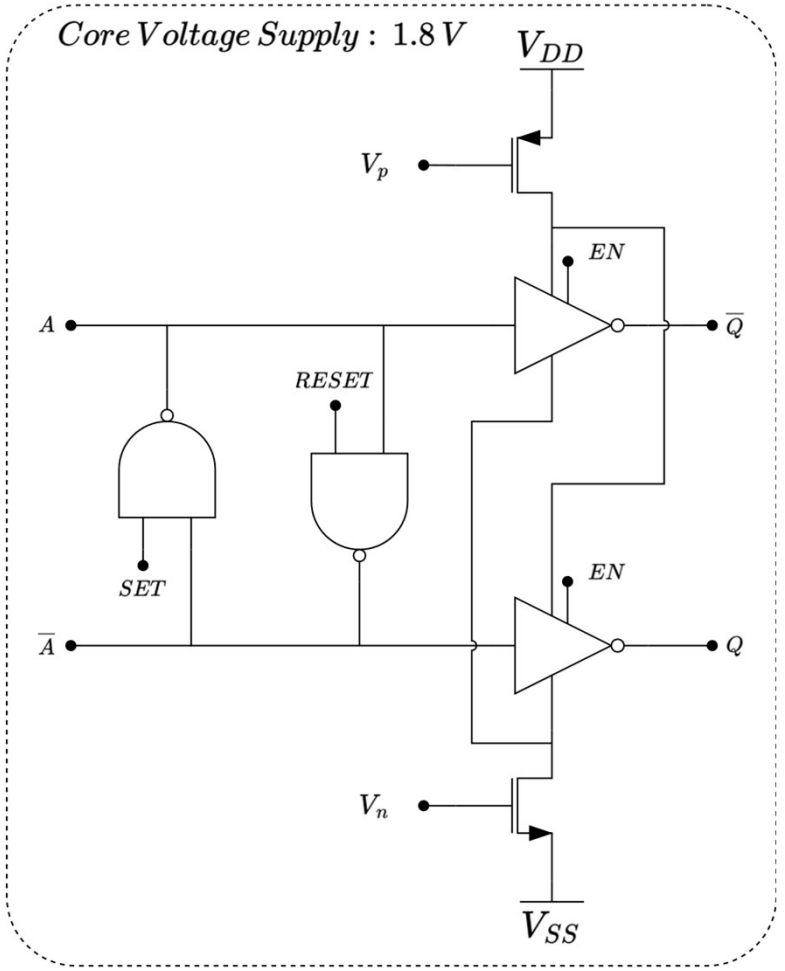
Johnson Encoding

$\overline{T_3}T_2\overline{T_1}T_0$	Binary Code
0000	000
0001	001
0011	010
0111	011
1111	100
1110	101
1100	110
1000	111

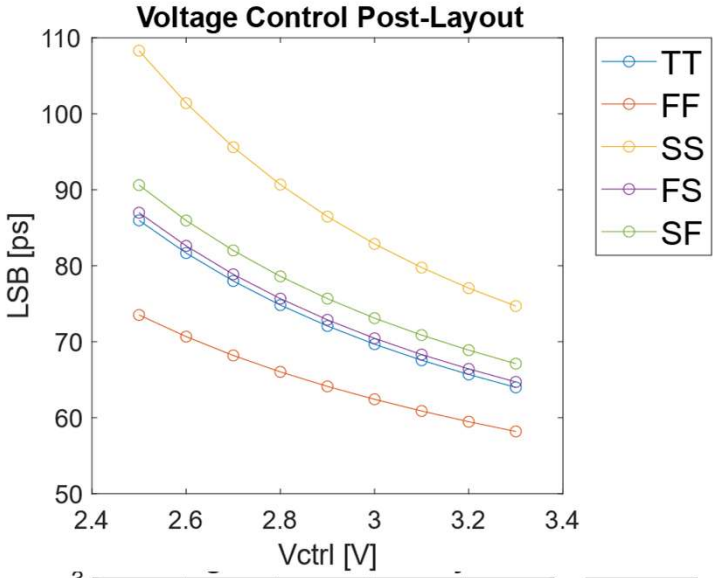
Voltage Control System

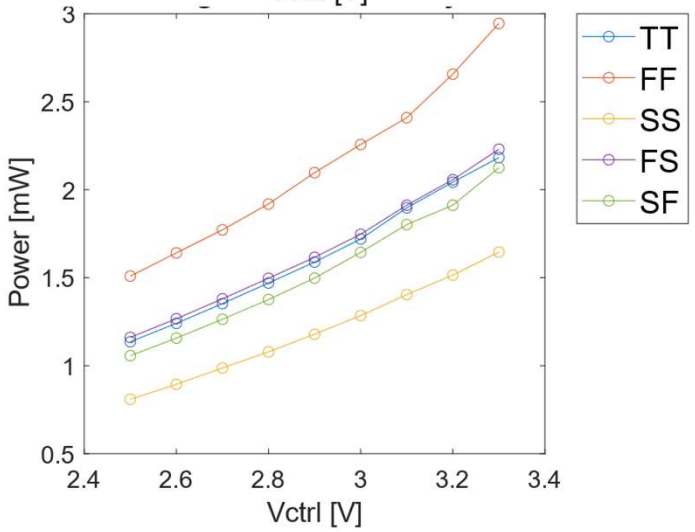


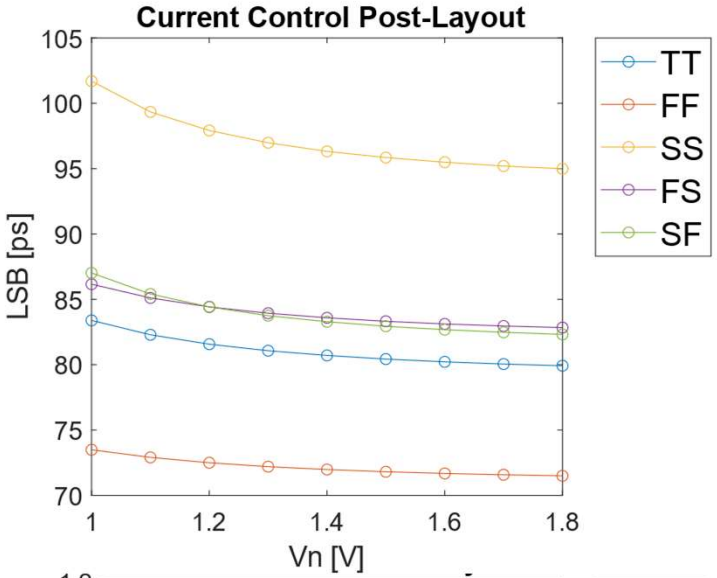
Current Control System

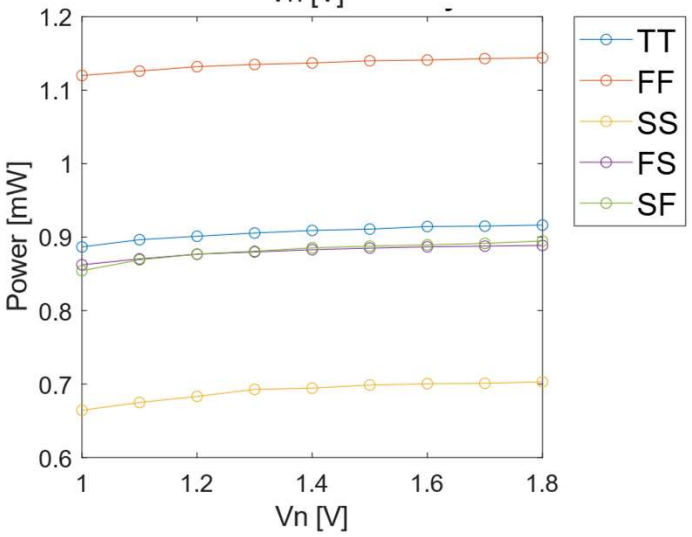


Results: LSB & Power

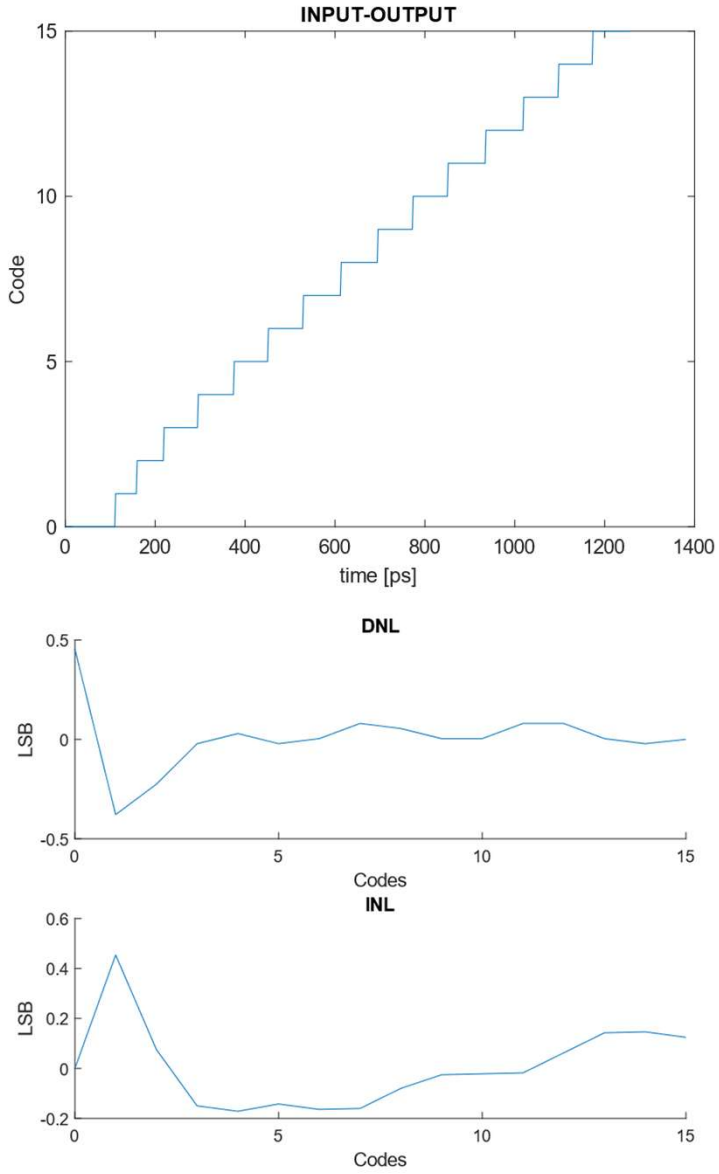


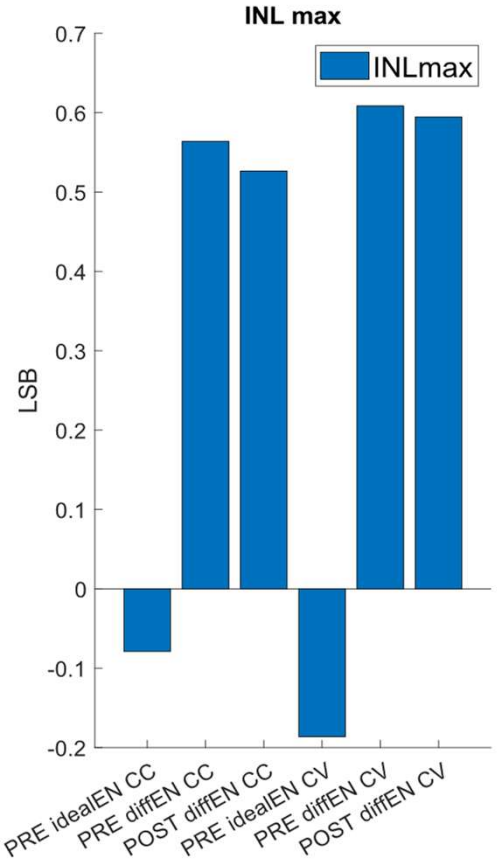


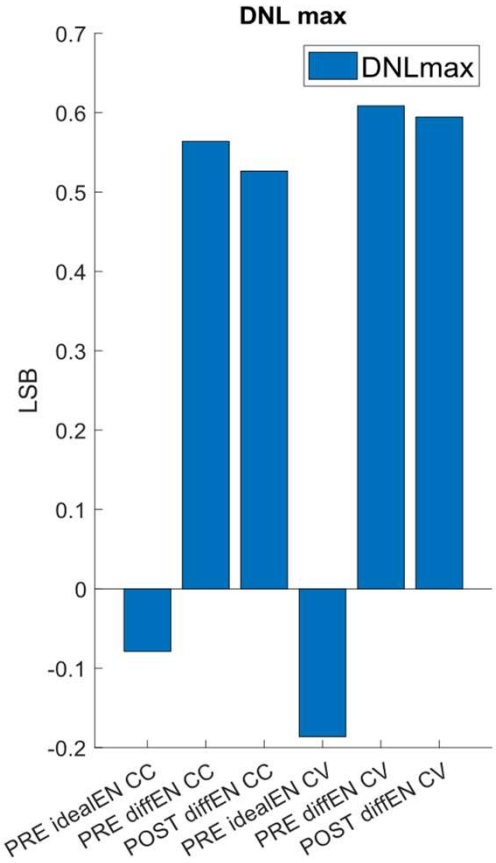




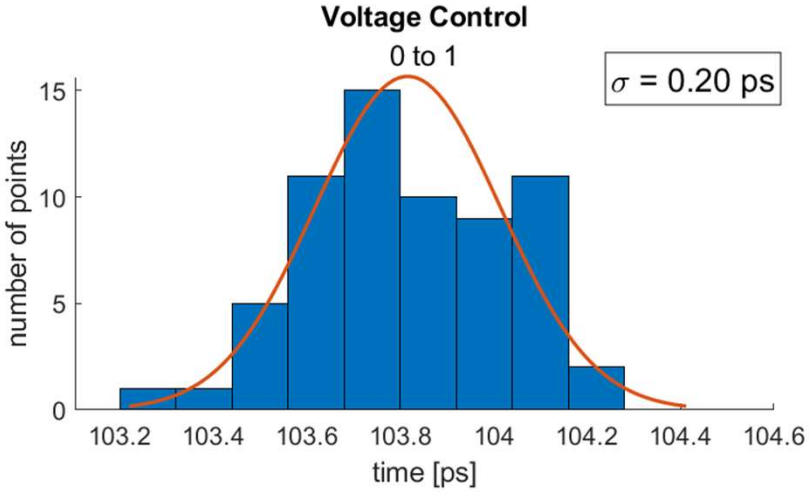
Results: DNL & INL

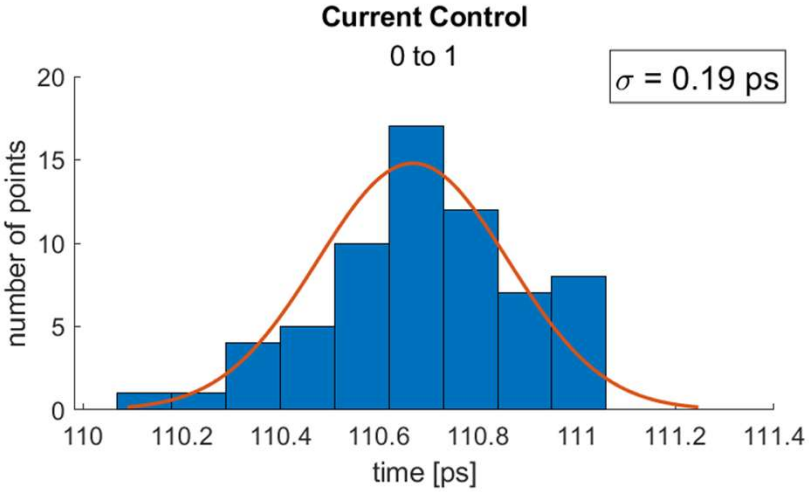


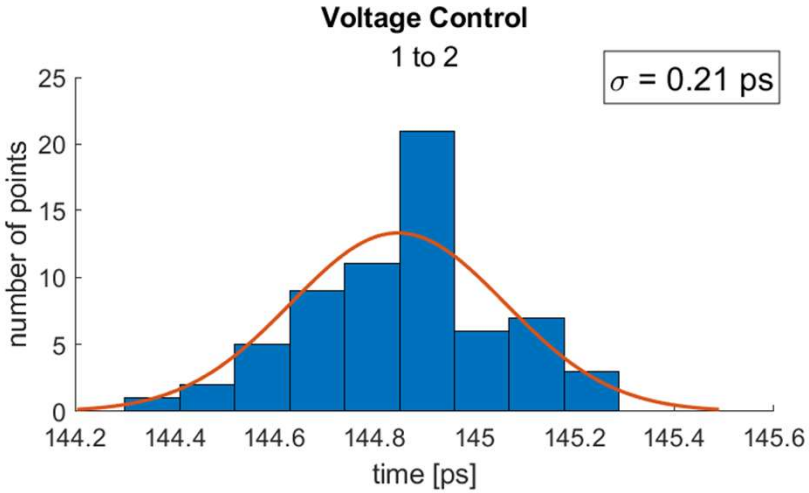


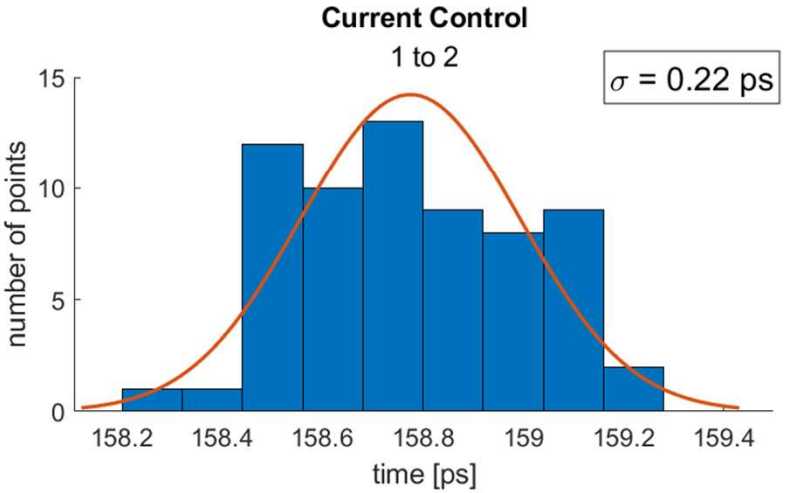


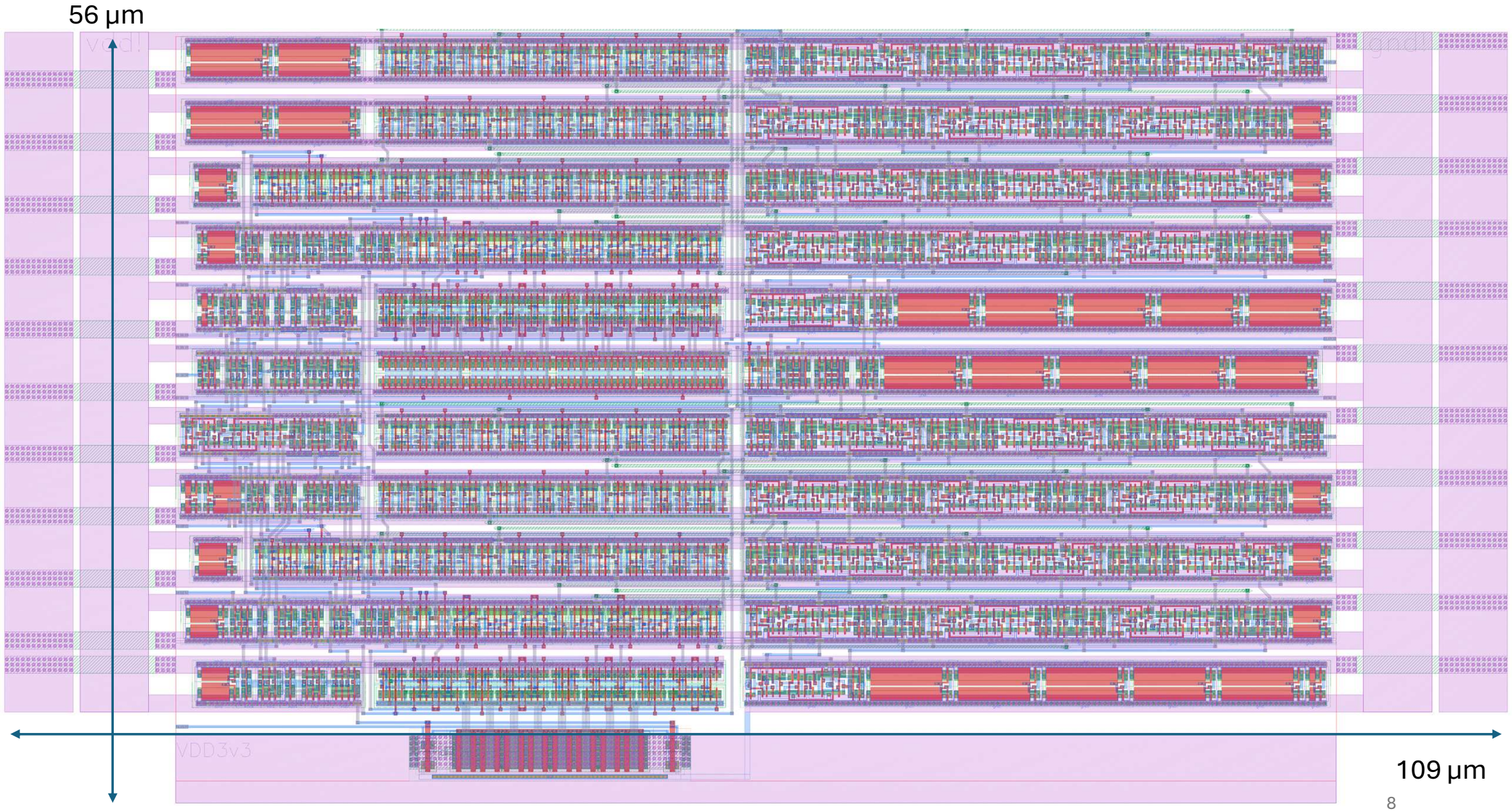
Results: Jitter










56 µm
VDD3v3
109 µm

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