Design of a multi-function ASIC for reading out large SiPM-based systems

Università di Siena & INFN Sezione di Pisa

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Introduction

- The idea of developing a new device for handling analog inputs from a multichannel photo-sensor arose from the ATLAS hadronic calorimeter need to enhance readout granularity for the HL-LHC era by replacing single-anode PMTs with MA-PMTs, while minimizing the increase in digital readout channels.

- Current market solutions require digitizing all input signals, but in large future SiPM-based systems, the cost of this approach can become unaffordable due to the large number of channels that need to be processed.

- **We aim to reverse this approach: first, perform an analog sum of selected subsets of readout channels, and then digitize only the desired sum(s).**

- **The new device will enable configurable calorimeter readout granularity, reducing ADCs and costs, facilitating future hadronic and electromagnetic calorimeters.**

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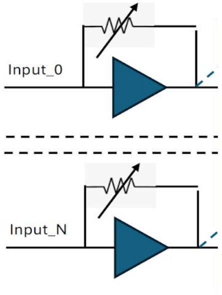
  1) A first stage with variable gain fast (2 GHz BW) amplifiers to allow for input weighting,



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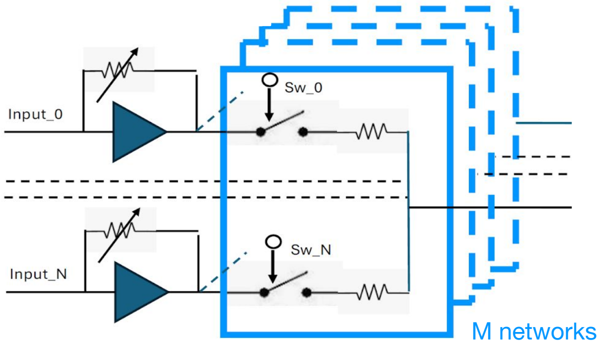

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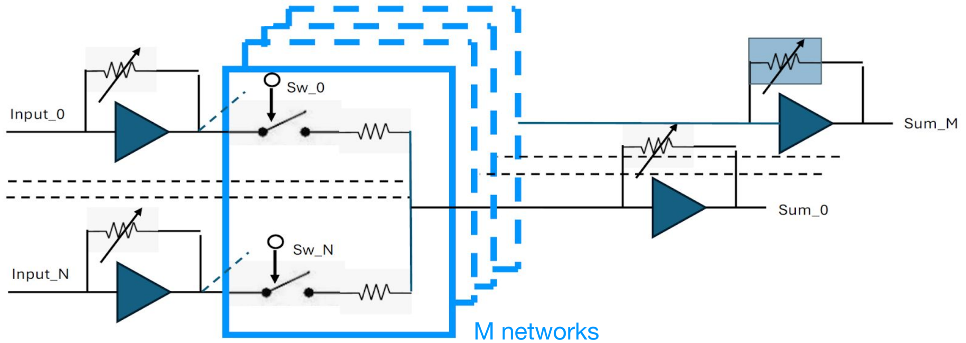

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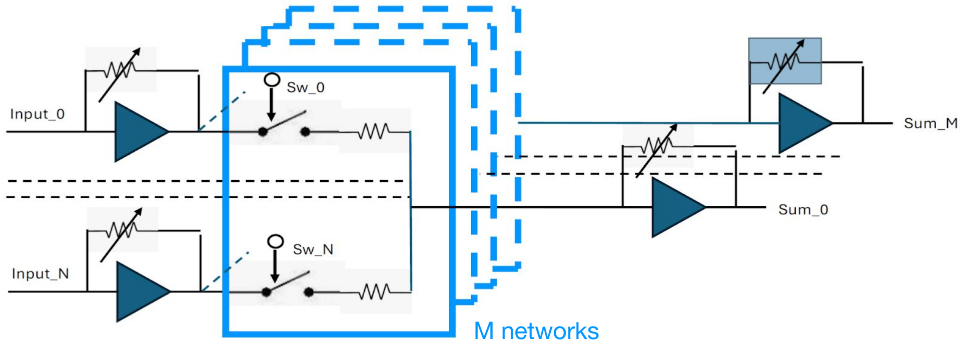
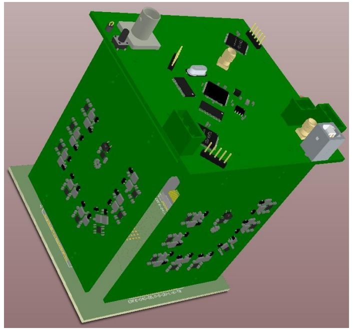
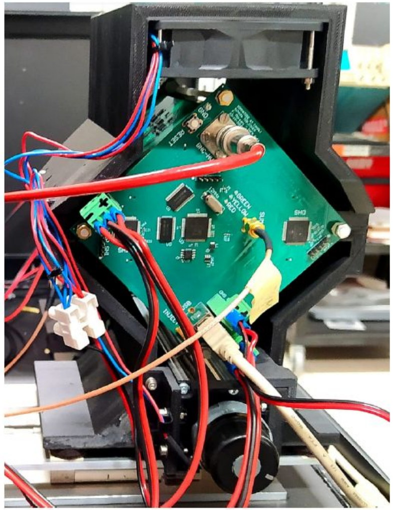


What was done?
A prototype for this type of readout with high-bandwidth integrated circuits was designed, built and tested at INFN Pisa.

The prototype

- The system is composed by 6 Printed Circuit Boards (PCBs), built with high-bandwidth Integrated Circuits (ICs).
- As a first proof of feasibility <u>no constraint on system dimensions, nor on power consumption (25 W) was applied</u>.





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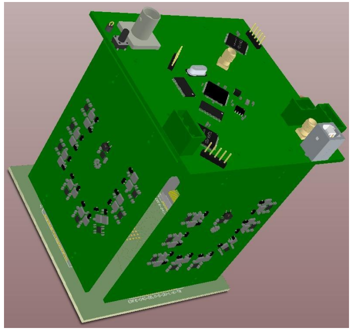
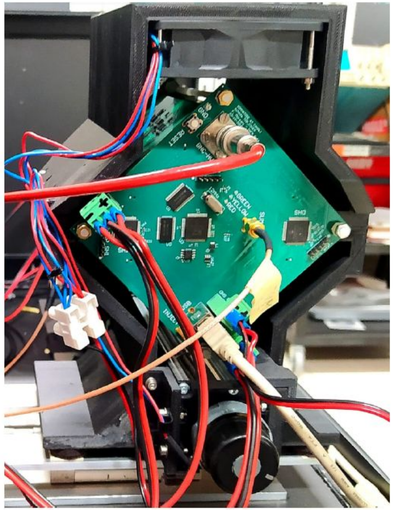
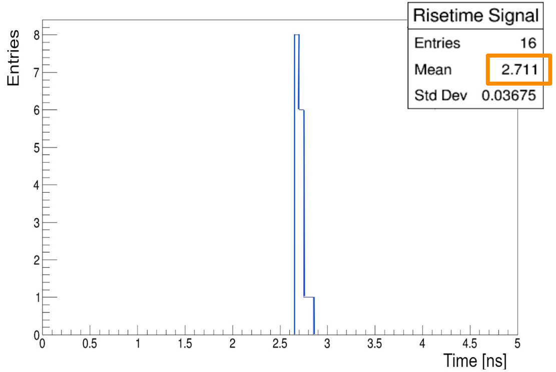


- The prototype has been tested in Pisa in terms of pulse **shape stability** and **linearity of the analog sum** of an arbitrary number of channels .



Prototype tests results

- The readout prototype guarantees pulse shape stability and linearity in the analog sum of the signals (rise times ~ 2.7 ns);



Single channel rise time distribution

Prototype tests results

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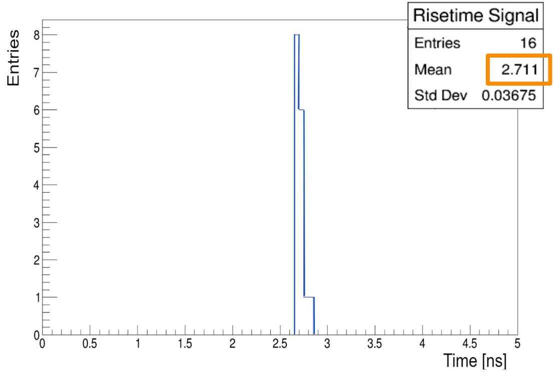
- The resistive summing networks do not alter the shape of the outputs;



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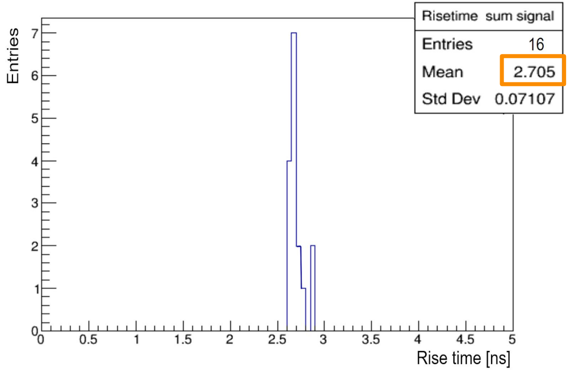
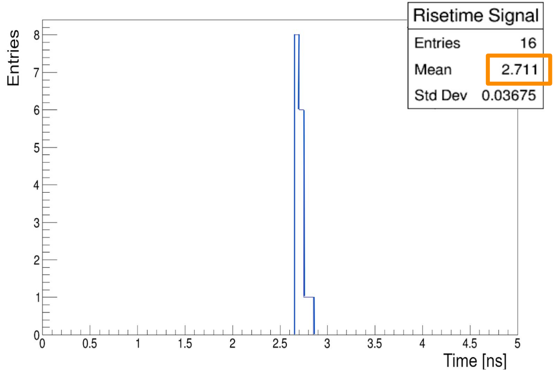


Distribution of the rise time of the analog sum for an increasing number of channels

Prototype tests results

- The readout prototype guarantees pulse shape stability and linearity in the analog sum of the signals (rise times ~ 2.7 ns);
- The resistive summing networks do not alter the shape of the outputs;
- Jitter time ~ 40 ps, good data transmission;



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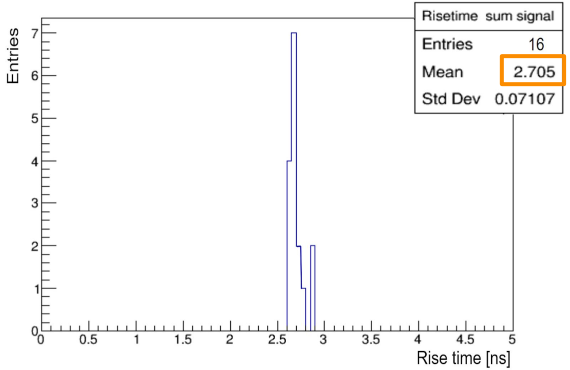
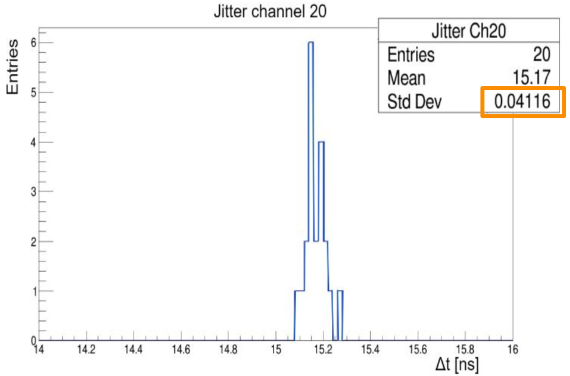


Distribution of the rise time of the analog sum for an increasing number of channels



Channel 20 Δt distribution for jitter estimation

A new analog ASIC (I)

- **The aim is to design a new ASIC device to readout multi-channel photodetectors, with the same features as the prototype, namely based on the equalization and on the analog sum of a programmable number of channels.**

- The chip can be used in any system that involves the use of SiPMTs, both in the field of particle physics and in industrial applications.

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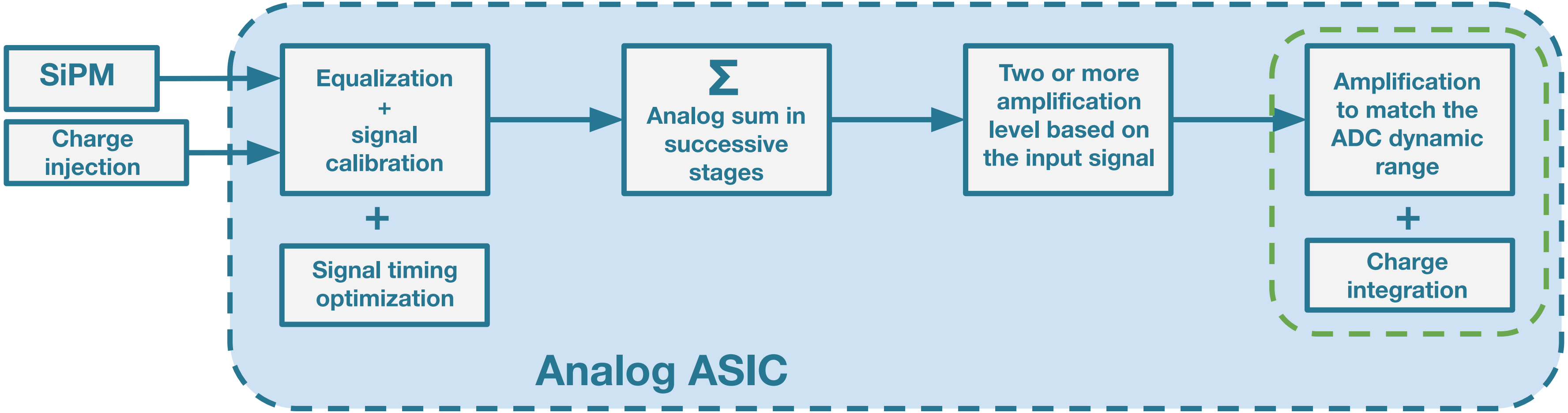


A new analog ASIC (II)

- The project is officially part of the CERN DRD6 project for the development of new sampling calorimeters with scintillating tiles (ALLEGRO HCAL, sub-task 3.3.2). Also the project for the development of Dual readout Dream-like calorimeters (HiDRa, sub-task 3.3.1) expressed interest in this device.

- **We are currently forming a collaboration of Italian institutes interested in the development of a 64-channel ASIC version of this device. At this stage, we are defining the potential roles of the institutions within the collaboration and identifying the ASIC characteristics based on the readout requirements of the relevant DRD6 projects.**

International institutes	Expertise
CERN	ALLEGRO project
Prague, Uni Bergen/ Gottingen, FOTON	SiPM readout
University of Valencia	RF amplifiers for SiPM readout

Italian institutes	Field of interest
INFN Pisa	Architecture development
Università di Siena	Architecture development
INFN Torino	ASIC design
INFN Pavia	Interface to HiDRa application
INFN Milano e Università dell’Insubria	Interface to HiDRa application

The table represents a possible division of tasks if the project moves forward.

Conclusions and next steps

- A prototype of a new analog device for the readout of SiPMs has been designed and tested by INFN Pisa. The tests on the prototype yielded excellent results in terms of pulse shape stability and time stability in the case of summing an arbitrary number of channels.

- Encouraged by the results of the prototype, the goal is to develop an ASIC version of the device. **The project is still in its early stages, and we are working to identify its main features**.

- The goal is to open an INFN acronym in Group V in September 2025, ideally having prepared a letter of intent signed by the interested Italian and international institutions.

- **All individuals interested in the project who wish to contribute to the development of the ASIC are welcome!**

Backup

Just a few examples

1) **All calorimeters**

Configurable sums of energy deposit would allow to use the same device for defining trigger towers in different regions (barrel/forward/end-cap) and for different calorimeter sections (e.m./hadronic).

2) **E.M. homogeneous calorimeters, like Calice/CMS, with SiPM readout**

Spatial separation of e.m. energy deposits obtained by tuning with energy (p_T) the size of readout cells would improve detection of isolated photons and reconstruction of energy clusters produced by electrons from decays of boosted bosons.

3) **Hadron sampling calorimeters à TileCal (<u>ALLEGRO HCAL barrel</u>), with SiPM readout**

Dynamics definition of Regions of Interest (ROIs) for energy deposits would improve both the separation of small radius jets and the definition of the contour of merged jets in hadronic decays of boosted particles.

Project overview of the first prototype

What we want to do?

- The aim is to design a **new ASIC device to readout multi-channel photodetectors**, based on the equalization and on the analog sum of a programmable number of channels.

➡ The system must be able to independently amplify each readout channel and sum a configurable number of channels into a single analog output signal.

➡ The chip can be used in any environment that involves the use of multi-channel photodetectors (MAPMTs e SiPMTs), both in the field of particle physics and in industrial applications.

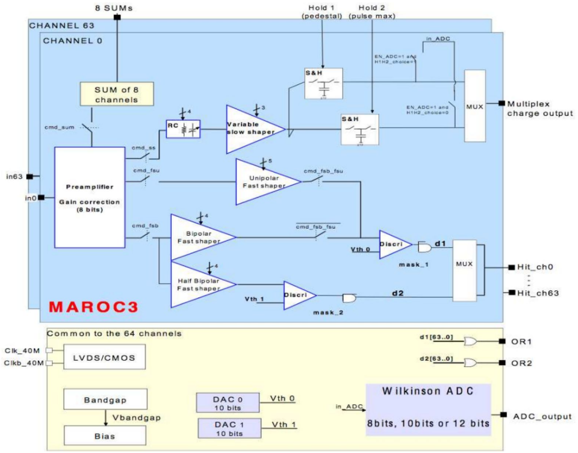
➡ The device we want to design offers broader functionality than similar existing readout systems.

Readout systems on the market

Multi-AnodeReadOut Chip (MAROC3)

- 64-channels readout, AMS SiGe 0.35 µm technology. Maximum amplification up to a factor 4.

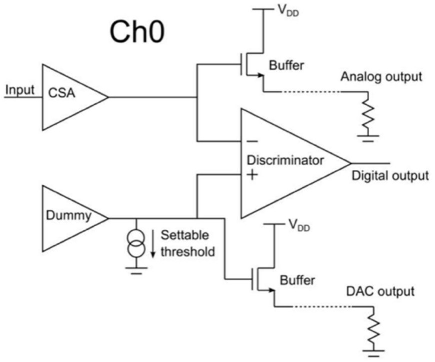
  More info: https://iopscience.iop.org/article/10.1088/1748-0221/5/12/C12007/pdf



CLARO8

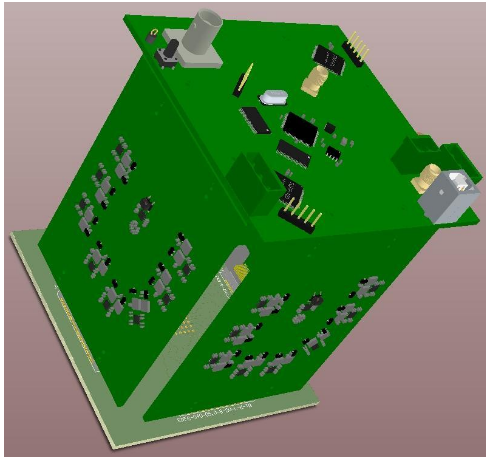
- 8-channels readout, 0.35 µm CMOS technology. CLARO8 provides mainly digital output signals, has only 4 gain settings and does not allow to sum the channel signals.

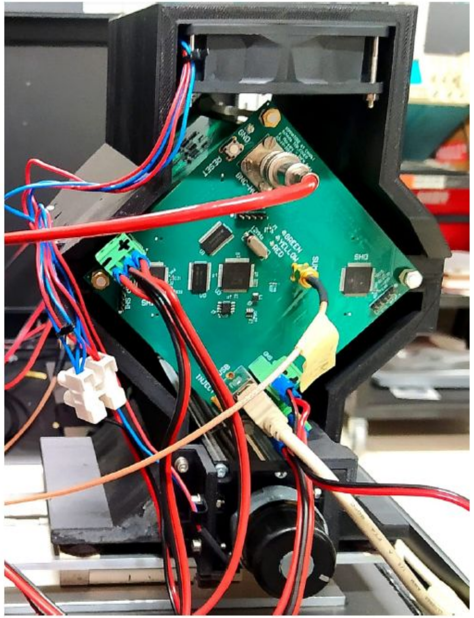
  More info: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7891728



Prototype description (1)

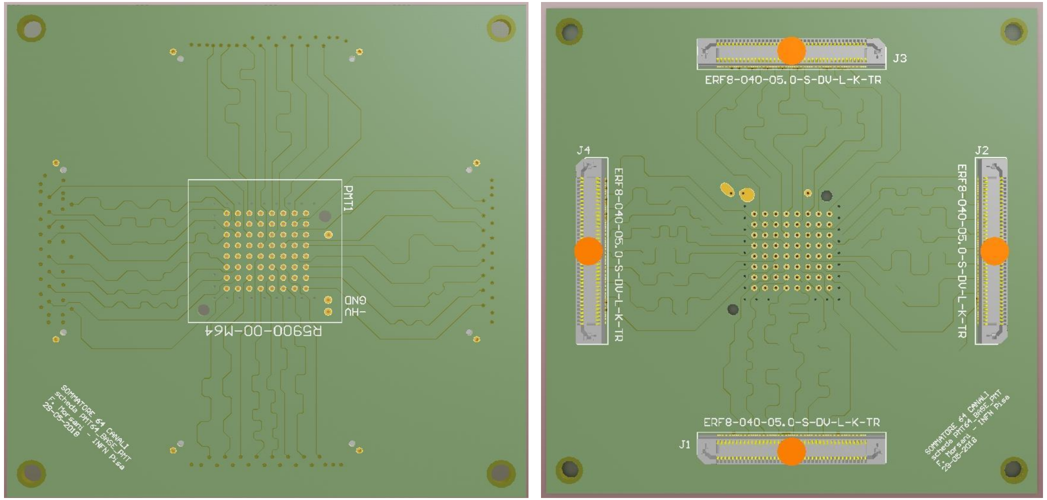
- Designed and developed by Dr. Fabio Morsani
- The system is composed by 6 Printed Circuit Boards (PCBs), built with high-bandwidth Integrated Circuits (ICs).





- As a first proof of feasibility no constraint on system dimensions, nor on power consumption (25 W) was applied.
- The 6 PCBs are arranged to form the faces of a parallelepiped with a square base and are assembled inside a metal support structure which also houses a cooling system.

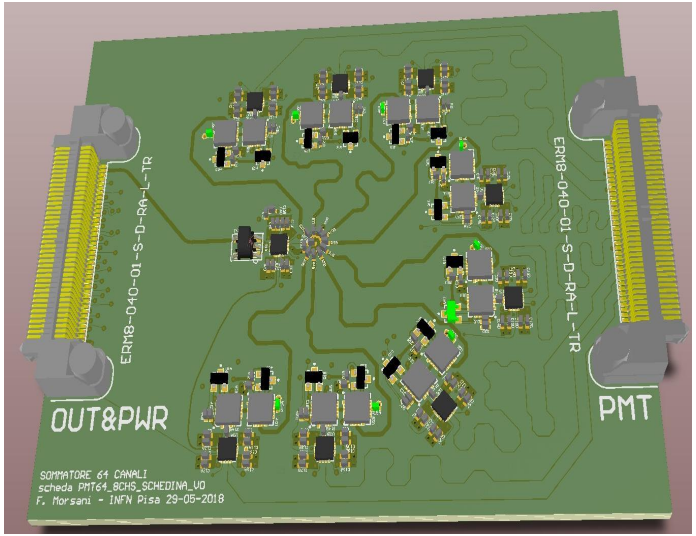
Prototype description (2)

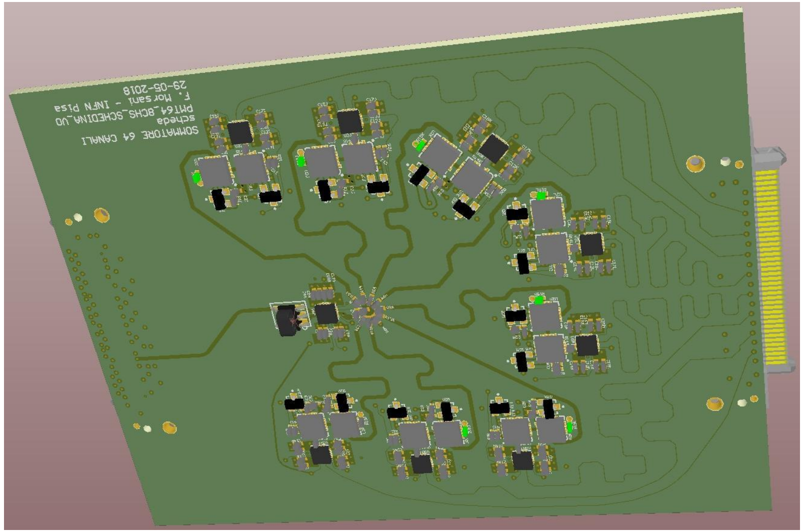


First base board (front and back)

- The prototype is designed to host a 64-channel MAPMT with a sensitive area of 18×18 mm^2 and an anode pitch of 2.54 mm.

Prototype description (3)

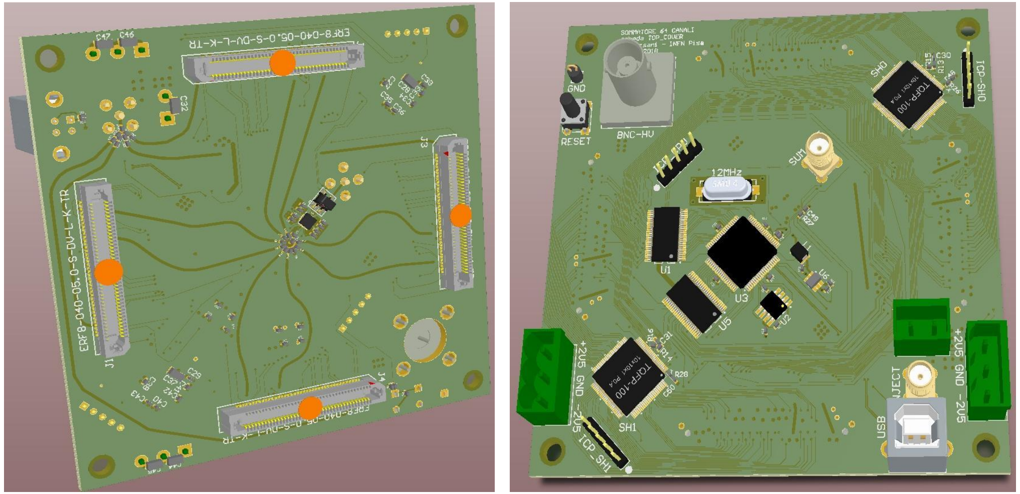




Lateral board

- 8 single-channel amplification systems
- 1 resistive network to perform analog sum of 8 channels

Prototype description (4)

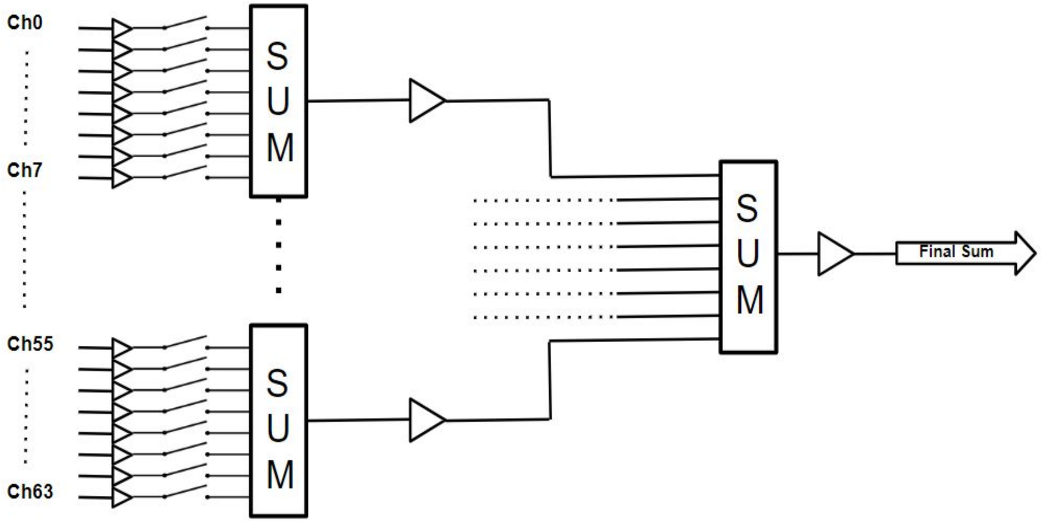


Second base board (front and back)

- Final sum stage (final resistive network + amplifier)
- Microcontroller and logic level shifters
- USB interface
- BNC-HV

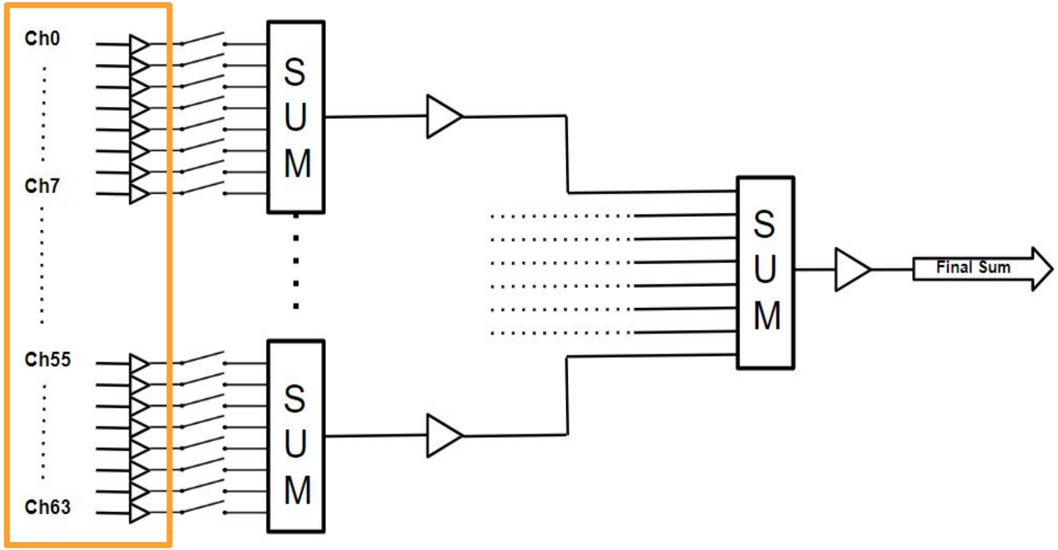
Description of the prototype functioning (1)

Circuit schematic of the prototype.



Description of the prototype functioning (2)

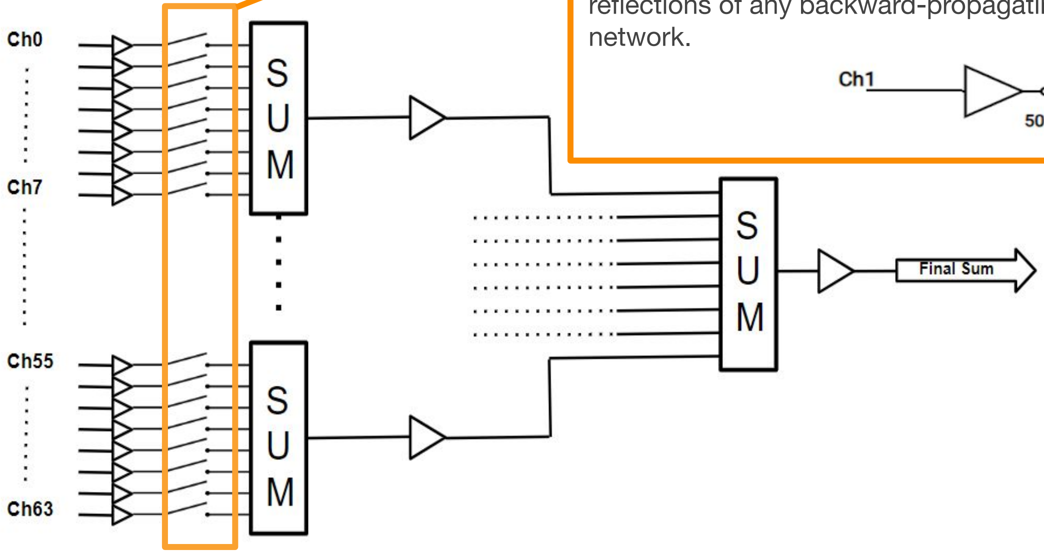
Circuit schematic of the prototype.



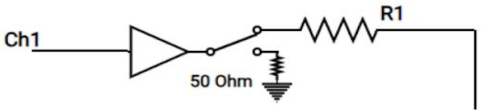
➡ Channels are first amplified with a configurable gain in a range between -6 dB and 26 dB (first amplification stage, equalization).

Description of the prototype functioning (3)

Circuit schematic of the prototype.



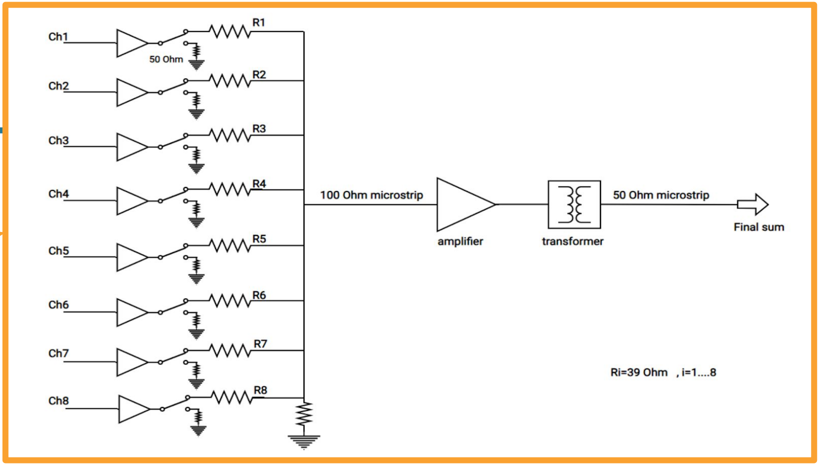
More info: The switches enabling the channels to enter the analog sum are SPDT switches (Single Pole, Double Throw) with a bandwidth of 3 GHz and high isolation. In the OFF mode, a 50 Ω resistor is switched onto the output line to ensure minimal reflections of any backward-propagating signal from the summing network.

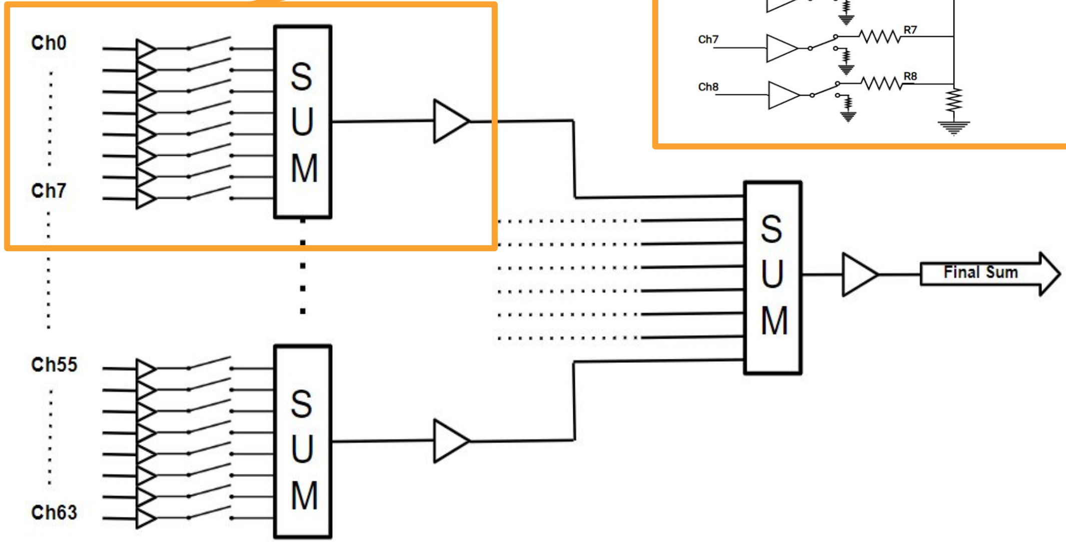


➡ The channels participating in the final sum are activated via switches.

Description of the functioning (4)

Circuit schematic of the prototype.

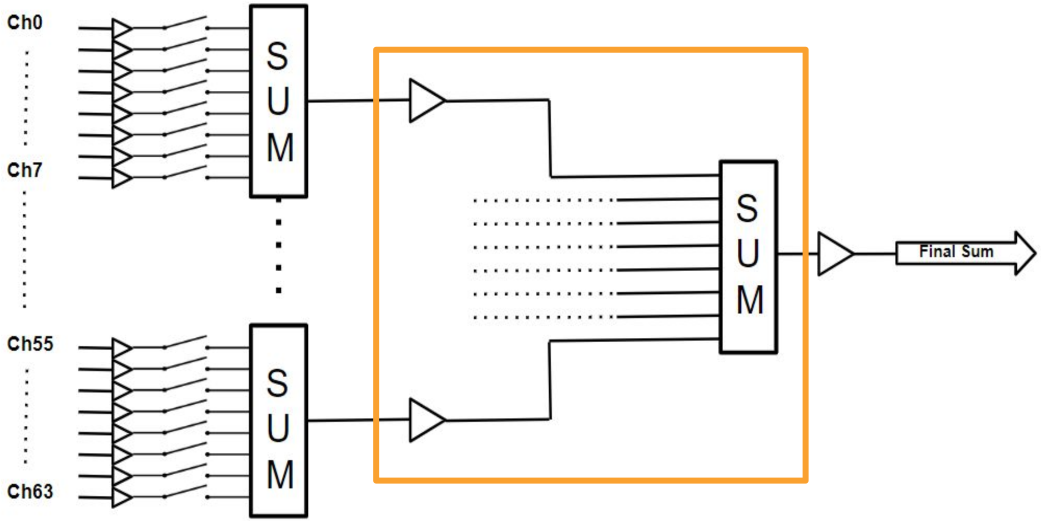




➡ The 64 amplified readout channels are fed to eight 8-channel resistive summing networks.

Description of the prototype functioning (5)

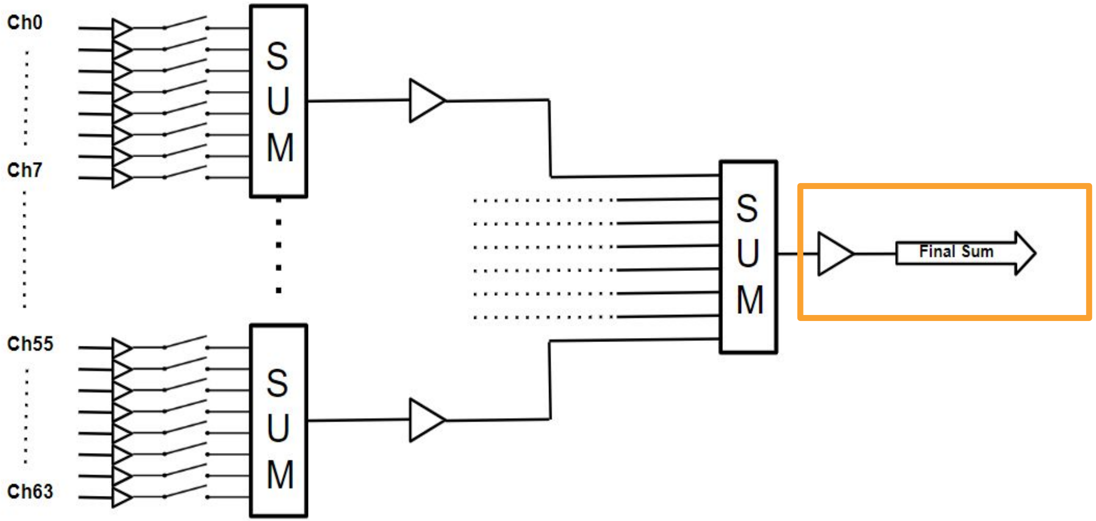
Circuit schematic of the prototype.



➡ The output of each 8-channel network is amplified before being fed into a resistive network for the final sum.

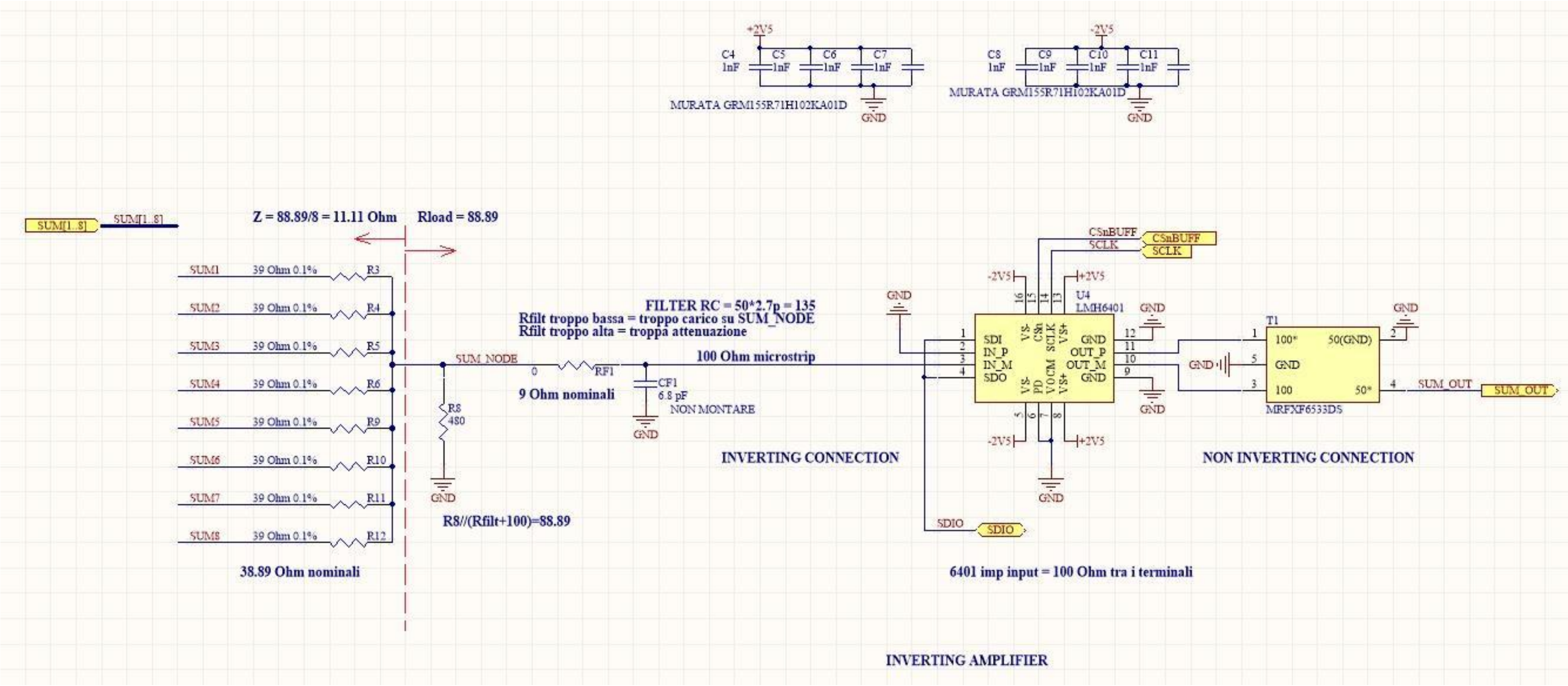
Description of the prototype functioning (6)

Circuit schematic of the prototype.

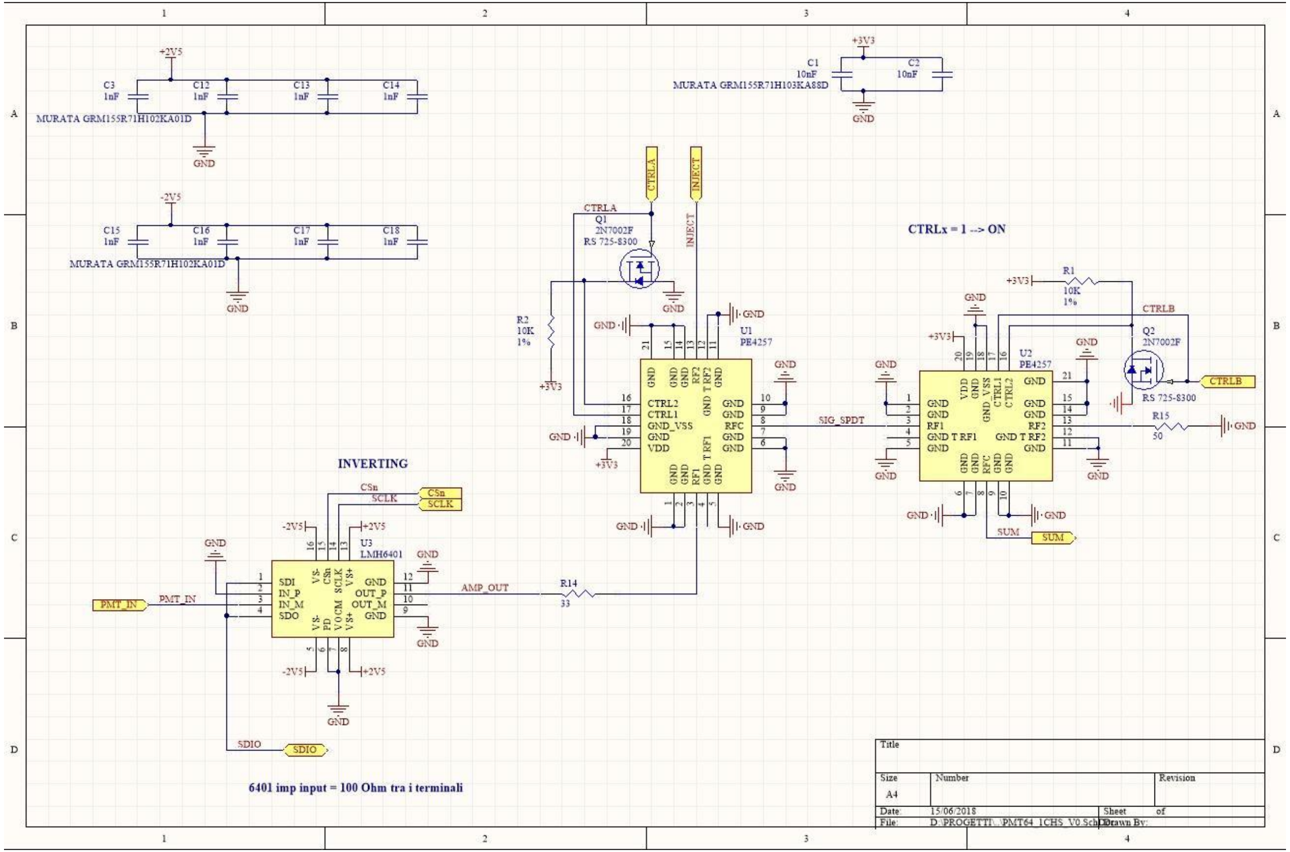


➡ The final analog sum can be further amplified to match the dynamic range of the ADC used for signal digitization. The gains of the three steps are configurable in a range from -6 to 26 dB.

Readout prototype schematics (1)

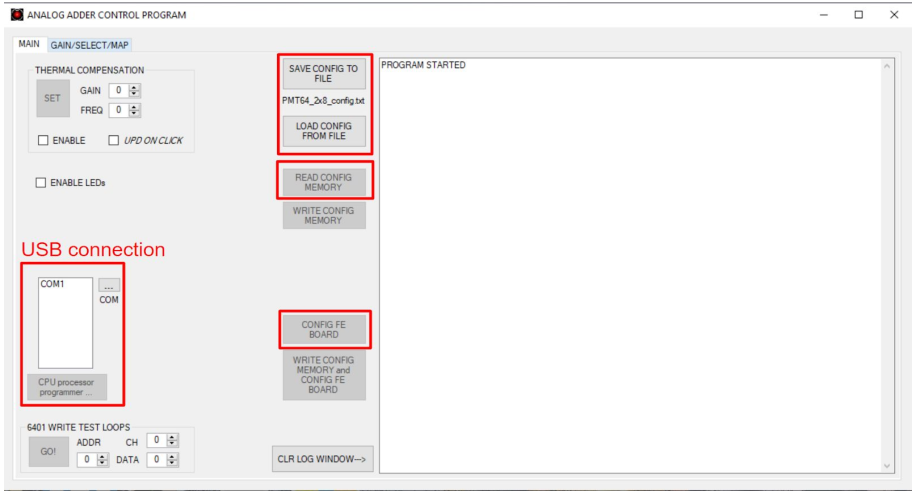


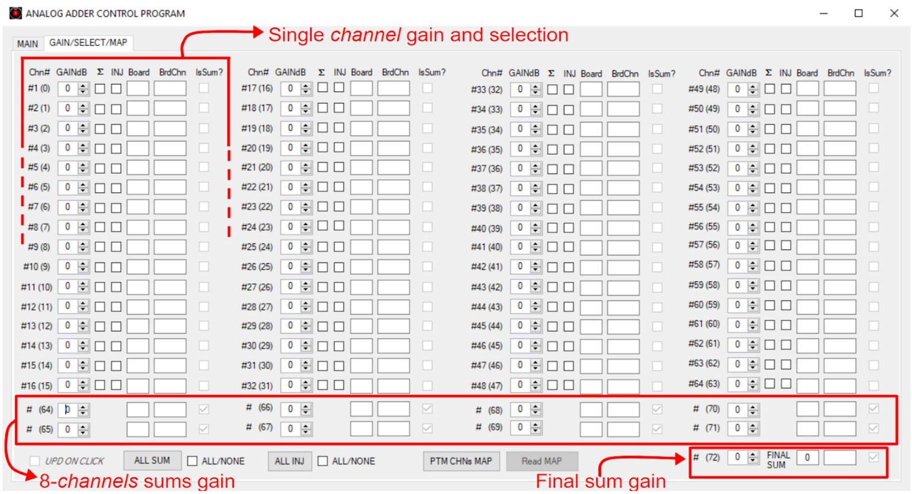
Readout prototype schematics (2)



GUIs

- The selected channels and all amplifications can be set through a GUI, allowing to establish USB connection with the prototype and to upload the selected configuration for the final sum.





Prototype tests: introduction

- The prototype has been tested in Pisa in terms of pulse shape stability and linearity of the analog sum of an arbitrary number of channels.

- Various tests were done with two different experimental setups:

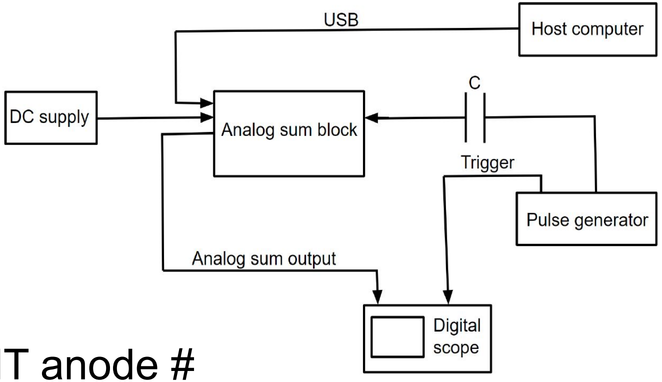
  ➡ test of the 16 central readout channels injecting an input signal

  ➡ test of the readout system using a MAPMT and a laser system

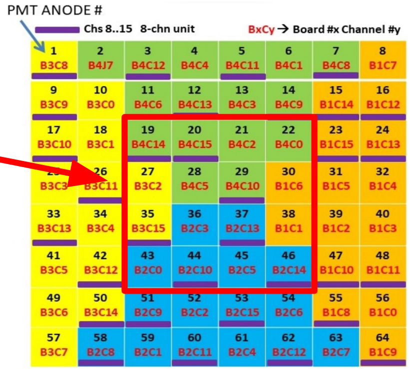
Readout prototype tests with signal injection

Experimental setup

- Analysis of the prototype performances in terms of shape stability and analog sum linearity.
- Digital oscilloscope used to analyze input/output signals.
- Pulse generator + capacitor system used to generate the <u>input signal</u> to inject in the 16 central readout channels.



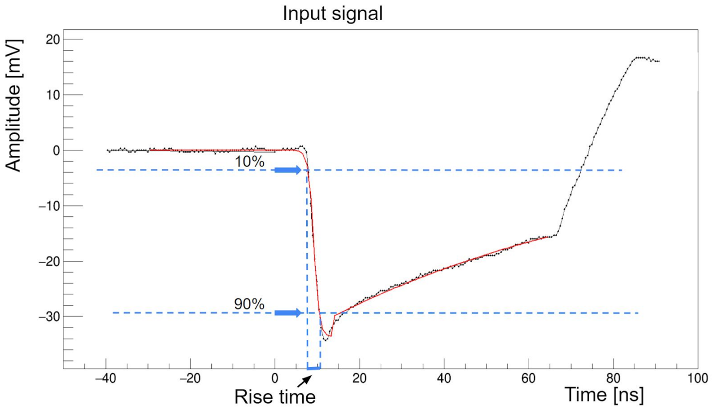
PMT anode #

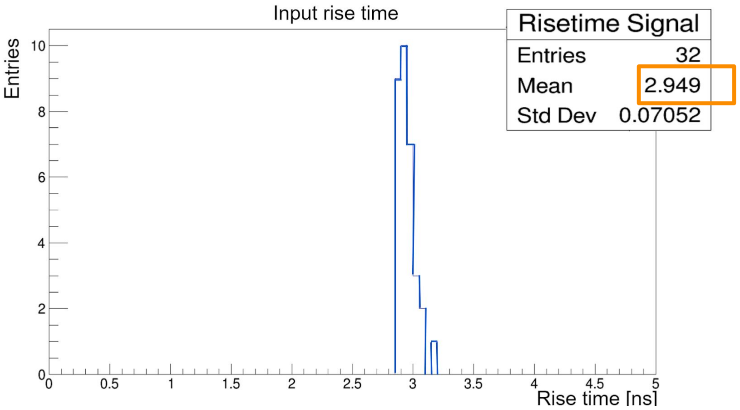


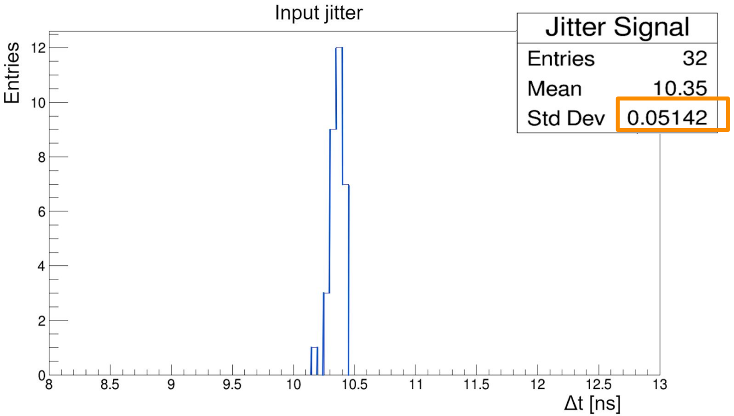
PMT back view

Input signal

- Input signal used to test the 3 readout prototype amplification stages.
- Generated by differentiating a square pulse with a 60 pF capacitor to simulate the signal produced by a PMT.

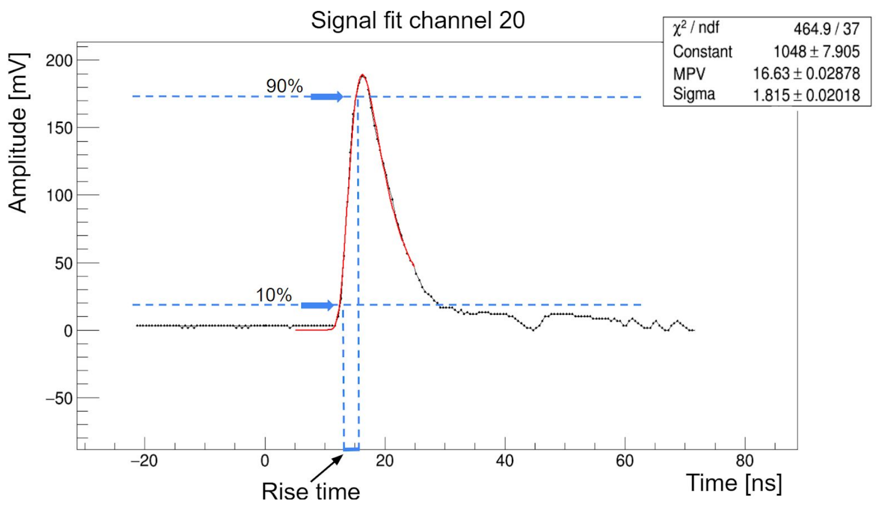


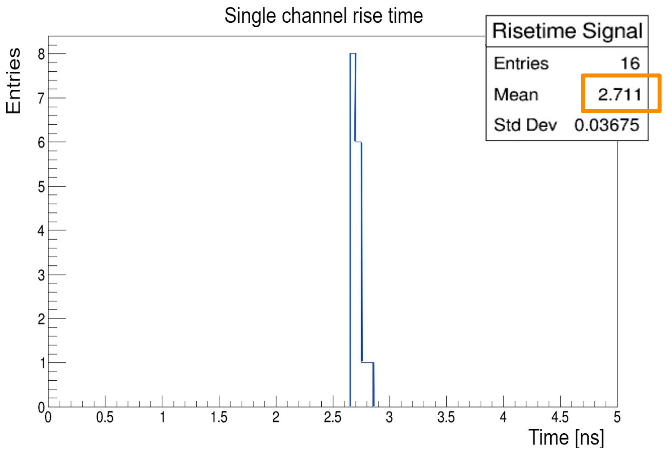




Single channel output signals: rise time

- Landau fit function to calculate the amplitude and the baseline of the signal for the rise time evaluation.

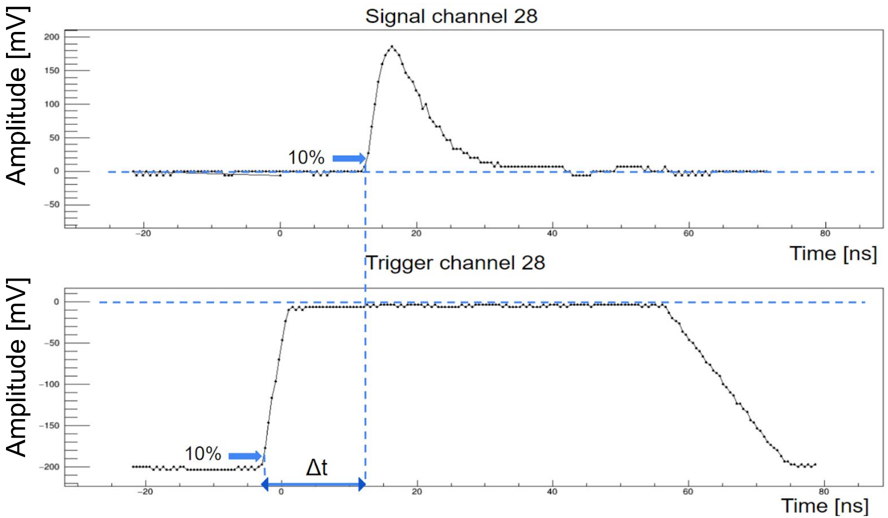


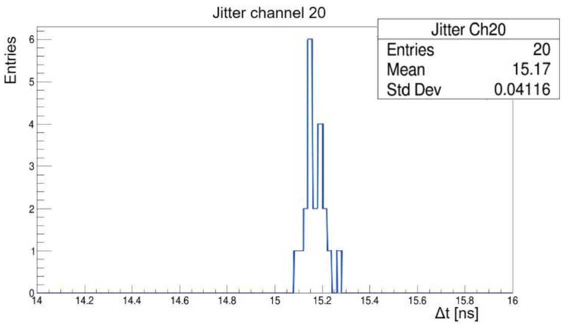


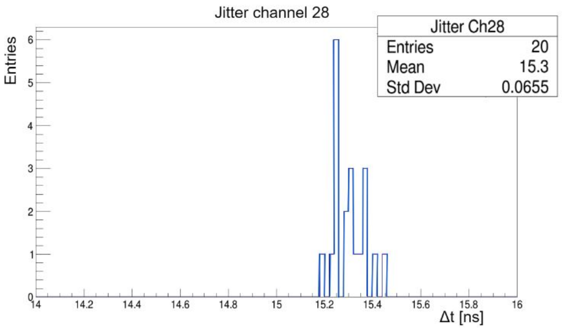
- Output signal rise times are ~ 2.7 ns.

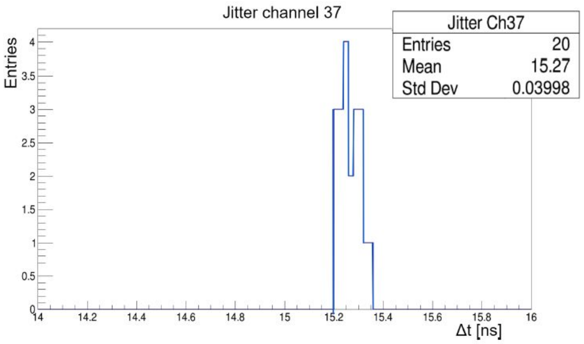
Single channel output signals: jitter time

- Jitter values ~ 50 ps.
  - ➡ Good temporal stability for this type of readout system;
  - ➡ Output jitter compatible with the input jitter ⟶ good data transmission through the readout prototype.

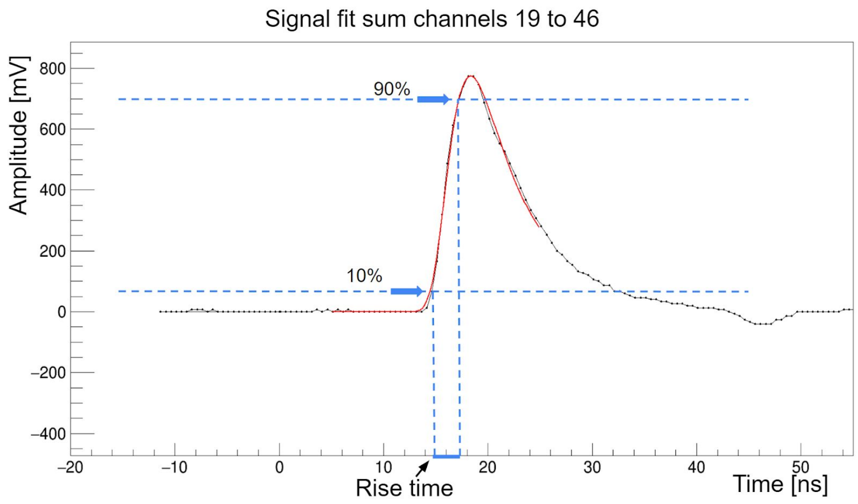


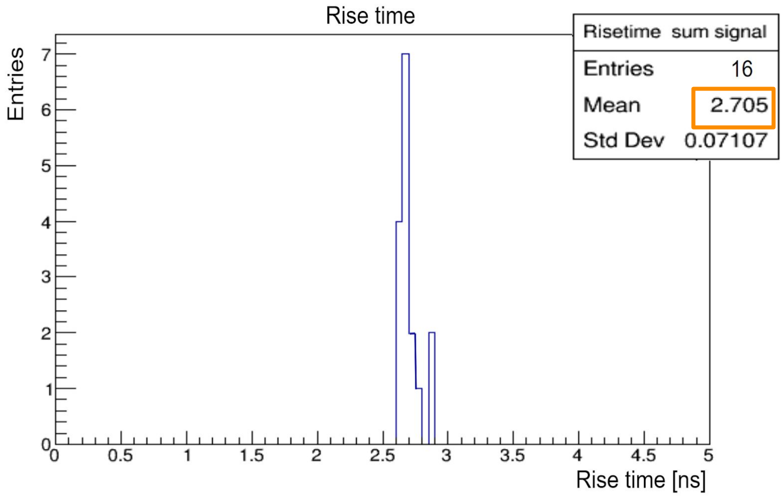






Signal stability as a function of the number of channels

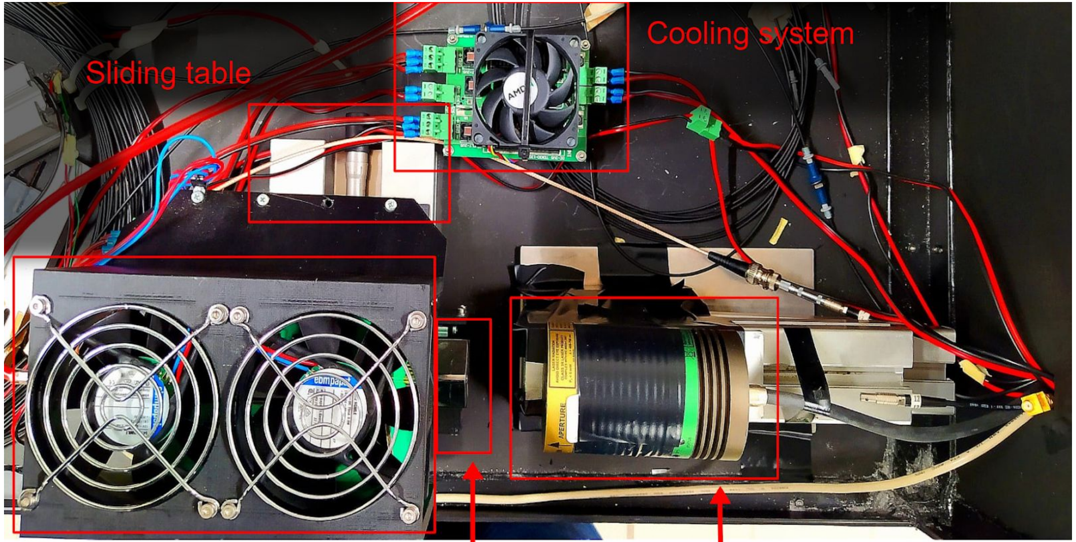




- Rise time value compatible within one standard deviation with the rise time of the individual channels.
- The operation carried out by the resistive networks to sum the analog signals does not alter the shape of the outputs.

Readout prototype tests with a MAPMT and a laser system

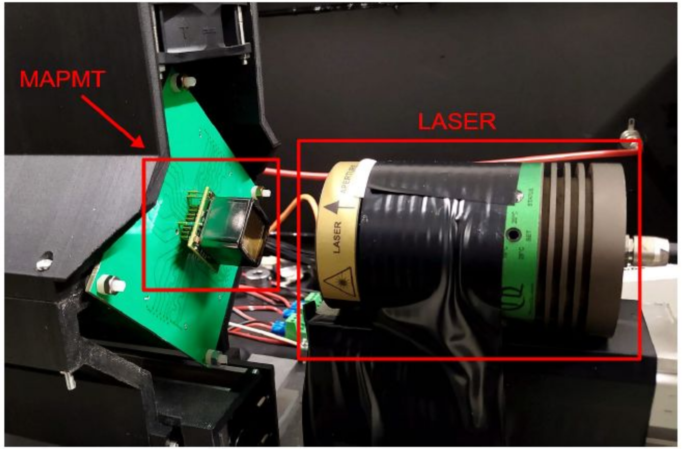
Test with MAPMT and laser: experimental setup



Readout prototype with cooling system

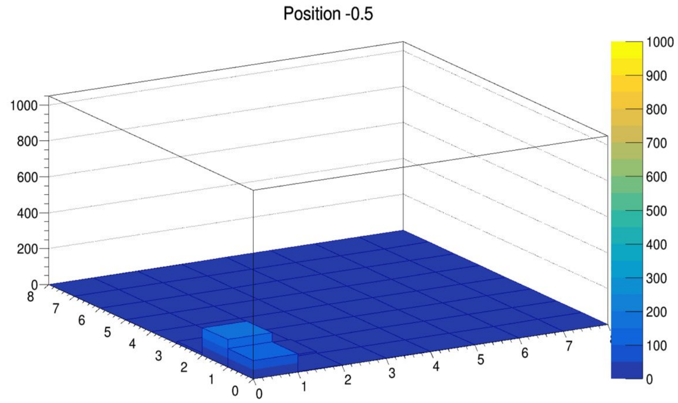
MAPMT

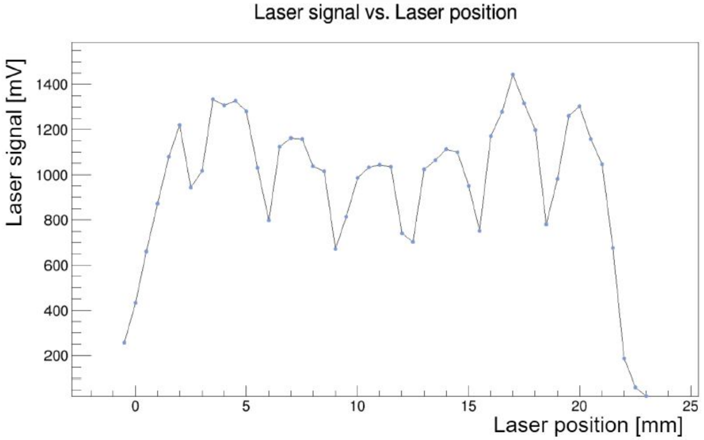
LASER

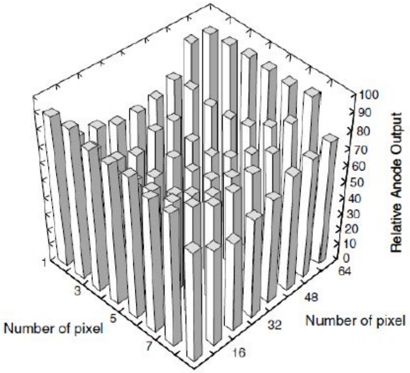


Scan of the MAPMT photocatode with a laser system

- The beam spot moves along the photocathode diagonal.
- Acquired the signal amplitudes for all 64 channels across 48 positions of the laser spot along the diagonal.
- Spot dimensions and optical crosstalk → the laser signal spreads in more than 1 channel.



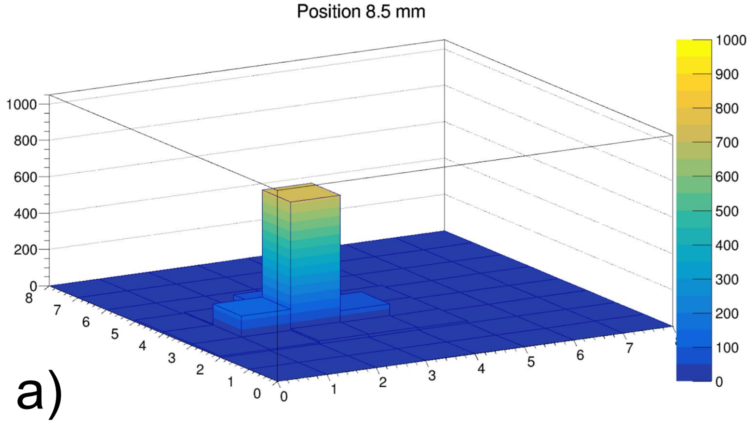


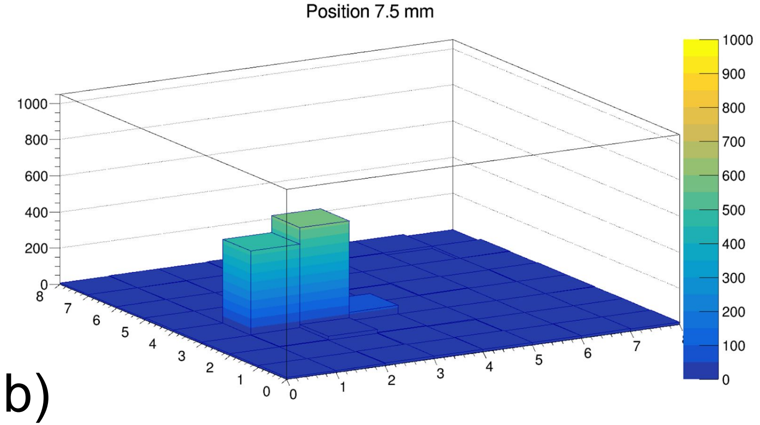


Two specific cases

a) The laser spot is centered on a given anode pixel of the MAPMT.

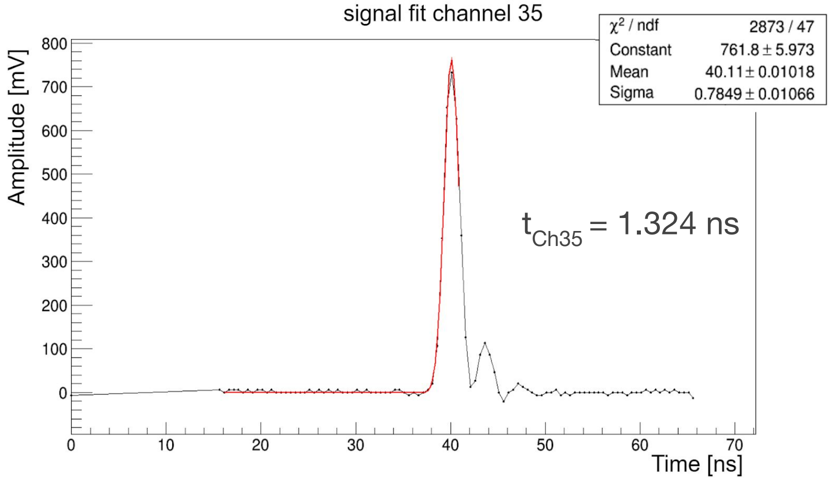
b) The laser spot is almost equally shared on two adjacent channels.



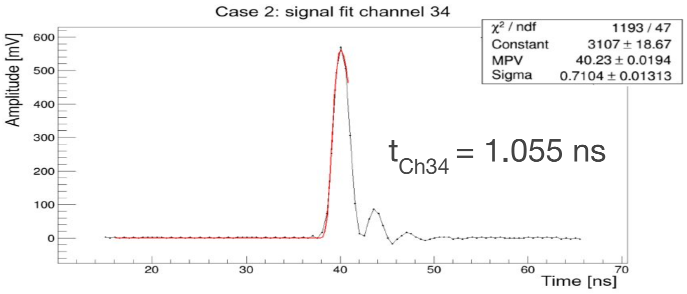


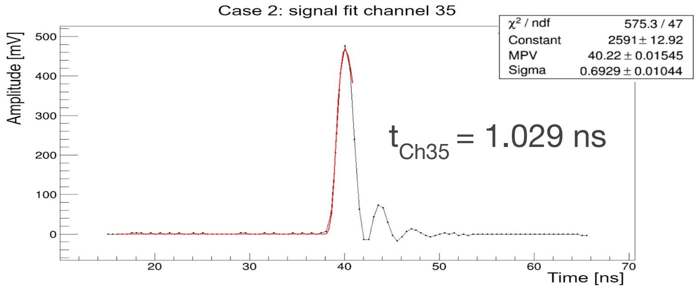
Single channel signals

1.



2.

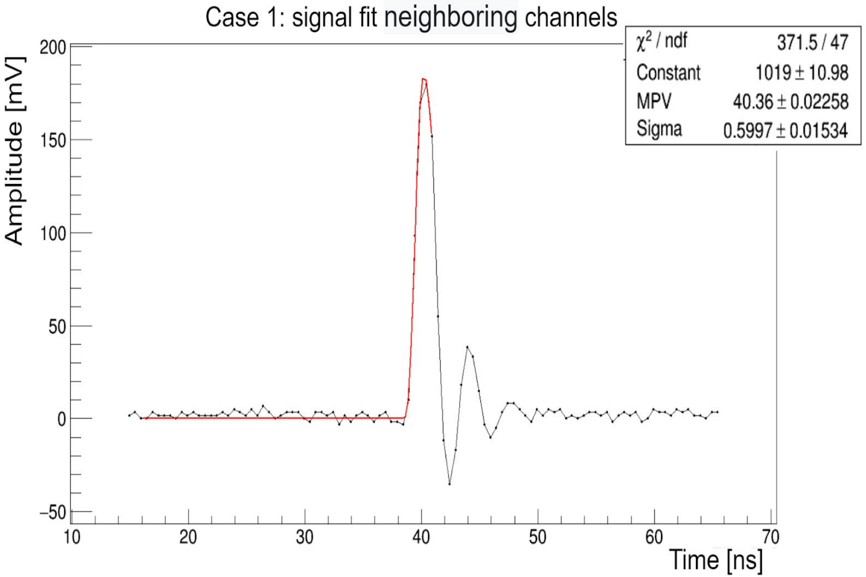




The rise time of *Ch35* is larger when it alone receives the most signal relative to the case when the signal is almost equally shared between *Ch34* and *Ch35*.

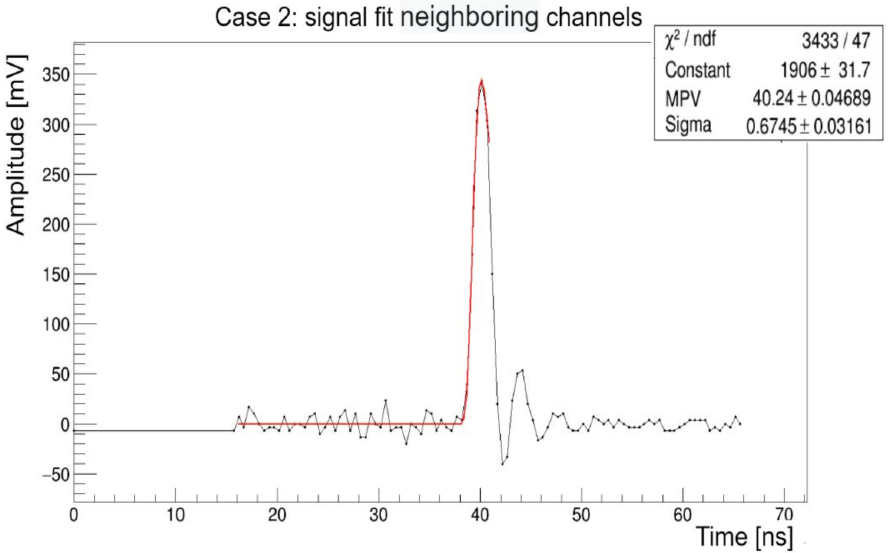
Analog sum of neighbouring channels

1.



$t_{sum}(8) = 1.002$ ns

2.



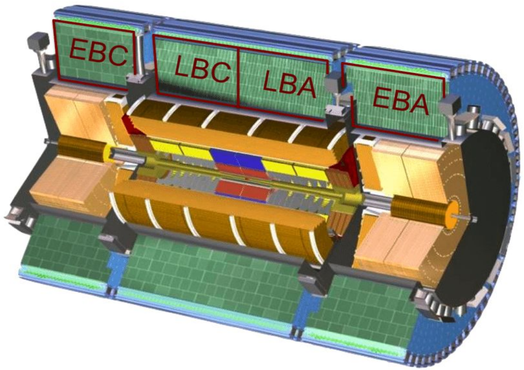
$t_{sum}(10) = 0.890$ ns

In both cases the signal rise time is larger for individual channels detecting the main part of the signal relative to the sum of the neighbouring channels.

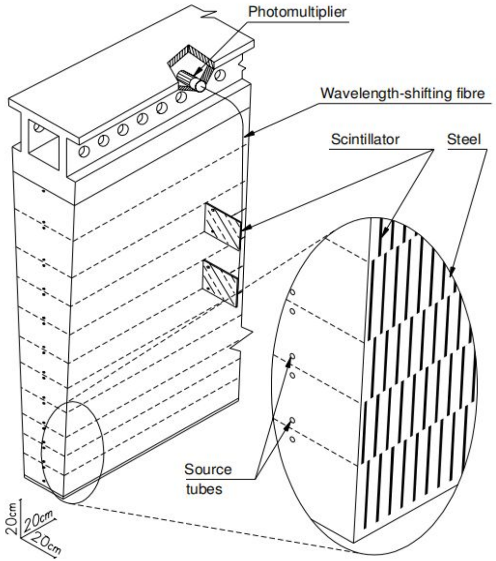
Prototype tests conclusions

- The readout prototype guarantees shape stability, in the analog sum of the signals (rise times ~ 2.7 ns);
- The resistive summing networks do not alter the shape of the outputs;
- Jitter time ~ 51 ps, good data transmission;
- Observed coupling effects between channel → minimal effect that does not alter the correct functioning.

TileCal calorimeter

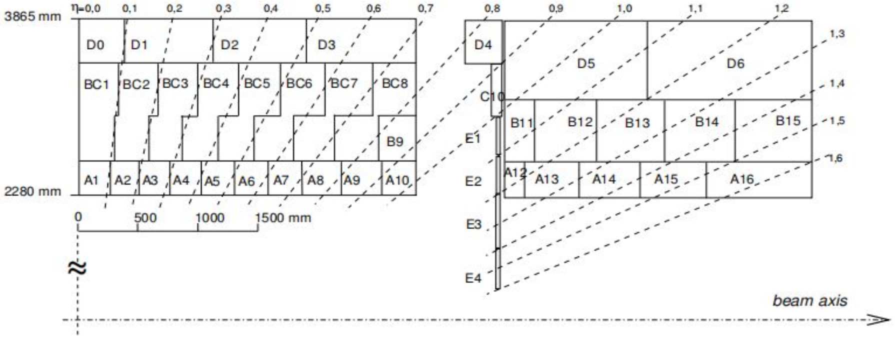


- TileCal (|η| < 1.7) is the central section of the hadronic calorimeter of the ATLAS experiment.
- Sampling calorimeter, composed by scintillating tiles (active material) and steel absorbers.



- 4 partitions: EBC,LBC, LBA and EBA;
- 64 modules (in each barrel), divided in 3 layers of cells read by 2 PMTs.

- The light produced in the scintillating tiles by crossing particles is collected by wavelength-shifting fibers (WLSs) and transmitted to PMTs.



General architecture for the new device (I)

- The solutions currently available on the market involve the digitization of too many signals.

- There are several advantages in this approach, and namely:
  - ➡ Possibility to apply digital filters to dump the noise,
  - ➡ Avoid problems of signal synchronization due to signal timing jitter in the digitization, time window,
  - ➡ Possibility to apply digital weights in the digital sum of different channels

  ….but <u>the cost of such a device could be unaffordable due to the very large number of channels to be digitized</u>

- We want to invert the concept flow chart:
  - ➡ first make an analog sum of selected subsamples of readout channels, than convert only the desired sum(s)

- The challenge is to avoid distortions of the time profile in the resulting analog sum and to keep at the same time all configuration flexibility that the other concept allows.