

Compact and Scalable Electronics for Sub-10 ps Timing in Particle Physics and Medical Imaging

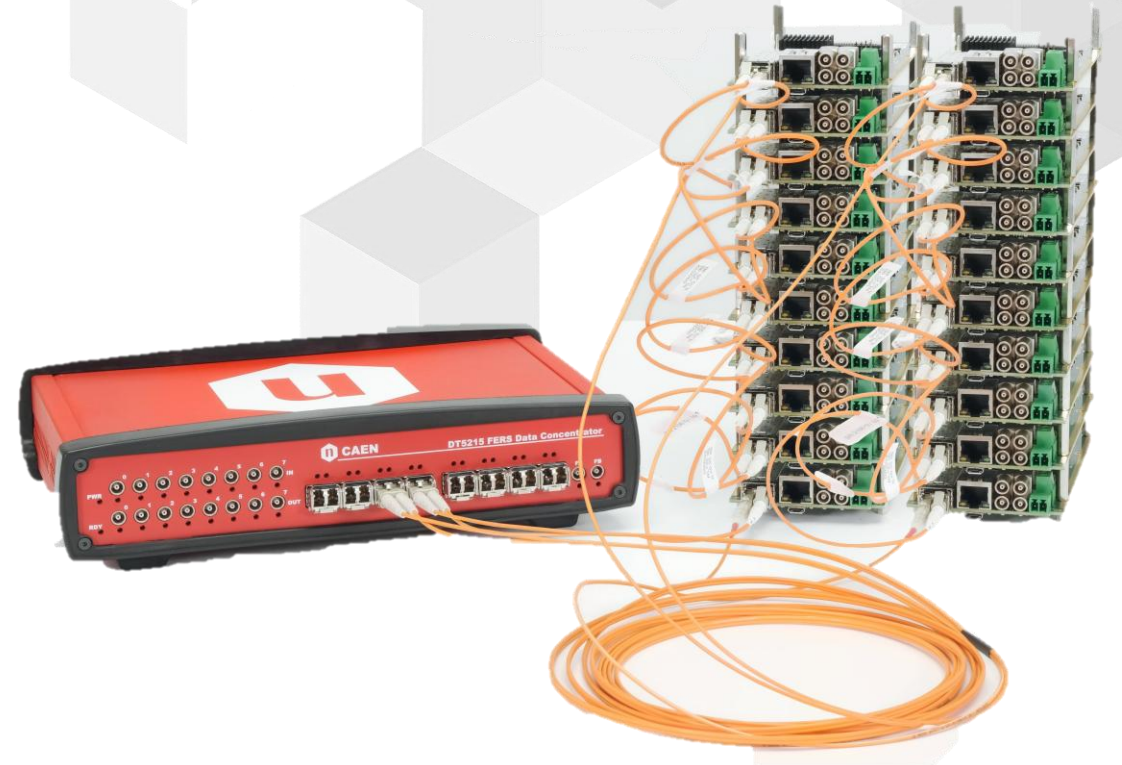
Yuri Venturini*,
y.venturini@caen.it

on behalf of

C. Tintori, Dr. A. Abba, Dr. C. Maggio, L. Colombini
Dr. D. Ninci, A. Mati, A. Picchi

Outline

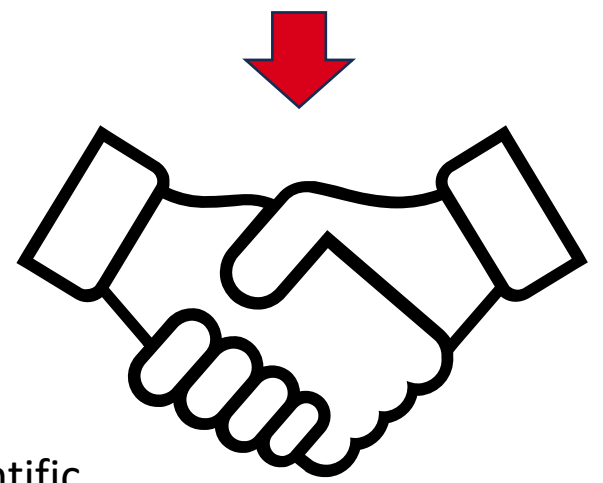
- FERS-5200 family: project core and architecture
- X5203: picoTDC timing unit
- Timing performances
- Feasibility study for SAND
- X5203 PET application: the Provision scanner
- Conclusions



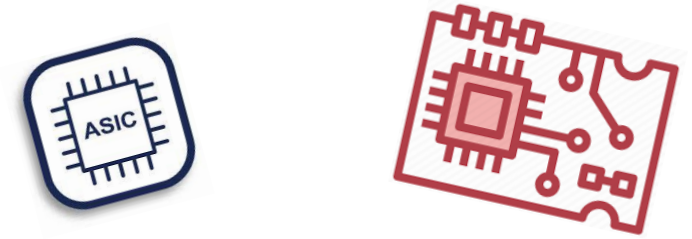
Front End Readout System 5200: The Core Idea



Off-the-shelf **front-end ASIC** for scientific instrumentation

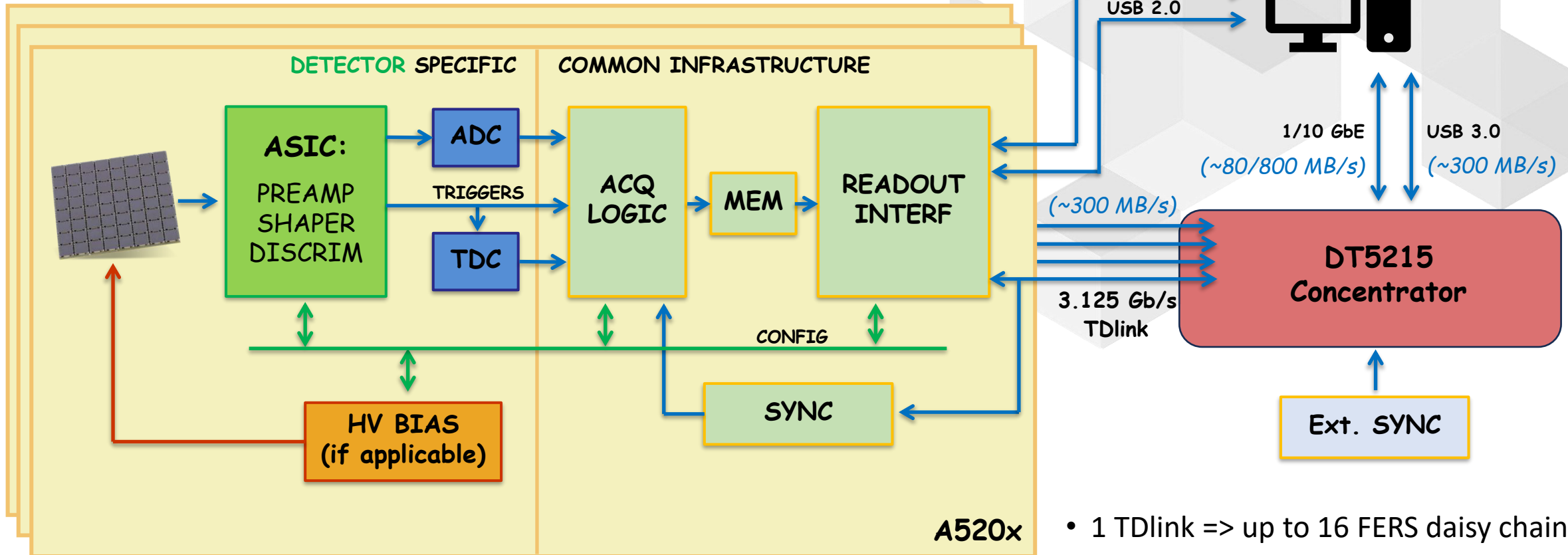


Design of **Readout Electronics and Power Supply** for NP and HEP



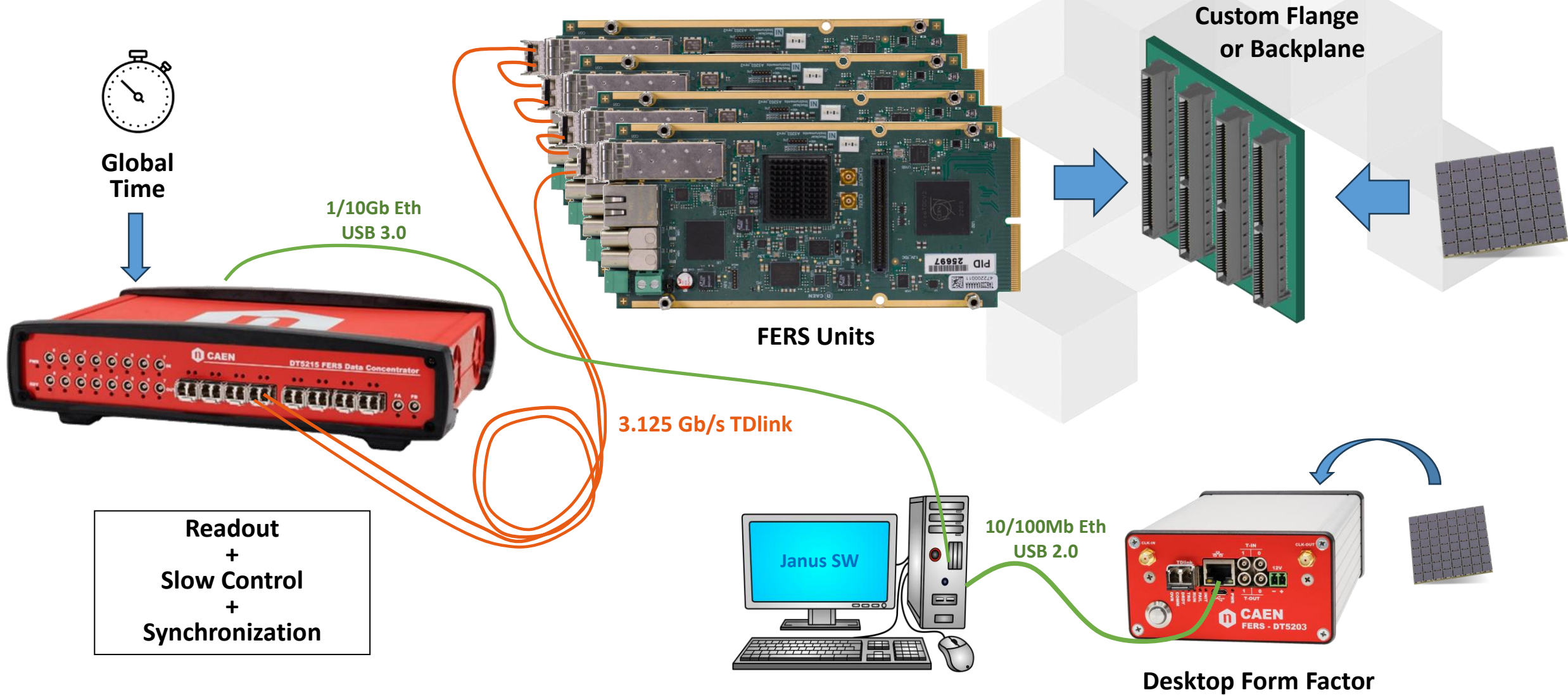
FERS-5200: block diagram

up to 128 FERS units



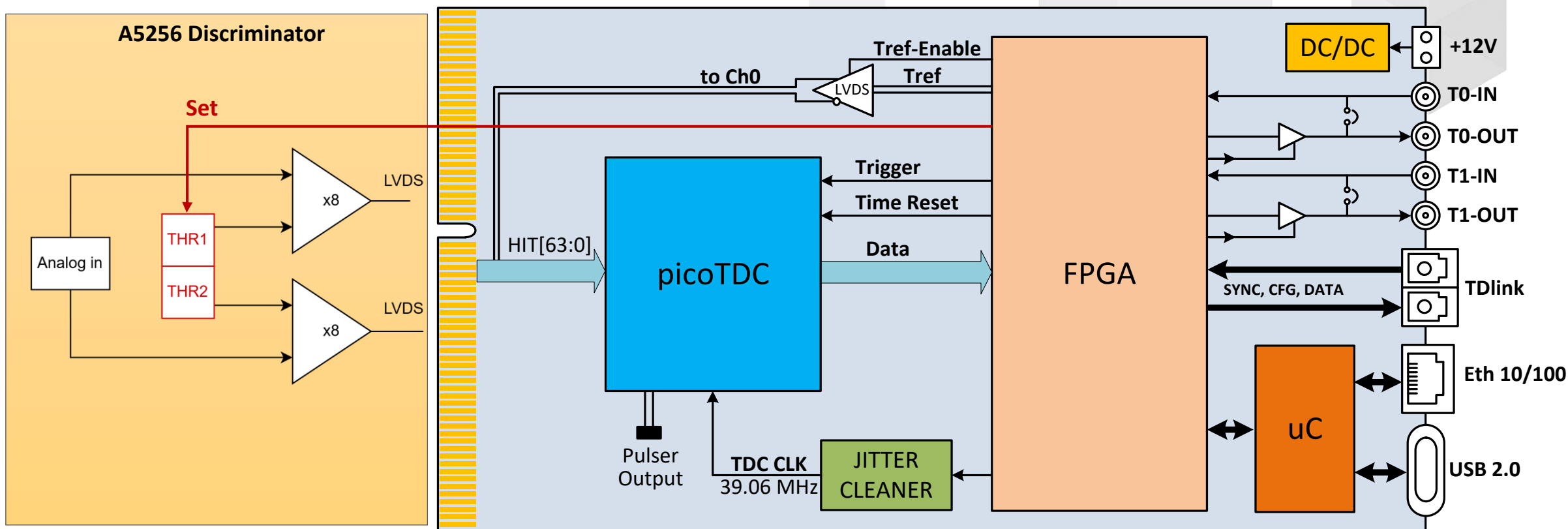
- 1 TDlink => up to 16 FERS daisy chain
- 1 DT5215 => 128 FERS = 8k/16k ch
- Sync to ext. GPS

FERS-5200 architecture



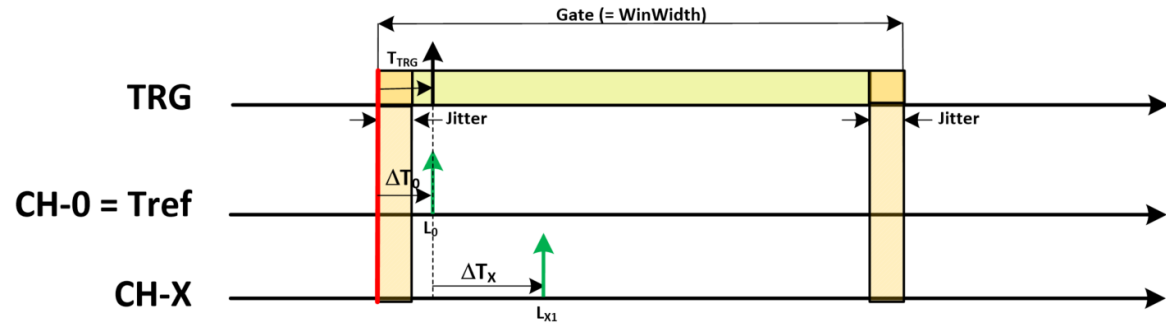
x5203: 64/128 channel 3.125 ps TDC

- **TDC:** 64/128 channels (1 picoTDC = 64 ch), LSB = 3.125 ps, dynamic range = 56 bit (extended by FPGA)
- **Inputs:** digital, LVDS → **A5256 Front-End** (= 16-ch discriminators)
- **Output Data:** Time of Arrival (ToA), Time over Threshold (ToT)
- **Data throughput:** up to ~64 Mcps/board

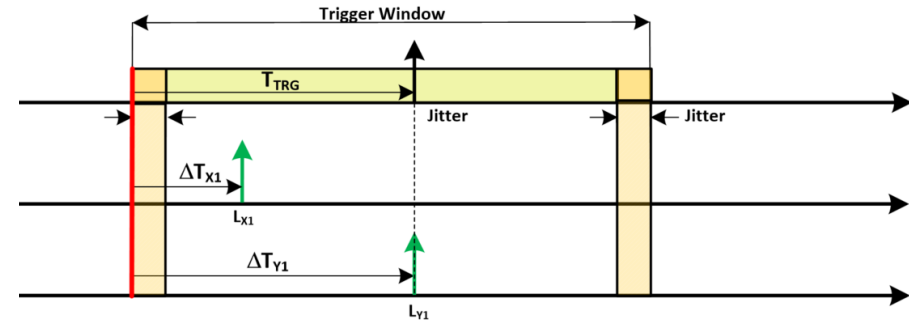


X5203 performances

Acquisition modes: Common Start/Stop (Tref=Ch0), Trigger Matching, Streaming



DATA
 - T_{TRG}
 - $CH0: ToA_0 = \Delta T_0$
 - $CHX: ToA_{X1} = \Delta T_{X1}$

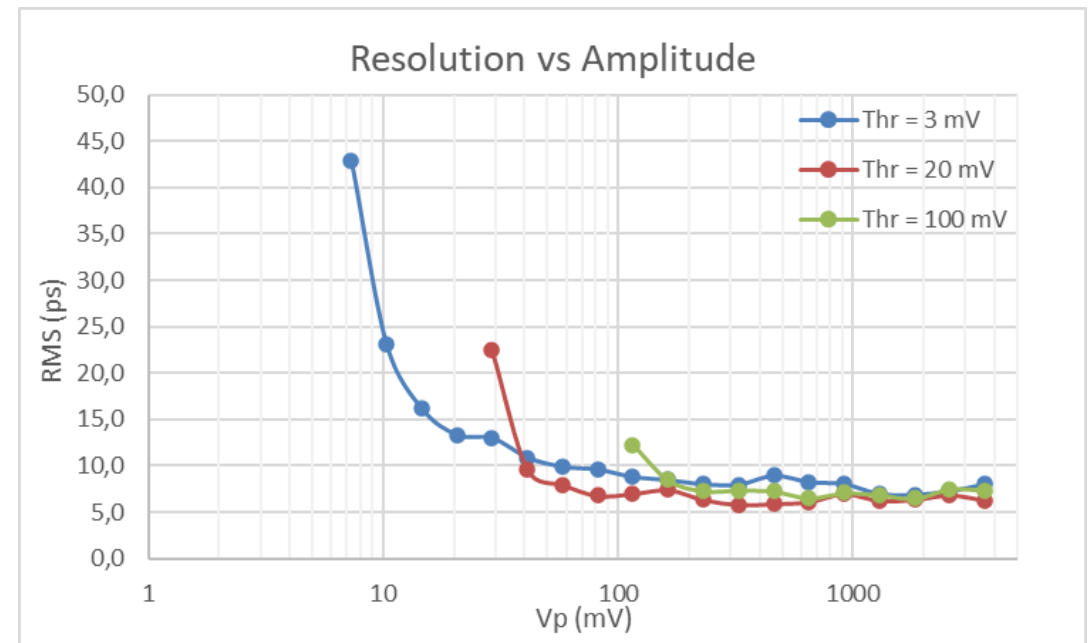


DATA
 - T_{TRG}
 - $CHX: ToA_{X1} = \Delta T_{X1}$
 - $CHY: ToA_{Y1} = \Delta T_{Y1}$

DeltaT Resolution (*) :

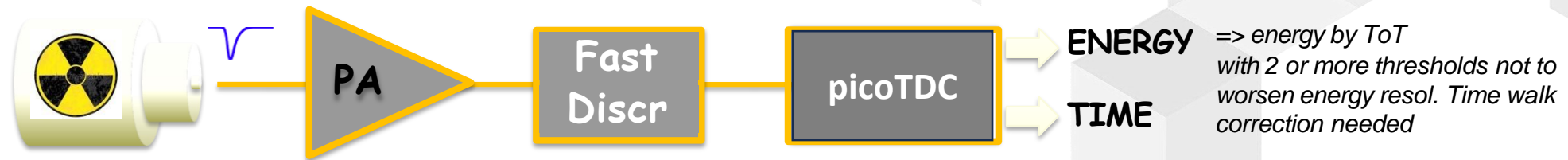
- Same board: **typ 5 ps RMS**
- Board to board: **~20 ps RMS** → Precision of the TDLink sync synchronized by DT5215 Concentrator Board via TDlink
- Board to board: **~8 ps RMS** synchronized by DT5215 Concentrator Board via TDlink with auxiliary daisy chain/fan out clock cables

(*) Tested with CAEN A5256 discriminator. Pulse: 0.5 Vpp, 0.8 ns rise time



Energy reconstruction

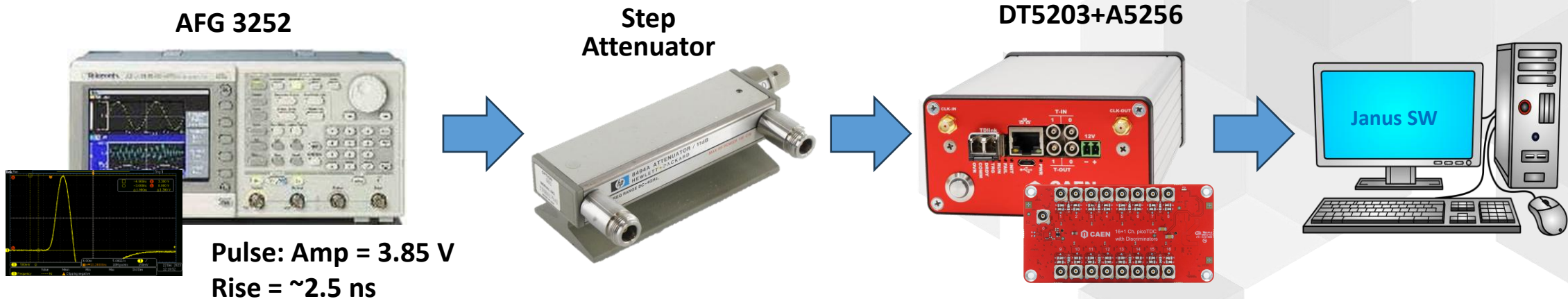
x5203 Pros	x5203 Cons
<ul style="list-style-type: none"> • high timing resolution (~ 5 ps), high channel density, almost no dead time • provides ToA and ToT in one word 	<ul style="list-style-type: none"> • ToA affected by walk effect • No energy information (PHA) acquired -> need for a separate ADC readout chain



-> ToT-Based Analysis: Walk correction and PHA

- **ToT** can be used to **correct for time walk** => no need of Constant Fraction Discriminator in hardware
- **ToT** can be used to **reconstruct pulse amplitude**: ToT – PHA curve is not linear => need calibration (pulse shape dependent)
- **FPGA ToT filter**: rejects pulses if **ToT < LowCut** or **ToT > HighCut** (remove noise, DCR, saturation...)

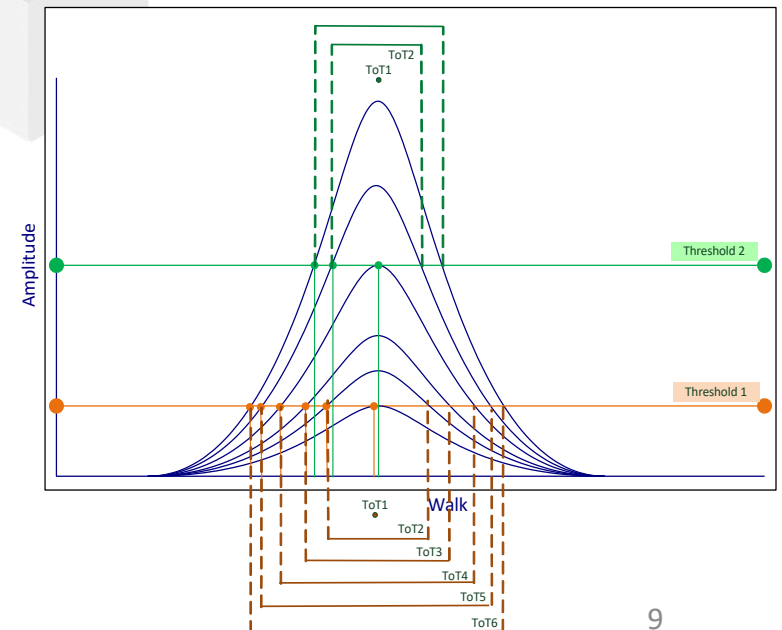
ToT Analysis Setup



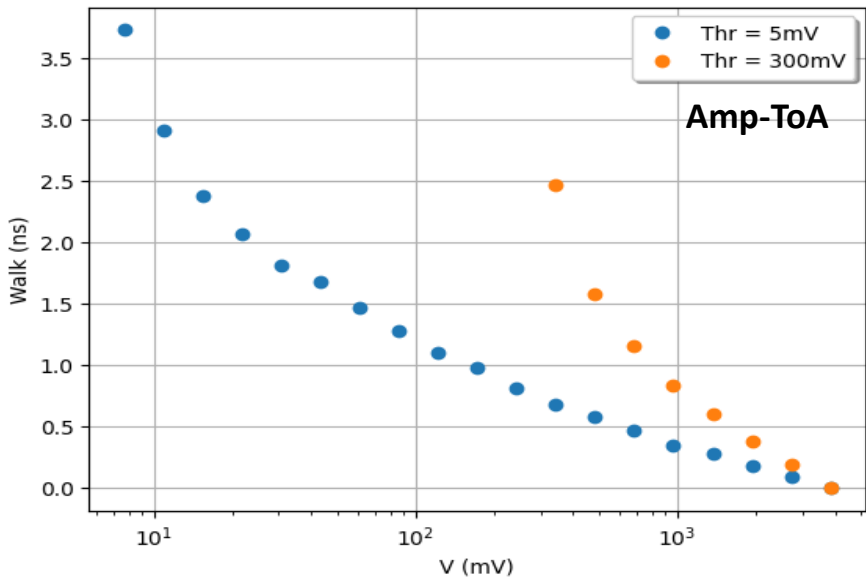
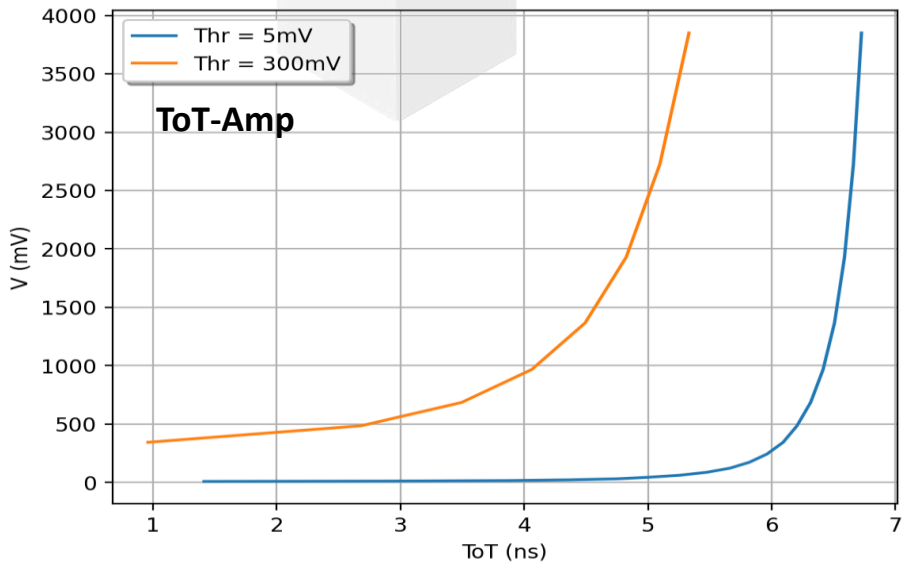
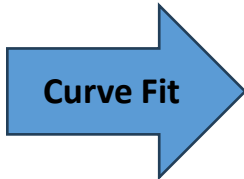
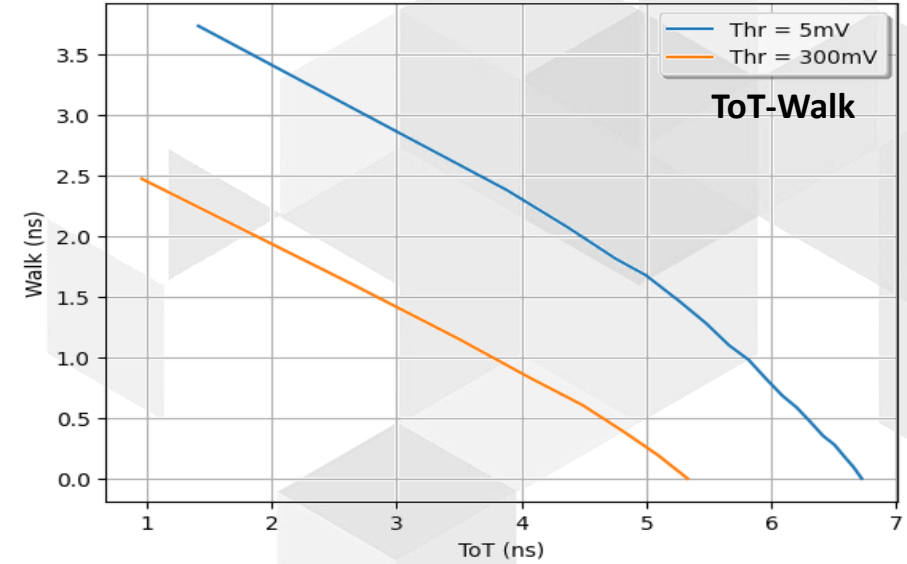
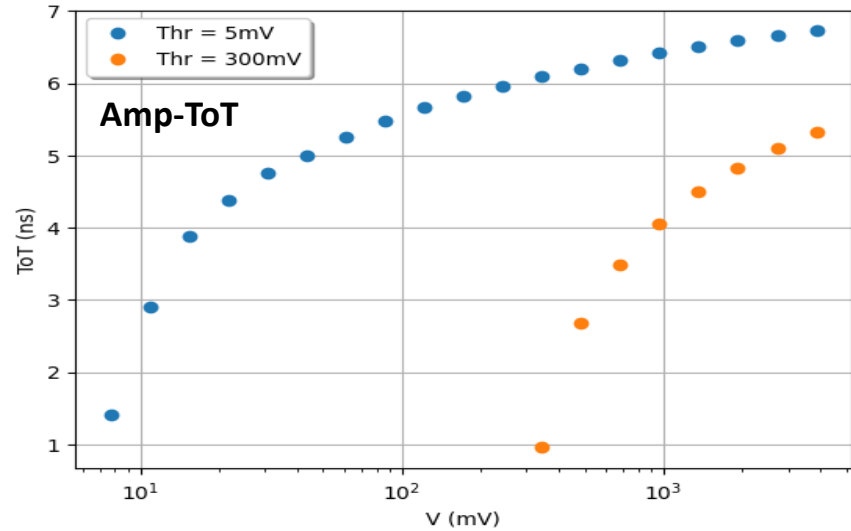
Pulse: Amp = 3.85 V
Rise = ~2.5 ns

Common Start Acquisition: start on Ch0 with fixed amplitude, stop on Ch1 and Ch2 (dual threshold) with variable amplitude (max = 3.85 V). Delay = 13 ns

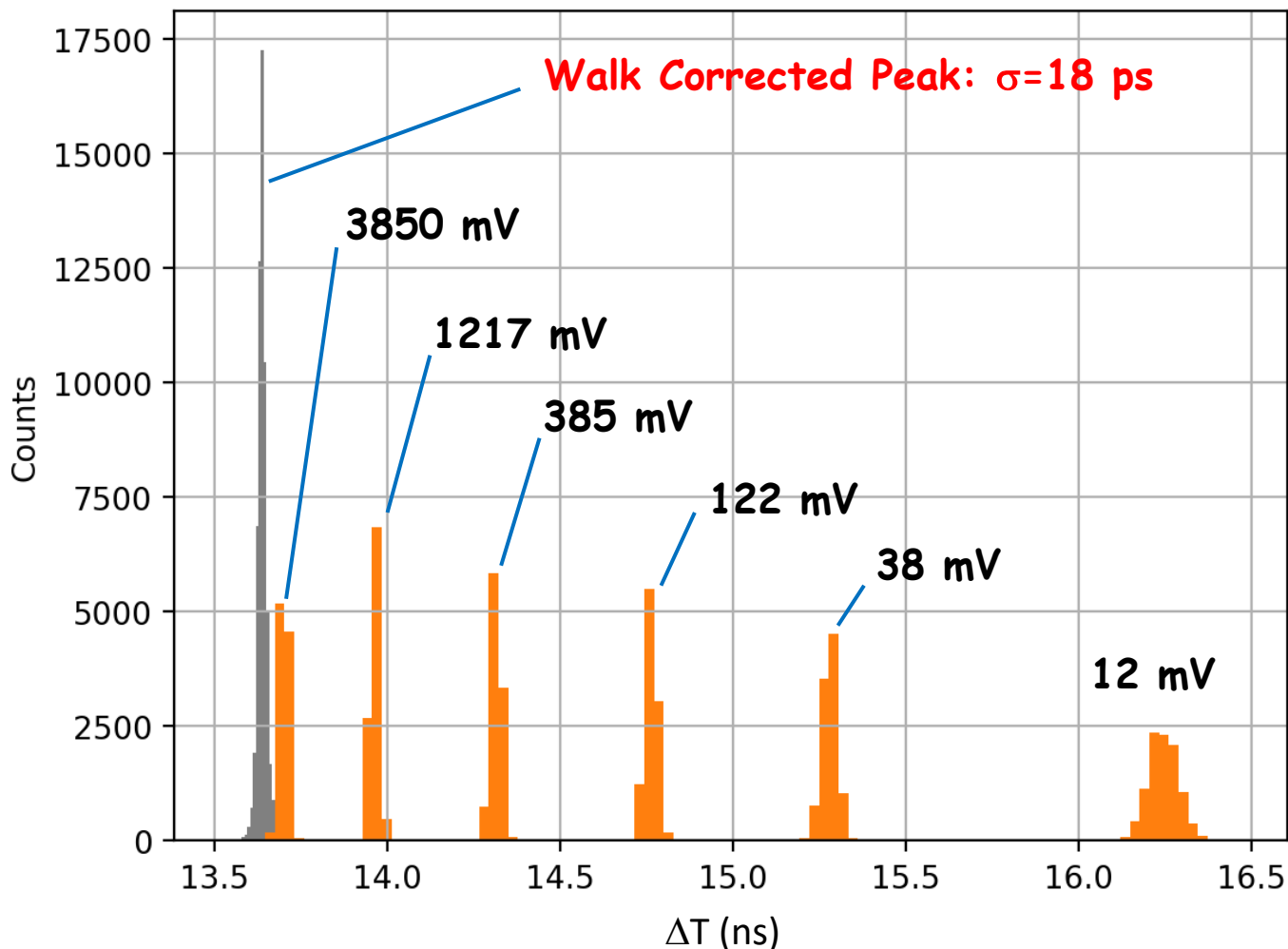
1. **Sweep:** acquire **ToT** and ΔT (**ToA**) at different amplitudes (from 0 to 54 dB, 3 dB step)
2. Fit points and build **ToT-Walk (ToA)** and **ToT-Ampl** curves
3. Use curves to **correct Walk** from ToT (replace CFD)
4. Use curves to **get Amplitude** from ToT (make ADC from TDC)



ToT calibration curves (double threshold)

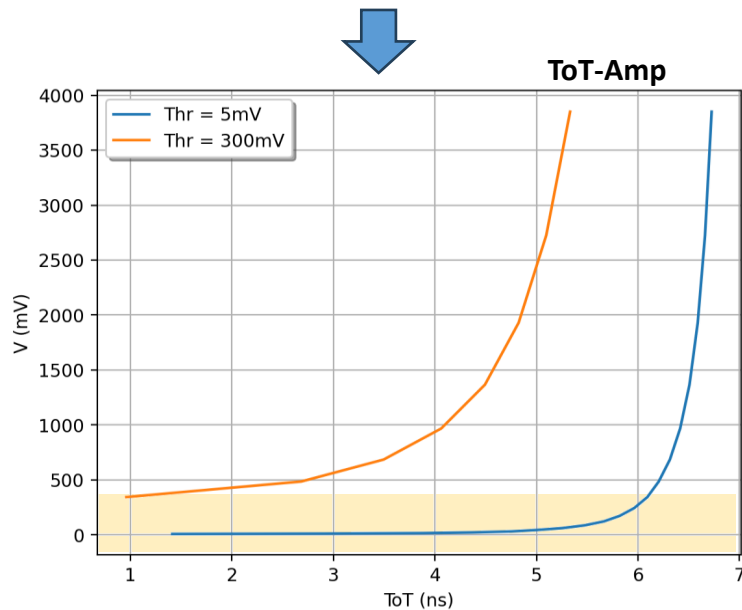
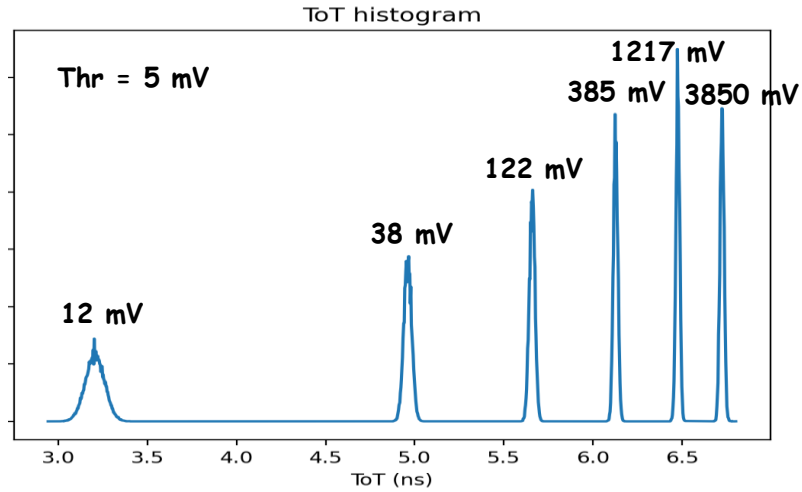


Walk Correction

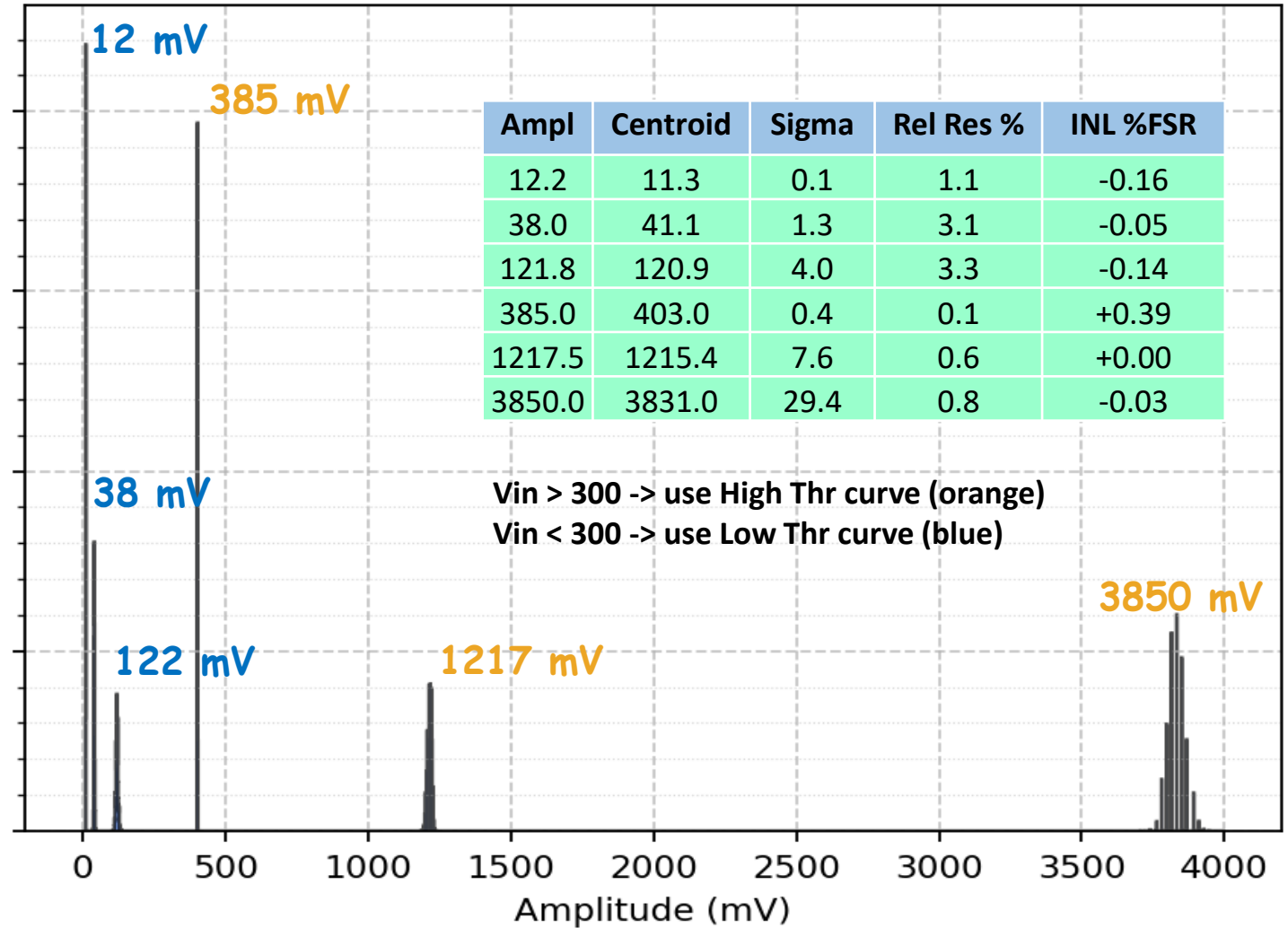


- Pulses at 6 different amplitudes over a 50 dB dynamic range
- ~ 2 ns spread on ΔT (ToA) caused by the walk effect: 6 separate peaks !!
 - ➔ timing resolution totally destroyed
- ΔT corrected by ToT using a 5th order polynomial fit of the **ToT-Walk** points taken at threshold = 5 mV
- Corrected ΔT histogram presents one single peak:
 - 18 ps RMS over 50 dB dynamic range**

Amplitude Reconstruction

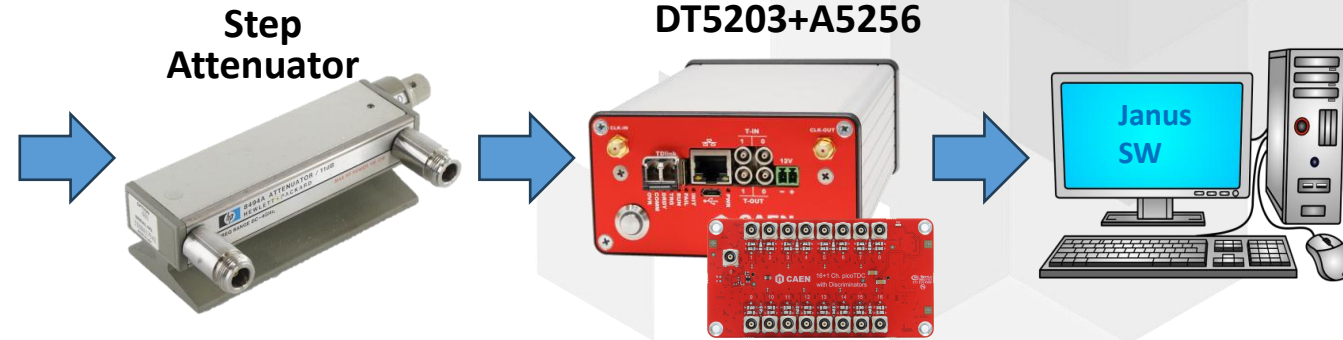


Amplitude histogram



Feasibility study for SAND calorimeter

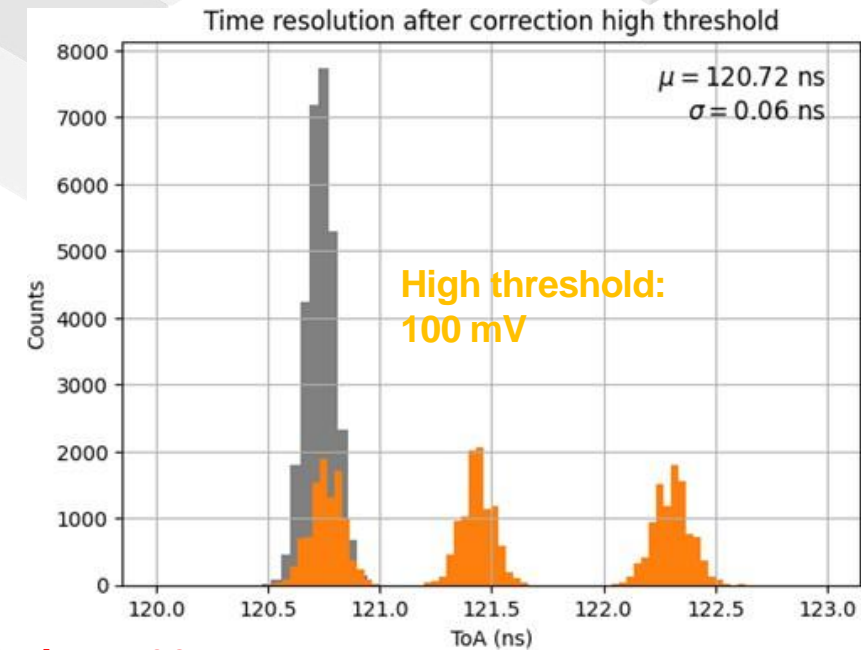
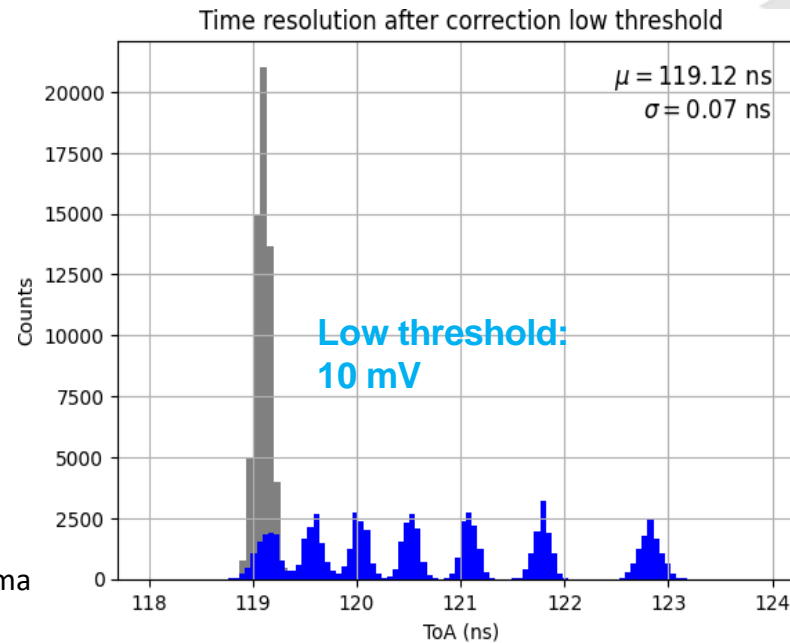
PMTs + Led Driver



Ongoing feasibility study of the ToT technique for the readout of **5000 PMTs** in SAND (DUNE)

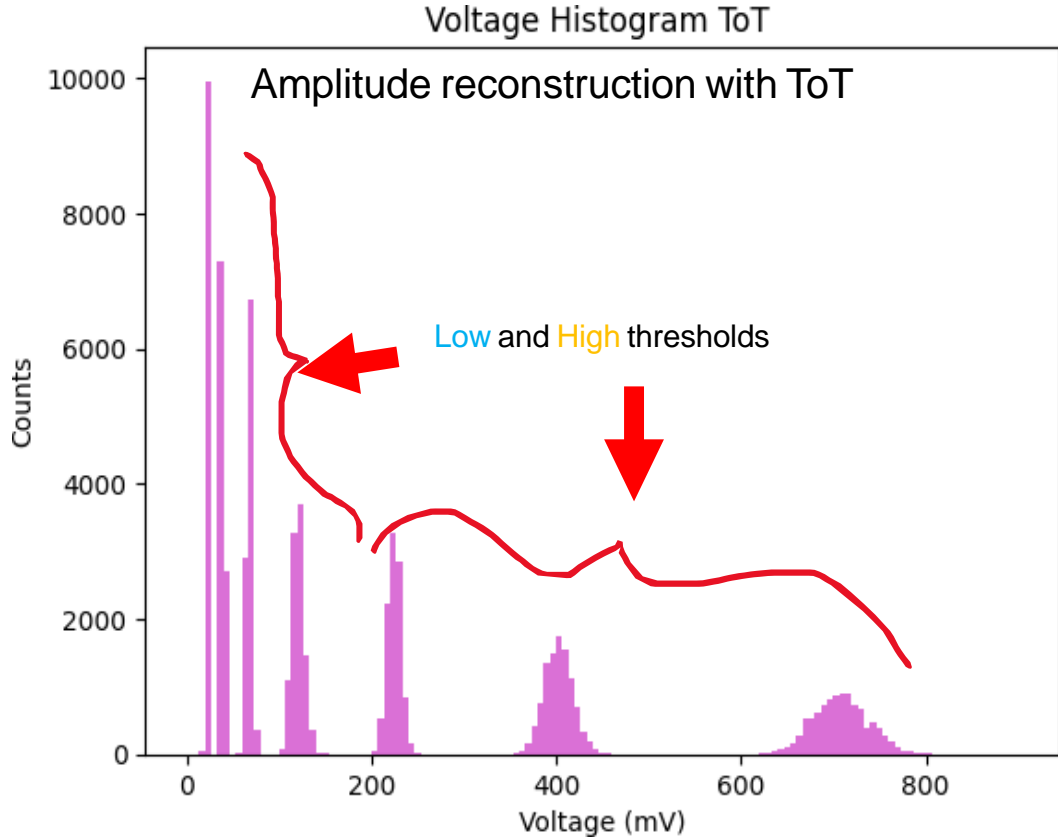
- Led Driver CAEN SP5601 ($\lambda \sim 400$ nm) + fiber splitter
- PMT signal \rightarrow variable amplitude
- DT5203 + A5256 \rightarrow dual threshold

Courtesy of A. Di Domenico, V. Di Silvestre, P. Gauzzi - INFN Roma



Time Resolution ~ 60 ps

Feasibility study for SAND calorimeter

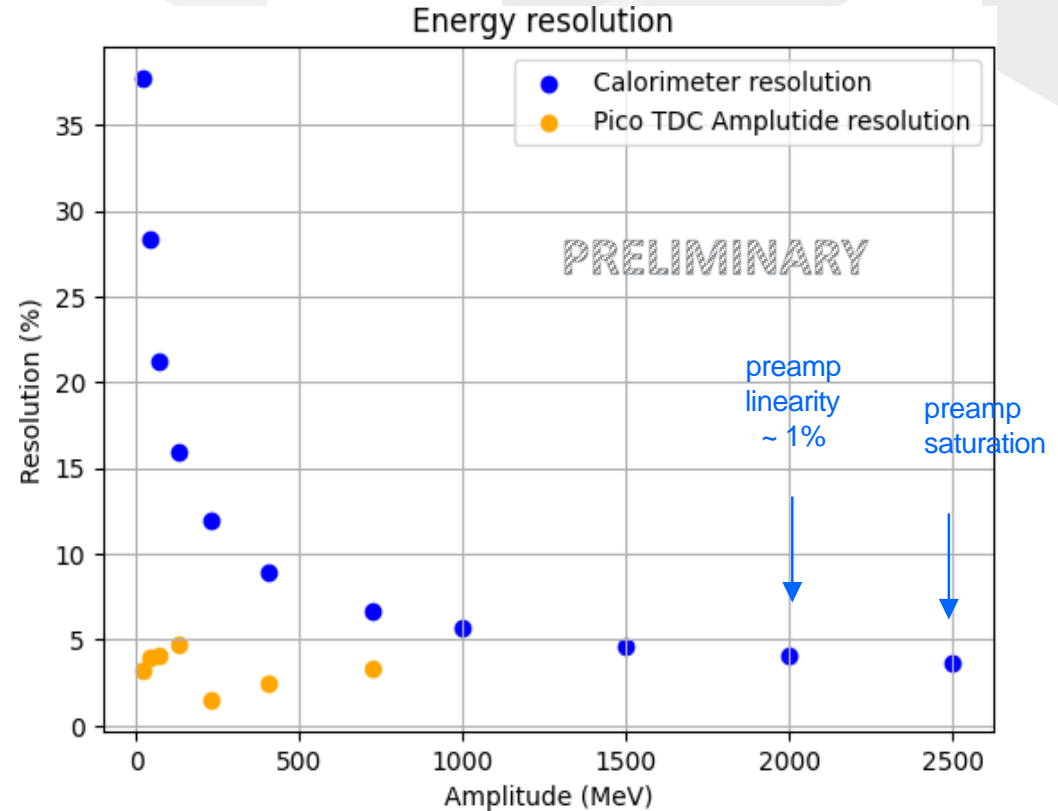


comparison with calorimeter resolution
 ($\sigma_E/E \sim 5.7\%/\sqrt{E}$)

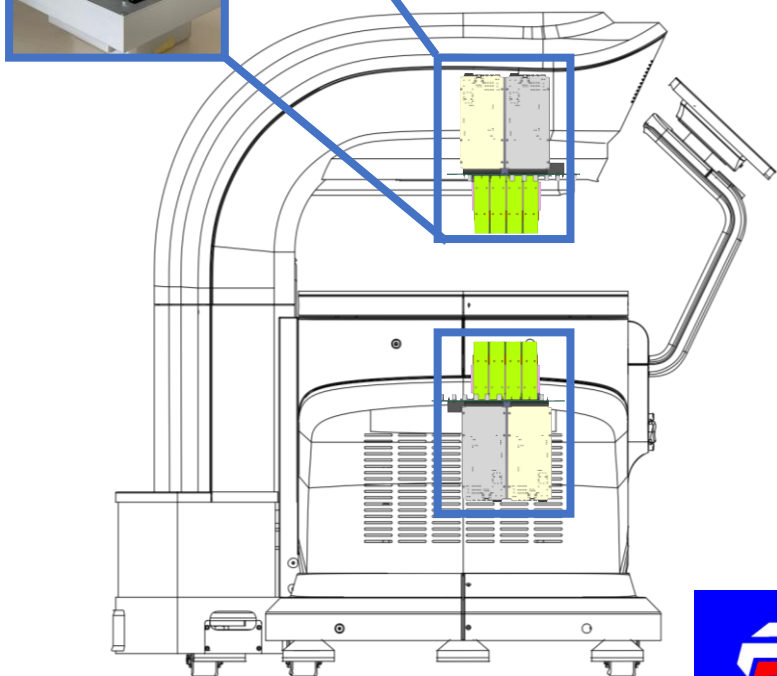
Courtesy of A. Di Domenico, V. Di Silvestre, P. Gauzzi - INFN Roma

Amplitude resolution obtained from ToT is compared with the intrinsic calorimeter resolution (assuming PMT gain 1 mV = 1 p.e. = 1 MeV => 1 V = 1 GeV)

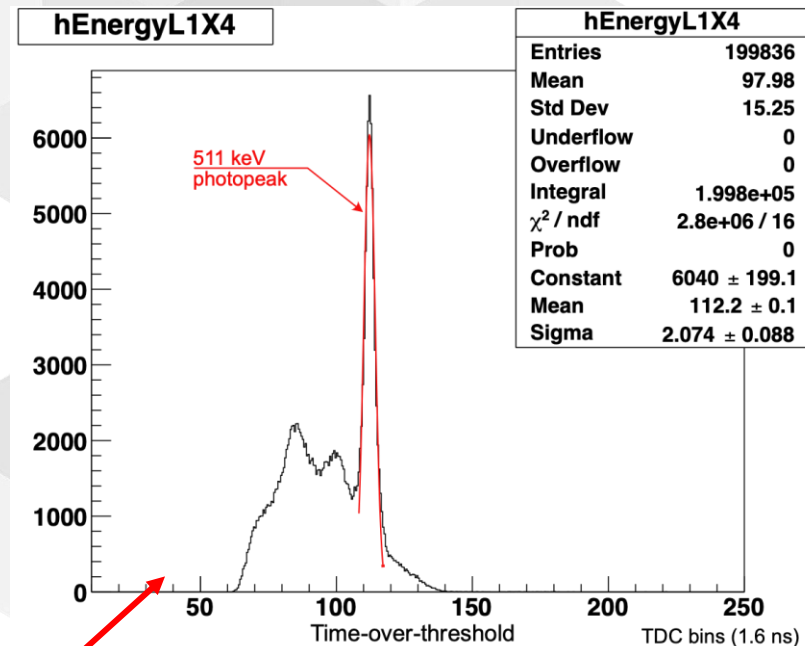
to be done: optimization of the thresholds for the best performance in the whole expected dynamic range (2.5-2000 mV)



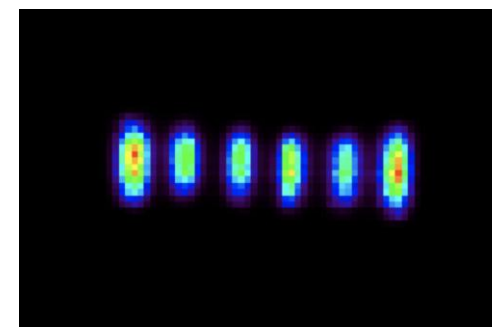
The Provision PET Scanner



- 2x768 SiPM channels
- 2x6 A5203Bs (128 ch TDC)
- 1 DT5215 Concentrator
- Precise timing and TOT measurement
- High throughput – almost zero deadtime
- ToT cut for Dark Count and noise suppression



'Empty' region thanks to TOT filter



Conclusions

- **ToA and ToT** measurements with a resolution of **5 ps RMS**
- **Walk correction** (mimic CFD) possible with single or double threshold: **18 ps RMS on a 50 dB dynamic range**
- **Amplitude reconstruction** (mimic ADC) requires at least 2 thresholds (2 TDC channels). **Linearity = ~0.4%. Resolution = ~3%**. Possible improvement with a more accurate threshold setting
- Optimal results in the Provision PET scanner: **few mm size radioactive sources easily detectable thanks to the excellent x5203 time resolution**
- Challenge: build ToA vs.ToT calibration curves in a real data acquisition case
 - ➔ Machine learning ???

- New FERS Units embedding the picoTDC +
 - ➔ Radioroc chip: **SiPM**
 - ➔ Psiroc chip: **GEMs, Si strip**

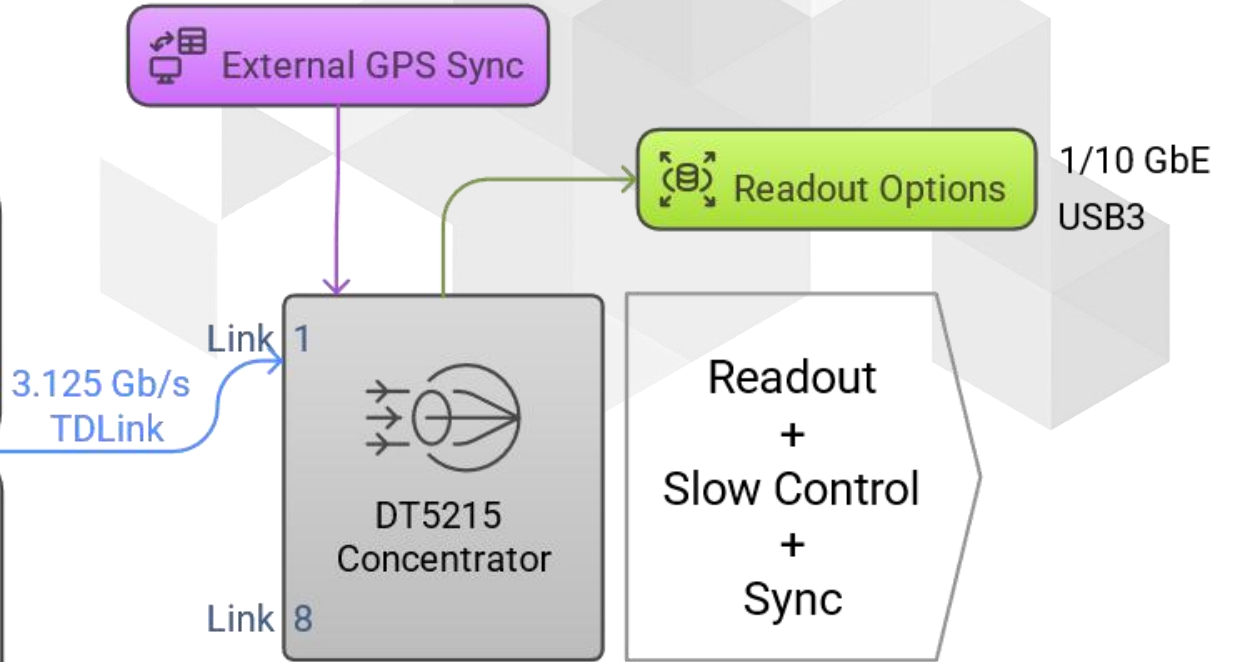
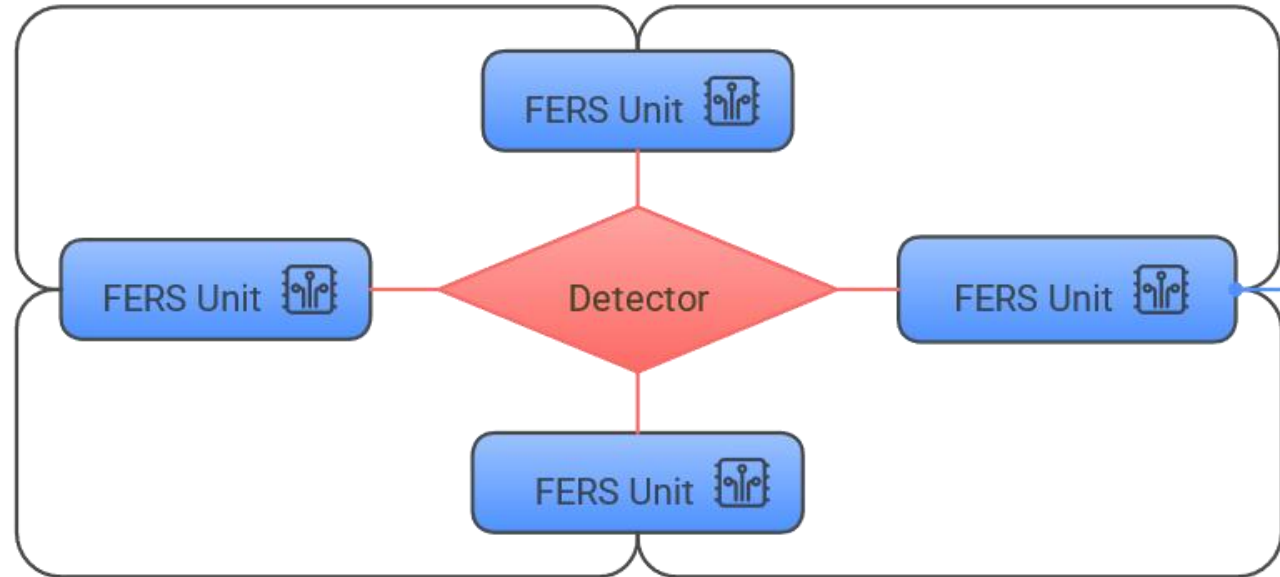


Thank you!

**Back-up
slides**

FERS-5200 architecture

Daisy chain --> Expansion up to 16 FERS/link --> 8/16k ch.



FERS-5200 Family

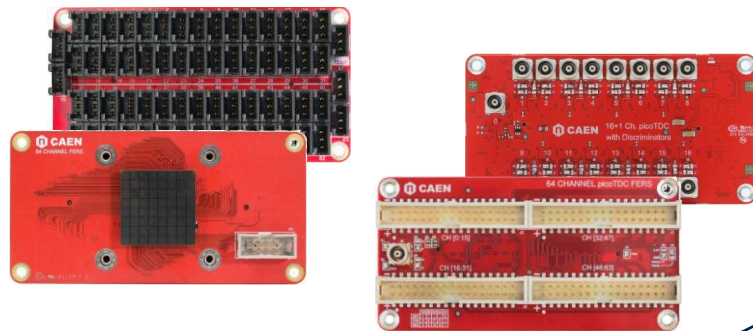
FERS-5200 Units



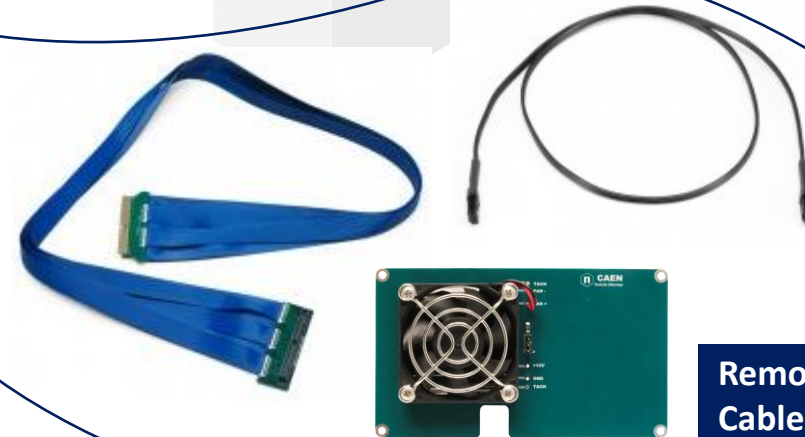
DT5215 Concentrator Board



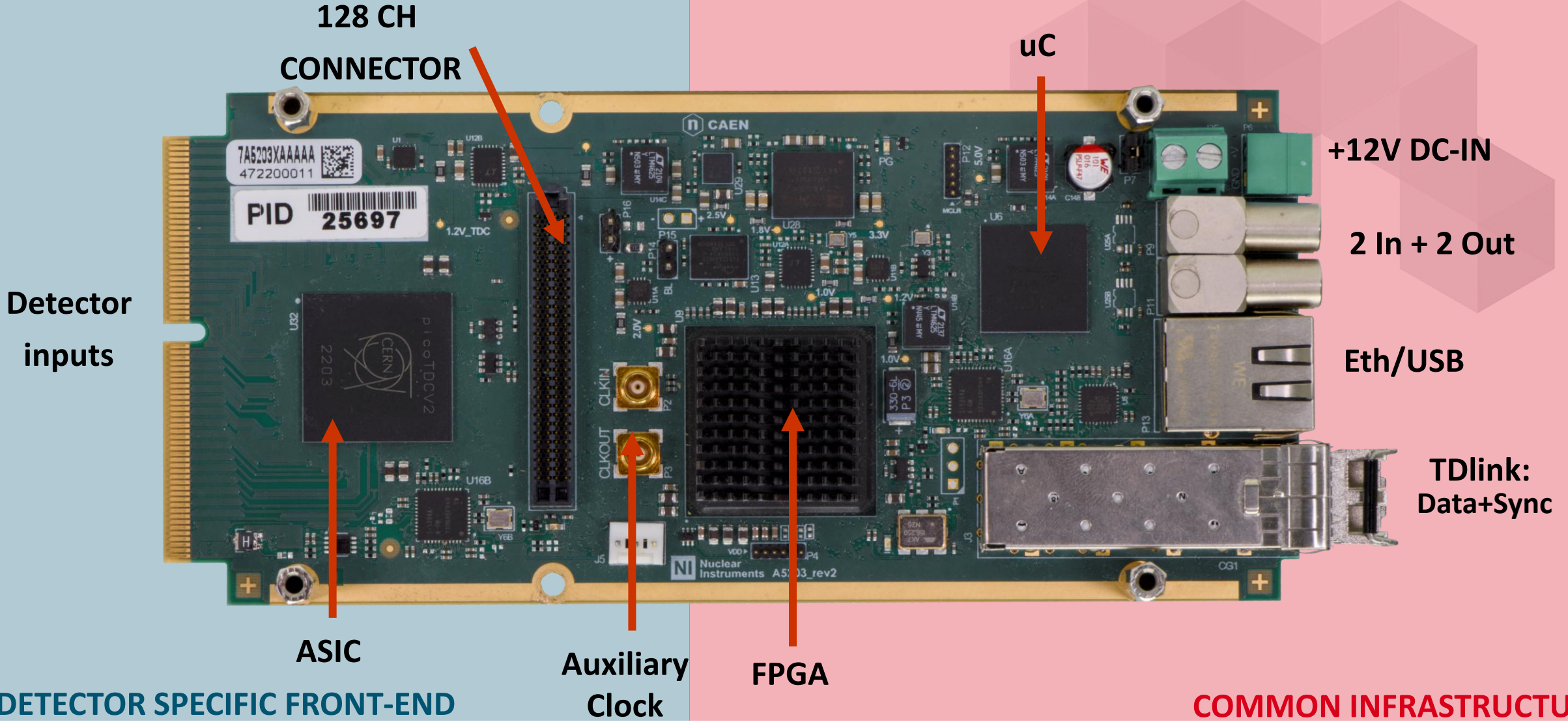
Adapters



Remotization
Cables &
Accessories



FERS A5203: 64/128 channel Readout



DETECTOR SPECIFIC FRONT-END

COMMON INFRASTRUCTURE

FERS Units: A520X(naked)/DT520X(boxed)



A5205

64 ch – Psiroc+picotDC

COMING SOON

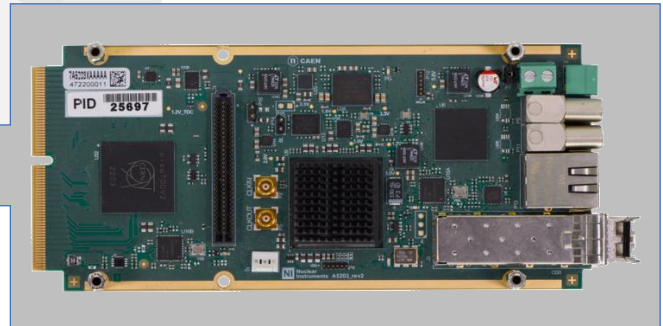
A5204

64 ch – Radioroc+picotDC

- **MPPC bias**
- **Spectroscopy (PHA)**
- **Timing**

A5203

64/128 ch - picotDC



A5202

64 ch – Citiroc 1A

- **Time Measurements (ToA & ToT)**
- **Amplitude Estimation**

Technical Specifications A5204 & A5205

COMING SOON

A5204: 64 channel SiPM Readout based on Citiroc/Radoroc+picotDC

- Analog inputs (charge, not voltage)
- All-in-one readout: Preamp + Shaper + Discr + ADC + TDC + HV Bias (20-80 V)
- Dynamic Range: 1 to 2500 p.e.
- Single photon detection (threshold at 1/3 p.e.)
- Timing resolution = 55 ps FWHM (A5204 only)
- **Acquisition Modes: Counting, Spectroscopy (PHA), Timing (ToA + ToT) , Mixed (PHA + ToA)**

A5205: 64 channel SSD, GEM, PIN diode readout based on Psiroc + picotDC

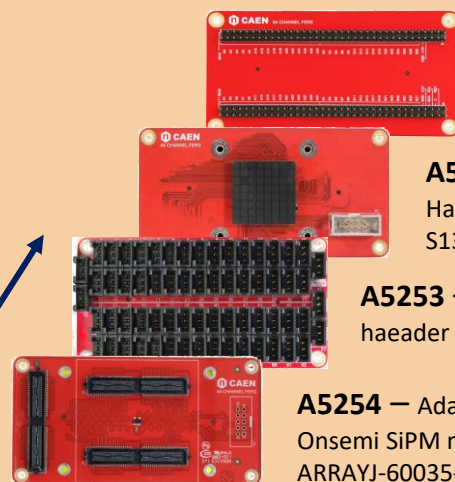
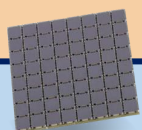
- Pos/Neg inputs. Dynamic range up to 5 pC with PHA, 100 pC with ToT
- Programmable gain: 125 mV/pC up to 4 V/pC. Min trigger threshold = 0.5 fC
- Linearized ToT

Different combos for all customers' needs

A5202

A5204

Detector

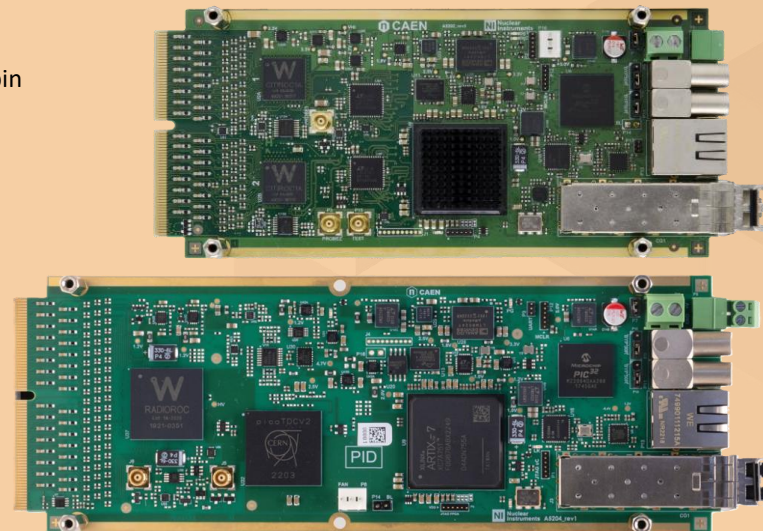


A5250 — 2.54 mm pin header adapter

A5251 — Adapter for Hamamatsu SiPM matrix S13361-3050AE-08

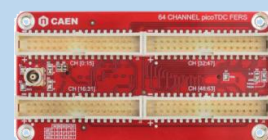
A5253 — 3-pin connectors haeader adapter

A5254 — Adapter for Onsemi SiPM matrices ARRAYJ-60035-64P-PCB, ARRAYC-60035-64P-PCB



64 CHANNELS:

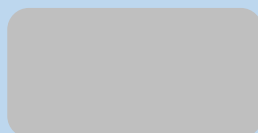
- ➔ MPPC bias
- ➔ Spectroscopy (PHA)
- ➔ Timing



A5255 — 4x17 2.54 mm pin header connectors adapter



A5256 — 16+1 channel single threshold, 8+1 channel dual threshold edge discriminator adapter



CUSTOM

A5203

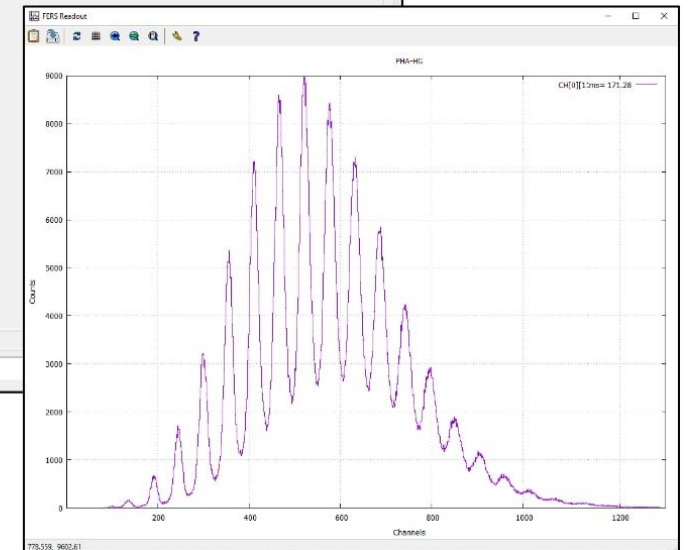
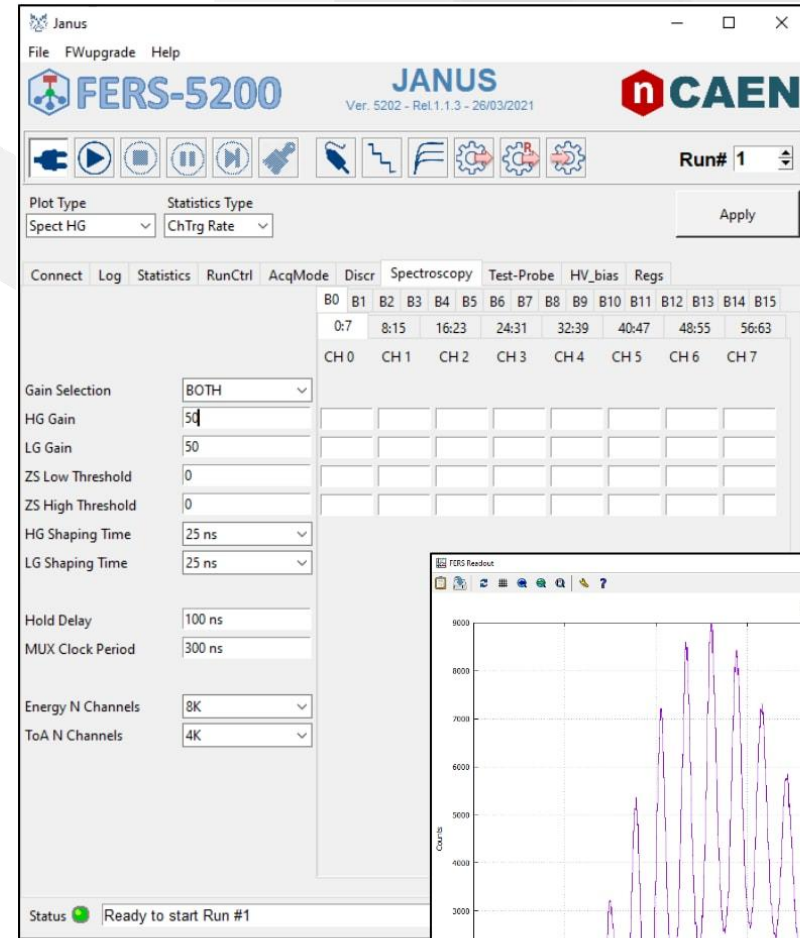


64/128 CHANNELS:

- ➔ Time Measurements (ToA & ToT)
- ➔ Amplitude Estimation

Janus Software

- **Open source** software for multi-board configuration and data readout
- Specific Janus version for each FERS unit (Janus 5202, Janus 5203, ...) with common FERSlib library
- **SDK** for user customization (lib + demo) **[COMING SOON]**
- **GUI (Python) and console mode** – based on C/C++ readout programs
- Multi parametric Jobs and Runs with time or counts preset
- Output files: lists in **.bin** or **.csv** format, spectra, raw data
- Off-line runs for Post-processing and Event Building
- Live plots (with gnuplot) and statistics monitor
- Up to 300 MB/s data throughput (with DT5215 Concentrator via USB 3.0 or 10 Gb Eth)



A5203 Technical Specification Table (1)

MECHANICAL	Weight 40 g (A5203 with spacers mounted); 163 g (A5203B with spacers mounted)	Dimension 73.0 W x 30.0 H x 174.5 L mm ³ 73.0 W x 25.0 H x 174.5 L mm ³
TDC INPUT	A5203: 64 channels (1 edge connector type HSEC8-170) A5203B: 128 channels (2 edge connectors type HSEC8-170) <ul style="list-style-type: none"> • Mating connector: Samtec HSEC8-170-01-S-DV • Input Type: reduced LVDS • Input voltage: Min = -40 mV Max = +1450 mV • Common Mode: Min = +70 mV Max = +1200 mV • Differential voltage: Min = +140 mV Max = +450 mV • Input Termination: 100 Ω 	
TIMING RESOLUTION	LSB = 3.125 ps <ul style="list-style-type: none"> • ΔT_{RMS} = ~5 ps. Tested with LVDS signals, two passive splitters and delay cables • ΔT_{RMS} = ~7 ps. Tested with pulse generator (1 Vpp, 0.8 ns rise/fall), passive splitter and 5 ns cable delay • ΔT_{RMS} = ~20 ps with variable amplitude pulses (30 mV to 1 V) and walk correction by ToT 	
DYNAMIC RANGE	Time measurement dynamic range in picoTDC: <ul style="list-style-type: none"> • Leading Edge only: T_{LEAD} = 24 bits (FSR = ~ 52 μs)* • Leading + Trailing Edge: T_{LEAD} / T_{TRAIL} = 24 bits (FSR = ~ 52 μs)* • Leading + ToT8: T_{LEAD} = 19 bits, T_{TOT} = 8 bits (LSB size and FSR can be programmed) • Leading + ToT11: T_{LEAD} = 16 bits, T_{TOT} = 11 bits (LSB size and FSR can be programmed) <p>Coarse time stamp in FPGA (56 bits @ 12.6 ns) can be combined with picoTDC data to extend the full scale range of the time measurement to a maximum dynamic of 64 bit (streaming acquisition mode).</p> <p>* 26bits (FSR = ~ 210 μs) optional</p>	
ACQUISITION MODES	Common Start: TDC ch0 is the common start that opens the acquisition gate and represents the time reference. All other channels provide ΔT time measurements: $T_{LEAD} = \Delta T_N = T_N - T_0$. The gate width is programmable by software. Any hit falling outside the gate will be discarded. Output Data: T_{LEAD} OR $T_{LEAD} + ToT$ Common Stop: Same as common start, but ch0 is used as a common stop that closes the acquisition gate: $\Delta T_N = T_0 - T_N$. Output Data: T_{LEAD} OR $T_{LEAD} + ToT$ Trigger Matching: The trigger signal (typ. from TO/TI inputs) defines an acquisition window with programmable width and offset. All hits falling into the window will be recorded. Multi-hit acquisition is supported. All time measurements are referred to the Coarse Trigger Time Stamp (LSB = 25.6 ns), while the relative time between the hits keeps the TDC timing resolution (minimum LSB = 3.125 ps). Output Data: T_{LEAD} OR $T_{LEAD} + T_{TRAIL}$ OR $T_{LEAD} + ToT$ Streaming: Continuous hit recording, without any gate or trigger windowing. All hit time measurements are expressed as 64 bit time stamps (minimum LSB = 3.125 ps) and saved in the form of a sorted list. Output Data: T_{LEAD} OR $T_{LEAD} + T_{TRAIL}$ (OR $T_{LEAD} + ToT$, COMING SOON)	

A5203 Technical Specification Table (2)

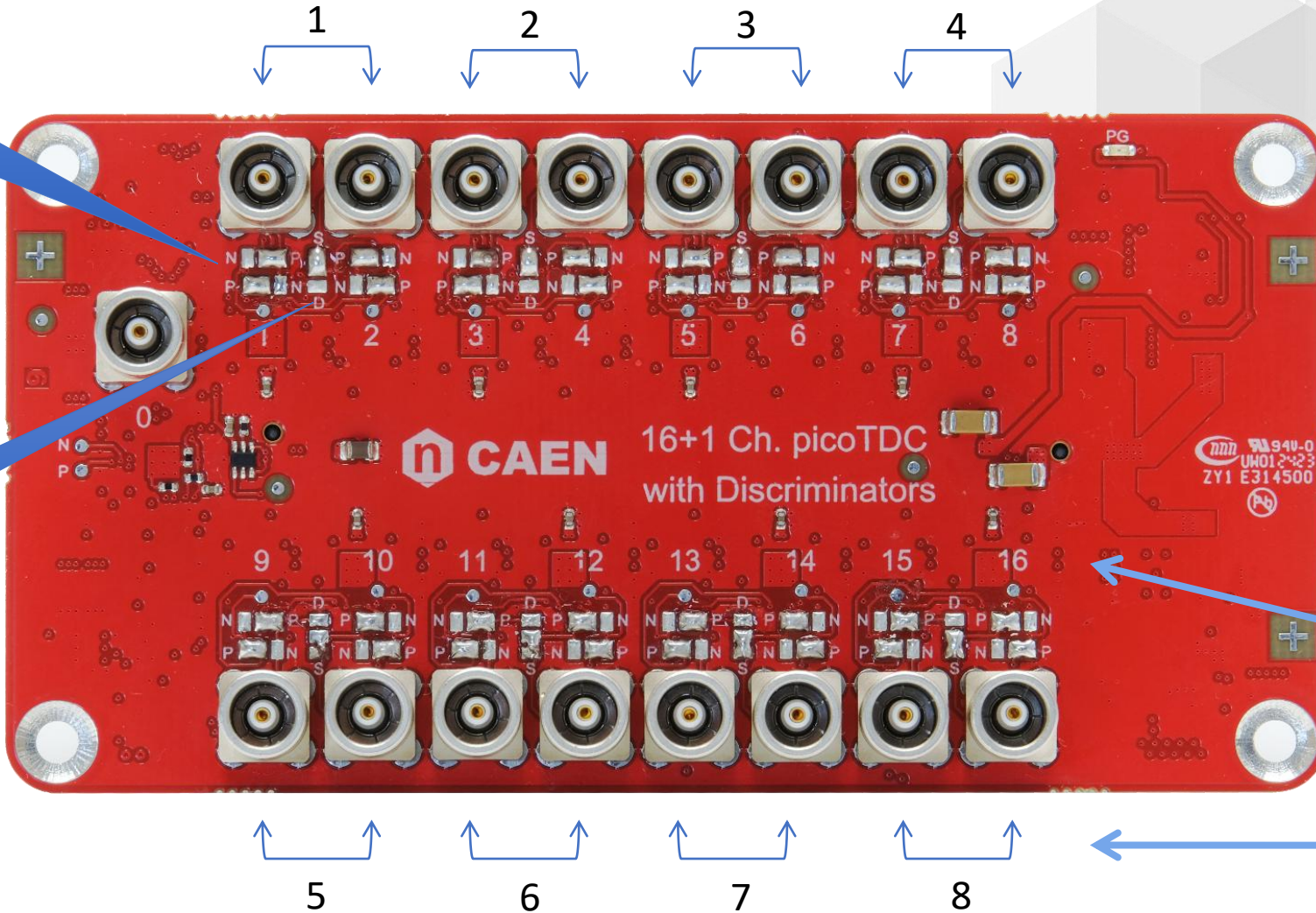
FPGA TRIGGER TIME STAMP	<ul style="list-style-type: none"> 56-bit counter, 25,6 ns step up to 128 boards can be synchronized with the DT5215 FERS-CB by sending a time stamp reset signal via TDlink 			
FRONT PANEL I/Os	<ul style="list-style-type: none"> TO-IN, TI-IN: LEMO-00 connector, NIM or TTL (terminated to 50 Ω) TO-OUT, TI-OUT: LEMO-00 connector, TTL (50 Ω termination required) <p>Jumpers for IN-OUT bypass and termination removal (daisy chaining).</p> <p>Functions (SW programmable): Trigger, Acquisition Start/Stop, Sync, Busy, Veto, Signal inspection, etc ...</p> <p>TO/TI inputs can be used to drive TDC – Ch0 = Tref (possible degradation of the resolution because of the FPGA temperature dependence)</p>			
FRONT PANEL LEDs	<ul style="list-style-type: none"> GREEN: Power-ON, Init-Done, Run, Trigger, Data Ready, TO-IN, TI-IN ORANGE: Event Overrun (rejected triggers because received while busy) RED: Failure (missing clock, over-temperature, etc...) 			
INTERNAL PULSER	Fast reduced-LVDS output (one signal only) with programmable frequency and width, for debug purposes			
COMMUNICATION INTERFACES	<table border="0"> <tr> <td style="vertical-align: top;"> <p>USB</p> <ul style="list-style-type: none"> USB2.0: microUSB connector Bandwidth = ~ 3 MB/s </td> <td style="vertical-align: top;"> <p>Ethernet</p> <ul style="list-style-type: none"> Ethernet connector, type RJ-45. Supports 10/100 Mbit/s connection to a PC Bandwidth = ~ 2.5 MB/s </td> <td style="vertical-align: top;"> <p>Optical Link</p> <ul style="list-style-type: none"> Small Form Factor Pluggable (SFP+) transceiver component for optical connection (3,125 Gbit/s). TDlink CAEN proprietary protocol allows for multi-board synchronization, slow control and data readout Data Concentrator DT5215 required </td> </tr> </table>	<p>USB</p> <ul style="list-style-type: none"> USB2.0: microUSB connector Bandwidth = ~ 3 MB/s 	<p>Ethernet</p> <ul style="list-style-type: none"> Ethernet connector, type RJ-45. Supports 10/100 Mbit/s connection to a PC Bandwidth = ~ 2.5 MB/s 	<p>Optical Link</p> <ul style="list-style-type: none"> Small Form Factor Pluggable (SFP+) transceiver component for optical connection (3,125 Gbit/s). TDlink CAEN proprietary protocol allows for multi-board synchronization, slow control and data readout Data Concentrator DT5215 required
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FIRMWARE	<ul style="list-style-type: none"> Firmware of FPGA upgrade via USB or Ethernet (or TDlink COMING SOON) Firmware of μC upgrade via Ethernet only 			
SOFTWARE	<p>Readout SW</p> <p>Fully controlled by the Janus 5203 open source software for Windows® and Linux®. It can run in console mode (C program, with console commands and gnuplot display for plots) or connected to a GUI (Python) that implements user friendly configuration panels and run controls. Janus 5203 can acquire, plot and save output files with ToA, ToT histograms, as well as list files (trigger timestamp, ToA and ToT for each channel).</p> <p>Web Interface</p> <p>Board information and monitoring, Ethernet configuration.</p>			
POWER REQUIREMENTS	<p>Single power supply: +12 V. Accepted voltage range: MIN +7 V, MAX +15 V</p> <p>(110 V/220 V AC/DC converter provided with Desktop version only)</p>			
POWER CONSUMPTIONS	<p>700 mA @ +12 V, i.e ~ 8.4 W (A5203 – 64 channels)</p> <p>tbd (A5203B – 128 channels)</p>			

A5256 Focus

A5256 Hardware Configuration

Channel Polarity

Single/Dual Threshold



16 single threshold channels

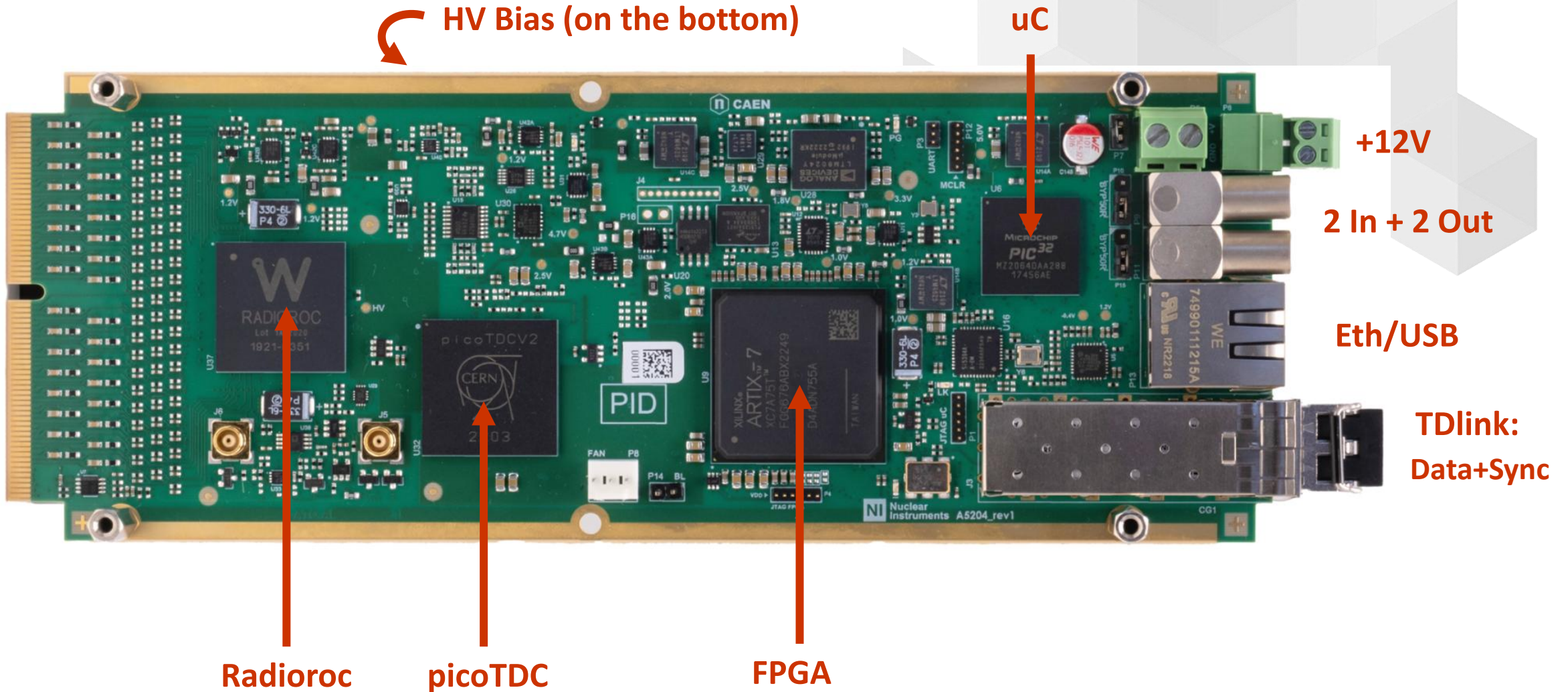
8 dual threshold channels

A5256 Technical Specification Table

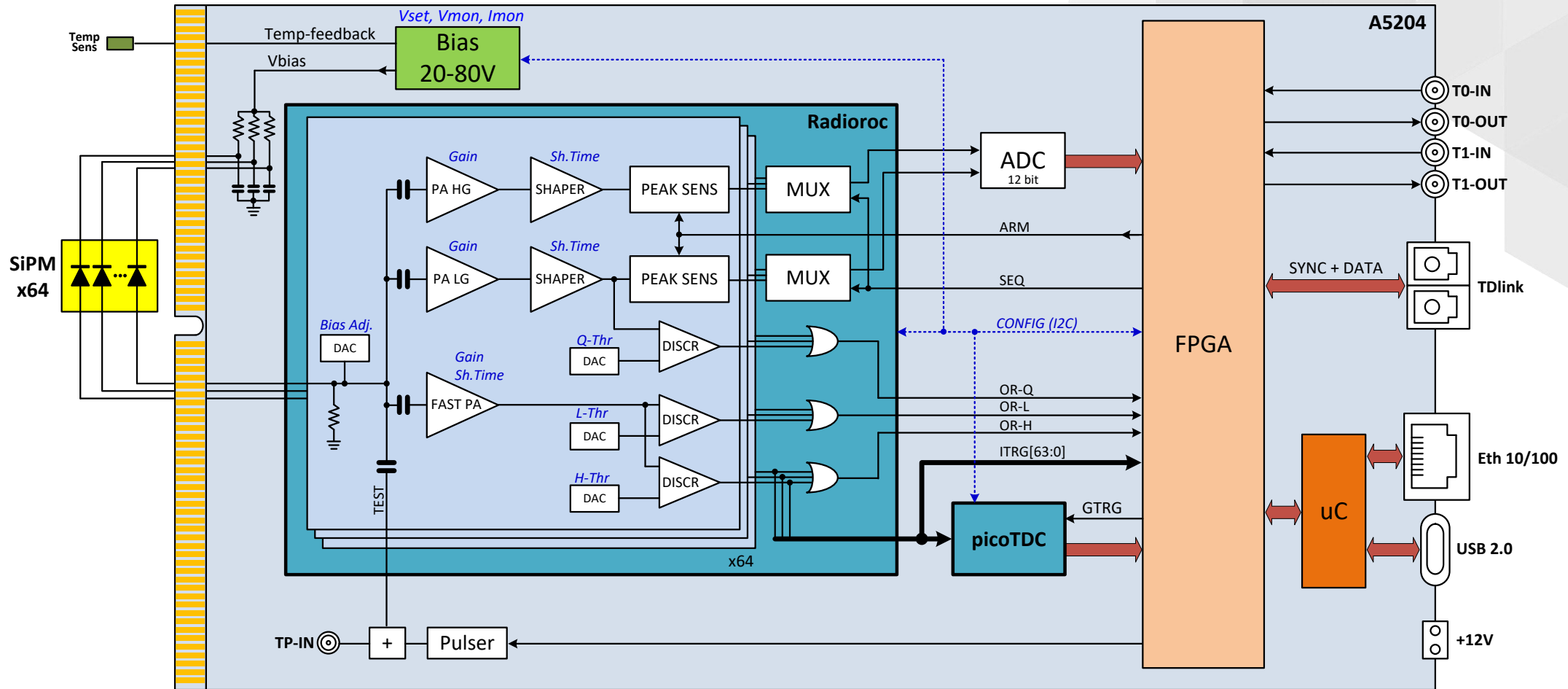
Inputs	Single Threshold: 16+1 inputs positive/negative polarity, 50 Ω impedance Double Threshold: 8+1 inputs positive/negative polarity, 50 Ω impedance
Min/Max Input Voltage	- 4 V / +3 V
Min Detectable Signal	1.5 mV
Threshold Range	-1.2 V / +1.2 V
Threshold Step	0.61 mV
Timing Resolution	A5256 mounted on A5203: $\Delta T_{RMS} = \sim 7$ ps. Tested with a pulse generator (1 Vpp, 0.8 ns rise/fall pulses), one passive splitter and delay cables. $\Delta T_{RMS} = \sim 20$ ps. with variable amplitude pulses (30 mV to 1V) and walk correction by ToT.
Non-Linearity	≤ 0.18 % typ.
Efficiency	<2 mV typ. (3 mV max) Measured with 150 mV signal, with 1.6 ns rise time

A5204 Focus

FERS A5204: 64 channel SiPM Readout



A5204: block diagram



A5204 Technical Specification Table (1)

MECHANICAL	Weight 161 g (A5204 with spacers mounted);	Dimension 72.8 W x 22.0 H x 208.5 L mm ³
INPUTS	64 channels Input edge connector type Samtec HSEC8-170 Mating connector: Samtec HSEC8-170-01-S-DV Signal polarity: Positive Each SiPM input has two pins: <ul style="list-style-type: none"> • Cathode with HV bias (min = +20V, max = +80V) • Anode closed to -100 ohm, feeding the Radioroc inputs 	
HIGH VOLTAGE (SiPM Bias)	HV module for SiPM biasing (A7585D) HV Range: +20V/+80V, Max 10 mA Individual bias adjustment on channel basis (8 bit DACs, LSB = -2 mV, adjust range = 550 mV) Automatic temperature feedback for SiPM gain stabilization	
ACQUISITION MODES	<p>Spectroscopy:</p> <p>The common trigger initiates the peak sensing detection and A/D conversion (12 bit) on all channels simultaneously. Conversion time = -10 μs. Output Data: Trigger time stamp, Trigger ID, PHA (Low and/or High Gain). Zero suppression with programmable threshold.</p> <p>Counting:</p> <p>32 bit counters, up to 200 MHz. Common trigger defines dwell time (i.e. counting window). No dead-time between subsequent windows. Internal period trigger from 16 ns to -34 s. Output Data: Trigger time stamp, Trigger ID, channel counts. Zero suppression available. Counters are automatically reset after each trigger.</p> <p>Timing (Common Start):</p> <p>The Tref signal (T0, T1 inputs) is a common start that opens the acquisition gate with programmable width. Channel self-triggers are acquired as $\overline{\text{T}}$ from Tref and, optionally, as ToT for PHA estimation. Output Data: Trigger (=Tref) time stamp, Trigger ID, $\overline{\text{T}}$ or $\overline{\text{T}}$+ToT</p> <p>Timing (Common Stop):</p> <p>Same as common start, with Tref used as a common stop that closes the acquisition gate. Acquired events are those ones arrived before the trigger (look back acquisition).</p> <p>Timing (Trigger Matching):</p> <p>The common trigger signal defines an acquisition window with programmable width and offset. All hits falling into the window will be recorded. Multi-hit acquisition is supported. Output Data: Trigger time stamp, Trigger ID, ToA or ToA+ToT</p> <p>Timing (Streaming):</p> <p>Continuous hit recording, without any gate or trigger windowing. All hit time measurements are expressed as 64 bit time stamps and saved in the form of a sorted list. Output Data: ToA or ToA+ToT</p>	
SENSITIVITY (GAIN) - SPECTROSCOPY	<p>High Gain: Min = 5, Max = 80, 16 steps (1 step = 5)</p> <p>Low Gain: Min = 0.5, Max = 8, 16 steps (1 step = 0.5)</p>	
SHAPING TIME - SPECTROSCOPY	<p>Short Range: Min = 20 ns, Max = 300 ns, 16 steps (1 step = 20 ns)</p> <p>Long Range: Min = 80 ns, Max = 1200 ns, 16 steps (1 step = 80 ns)</p>	

A5204 Technical Specification Table (2)

DYNAMIC RANGE - SPECTROSCOPY	Up to 2000 photo-electrons @ 10 ⁶ SiPM gain
SELF TRIGGERS - TIMING & COUNTING	Dedicated fast preamps + discriminator for SiPM pulse detection. Trigger down to 1/3 p.e. Fast Preamp Gain: Min = 15 (BW = 480 MHz), Max = 100 (BW = 55 MHz), 32 steps Discriminator Dual Threshold: Range = 278 mV; 1024 steps, 1 step = 0.27 mV
TIMING RESOLUTION - TIMING & COUNTING	55 ps FWHM on a single p.e. Time Stamp Range: 64 bit Intrinsic timing resolution of picoTDC = 3.125 ps LSB
ToT - TIMING & COUNTING	Time over Threshold (ToT): 1% linearity energy measurement up to 2000 p.e.
COUNTING - TIMING & COUNTING	Photon counting up to 200 Mcps per channel MCS mode with programmable dwell time: from 16 ns to ~34 s
TRIGGER LOGIC	Global trigger common to 64 channels: used in Spectroscopy mode to start Peak acquisition, in Timing mode to generate the acquisition windows (Gate). Trigger-less acquisition only in Streaming mode. Global Trigger Sources: <ul style="list-style-type: none"> • OR of self-triggers = OR(0..63) • Plane coincidence: OR(0..31) AND OR(32..63) • Paired channels: AND(0..1) OR AND(2..3) ... OR AND(62..63) • Majority with programmable threshold • External trigger (TO-IN, TI-IN, LEMO, TTL/NIM) • Internal periodic trigger with programmable frequency
TIME STAMP & SYNCHRONIZATION	Acquisition Trigger Time Stamp: 56 bit, step = 8 ns Two synchronization modes: <ul style="list-style-type: none"> • TO or TI IN-OUT daisy chain: max jitter = 100 ns • fiber optic (TDlink) and DT5215 Concentrator: up to 128 boards, max jitter 50 ps
FRONT PANEL I/Os	TO-IN, TI-IN: LEMO-00 connector, NIM or TTL (terminated to 50 Ω) TO-OUT, TI-OUT: LEMO-00 connector, TTL (50 Ω termination required) SW selectable IN-OUT bypass and termination removal for daisy chaining Functions (SW programmable): Trigger, Acquisition Start/Stop, Sync, Busy, Veto, Signal inspection, etc...
FRONT PANEL LEDs	GREEN: Power-ON, Init-Done, Run, Trigger, Data Ready, TO-IN, TI-IN ORANGE: Event Overrun (rejected triggers because received while busy) RED: Failure (missing clock, over-temperature, etc...)

A5204 Technical Specification Table (3)

INTERNAL PULSER	Radioroc provides a test input pin that can be internally connected to the pre-amplifier inputs, channel by channel. The test signal can come from an external signal (MCX connector on the PCB) or generated by an internal pulser with programmable amplitude. The internal pulser can be trigger by TO/T1 IN or by the internal periodic trigger.			
COMMUNICATION INTERFACES	<table border="0"> <tr> <td data-bbox="978 396 1243 476">USB USB2.0: microUSB connector Bandwidth = ~ 3 MB/s</td> <td data-bbox="1258 396 1589 499">Ethernet Ethernet connector, type RJ-45. Supports 10/100 Mbit/s connection to a PC Bandwidth = ~ 2.5 MB/s</td> <td data-bbox="1605 396 2040 576">Optical Link Small Form Factor Pluggable (SFP+) transceiver component for optical connection (3.125 Gbit/s). TDlink CAEN proprietary protocol allows for multi-board synchronization, slow control and data readout Data Concentrator DT5215 required</td> </tr> </table>	USB USB2.0: microUSB connector Bandwidth = ~ 3 MB/s	Ethernet Ethernet connector, type RJ-45. Supports 10/100 Mbit/s connection to a PC Bandwidth = ~ 2.5 MB/s	Optical Link Small Form Factor Pluggable (SFP+) transceiver component for optical connection (3.125 Gbit/s). TDlink CAEN proprietary protocol allows for multi-board synchronization, slow control and data readout Data Concentrator DT5215 required
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FIRMWARE	Firmware of FPGA be upgraded via USB or Ethernet Firmware of μ C can be upgraded via Ethernet only			
SOFTWARE	<p>Readout SW Fully controlled by the Janus 5204 open source software for Windows® and Linux®. It can run in console mode (C program, with console commands and gnuplot display for plots) or connected to a GUI (Python) that implements user friendly configuration panels and run controls.</p> <p>Janus 5204 can perform multiple board acquisition of PHA energy spectrum (Low and High Gain). ToT spectrum (represents PHA in timing mode) DT spectrum, with event building based on trigger ID or time stamp.</p> <p>Live Display: channel hit count and rate, trigger rate, lost triggers, data throughput, acq. time, etc... Plots: PHA, DT, ToT, hit rate, 2-D heat map with channel hit rates or PHA.</p> <p>Output Files: histograms (spectra), list files (PHA, ToA, ToT, DT), Run Info, Sync file.</p> <p>Web Interface Board information and monitoring, Ethernet configuration.</p>			
POWER REQUIREMENTS	Single power supply (+12 V). Regularly working in a range between +7 V and +15 V 110V/220V AC/DC converter provided with Desktop version only.			
POWER CONSUMPTIONS	t.b.d.			