BULLKID-DM Readout Electronics

BULLKID collaboration meeting Pisa, 17.01.2025

Timo Muscheid, Robert Gartmann, Luis E. Ardila-Perez
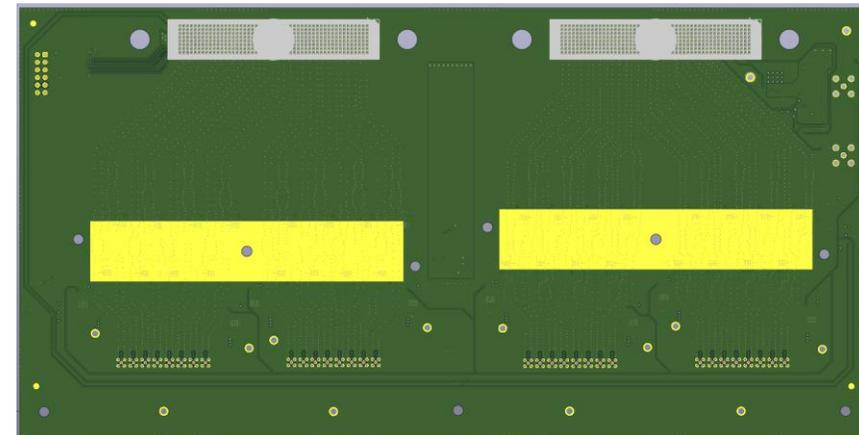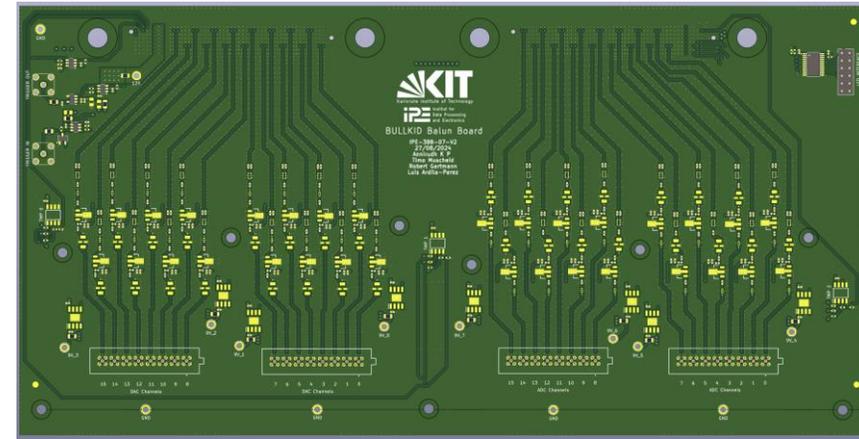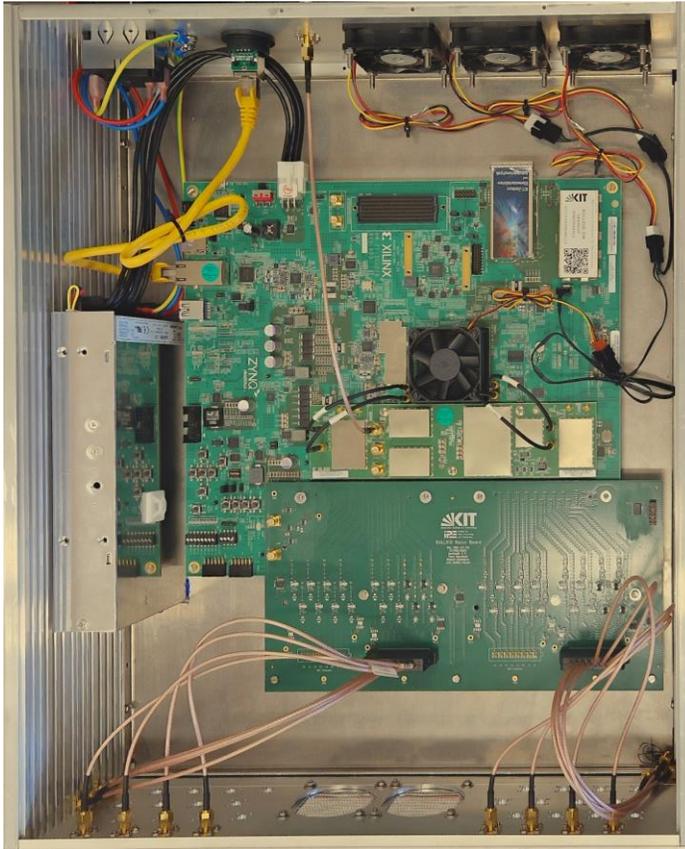
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Custom frontend v2

- 16 coaxial signal line breakout (TX and RX)

- Includes transformer, low-pass filters, amplifier on each line

- Additional feature
  - Temperature sensors
  - Trigger input/output for calibration

- 1 unit built (partial assembly), 2 more in preparation

Prototype system installed in Rome

Funding for hardware secured, system can stay in Rome
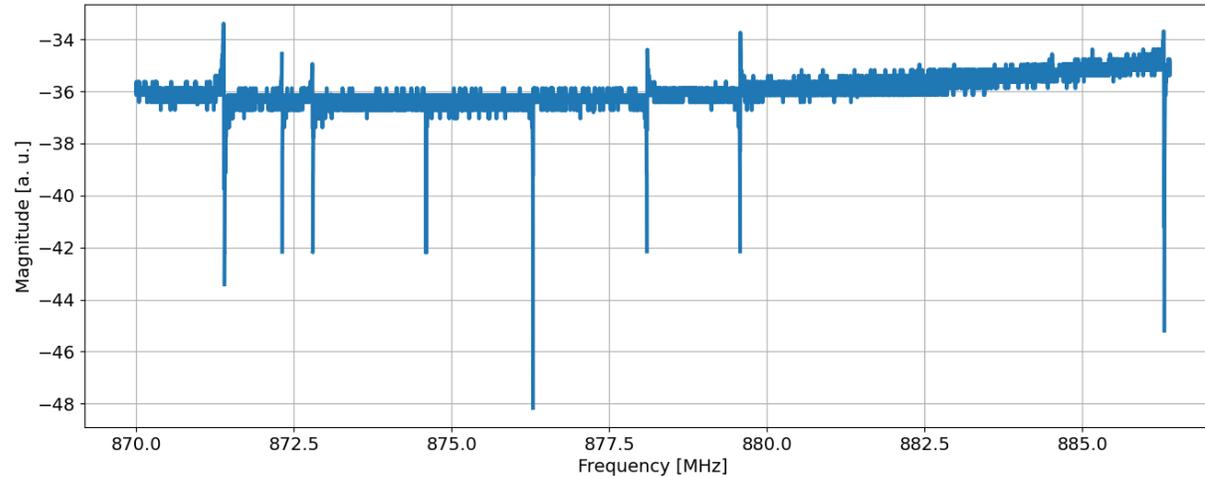
Measurements October 2024 @ Rome

- ☑ Generation of 30 resonator tones + downconversion of carrier signals
- ☑ Detection and extraction of pulses on all resonators
- ☑ Setup infrastructure for remote access

- ☒ Sweep of integrated VNA showed incorrect result depending on settings
- ☒ Converter clocks not synchronized -> impossible to acquire circles
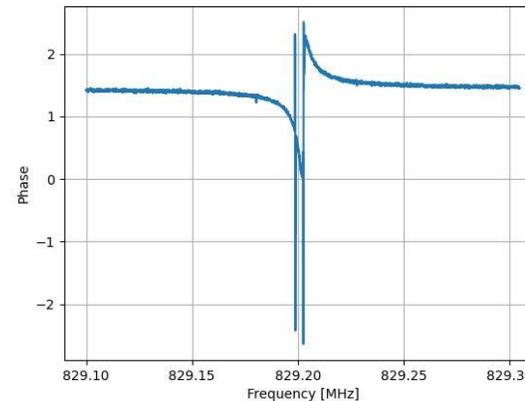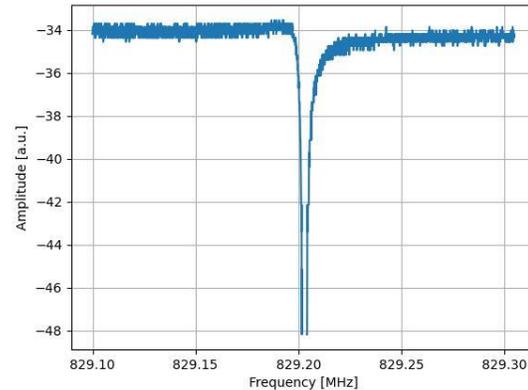- ☒ Several bugs

Improvements verified during remote measurement on 03.01.2025

January 15, 2025   Timo Muscheid (timo.muscheid@kit.edu)   Part 1: Status report

VNA on FPGA

Wideband measurement

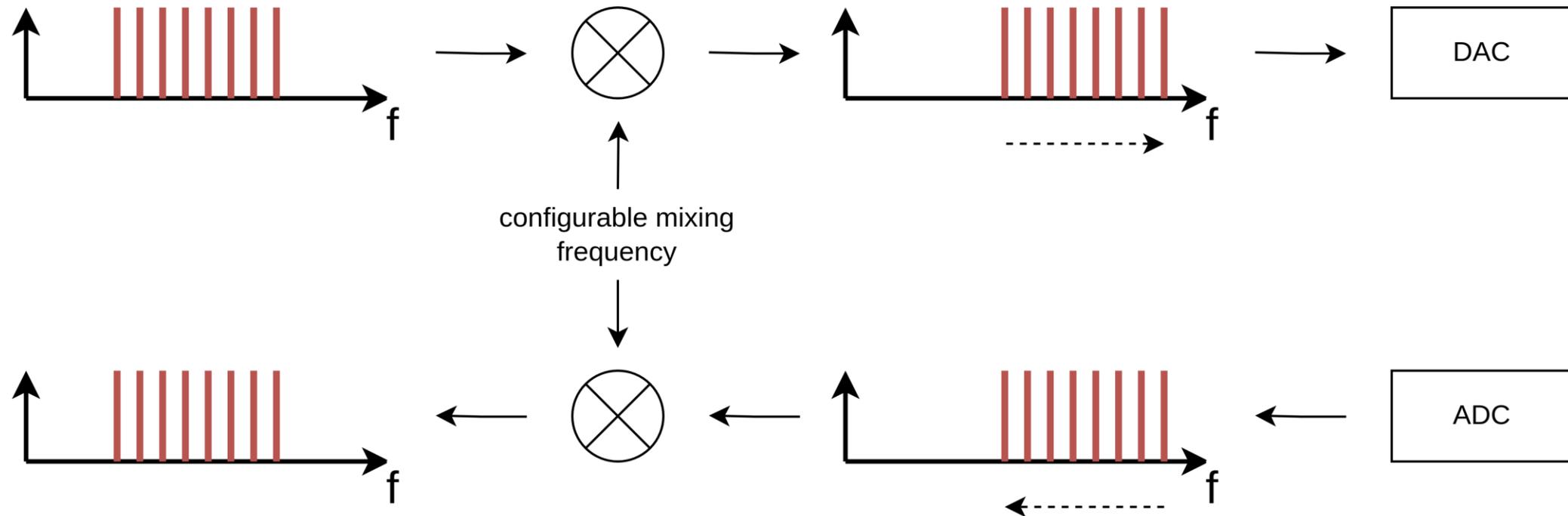Measurement of single resnator

- Adjustable parameters:
  - Frequency range
  - Averages
  - Setup time
  - Transmission line delay

- Work in progress:
  - Adjustable input power
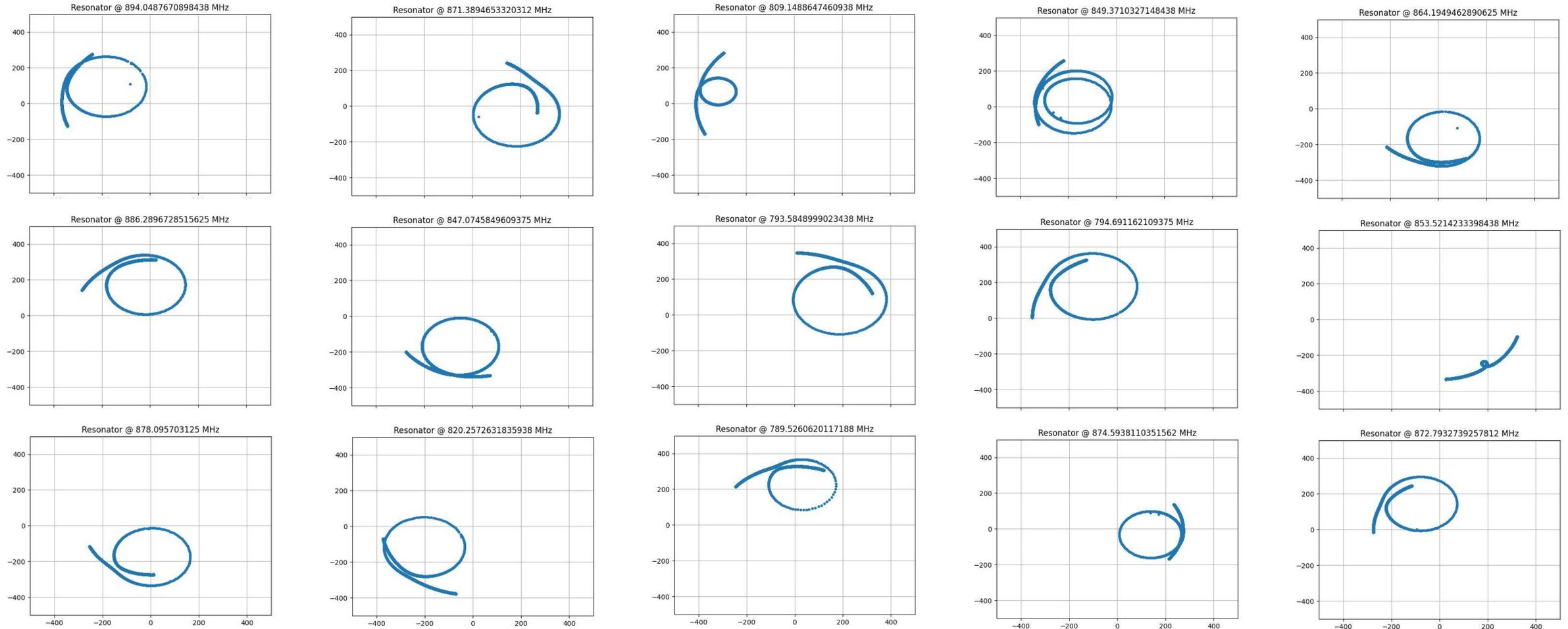 - Fix random phase jumps

Locate resonators through frequency sweep

Comb mixing: Custom FPGA module

Fully digital mixing of entire frequency comb with phase stability

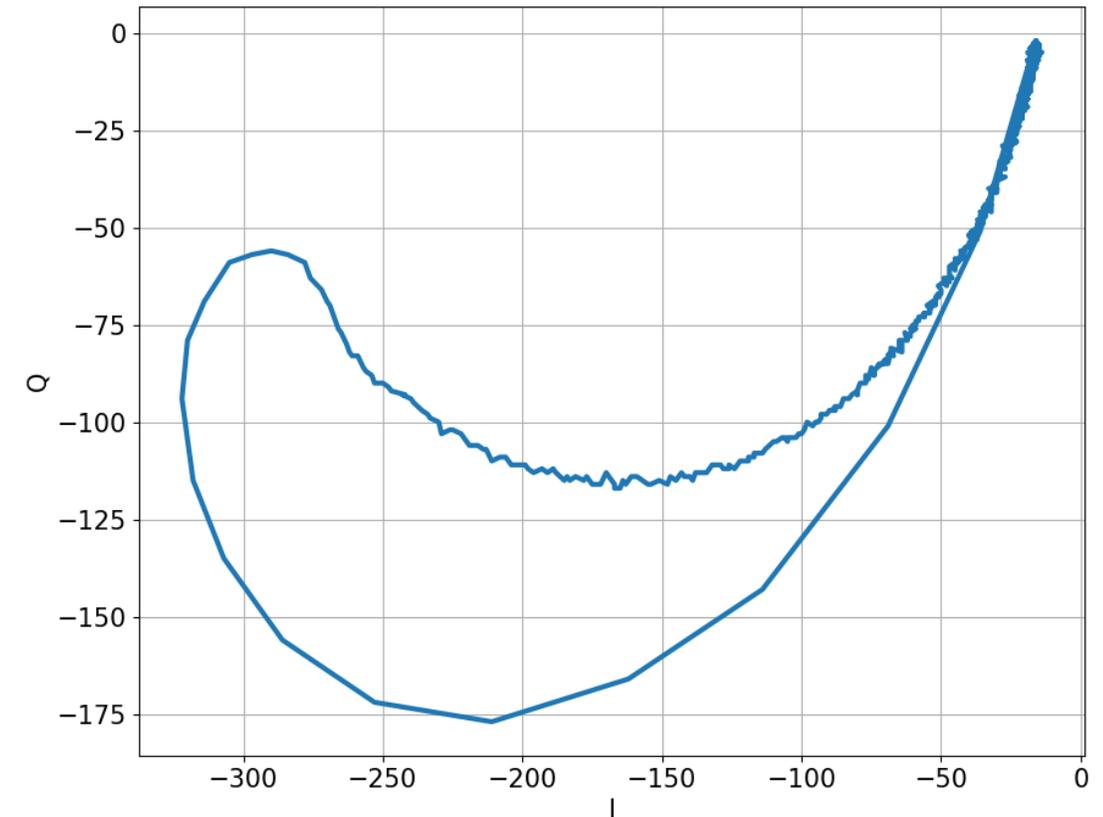# Comb mixing: Resonance circle acquisition

All resonance circles acquired simultaneously (< 50s for 8000 points à 1000 samples)

Pulse acquisition

- 45 min on 29 resonators:
  > 10.000 pulses detected

- Measurement limitations:
  - Uncalibrated location on I/Q circle
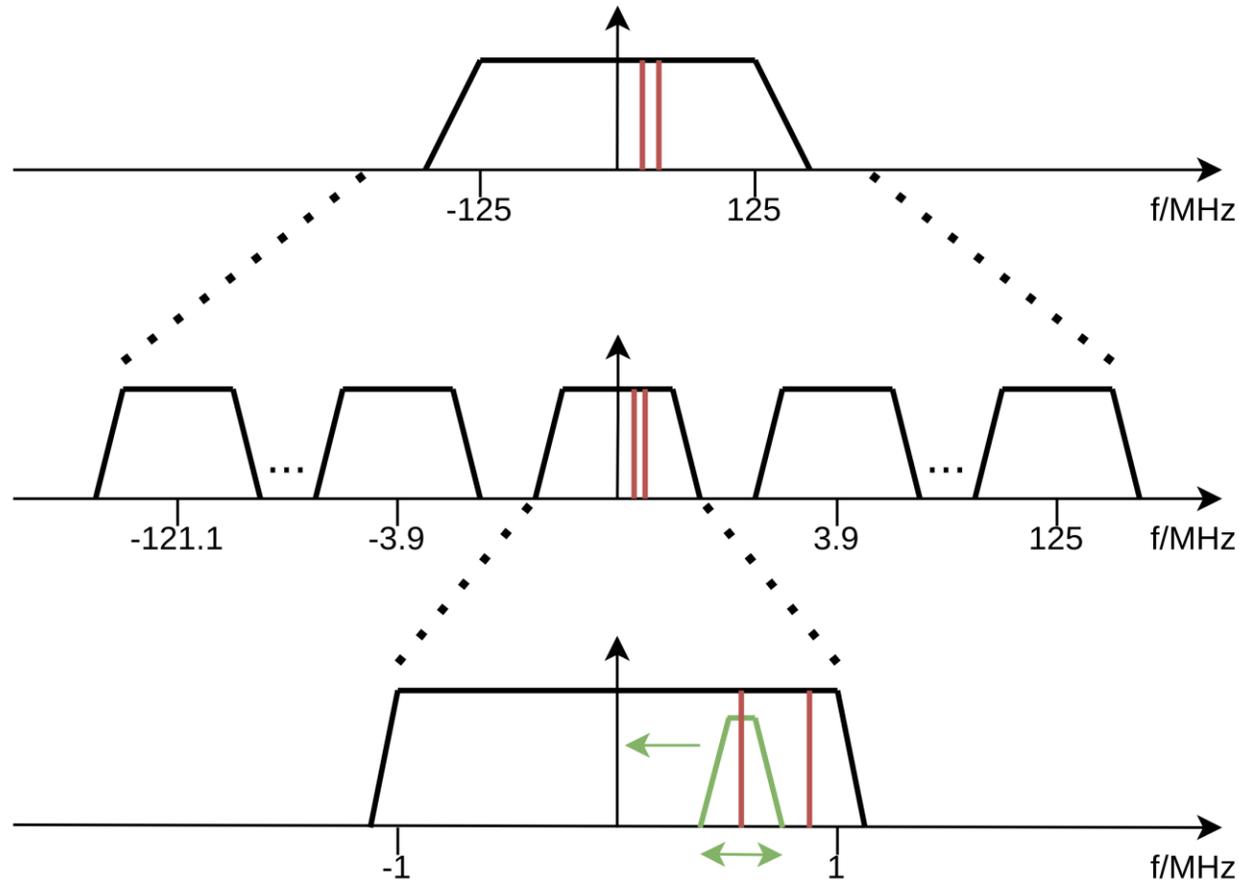 - Simple trigger with digital differentiation

- Energy resolution => TBD

Events successfully detected on 28 channels

Exemplary pulse package:

Work package 1: Channelization scheme
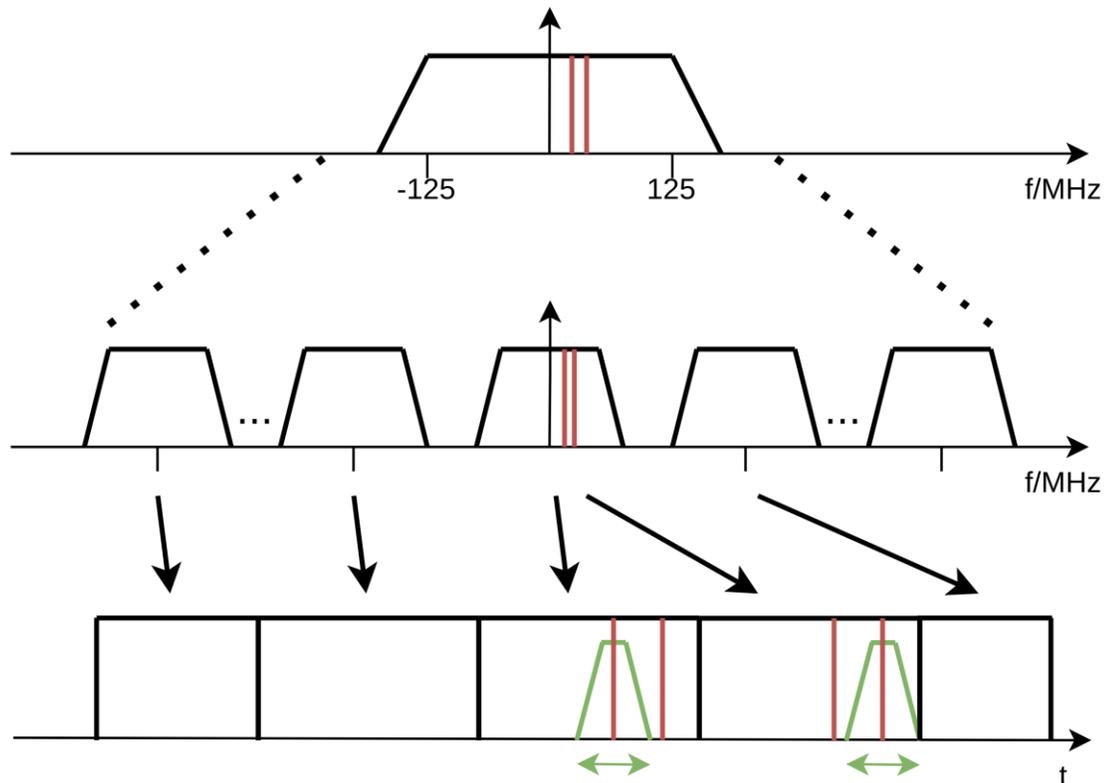
Current channelization scheme:

- Limitation:
  - Only one tone per channel
  - Channel spacing: ~2 MHz

- Closely spaced tones cannot be downconverted, one tone is discarded

- Measurement with 29/38 resonators (~76%)

Channelization concept needs improvement for full scale system

Improved channelization concept
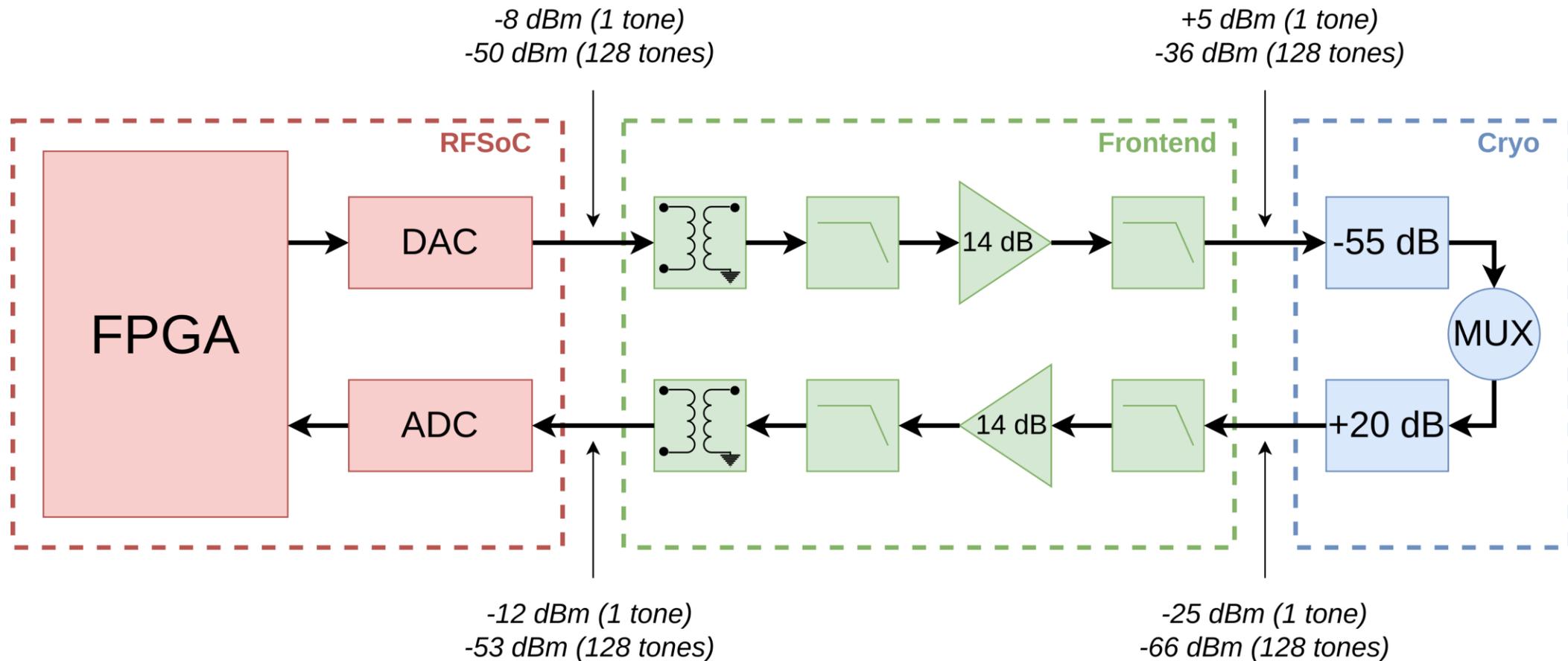

- Two options:
  - Higher number of bins
  - <u>Multiple usage of single bins</u>

- Advantages:
  - Fully flexible
  - Minimal additional ressources

Development of new firmware module
for bin selection in progress

Work package 2: Output power

Output power not sufficient for full scale system (+5 dBm per tone)

External Power Amplifier Evaluation

[MW7IC915NT1](#) Amplifier:

Evaluation Board:

Driver Application — 900 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 28 Volts, I_{DQ1} = 52 mA, I_{DQ2} = 134 mA, P_{out} = 1.6 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
865 MHz	37.9	17.1	−50.4
880 MHz	38.0	17.4	−50.6
895 MHz	37.8	17.5	−51.3

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 880 MHz, P_{out} = 23.5 Watts CW (3 dB Input Overdrive from Rated P_{out})
- Stable into a 5:1 VSWR. All Spurs Below −60 dBc @ 30 to 41.5 dBm CW P_{out}.
- Typical P_{out} @ 1 dB Compression Point ≃ 15.5 Watts CW

Driver Application — 700 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 28 Volts, I_{DQ1} = 50 mA, I_{DQ2} = 144 mA, P_{out} = 1.6 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
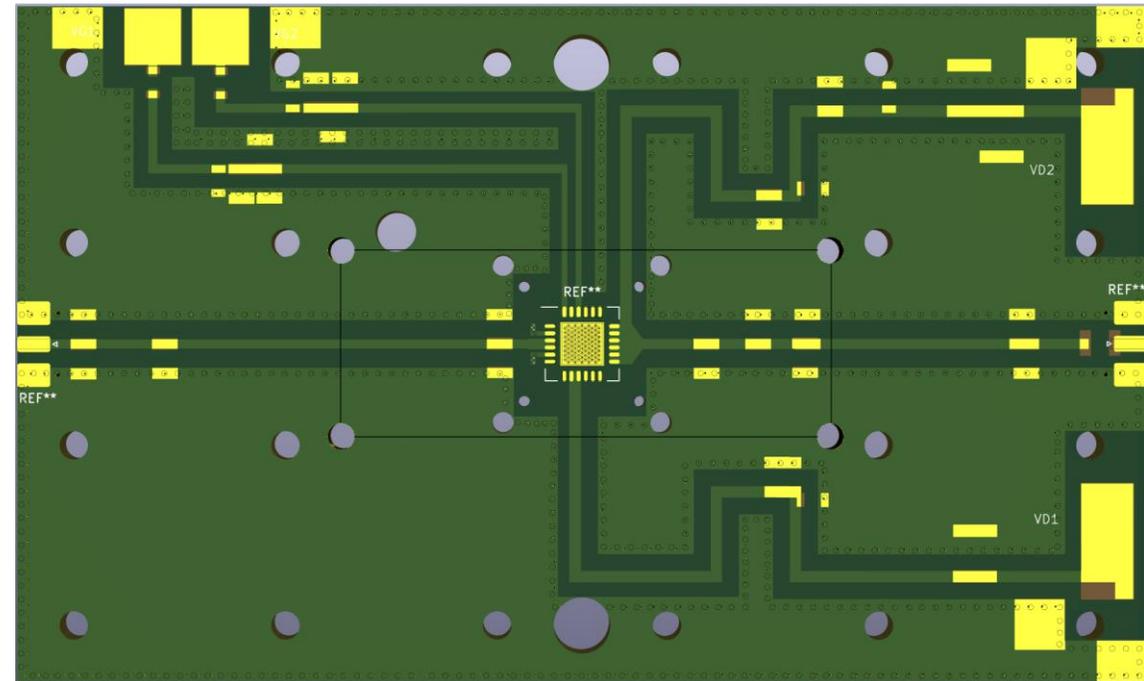
Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
728 MHz	37.8	17.2	−49.5
748 MHz	37.8	17.3	−50.5
768 MHz	37.7	17.3	−51.4

Amplifier can provide the required power

Other work packages

- Trigger implementation
  - Master thesis on complex triggers started in December
  - Currently drafting filters for implementation in FPGA

- H5 file format conversion
  - Python methods almost done (VNA sweep, resonance circles and events)
  - Evaluation how to implement into userspace code on the platform

- Front-end board assembly underway
  - Demonstrator at Gran Sasso
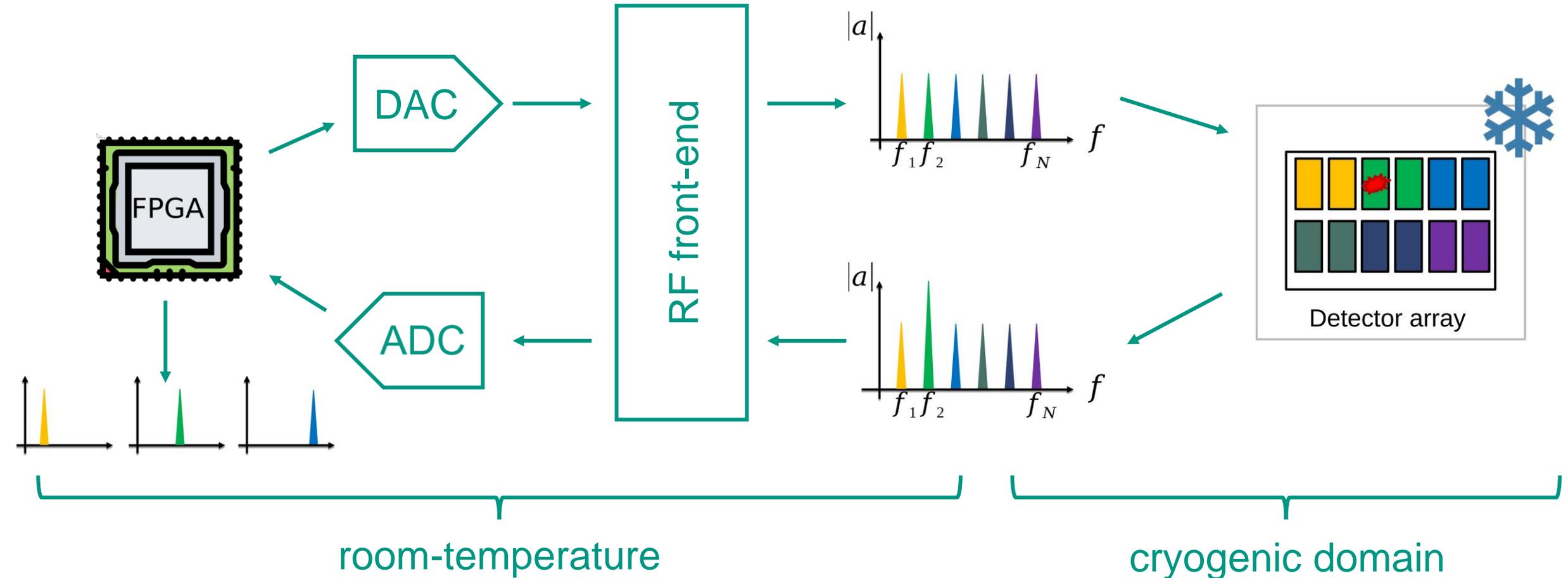 - Noise measurements in Karlsruhe

Time schedule

- 2024: Operation of one prototype wafer with 60 MKIDs
  - Firmware of room-temperature readout system ready with simple trigger (✓)
  - Custom frontend v2 to be installed ✓

- 2025: Operation of one full-scale wafer with 145 MKIDs
  - First tests at Gran Sasso   wip
  - Change parameters of channelization module   wip
  - Implement complex trigger to reduce background noise   wip

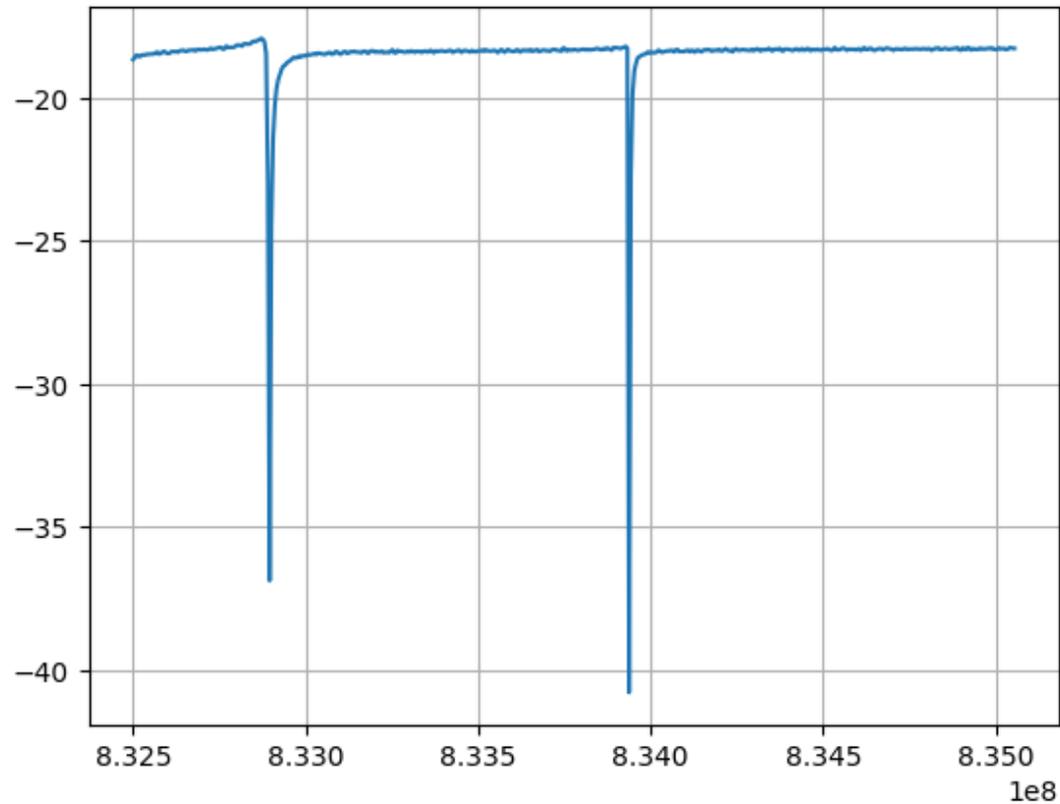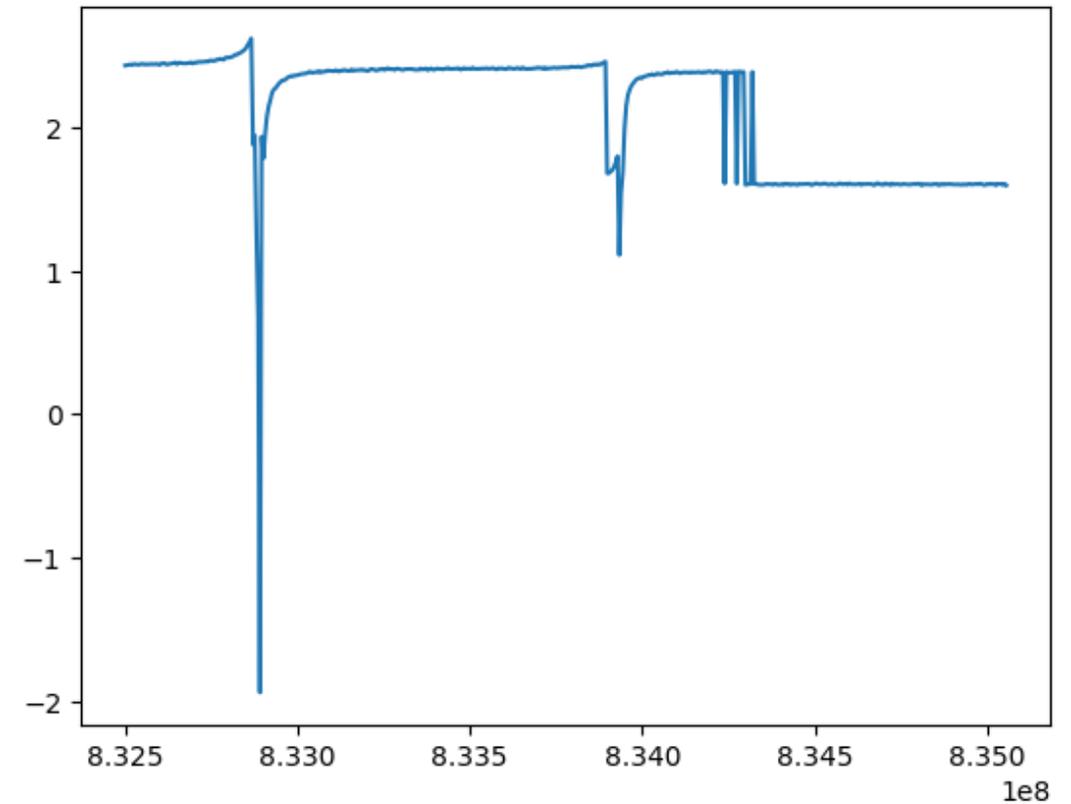Development progress is well on track with the milestones

Backup

January 15, 2025   Timo Muscheid (timo.muscheid@kit.edu)

SDR readout concept

Timo Muscheid (timo.muscheid@kit.edu)

Incorrect VNA measurements (10.2024)

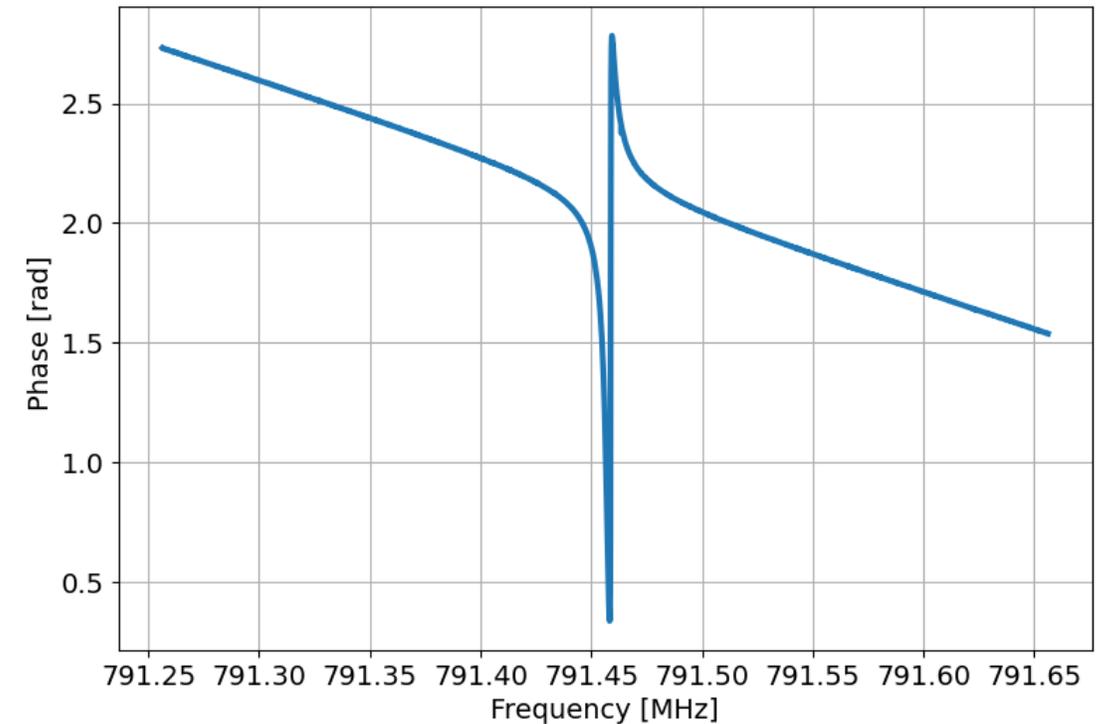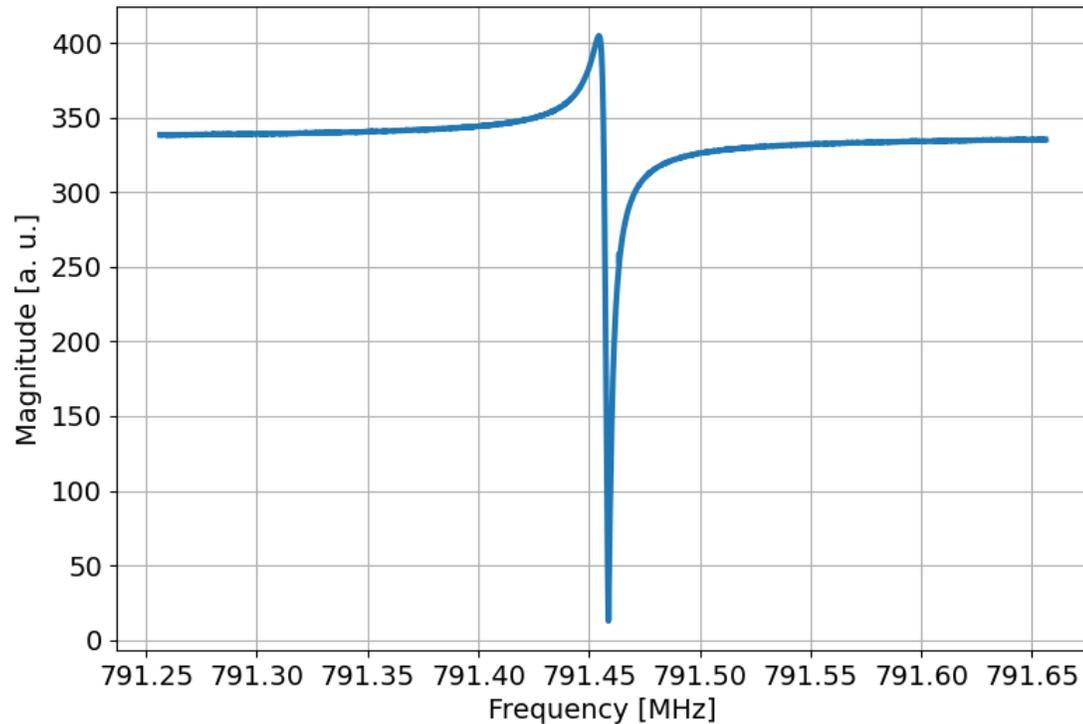January 15, 2025 Timo Muscheid (timo.muscheid@kit.edu)
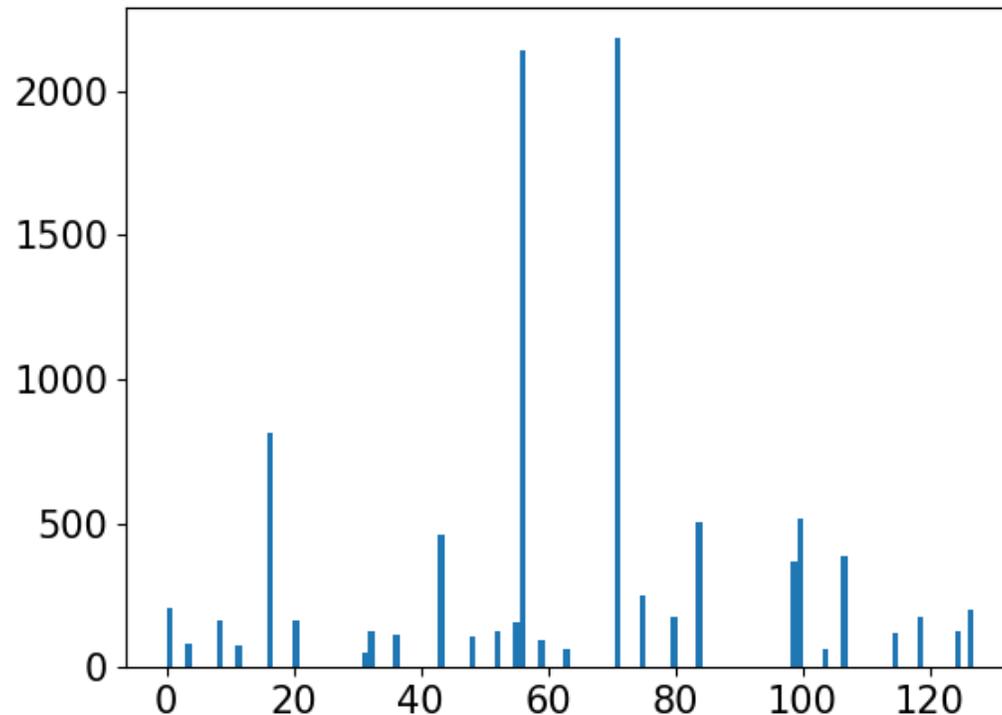
Comb mixing: Firmware integration

Seamless integration of new module into existing firmware

Comb mixing: Resonator shape

Pulse measurement analysis

Distribution of captured events:

- Resonator with highest number of events (> 2000):
  - 802.084 MHz
  - 859.235 MHz

- No event captured on resonator at 853.521 MHz
  - Resonator with smalles circle
  - Trigger threshold to high

Timo Muscheid (timo.muscheid@kit.edu)