

Università degli Studi di Padova



Ajay Sharma PhD Retreat at LNGS 17th - 21st February 2025

Background Details

Master's Degree in Physics at University of Delhi, India.



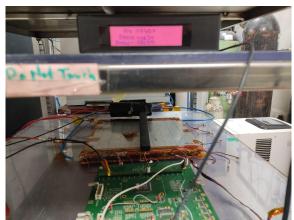
Past Research Work

•Research Project on Resistive Plate Chambers (RPC)

Department: Physics and Astrophysics, University of Delhi, India
Supervisors: Dr. Aman Phogat and Dr. Mohammad Naimuddin
Title: Development and testing of eco-friendly gas mixtures for RPC detectors

Key Activities

Gas calibration and choice of gases for optimal performance
Development and testing of front-end electronics and readout systems
Construction and characterization of RPC detectors



RPC Detector at University of Delhi



•Current Position at INAF-OAS Bologna
 •Supervisors: Riccardo Campana and Enrico Virgilli
 •Project: Development and Testing of Test Equipment for Silicon Drift Detectors.

Research Focus

•**Objective**: Development of test equipment for a new prototype of front-end electronics for Silicon Drift Detectors in a high-energy astrophysics experiment.

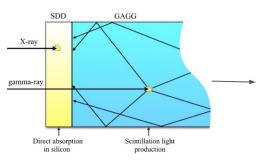
Key Activities

- •Development and optimization of FPGA firmware and interface client PC software.
- •Laboratory testing of the setup with and without Silicon detectors to characterize the FEE and detectors
- •Aiming to deliver a well-developed test equipment along with comprehensive spectroscopic data and analysis





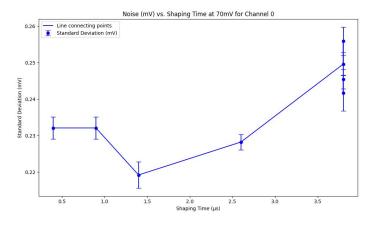
PhD Project





Parameter	Value
Chip dimensions	4900 × 4320 μm ²
Number of channels	32
Channel pitch	150 μm
Equivalent Noise Charge	< 17 e ⁻ _{rms}
Time resolution	< 10 µs

Main parameters of the AFE ASIC



board name: Arty 27	Serial port:	~	Refresh	Connect		Pause		St	top
C Configuration Serial Monitor									
ASIC 00 Channels									
00 01 02 03 04 05 06 07 08 09	10 11 12 13 14 15 16 17 18 19	20 21 22 23 24 25 26 27 28	3 29 30 31						
					Internal OR [1,1]		t DAC Threshold	1. 900	* (1 570
			DISC Disable a	Signal Select:	Stretcher [0]	~ Br	t DAC Reset:	233	\$ [0.751
				Signal Select: Bit Tau:	Stretcher [0] 7	~ 81 \$ 81	t DAC Reset: t DAC AGND:	233 450	 (0.751 (1.450
			DISC Disable a	Signal Select: Bit Tau:	Stretcher [0]	~ Br	t DAC Reset: t DAC AGND:	233	 (0.751 (1.450
			DISC Disable a	Signal Select: Bit Tau:	Stretcher [0] 7	~ 81 \$ 81	t DAC Reset: t DAC AGND:	233 450	 (0.751 (1.450
	Seve configuration		Image: Construction of the second	Signal Select: Bit Tau: Address:	Stretcher [0] 7	~ 81 \$ 81	t DAC Reset: t DAC AGND:	233 450	 (0.751 (1.450
	Save configuration file		O ISC Disable al O ISC Disable al O ISC Disable al O ISC Disable al	Signal Select: Bit Tau: Address: Single N	Stretcher [0] 7 0	- Bi C Bi	t DAC Reset: t DAC AGND: Set Fine	233 450	€ [0.751 € [1.450 olds
nfgure ASICS	Load configuration file		O ISC Disable al O ISC Disable al O ISC Disable al O ISC Disable al	Signal Select: Bit Tau: Address: Single M Readout	Stretcher [0] 7 0 WX Channel:	- 88 : 87 : 0	t DAC Reset: t DAC AGND: Set Fine	233 450	\$ [0.751 \$ [1.450 olds \$
onfigure ASICs	Load configuration file Write configuration to ASICs		O ISC Disable al O ISC Disable al O ISC Disable al O ISC Disable al	Signal Select: Bit Tau: Address: Single M Readout	Stretcher [0] 7 0 8.0K Channel: : clock period [µs]: retition delay [µs]:	0 10.	t DAC Reset: t DAC AGND: Set Fine .00	233 450	\$ [0.751 \$ [1.450 blds
onfigure ASICs	Load configuration file		O ISC Disable al O ISC Disable al O ISC Disable al O ISC Disable al	Signal Select: Bit Tau: Address: Single M Readout Mux trai EOC del	Stretcher [0] 7 0 8.0K Channel: : clock period [µs]: retition delay [µs]:	BI BI D D D D D	t DAC Reset: t DAC AGND: Set Fine .00 .00	233 450	2 [0.751 2 [1.450 olds 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2

TECH-FPA PhD Retreat LNGS 2025