Electronics:

A Roadmap for the Development of Innovative Sensors and Readout for Future Lepton Colliders

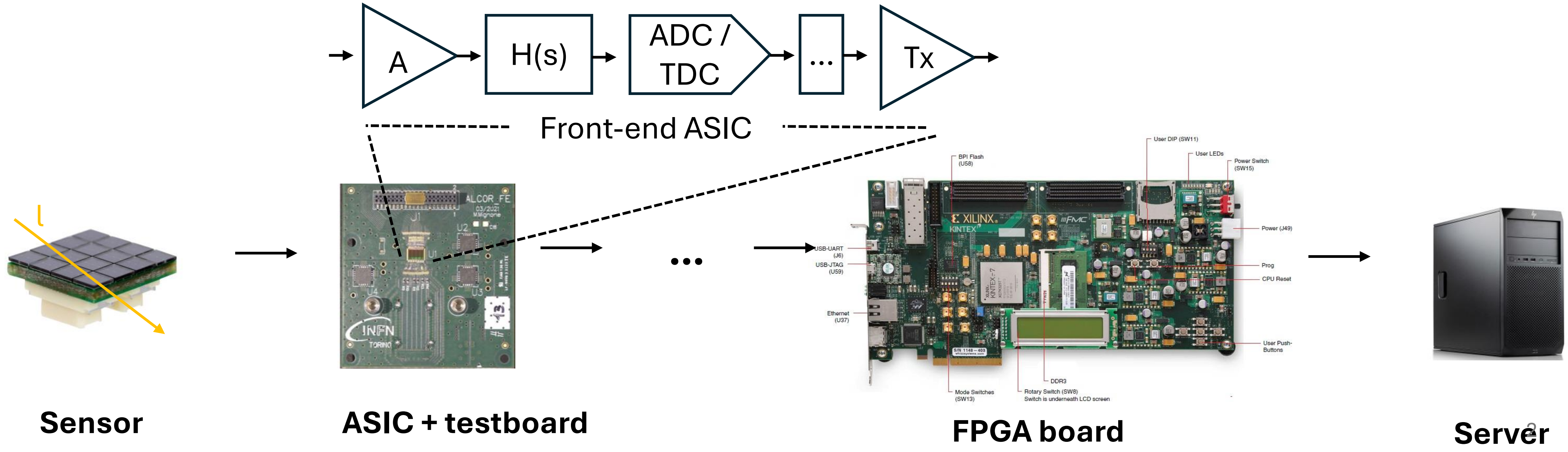
Stefano Durando
University of Genova
Physics Department and
INFN Torino

Workshop on FCC-ee and Lepton Colliders – Jan 2025 - Frascati

Stefano Durando

Complex system with interdependent boundaries:

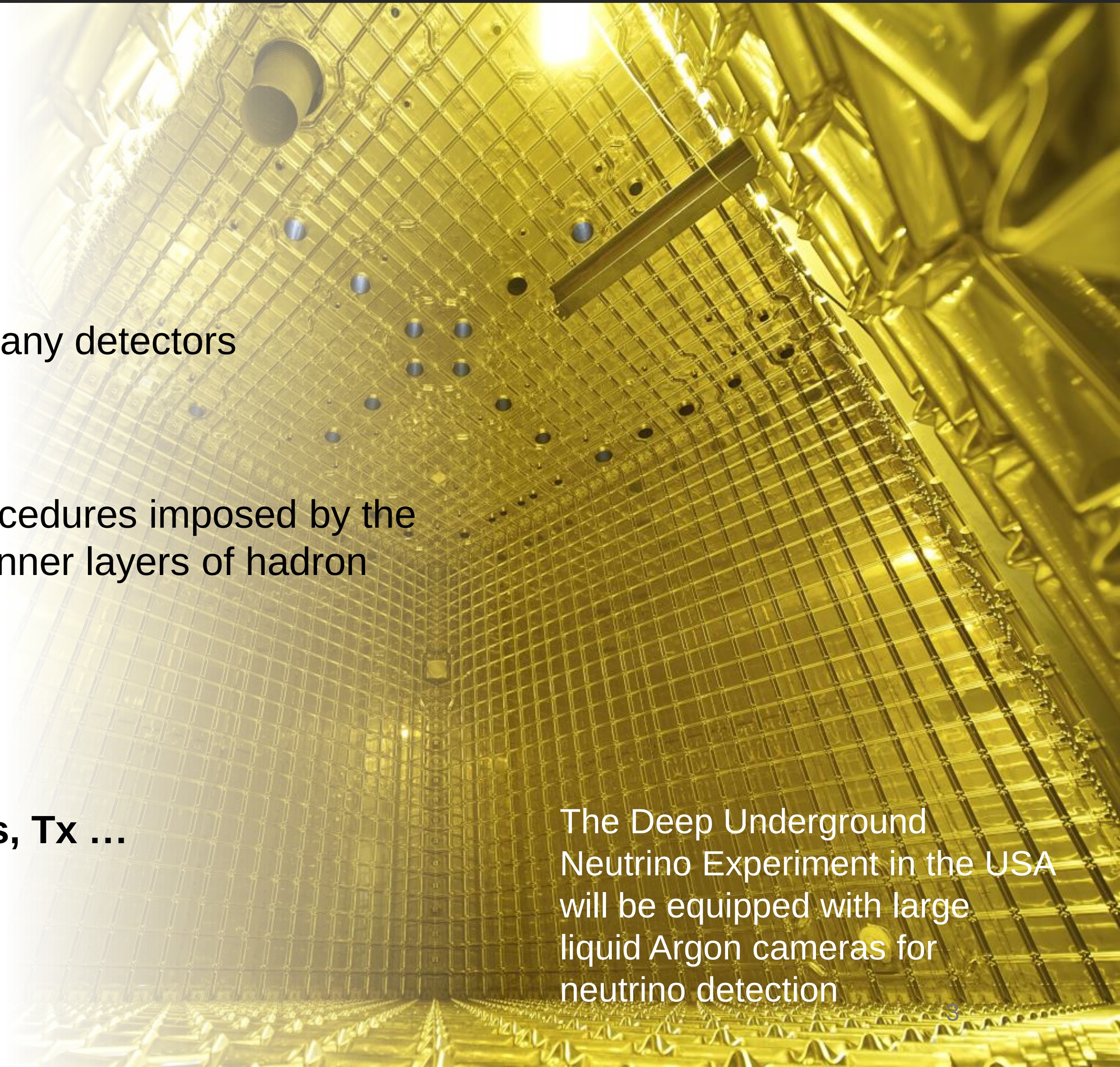
- The **sensor choice** directly influences the **front-end ASIC design**, while the ASIC architecture has a significant impact on the **DAQ system**, and vice versa.
- **This talk focuses on front-end ASICs**, which are responsible for signal amplification and conditioning
- **Future colliders** with demands for high granularity and low power consumption require the development of **dedicated ASICs**



Trends in ASICs for HEP detectors

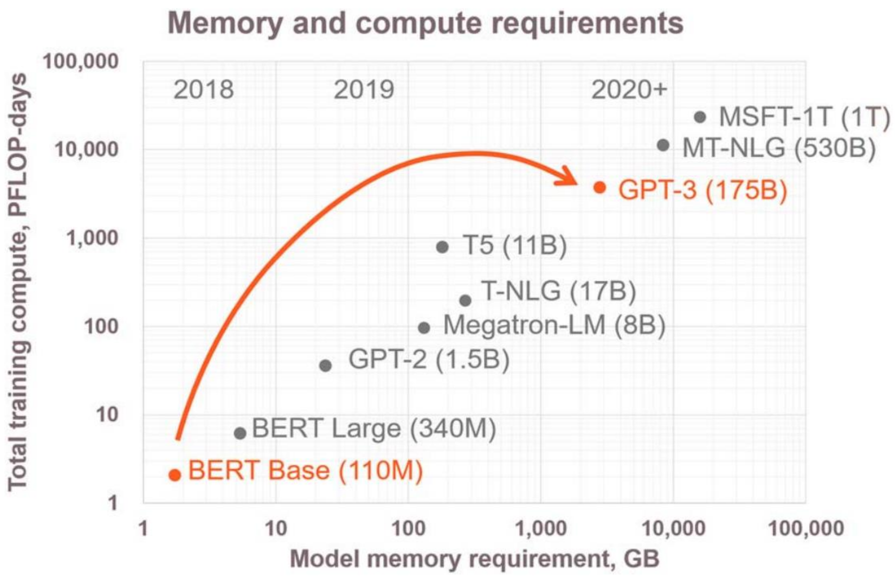
Stefano Durando

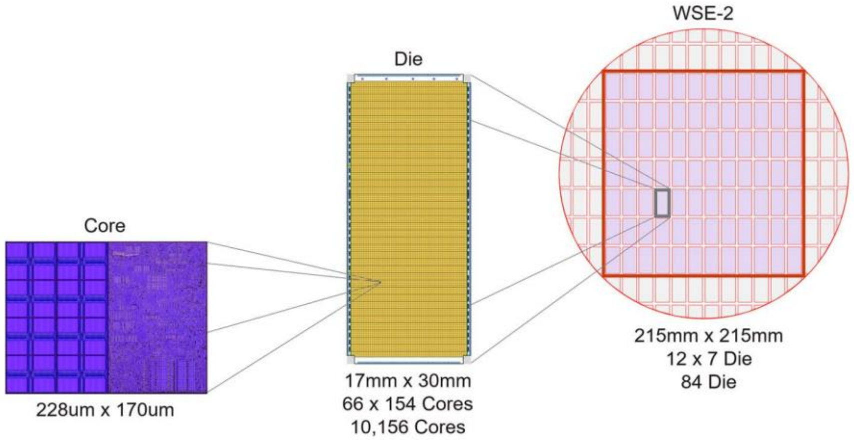
- **Finer granularity**, less power
- **CMOS Sensors increasingly used**
- **High-timing resolution** is becoming a must for many detectors
- **Harsh environment:**
  - Lengthy technology testing and validating procedures imposed by the high radiation environment (especially in the inner layers of hadron colliders)
  - The use of cryogenic CMOS is emerging
- Front-end ASICs rely on
  key common blocks : ADCs, TDCs, PLLs, DLLs, Tx …



The Deep Underground Neutrino Experiment in the USA will be equipped with large liquid Argon cameras for neutrino detection

A Wafer-Sized Processor Chip for extreme-scale ML models





Source: S. Lie, "Cerebras Architecture Deep Dive: First Look Inside the Hardware/Software Co-Design for Deep Learning," in *IEEE Micro*, vol. 43, no. 3, pp. 18-30, May-June 2023, doi: 10.1109/MM.2023.3256384

Fabrication Process	**5 nm**
Silicon Area	**46,225 mm^2**
Transistors	**4 trillion**
AI-optimized cores	**850000**
SRAM Memory (on-chip)	**44 GB**
Memory Bandwidth	**21 PB/s (7000x faster than the leading GPU)**
Fabric Bandwidth (between cores)	**214 Pb/s**

CEREBRAS

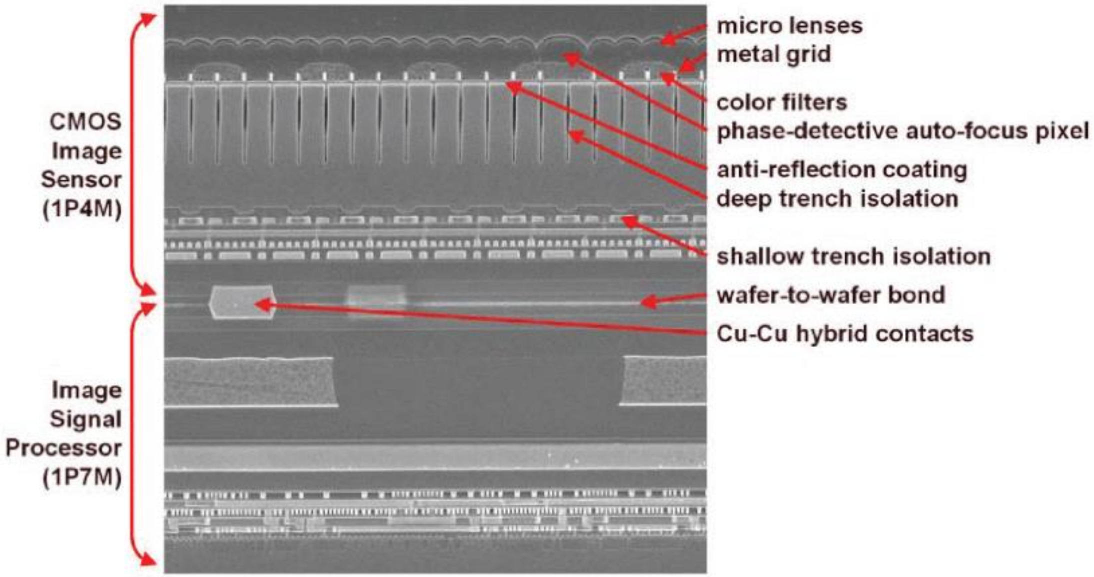
Wafer-Sized Chip

Source : https://cerebras.ai/product-chip/

CMOS Image Sensors

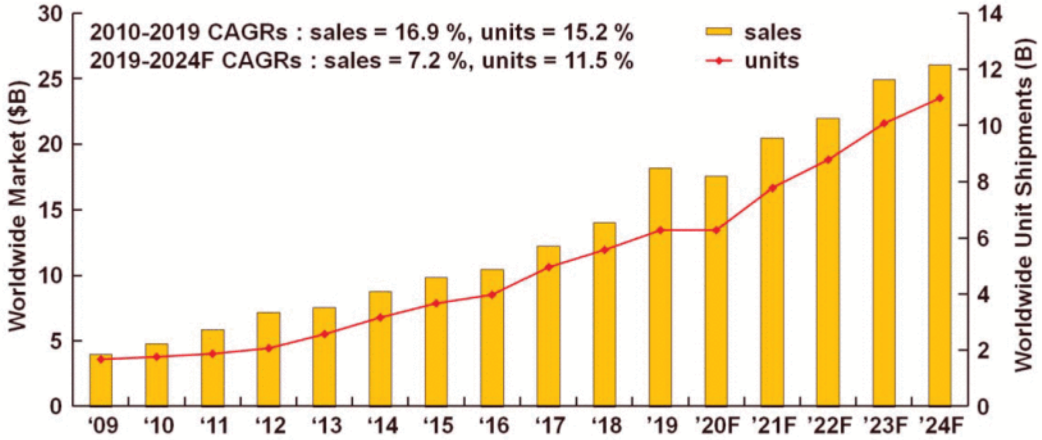
CIS market is expanding rapidly

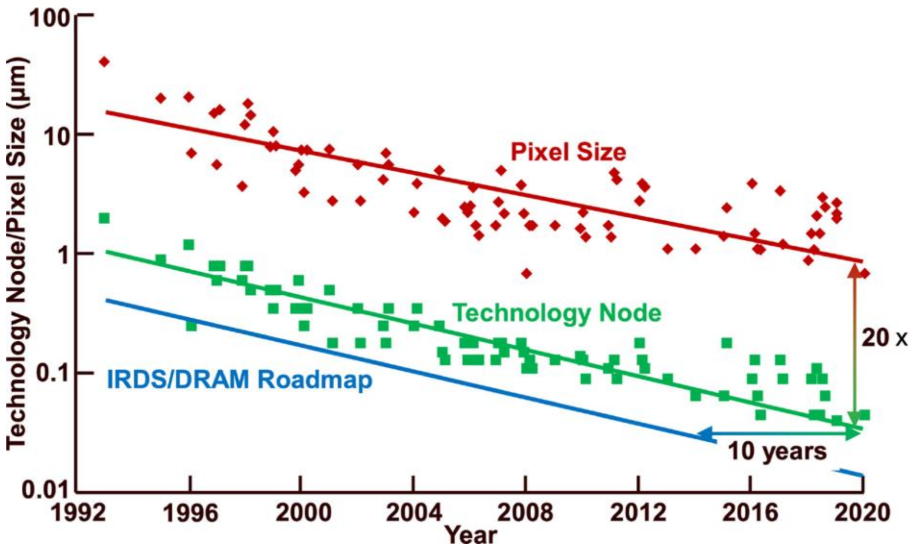
- **Primarily driven by visible light cellular camera phones**, which account for 60% of developments and sales.
- However, CISs also find crucial applications in security, human recognition, and machine vision, as well as in **scientific and medical fields**



Source: A. Theuwissen, "There's More to the Picture Than Meets the Eye, and in the future it will only become more so," *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2021, pp. 30-35, doi: 10.1109/ISSCC42613.2021.9366058.

In 2020, approximately **200 CMOS sensors per second** were produced, equating to **~10^7 wafers per year,** and these numbers continue to grow.





IRDS :International Roadmap for Devices and Systems
This represents the most advanced CMOS technology currently available in the industry.

"A 316MP, 120FPS, High Dynamic Range CMOS Image Sensor for Next Generation Immersive Displays"

Agarwal, Abhinav, Jatin Hansrani, Sam Bagwell, Oleksandr Rytov, Varun Shah, Kai Ling Ong, Daniel Van Blerkom, Jonathan Bergey, Neil Kumar, Tim Lu et al. 2023.

Sensors 23, no. 20: 8383. url: https://www.mdpi.com/1424-8220/23/20/8383

Parameter	**Specification**
Pixel Pitch	4.3 µm
Total Pixels	18400 x 17712
Active Pixels	18000 x 17568
Row Time	Single Gain: 5.5 µs, Dual Gain : 11 µs
Maximum Frame Rate	Single Gain: 120 Fps, Dual Gain: 60 Fps
ADC Resolution	12-bit (2.8 GHz count rate)
Total Sensor Power	23 W
Die Size	**9.92 cm x 8.31 cm**

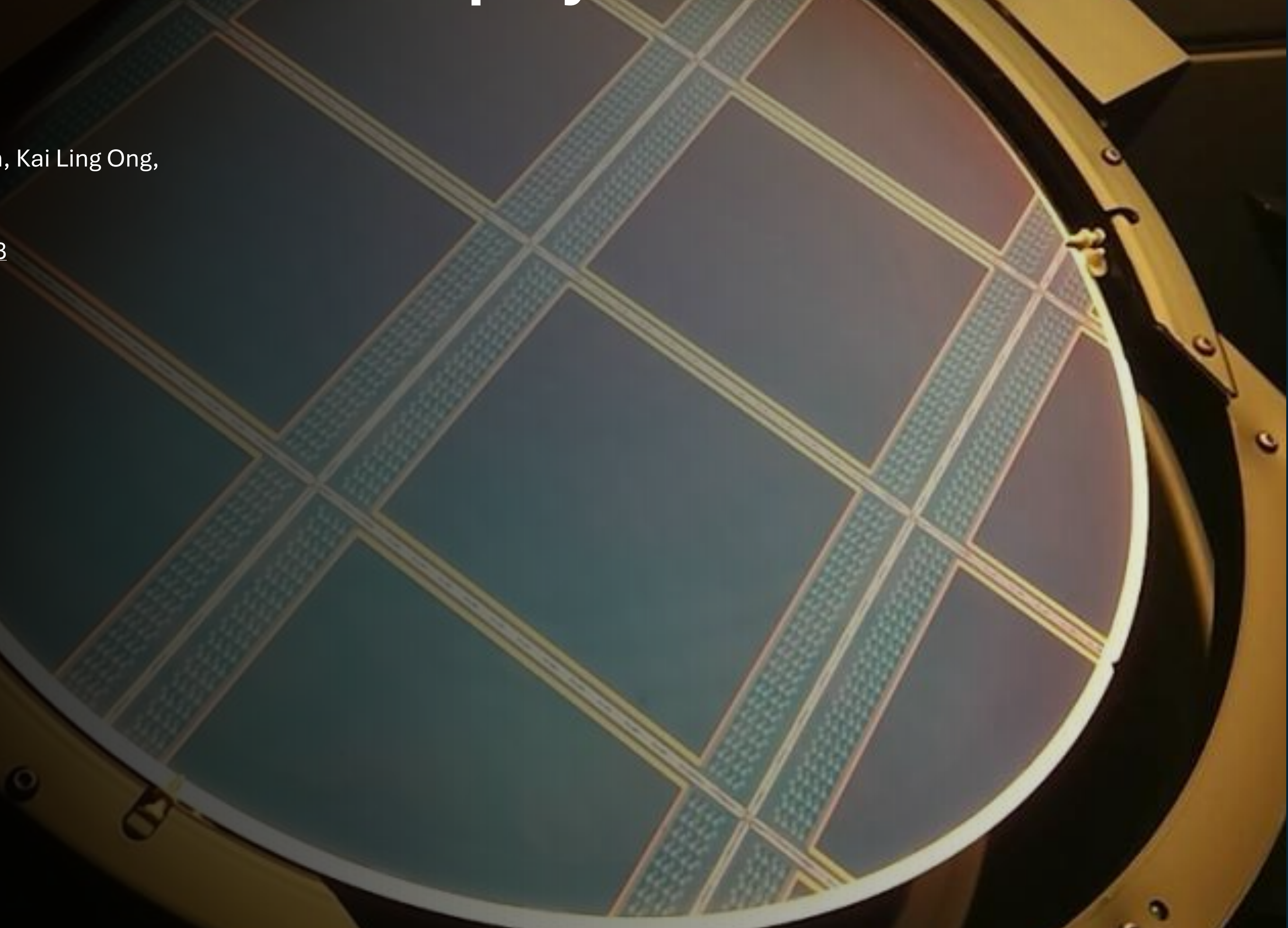
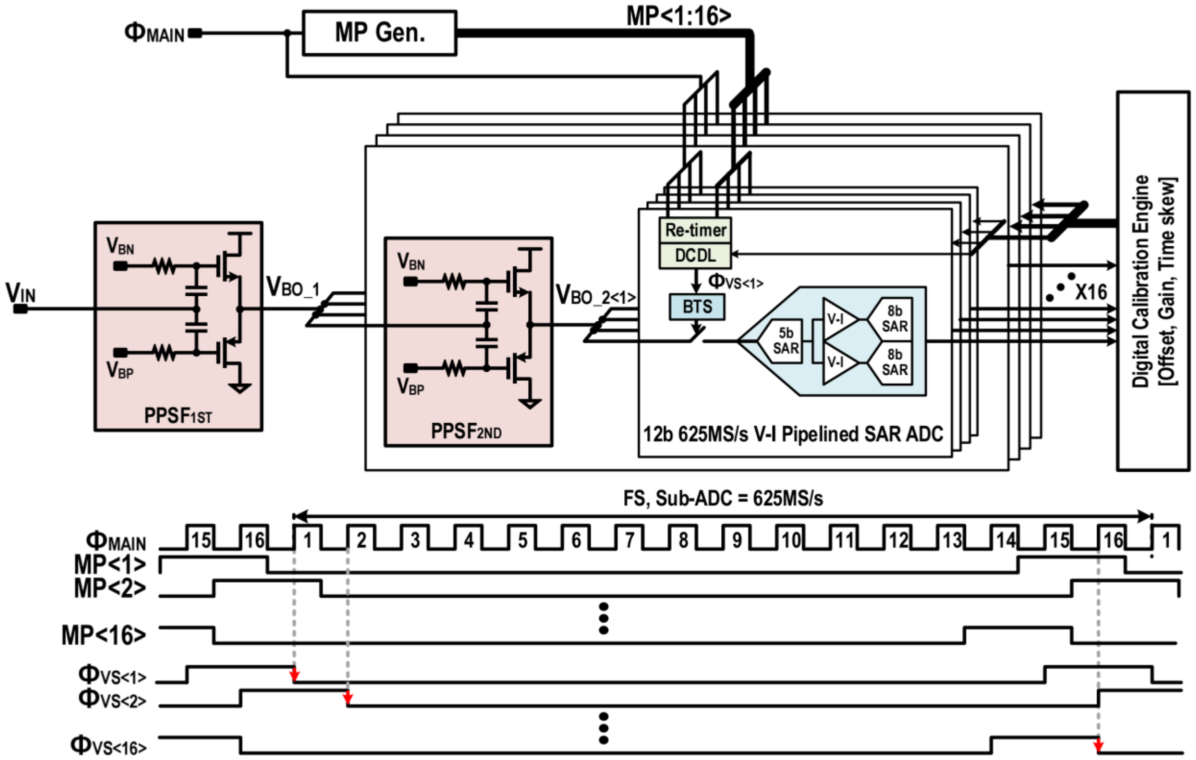


Image credits © ST Microelectronics and Sphere Entertainment Co.

Ultra - Scaled ADC

"A 12-bit 10GS/s 16-Channel Time-Interleaved ADC with a Digital Processing Timing-Skew Background Calibration in 5nm FinFET"

Source: K. -J. Moon *et al*., "A 12-bit 10GS/s 16-Channel Time-Interleaved ADC with a Digital Processing Timing-Skew Background Calibration in 5nm FinFET," *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2022, pp. 172-173, doi: 10.1109/VLSITechnologyandCir46769.2022.9830208.



Technology	**5 nm FinFET**
Architecture	**TI Pipelined SAR**
Resolution	**12**
Fs	**10 GS/s**
Supply Voltage	**0.85 V**
Power	**0.625 W**
Area (16 ch)	**2.1 mm^2**

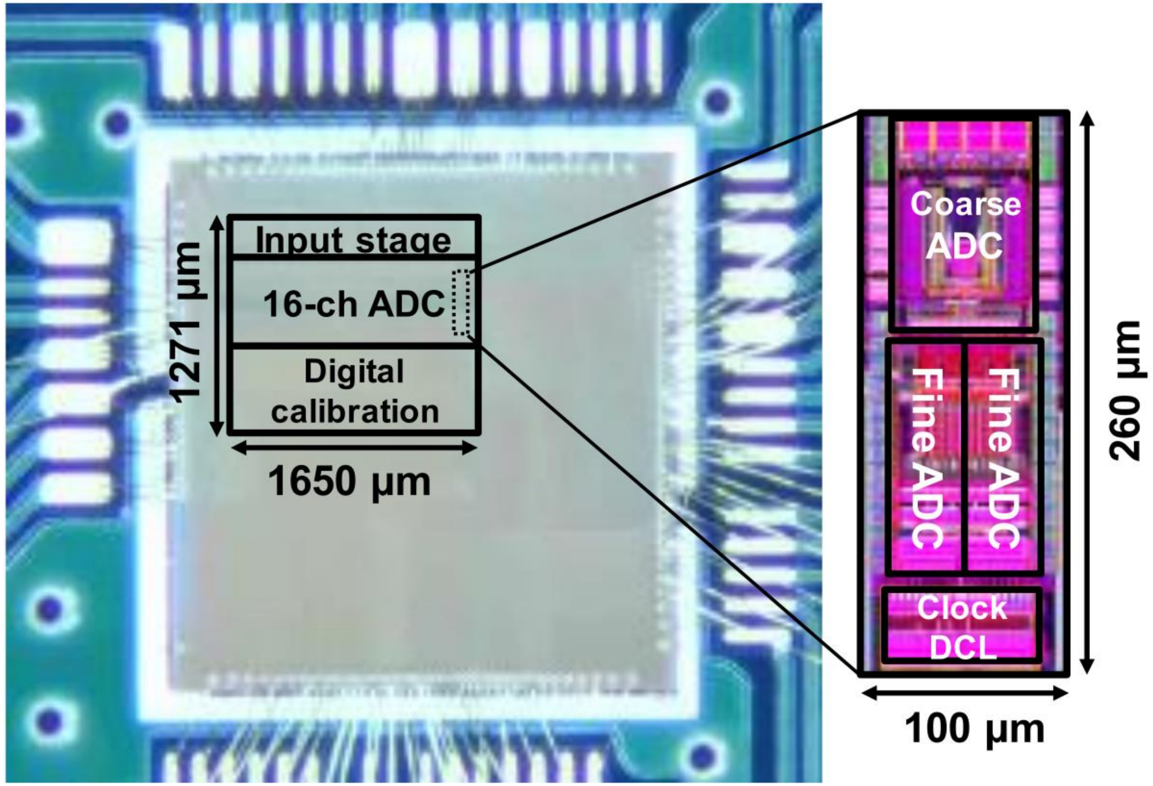
Ultra - Scaled ADCs

"A 12-bit 10GS/s 16-Channel Time-Interleaved ADC with a Digital Processing Timing-Skew Background Calibration in 5nm FinFET"

Source: K. -J. Moon *et al*., "A 12-bit 10GS/s 16-Channel Time-Interleaved ADC with a Digital Processing Timing-Skew Background Calibration in 5nm FinFET," *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2022, pp. 172-173, doi: 10.1109/VLSITechnologyandCir46769.2022.9830208.

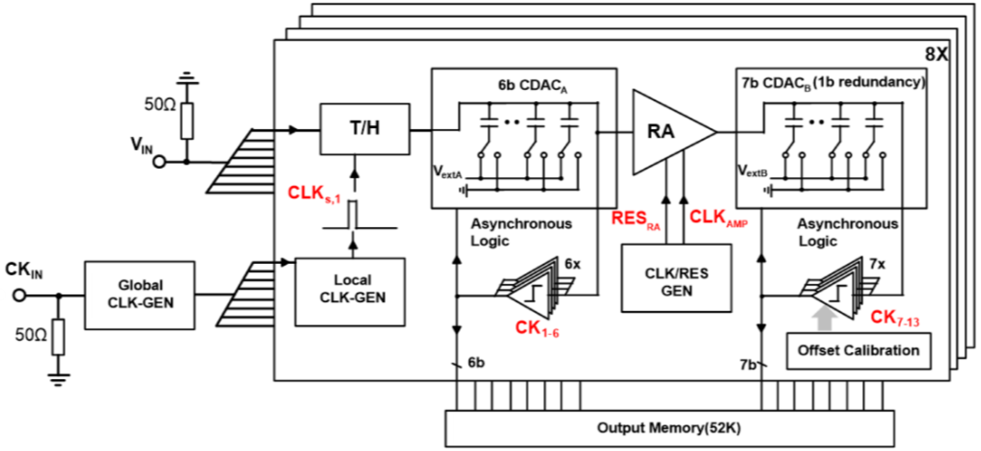
Impact of scaling:

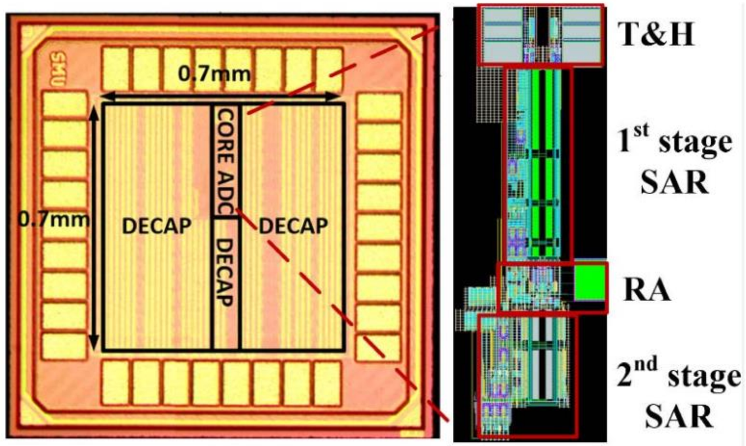
- **Size reduction** density of integration; increased dice per wafer: lower volume production costs
- **More complex structures** in the same area
- Power per transistor in principle, decreases, still, due to higher leakage currents and other effects, **the power consumption does not scale with the area of the ADC**
- **Keeping the SNR high gets very challenging**



65 nm ADC

“A 2.56-GS/s 12-bit 8x-Interleaved ADC With 156.6-dB FoM in 65-nm CMOS”





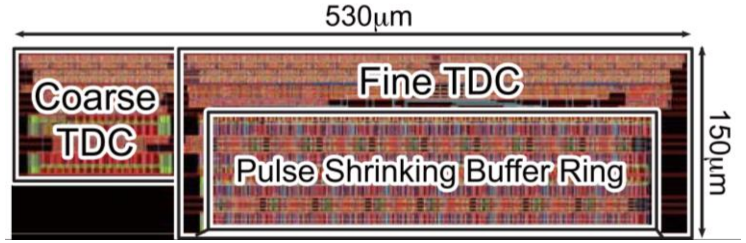
Source: L. Fang *et al*., "A 2.56-GS/s 12-bit 8x-Interleaved ADC With 156.6-dB FoMS in 65-nm CMOS," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 30, no. 2, pp. 123-133, Feb. 2022, doi: 10.1109/TVLSI.2021.3133451.

Technology	**65 nm**
Architecture	**Pipelined SAR**
Resolution	**12**
Fs	**2.56 GS/s**
Supply Voltage	**1.2 V**
Power	**0.105 W**
Area (1 ch)	**0.01 mm^2**

TDCs

“A 16-bit <u>2.0-ps</u> Resolution Two-Step TDC in <u>0.18-μm</u> CMOS Utilizing Pulse-Shrinking Fine Stage With Built-In Coarse Gain Calibration”

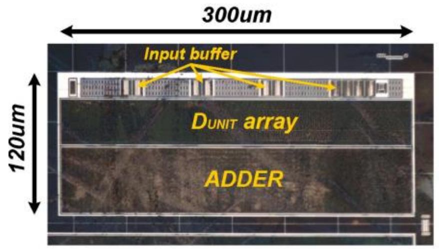
R. Enomoto, T. Iizuka, T. Koga, T. Nakura and K. Asada, in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 1, pp. 11-19, Jan. 2019, doi: 10.1109/TVLSI.2018.2867505.



Technology	180 nm CMOS
Architecture	Pulse shrinking + Two Steps
<u>Time Resolution</u>	<u>2 ps</u>
Range	16 bit
INL [LSB]	4.2
<u>Fs</u>	<u>3 MS/s</u>
Supply Voltage	1.8 V
Power	18 mW
Area	0.08 mm^2

“15.5 A 0.6V 1.17ps PVT-tolerant and synthesizable time-to-digital converter using stochastic phase interpolation with 16× spatial redundancy in 14nm FinFET technology”

S. -J. Kim, W. Kim, M. Song, J. Kim, T. Kim and H. Park, *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, San Francisco, CA, USA, 2015, pp. 1-3, doi: 10.1109/ISSCC.2015.7063035

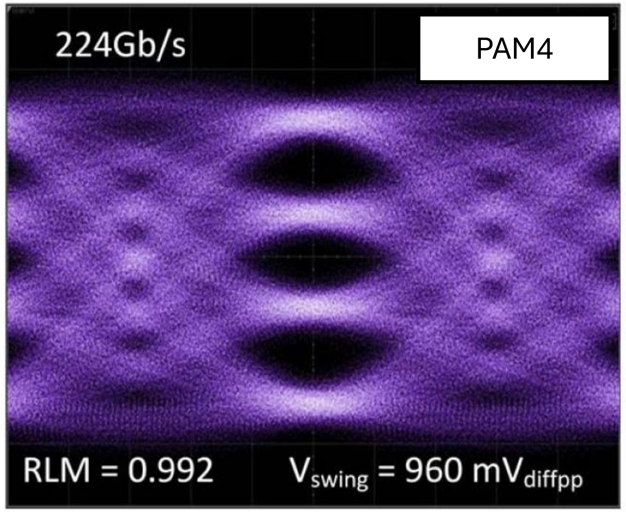


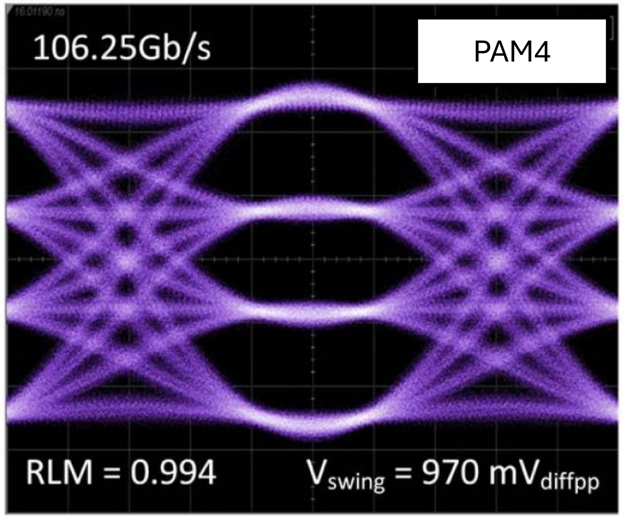
Technology	14 nm FinFET
Architecture	Stochastic
<u>Time Resolution</u>	<u>1.17 ps</u>
Range	10 bit
INL [LSB]	2.3
<u>Fs</u>	<u>100 MS/s</u>
Supply Voltage	0.6 V
Power	0.78 mW
Area	0.036 mm^2

State-of-the-art TXs

"7.3 A 224Gb/s 3pJ/b 40dB Insertion Loss Transceiver in 3nm FinFET CMOS"

D. Pfaff et al., 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 128-130, doi: 10.1109/ISSCC49657.2024.10454537.





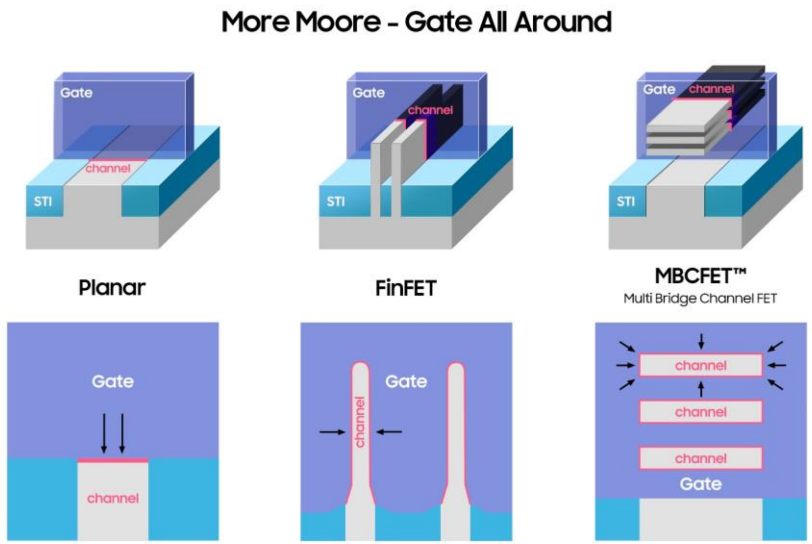
Measured transmitter eye diagrams

Technology	3 nm
Data Rate	224 Gb/s
Supply Violtage	1.1 V
Efficiency (Tx)	1.0 pJ/bit

A Technology Ecosystem

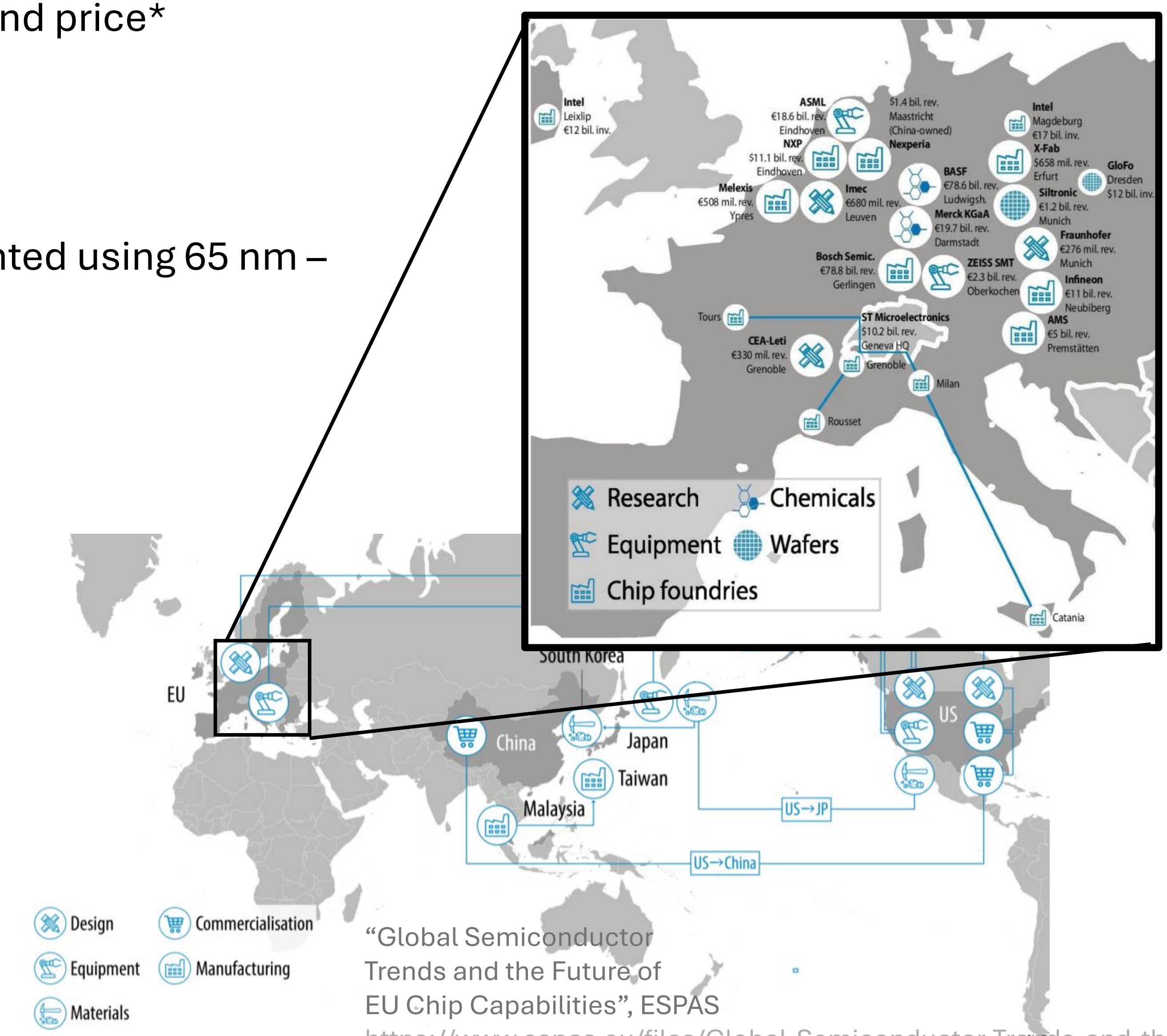
Stefano Durando

- Two orders of magnitudes in transistor gate length and price*
  - 3 nm – 350 nm
- The technology choice depends on the purpose
- At present, system grade chip for HEP are implemented using 65 nm – 130 nm
- Solid R&D for 28 nm and initial activities on FinFETs



Source: https://semiconductor.samsung.com/news-events/tech-blog/3nm-gaa-mbcfet-unrivaled-sram-design-flexibility/

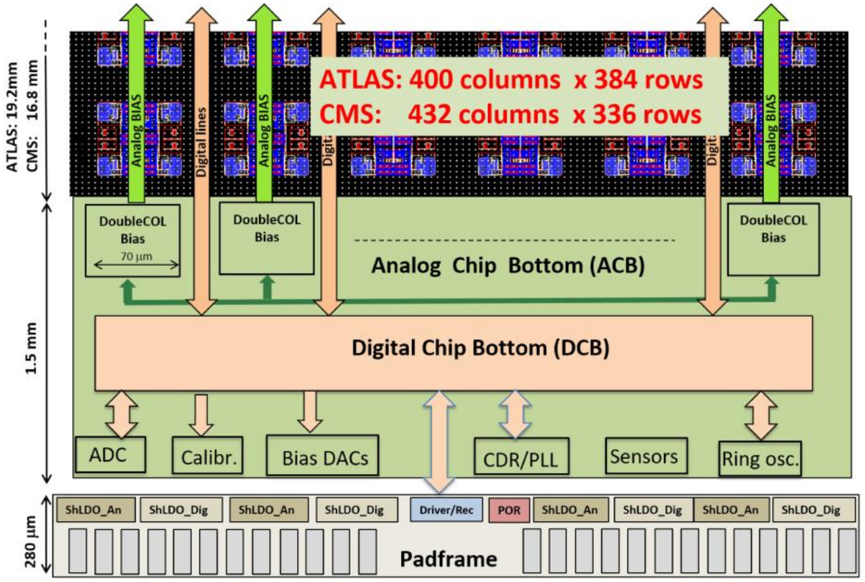
https://europractice-ic.com/technologies/asics/



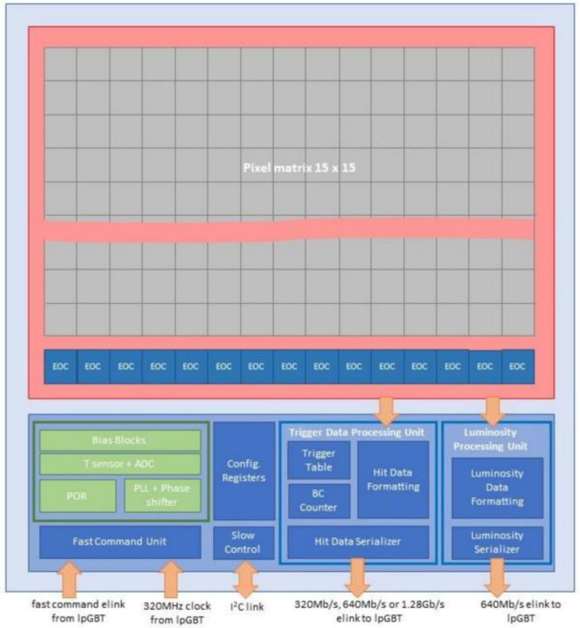
“Global Semiconductor Trends and the Future of EU Chip Capabilities”, ESPAS https://www.espas.eu/files/Global-Semiconductor-Trends-and-the-Future-of-EU-Chip-Capabilities-2022.pdf

ASICs for Hybrid Detectors

Stefano Durando



Source: «The RD53C-ATLAS Pixel Readout Chip Manua», CERN-RD53-PUB-xxxx Version 1.92, September 18, 2024, url:



Source: «ALTIROC2, a readout ASIC for the High Granularity Timing Detector in ATLAS», url: https://indico.cern.ch/event/799025/contributions/3486217/attachments/1903456/3142875/TWEPP2019_HGTD.pdf

RD53

- Comon design framework for ATLAS and CMS HL-LHC pixel detectors (25 / 50 µm pitch)
- Extreme hit rates condition (3 GHz/cm^2), high trigger rate (1MHz) 1 Grad over 10 y
- **65 nm** CMOS technology
- Readout up to **5.12 Gbits/s**.
- Strucutre: Pixel Matrix + chip bottom (reticle size)

ALTIROC

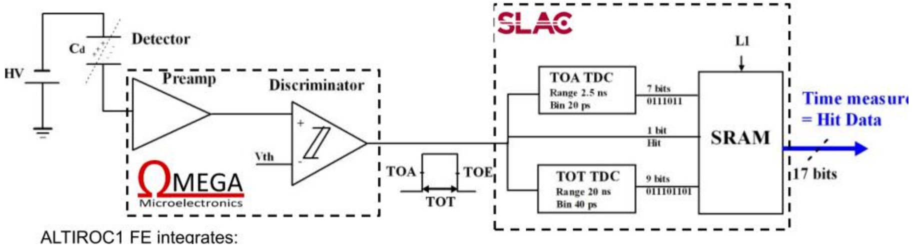
- ASIC for the ATLAS High Granularity Timing Detector
- Precision timing of charged particles (30 ps, MIP) and beam luminosity measurement
- Reading-out 225 LGADs
- **130 nm** CMOS tecnology
- 20 ps bin TDC on-pixel
- 320-640 Mb/s or 1.28 Gb/s e-links to lpGBT boards

Achieving **sub-50 ps timing resolution** for Minimum Ionizing Particles (MIPs) is a key requirement for the next generation of collider experiment detectors

This necessitates **end-to-end optimization**, from the **sensor and front-end electronics** to the **entire system architecture**:

$$\sigma_t^2 = \sigma_{sensor}^2 + \sigma_{FE\,jitter}^2 + \sigma_{timewalk}^2 + \sigma_{TDC}^2 + \sigma_{clk\,jitter}^2 + \;\ldots$$

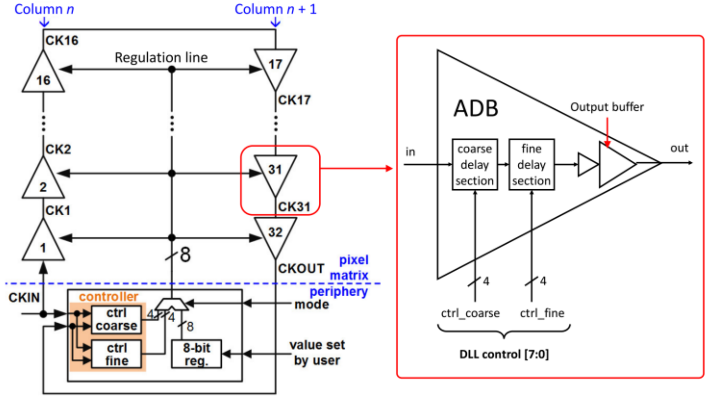
- In principle, **Time-to-Digital Converters (TDCs)** are not a limiting factor, as **state-of-the-art architectures** offer resolution on the order of **≈ 1 ps**
- Once the front-end design is finalized, it is critical to maintain low-jitter clock propagation across the channel matrix.



ALTIROC1 FE integrates:

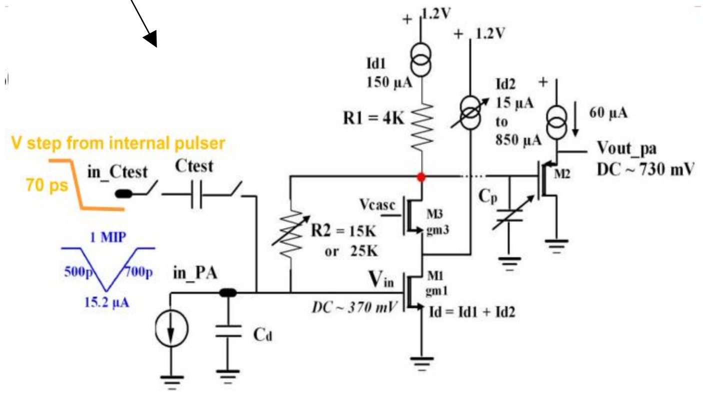
TimePix4:

- **65 nm CMOS**
- Gas-filled detectors and Si pixels (55 µm pitch)
- 512 x 448 pixels
- 4-side buttable, 1.5 bn transistors
- ToA (200ps) and ToT (Q), 60 ps TDC
- **A 40 MHz reference clock is distributed across the matrix using a digital delay-locked loop (DLL) to ensure a well-defined clock phase at the pixels, with a target skew of less than 100 ps**

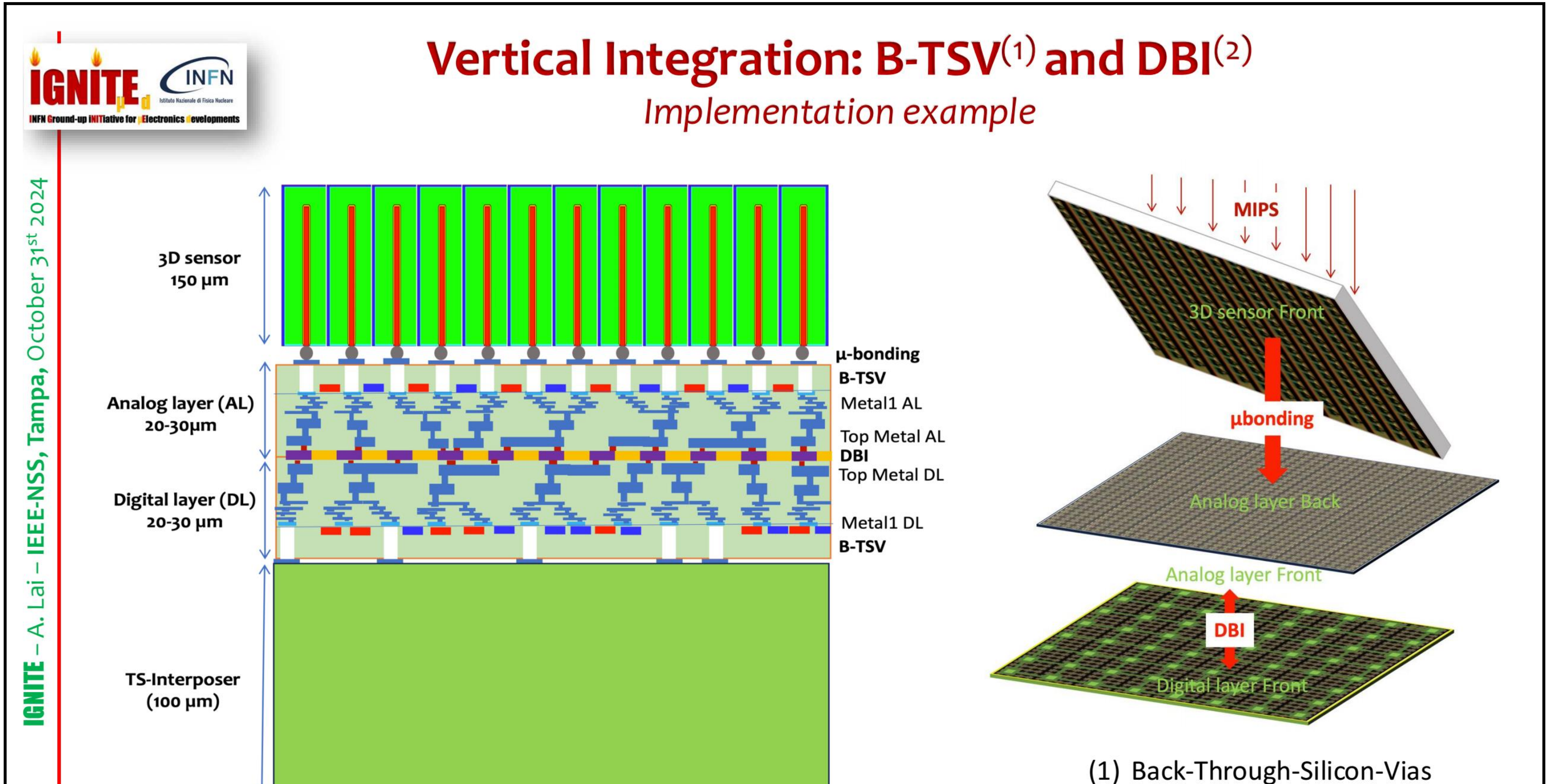


K. Heijhoff *et al* 2022 *JINST* **17** P07006
url: https://iopscience.iop.org/article/10.1088/1748-0221/17/07/P07006

ALTIROC Channel and VFE



IGNITE



NSS 2024
The Fractal ASIC series of IGNITE:
CMOS 28-nm technology for high-precision 4D-tracking

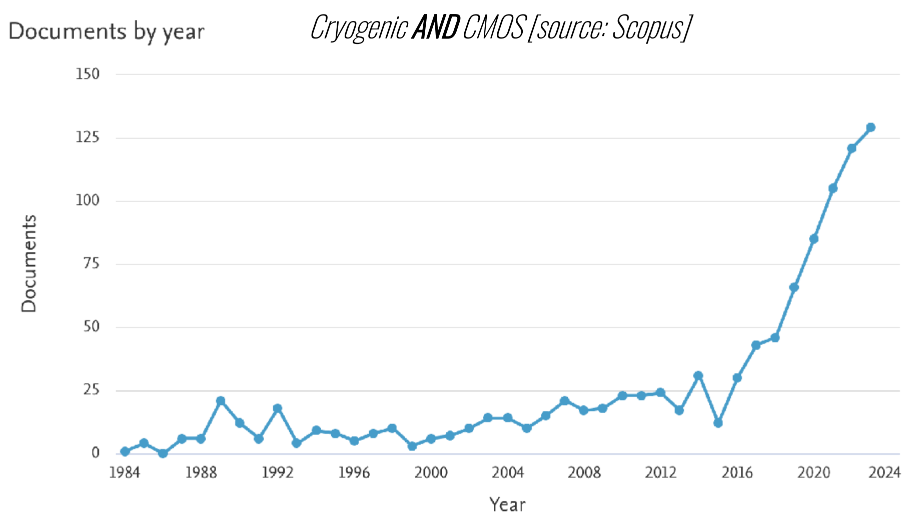
- **INFN project**
- **4D tracking**
- **28 nm**
- **Modular Structure**

Cryogenic ASICs

Stefano Durando

CMOS technologies capable of operating at **cryogenic temperatures** are attracting increasing interest :

- **Rare event search on astroparticles** — Mild cryogenic
  Neutrino and Dark Matter detection using Liquid Argon (88K) and Xenon (165 K)
- **Quantum computing:** — Deep cryogenic (< 4 K)
  Q bits operate in the mK range,
- **Extensive modeling campaign** → **Cryo-PDKs**
  GF22 nm FDSOI: A Collaborative Effort Between Fermilab and Synopsys
  Fermilab 65 nm cryo models and IPs: LVDS Tx and Rx, bandgap, level shifters, IOs…
  ECFA, DRD7.4.a "Device Modelling and Development of Cryogenic CMOS PDKs and IP"

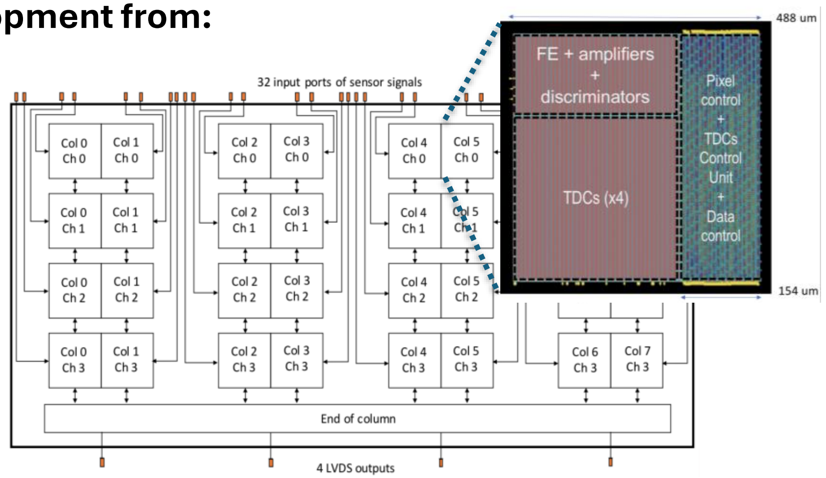


Deep Underground Neutrino Experiment (DUNE)

A 1024 ch ASICs for GRAIN lAr detector in the ND is being developed at INFN . Baseline development from:

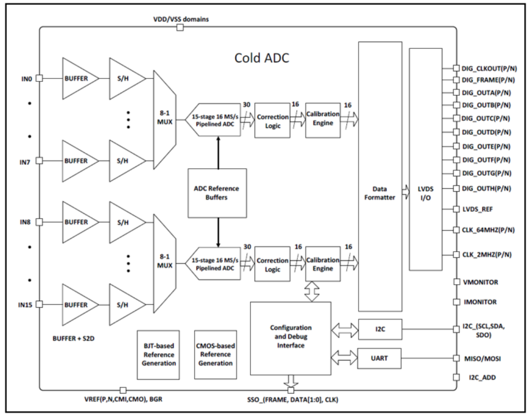
ALCOR ASIC for SiPM readout at low T

- INFN (TO), Darkside framework
- 110 nm UMC
- 32 pixels mixed signal ASIC
- Single Photon time tagging or time and charge measurements
- 50 ps bin TDC
- 4 LVDS Tx data links, SPI, up to 320 MHz

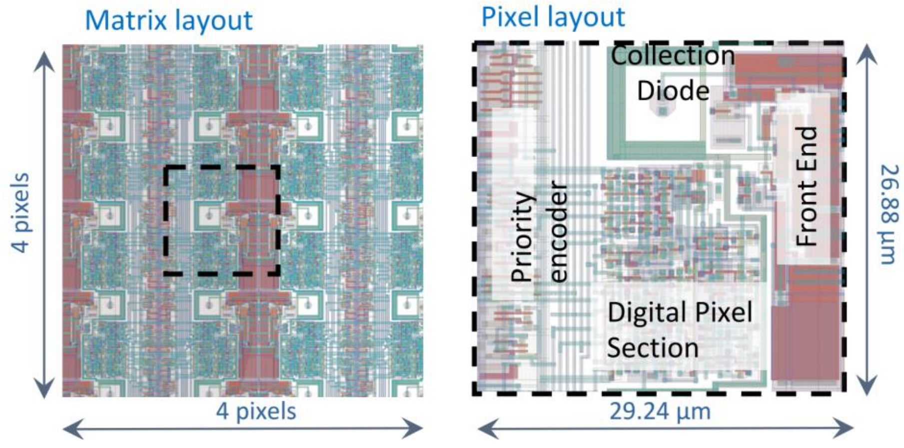


COLDADC (LBNL, FNAL, BNL)

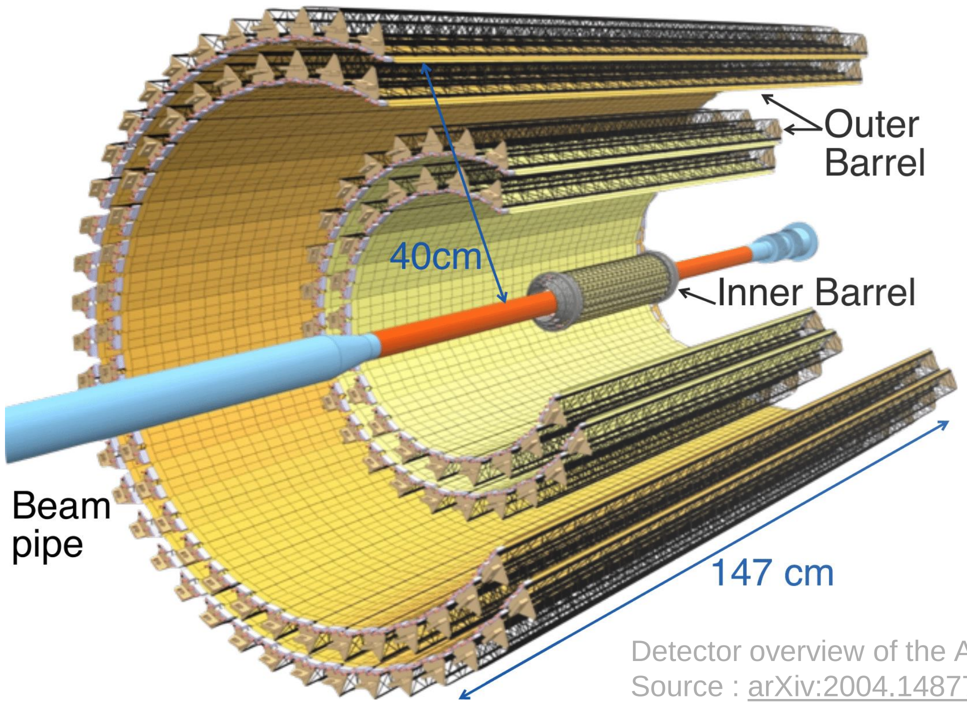
- 65 nm CMOS
- Two 15-stage pipeline ADCs operating at 16 MHz
- Digital calibration with automatic calibration
- For both single ended and differential input signals
- 11.8 b ENOB at 77 K



From CMOS Image Sensors to HEP Applications



ALPIDE Layout



Detector overview of the ALICE ITS2.
Source : arXiv:2004.14877

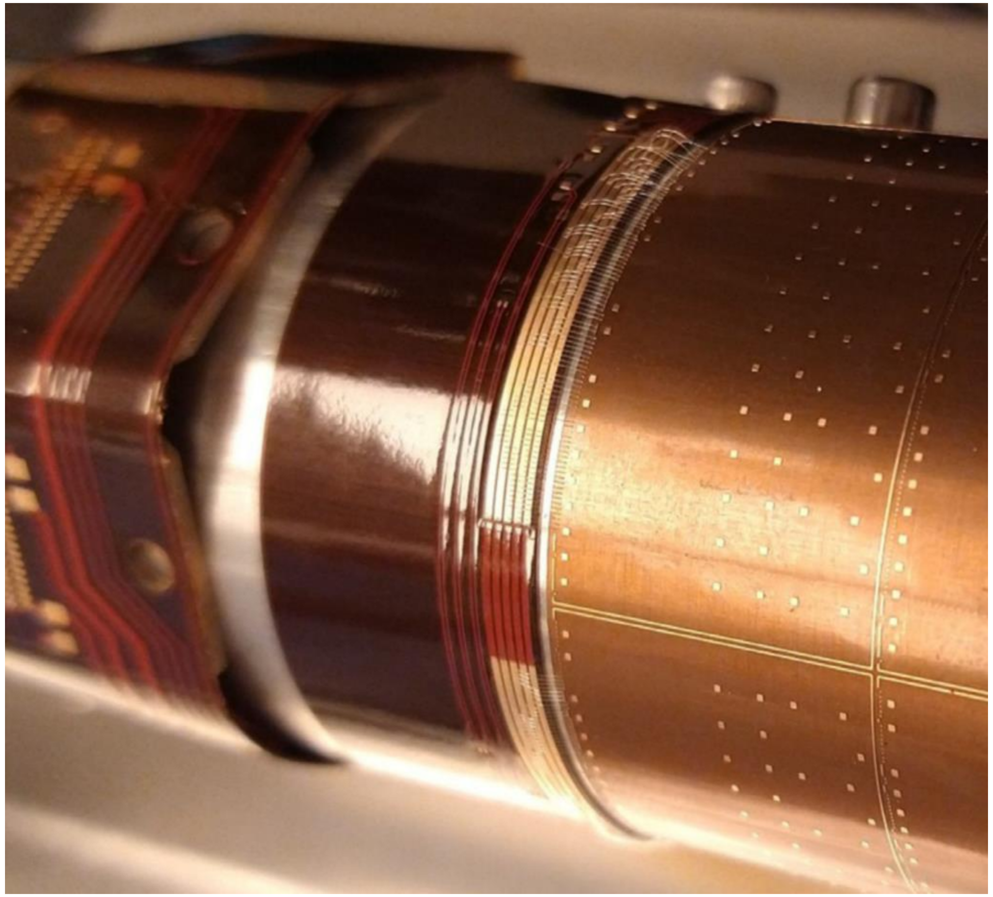
- **Higher functionality on-pixel** which limits the minimum pixel pitch (tens of micrometers)
- **Capability to distinguish single particle hits** with less than 1% of hit pixels per frame
- **High position resolution**, down to a few micrometres for tracking applications
- **High time resolution for single events** (<100 ps with MIPs), driven by increasingly accurate Time of Flight systems or 4D/5D tracking, beam-induced background suppression in muon colliders …
- **High collection efficiency** over the full coverage area
- **Enhanced radiation tolerance**, withstanding doses up to 10 MGy and fluences up to $10^{16\text{-}17}\ \frac{n_{eq}}{cm^2}$ or more (FCC)
- **Large area multichannel systems** (tens of m^2), necessitating low power densities ($\frac{mW}{cm^2}$)

MAPS for tracking applications: Stitching and Bending

ALICE is leading the adoption of **bent, wafer-scale pixel sensors** for the ITS3, targeted for **Run 4 at the LHC in 2029:**

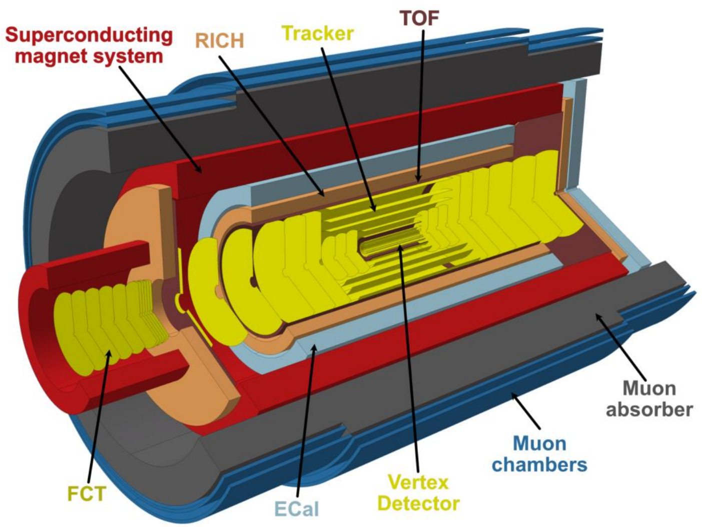
- **Stitching**: Enables the integration of large-area sensors
- **Bending**: Achieved with **30 µm-thick silicon**, allowing for curved geometries
- **Cooling**: Utilizes an **airflow-based system**

→ Advantage: Minimal material budget



A. Kluge, ALICE - ITS3 — A bent, wafer-scale CMOS detector,
NIM, Detectors and Associated Equipment, Volume 1041, 2022, 167315, ISSN 0168-9002, https://doi.org/10.1016/j.nima.2022.167315.
url::https://www.sciencedirect.com/science/article/pii/S0168900222006386

MAPSs for Timing Applications: ALICE 3 (LHC)



Component	Observables	Barrel ($|\eta| < 1.75$)	Forward ($1.75 < |\eta| < 4$)	Detectors
Vertexing	(Multi-)charm baryons, dielectrons	Best possible DCA resolution, $\sigma_{DCA} \approx 10\,\mu m$ at $p_T = 200\,MeV/c$, $\eta = 0$	Best possible DCA resolution, $\sigma_{DCA} \approx 30\,\mu m$ at $p_T = 200\,MeV/c$, $\eta = 3$	retractable Si-pixel tracker: $\sigma_{pos} \approx 2.5\,\mu m$, $R_{in} \approx 5\,mm$, $X/X_0 \approx 0.1\,\%$ for first layer
Tracking	(Multi-)charm baryons, dielectrons, photons ...	$\sigma_{p_T}/p_T \approx 1 - -2\,\%$		Silicon pixel tracker: $\sigma_{pos} \approx 10\,\mu m$, $R_{out} \approx 80\,cm$, $L \approx \pm 4\,m$ $X/X_0 \approx 1\,\%$ per layer
Hadron ID	(Multi-)charm baryons	$\pi/K/p$ separation up to a few GeV/c		Time of flight: $\sigma_{tof} \approx 20\,ps$ RICH: $n \approx 1.006 - 1.03$, $\sigma_\theta \approx 1.5\,mrad$
Electron ID	Dielectrons, quarkonia, $\chi_{c1}(3872)$	pion rejection by 1000x up to 2–3 GeV/c		Time of flight: $\sigma_{tof} \approx 20\,ps$ RICH: $n \approx 1.006 - 1.03$, $\sigma_\theta \approx 1.5\,mrad$
Muon ID	Quarkonia, $\chi_{c1}(3872)$	reconstruction of J/ψ at rest, i.e. muons from $p_T \sim 1.5\,GeV/c$ at $\eta = 0$		steel absorber: $L \approx 70\,cm$ muon detectors
ECal	Photons, jets	large acceptance		Pb-Sci sampling calorimeter
ECal	χ_c	high-resolution segment		$PbWO_4$ calorimeter
Soft photon detection	Ultra-soft photons		measurement of photons in p_T range 1–50 MeV/c	Forward conversion tracker based on silicon pixel tracker

ALICE 3 Upgrade: Planned Data Taking from 2035

Among LHC experiments, ALICE 3 has specifications closely aligned with the **first stage of the FCC-ee:**

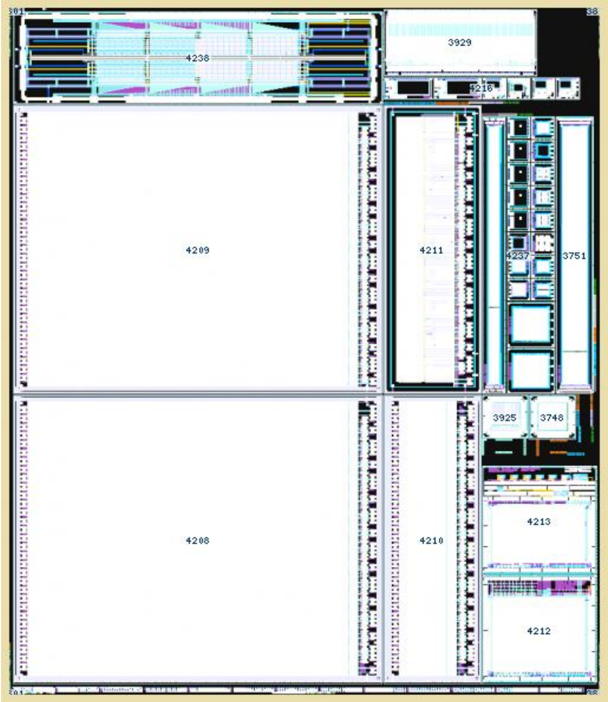
- **Moderate hit rate**
- **Moderate radiation hardness**
- **Very low material budget**

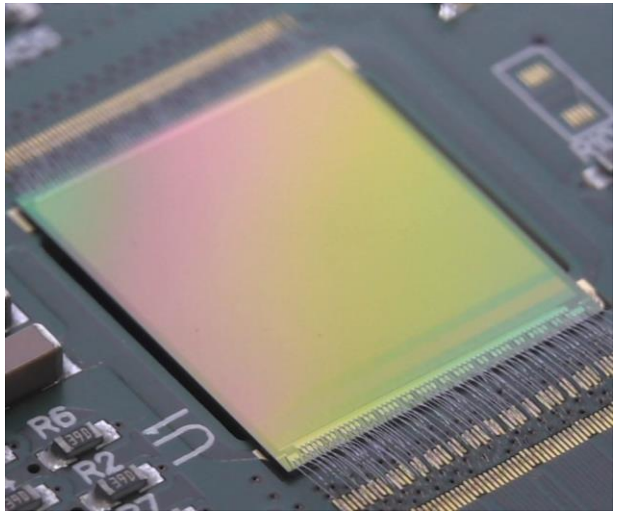
It will implement MAPSs in the ITS

and a **MAPS-based solution** is being explored for the new **46 m^2 Time-of-Flight (ToF) layers**.

- Targeting **sub-20 ps time resolution** for Particle Identification (PID)
- Currently, no existing technology meets the **timing requirements** and is scalable to **46 m^2**.
- The INFN ToF Working Group has initiated R&D efforts, leveraging the **ARCADIA project** based on a **CIS 110 nm technology by LFoundry**

ARCADIA Main Demonstrator



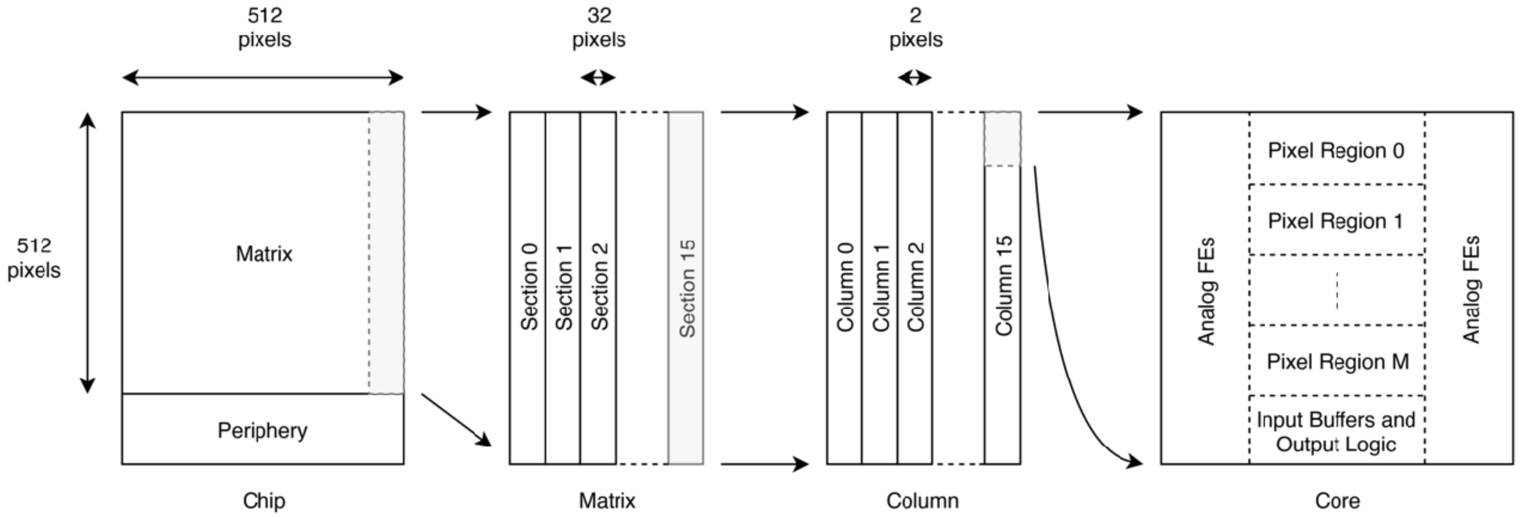


LFoundry 110-nm commercial CIS process, enabling in-pixel complex circuitry with low prototyping costs, **3 engineering runs** (2020-2022)

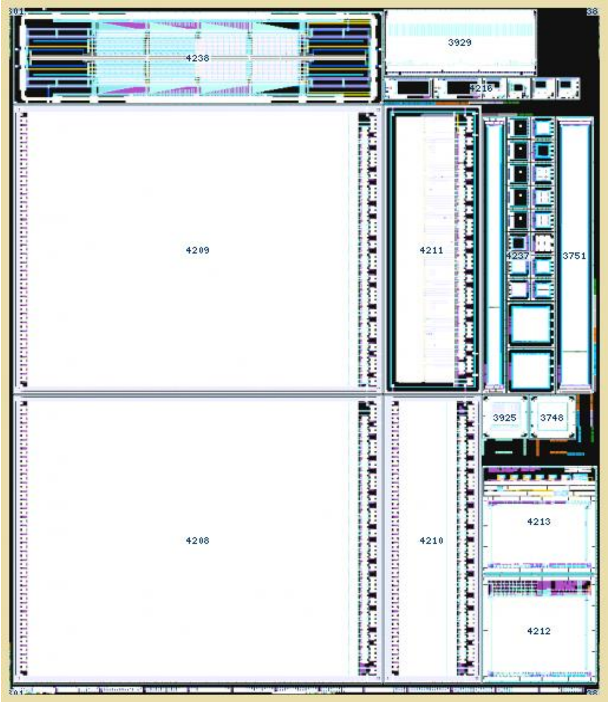
Main Demonstrator (MD):

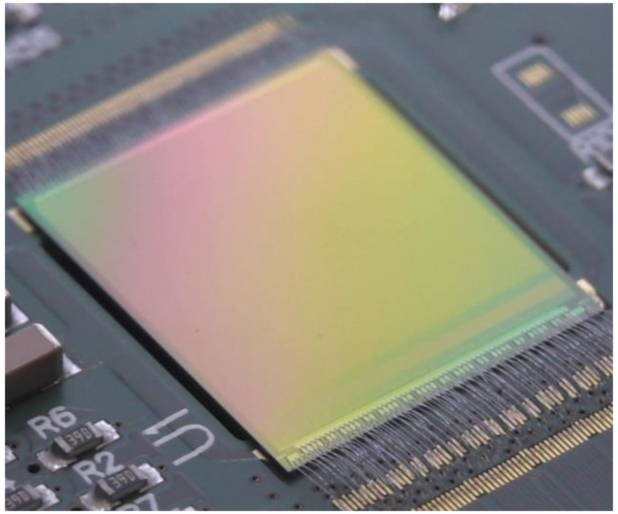
- Pixel size **25 µm x 25 µm**, Matrix core **512 x 512**, **1.28 x 1.28 cm^2** silicon active area, “side-buttable"
- Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
- Event rate up to **100 MHz/cm^2** (design post-layout simulations)
- High-rate operation (16 Tx): **17-30 mW/cm^2** depending on transceiver driving strength (measured)
- Low-power operation (1 Tx): **10 mW/cm^2** (all data conveyed in 1 transceiver, others turned-off)

→ Baseline Technology for the Vertex Detector of IDEA



ARCADIA Main Demonstrator



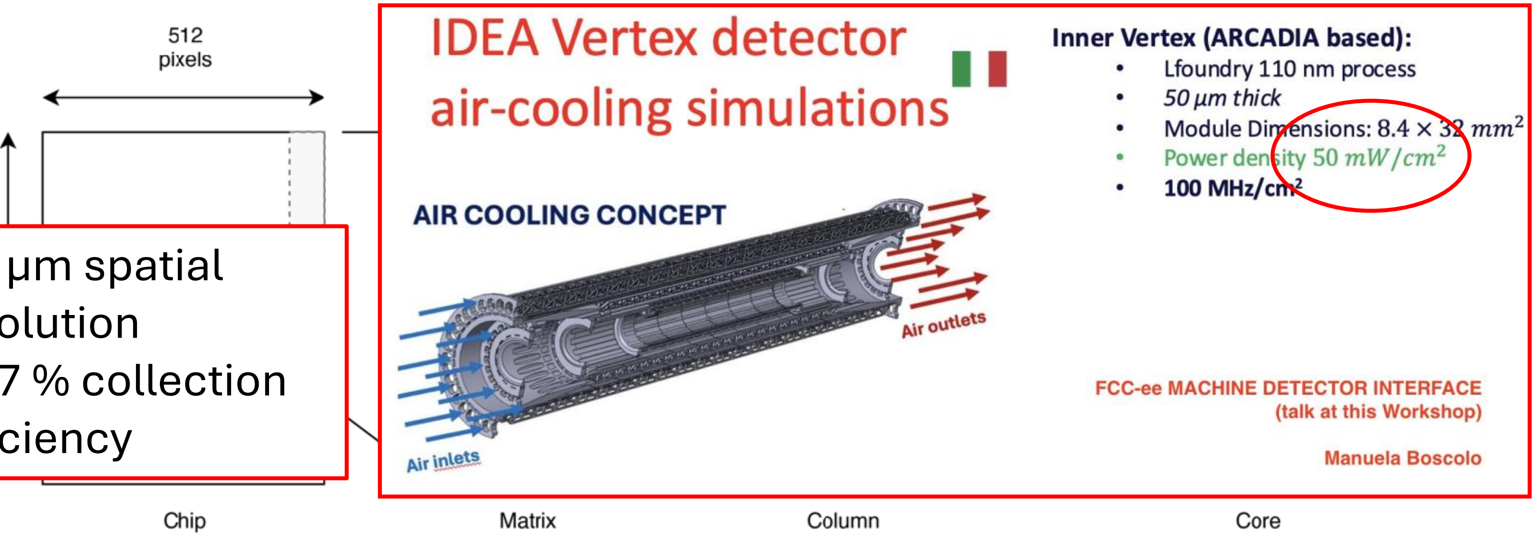


LFoundry 110-nm commercial CIS process, enabling in-pixel complex circuitry with low prototyping costs, **3 engineering runs** (2020-2022)

Main Demonstrator (MD):

- Pixel size **25 µm x 25 µm**, Matrix core **512 x 512**, **1.28 x 1.28 cm^2** silicon active area, "side-buttable"
- Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
- Event rate up to **100 MHz/cm^2** (design post-layout simulations)
- High-rate operation (16 Tx): **17-30 mW/cm^2** depending on transceiver driving strength (measured)
- Low-power operation (1 Tx): **10 mW/cm^2** (all data conveyed in 1 transceiver, others turned-off)

→ **Baseline Technology for the Vertex Detector of IDEA**



- 4.7 µm spatial resolution
- 99.7 % collection efficiency

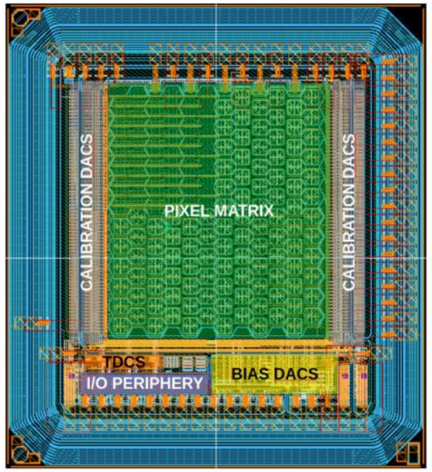
MAPSs with Internal Gain

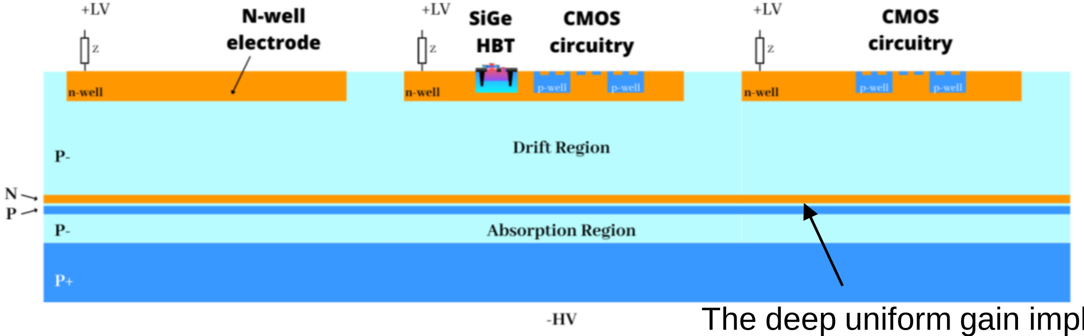
Stefano Durando

The integration of **internal amplification within MAPS sensors** marks a significant step toward a new generation of **high-time-resolution monolithic detectors**

Picosecond Avalanche Detector (PicoAD)

- University of Geneva
- SiGe BiCMOS,
  IHP microelectronics 130 nm
- $\boldsymbol{\sigma_{t-MIP}} \approx$ **20 ps; 2.7 W/cm^2**
  $\boldsymbol{\sigma_{t-MIP}} \approx$ **30 ps; 0.04 W/cm^2**
- Hexagonal pixels,
  pitch = 65 -130 µm
  C ≈ 100 fF



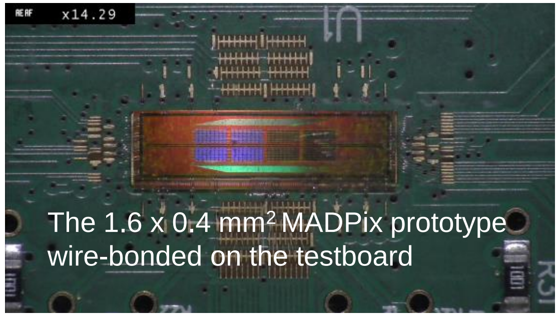


The deep uniform gain implant provides a uniform electric field

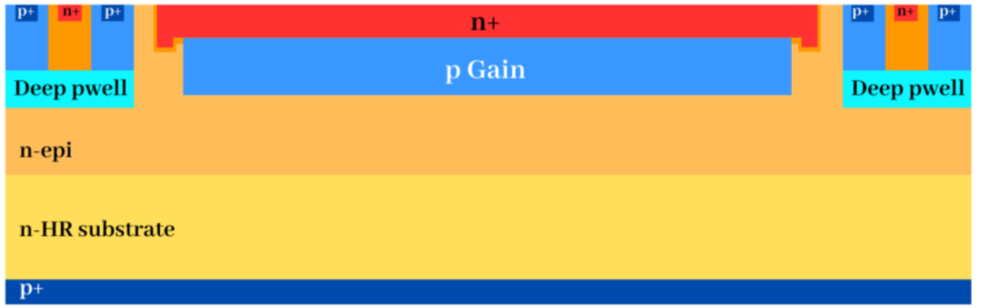
Source: PicoAD G. Iacobucci *et al* 2022 *JINST* **17** P10040

Monolithic Avalanche Detector Pixelated prototype **(MADPix)**

- INFN (ARCADIA)
- Lfoundry 110 nm CIS process
- **Under development, targeting 20 ps**
- Rectangular pixels,
  pitch = 250 µm
  N+ electrode = 220 µm,
  C ≈ 300 fF



The 1.6 x 0.4 mm^2 MADPix prototype wire-bonded on the testboard



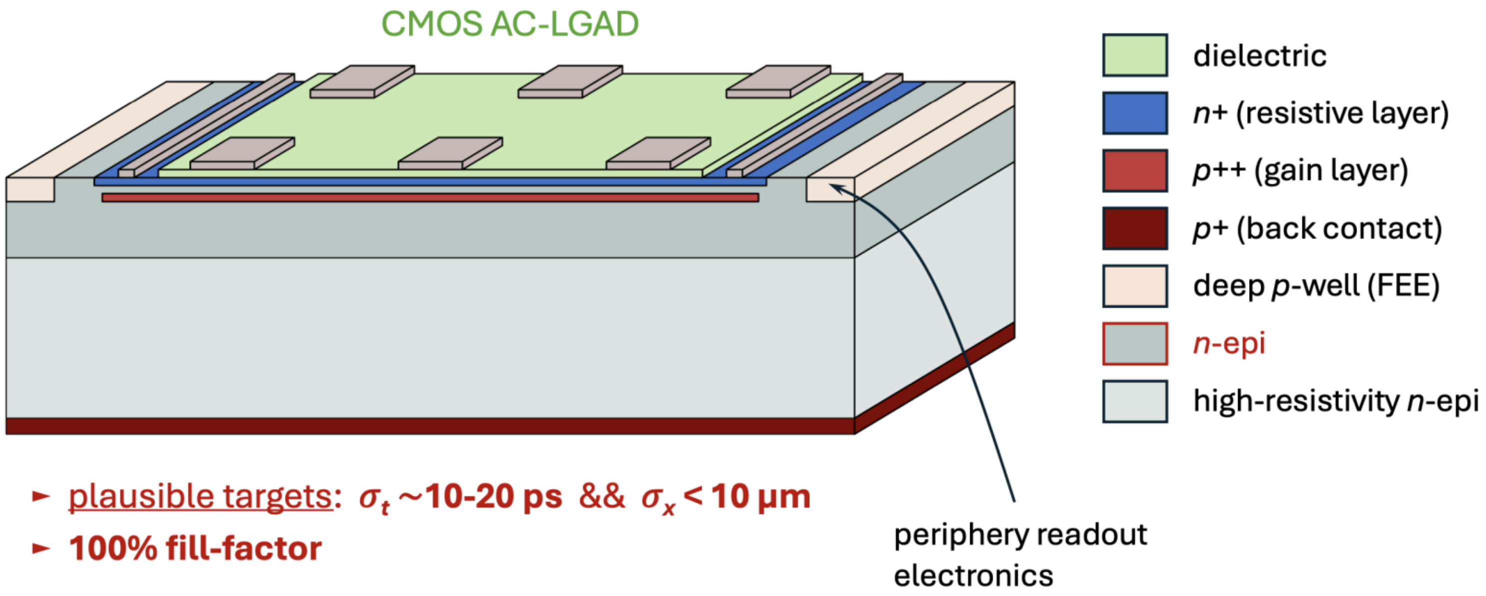
More info on the first characterization: U. Follo *et al* 2024 *JINST* **19** P07033

R&D for Si-Wrapper with AC-LGADs

- **LGAD detector with continuous gain layer (RSD)**, charge collection through resistive n-layer and readout by induction on AC coupled pads, for a
- **Fully active detector**, avoiding isolation implants (used to prevent early breakdown) in segmented LGADs
- Timing resolution approximatively independent from pixel pitch
- CMOS integration of the LGAD technology already demonstrated (in LF11is) with the ARCADIA masksets
- **Up next for CMOS AC-LGAD**: demonstrate the compatibility between the RSD readout scheme and the LF11is ARCADIA CMOS process flow
- **First prototypes in next silicon production runs** - paper on the numerical proof-of-concept describing the CMOS integration is in preparation.
- **Such a monolithic detector enables the development of <u>high-granularity, high-fill-factor and fast-timing detectors with low material budget and power consumption</u>!**

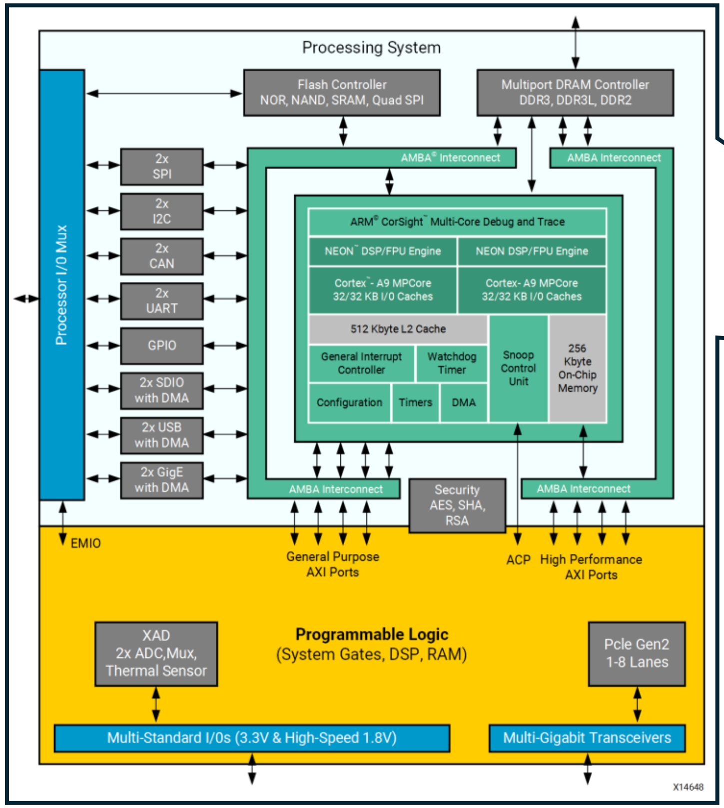
Courtesy of M. Mandurrino

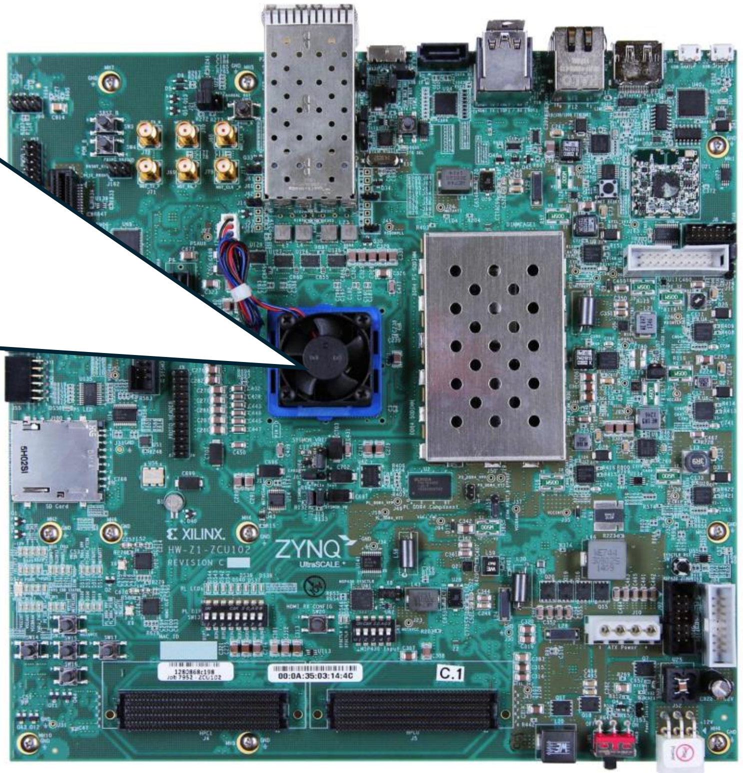
More info on RSD: project, 10.48550/arXiv.2003.04838, 10.1016/j.nima.2021.165319



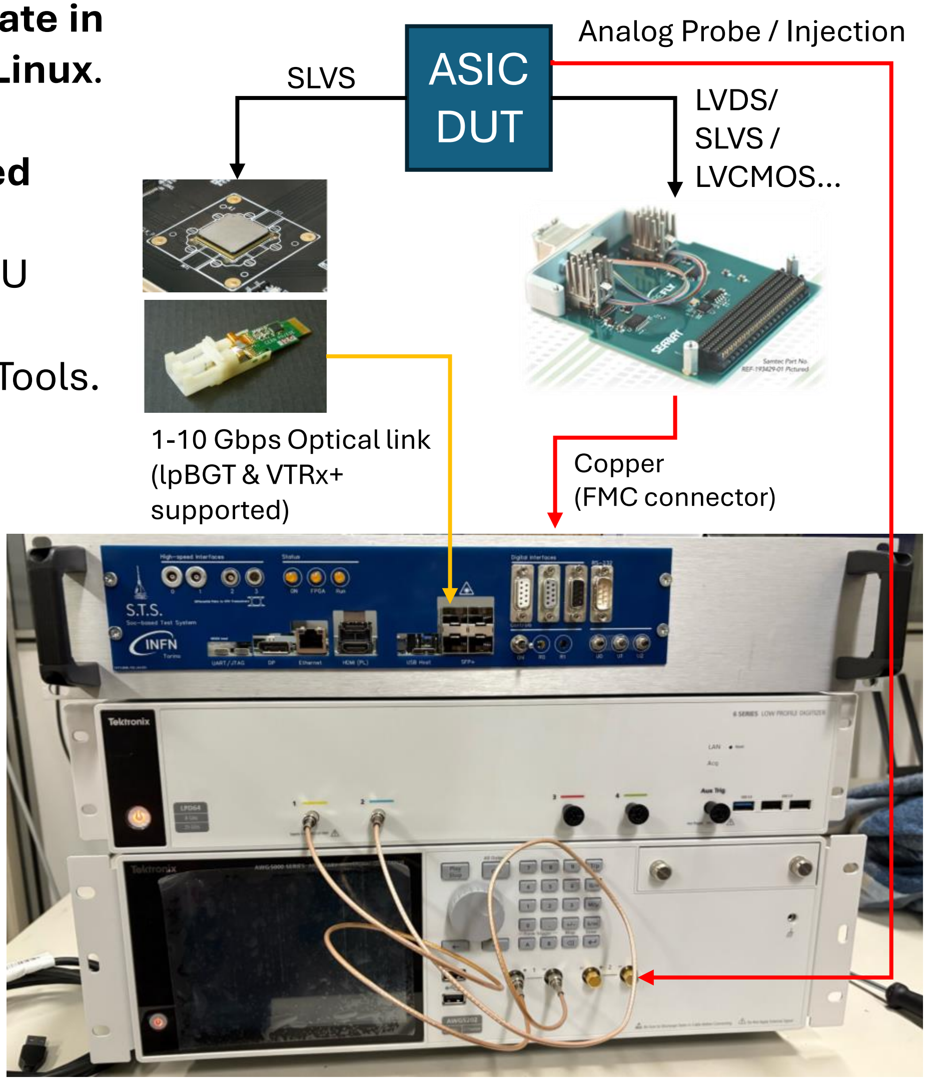
From FPGAs to SoCs and adaptive computing platforms

- Thanks to more advanced deep-submicron nodes, the technology allows to **integrate in a single chip the FPGA** programmable logic **and a multi-core ARM CPU running Linux**.
- This allows to receive **high-bandwidth data from the frontend ASIC** with custom protocols while being able to run very complex algorithms with a **software-oriented approach**.
- The FPGA logic can also be used to offload computing-intensive tasks from the CPU because of its **parallel-computing capabilities**. These acceleration cores can be **programmed using high-level languages** (es. C/C++) using High-Level Synthesis Tools.





Example: AMD/Xilinx MPSoC Architecture, ZCU102



Example: MPSoC-based ASIC test system in Torino, software-oriented, with mixed-signal capabilities

Conclusions

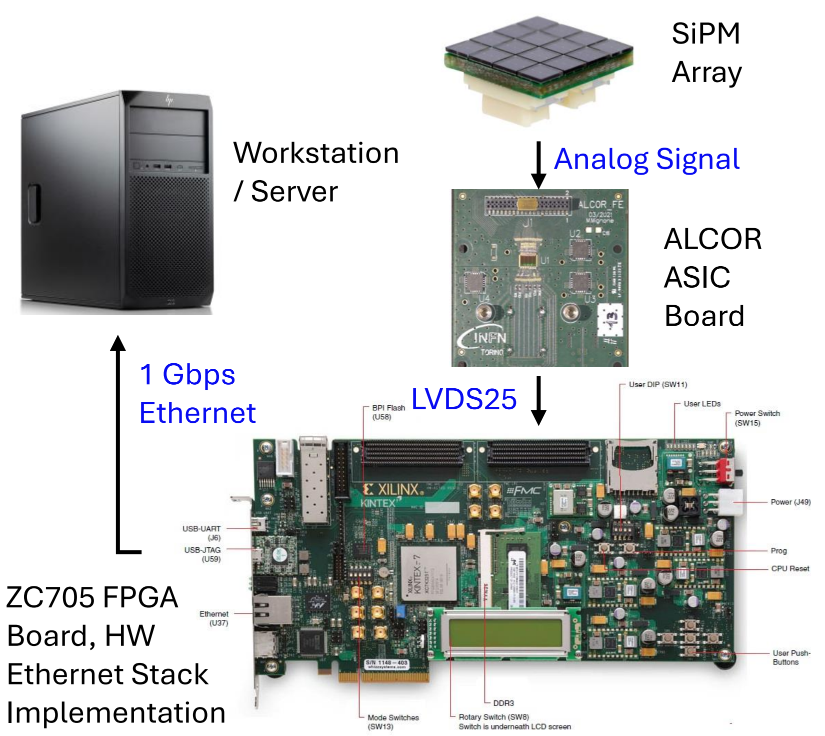
- **Legacy CMOS technologies will remain keystone** and cost-effective solution for calorimetry and readout of gas detectors
- **Growing interest on the modelling of and use of CMOS technologies at cryogenic** temperatures will create new opportunities for the development of on-detector cold electronics for noble liquid based detectors
- **CMOS monolithic sensors**, which are getting bigger and thinner, become leading candidates for **Vertex detectors**, middle trackers and outer trackers with outstanding timing capabilities
- We will need in the following years to **revise the definition of "monolithic**", as industry advances on innovative **3D stacking processes** and wafer-bonding techniques
- How far we'll get bringing AI from the back-end data acquisition electronics to front-end chips?
- Complex chips developed by INFN (including CMOS Sensors), but
- Verification and appropriate size of design teams keys for system-grade ASIC Design

BACK UP

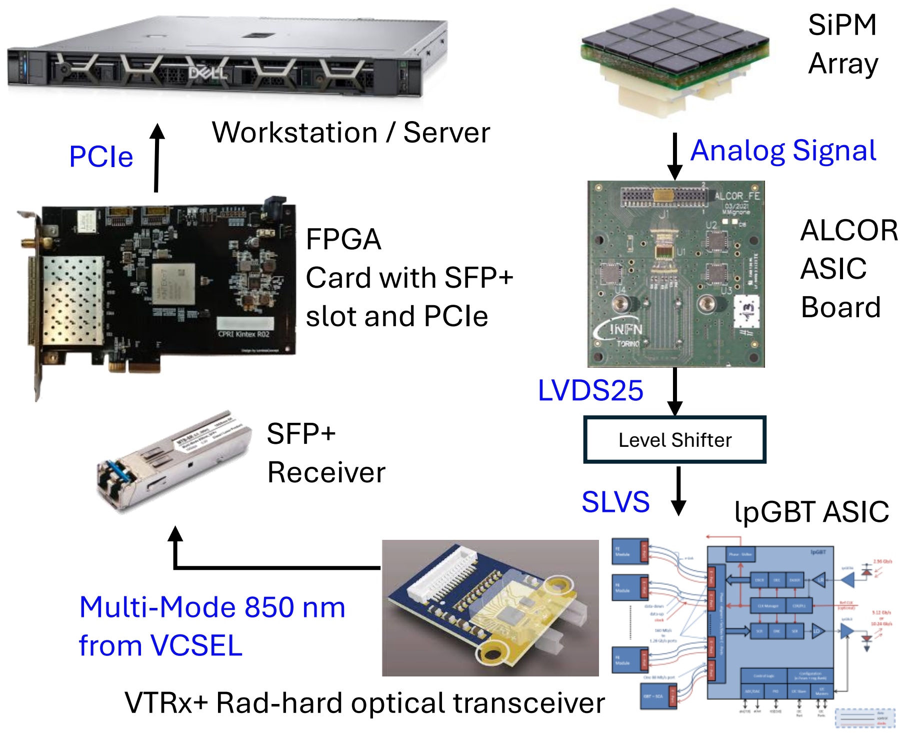
Data Acquisition for HEP: Field Programmable Gate Arrays and beyond

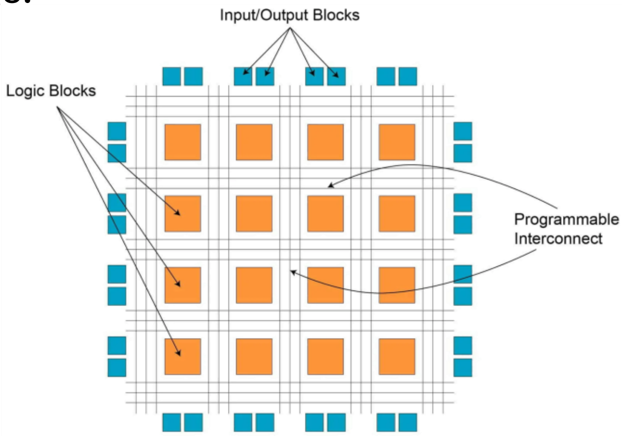
- After the front-end ASIC, **the signal from the detector is transferred on high-speed digital lines** using a variety of protocols. These **data needs to be processed in the digital domain, encoded to standard protocols** (Ethernet, PCIe...) that can be **received by an acquisition computer** in order to be stored on disk.
- These digital operations are carried out by the **data acquisition system (DAQ)** that is usually **implemented on FPGAs** because of the **very high cost of implementing high speed protocols such as Ethernet on ASICs** and because **they can be programmed many times**, thus adding flexibility
- **The FPGAs consist of logical blocks** such as Lookup Tables, Flip-Flops, Digital Signal Processor and memories **that can be programmed for implementing digital circuits,** described using an Hardware Description Language.

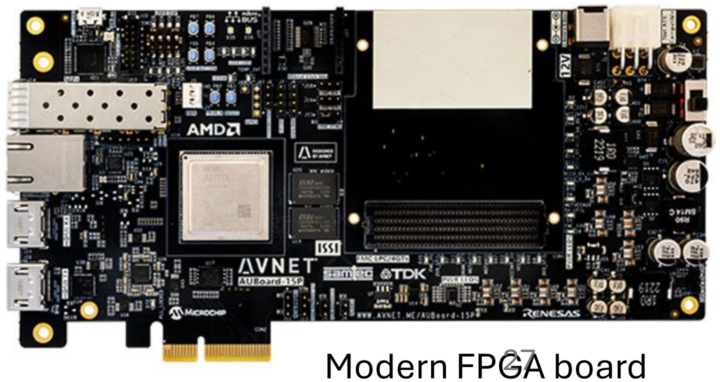
Example 1: DAQ for the ALCOR ASIC



Example 2: lpGBT & VTRx+ based DAQ

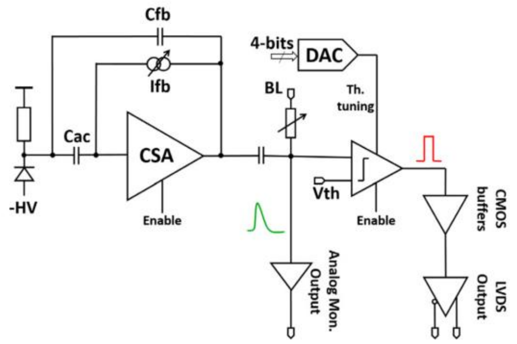






Modern FPGA board

State of the Art Monolithic CMOS Sensors for Timing Applications

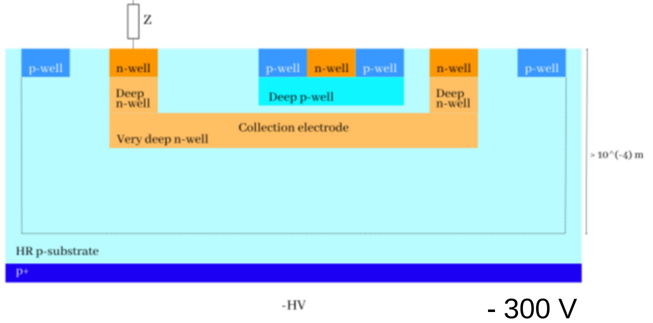


CACTμS and MiniCACTμS
(CIS LFoundry 150 nm)

σ_{t-MIP} = 303 ps
σ_{t-MIP} = 88 ps; 0.3 W/cm^2

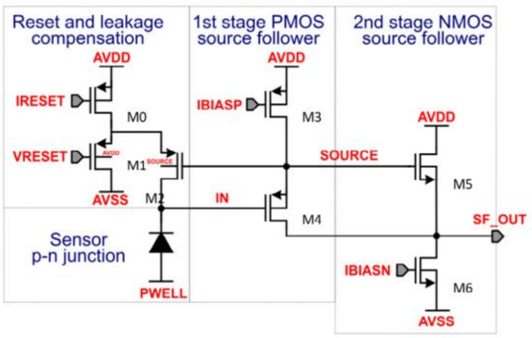
Rectangular pixels, pitch = **500-1000 μm**
Deep-n-well electrode, C ≈ 1.5 pF
R Epi-layer > 2kΩ, d = 200 μm

MiniCACTμS



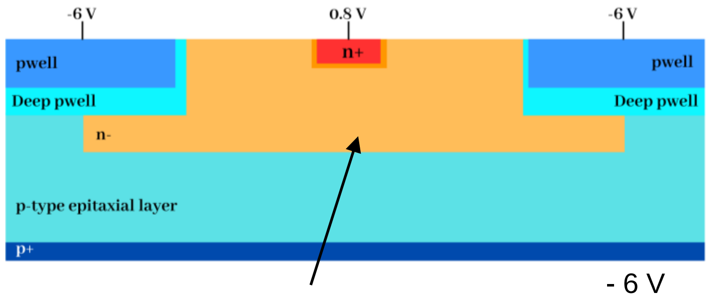
Deep-n-well collects the electrons
FE elctronics hosted above with deep-p-wells with the drawback of a larger pixel capacitance

Y. Degerli *et al* 2020 *JINST* **15** P06011



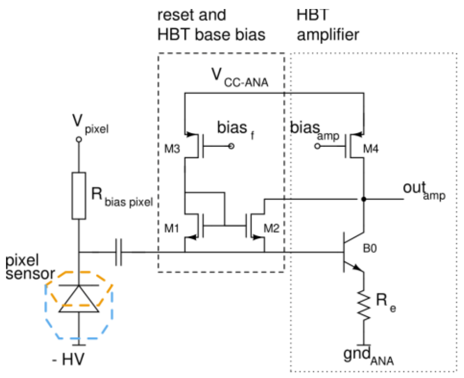
ATTRACT FASTPIX
(CIS Towerjazz 180 nm)

σ_{t-MIP} = 100 ps, ≈ 20-200 μW/ch
(5-50 W/cm^2)
Hexagonal pixels, pitch = **8.7-20 μm**
N+ electrode = 2 x 2 μm^2, C ≈ fF
R Epi-layer > 1kΩ, d = 25 μm



A gap in the low dose n-type implant improves lateral field near the pixel boundary and accelerates the signal charge to the collection electrode

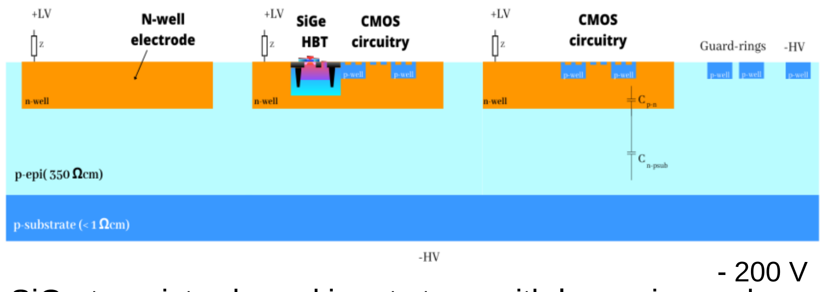
T. Kugathasan et al 2020, NIM 164461



MONOLITH
SiGe BiCMOS,IHP microelectronics 130 nm

σ_{t-MIP} = 77.9 ps, 0.36 W/ cm^2
σ_{t-MIP} = 20.7 ps, 2.7 W/ cm^2

Hexagonal pixels, pitch = 65-130 μm
N electrode = 2 x 2 μm^2, C ≈ 70 -220fF
R Epi-layer > 1kΩ, d ≈ 50 μm



SiGe transistor-based input stage with low noise and larger BW

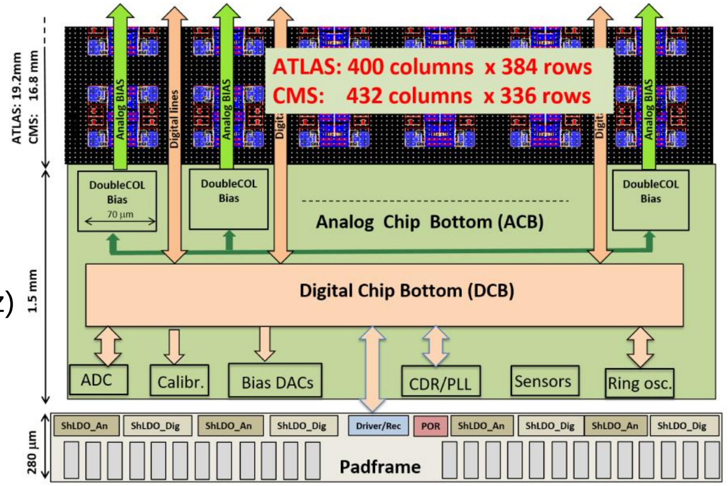
S. Zambito *et al* 2023 *JINST* **18** P03047

ASICs for HEP Hybrid Detectors

Stefano Durando

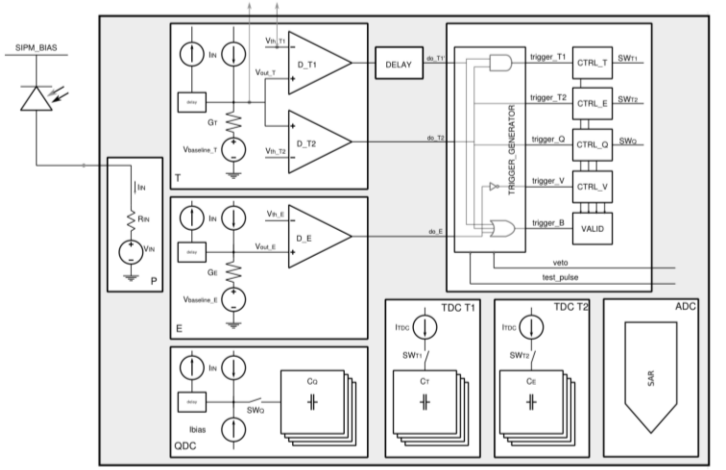
RD53

- Comon design framework for ATLAS and CMS HL-LHC pixel detectors (25 / 50 µm pitch 24 institutes, ~ 100 people, 10 years colaboration
- Extreme hit rates condition (3 GHz/cm^2), high trigger rate (1MHz) 1 Grad over 10 y
- **65 nm** CMOS technology
- Readout up to **5.12 Gbits/s**.
- Strucutre: Pixel Matrix + chip bottom (reticle size)



Source: «The RD53C-ATLAS Pixel Readout Chip Manua», CERN-RD53-PUB-xxxx Version 1.92, September 18, 2024, url:

TOFHIR2

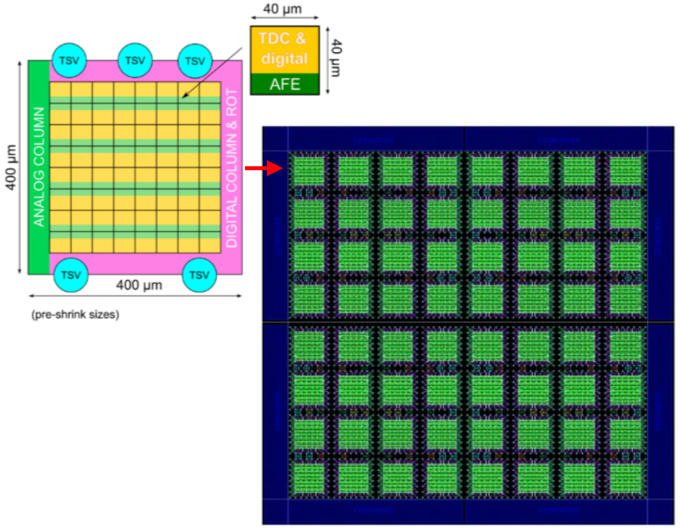


Source: E. Albuquerque *et al* 2024 *JINST* **19** P05048, url: https://iopscience.iop.org/article/10.1088/1748-0221/19/05/P05048

- ASIC for the CMS MIP Timing Detetcor (MTD) in the HL-LHC
- Precision timing of charged particles (30 - 40 ps MIP)
- **130 nm** CMOS technology
- 20 ps bin TDC on-pixel
- 40 MHz 10-bit SAR ADC on-pixel
- 320 Mb/s links compatible with lpGBT

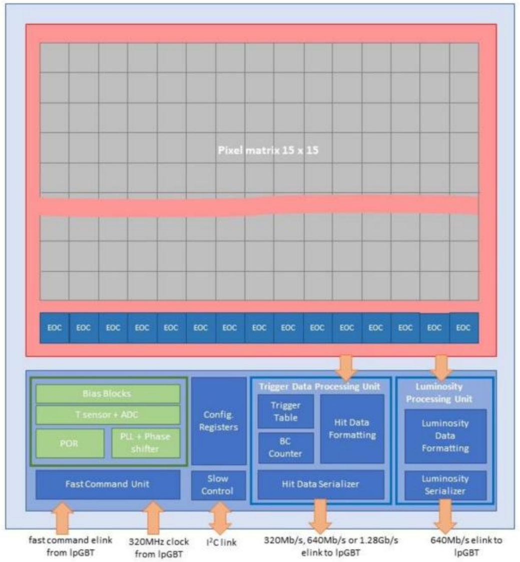
IGNITE

- INFN project targeting the new generation of high-luminosity experiments at the LHC.
- 4D tracking, high space-time resolution (45-55 µm pitch,<50 ps) 1.5 mW/ cm^2
- **28 nm** CMOS technology
- High BW optical data trasmission
- 3D integration with TSV, F2F and F2B technologies
- TDC on-pixel, 12 ps rms
- PLL for jitter reduction down to <5 ps



Source: Sandro Cadeddu *et al* 2024 *JINST* **19** C01040, url: https://iopscience.iop.org/article/10.1088/1748-0221/19/01/C01040

ALTIROC



Source: «ALTIROC2, a readout ASIC for the High Granularity Timing Detector in ATLAS», url: https://indico.cern.ch/event/799025/contributions/3486217/attachments/1903456/3142875/TWEPP2019_HGTD.pdf

- ASIC for the ATLAS High Granularity Timing Detector
- Precision timing of charged particles (30 ps, MIP) and beam luminosity measurement
- Reading-out 225 LGADs
- **130 nm** CMOS tecnology
- 20 ps bin TDC on-pixel
- 320-640 Mb/s or 1.28 Gb/s e-links to lpGBT boards

CMOS Radiation Sensors for ALICE3 ToF Layers

Component	Observables	Barrel ($\lvert\eta\rvert < 1.75$)	Forward ($1.75 < \lvert\eta\rvert < 4$)	Detectors
Vertexing	(Multi-)charm baryons, dielectrons	Best possible DCA resolution, $\sigma_{DCA} \approx 10\,\mu m$ at $p_T = 200\,MeV/c$, $\eta = 0$	Best possible DCA resolution, $\sigma_{DCA} \approx 30\,\mu m$ at $p_T = 200\,MeV/c$, $\eta = 3$	retractable Si-pixel tracker: $\sigma_{pos} \approx 2.5\,\mu m$, $R_{in} \approx 5\,mm$, $X/X_0 \approx 0.1\,\%$ for first layer
Tracking	(Multi-)charm baryons, dielectrons, photons …	$\sigma_{p_T}/p_T \approx 1 - -2\,\%$		Silicon pixel tracker: $\sigma_{pos} \approx 10\,\mu m$, $R_{out} \approx 80\,cm$, $L \approx \pm 4\,m$, $X/X_0 \approx 1\,\%$ per layer
Hadron ID	(Multi-)charm baryons	$\pi/K/p$ separation up to a few GeV/c		Time of flight: $\sigma_{tof} \approx 20\,ps$ RICH: $n \approx 1.006 - 1.03$, $\sigma_\theta \approx 1.5\,mrad$
Electron ID	Dielectrons, quarkonia, $\chi_{c1}(3872)$	pion rejection by 1000x up to 2–3 GeV/c		Time of flight: $\sigma_{tof} \approx 20\,ps$ RICH: $n \approx 1.006 - 1.03$, $\sigma_\theta \approx 1.5\,mrad$
Muon ID	Quarkonia, $\chi_{c1}(3872)$	reconstruction of J/ψ at rest, i.e. muons from $p_T \sim 1.5\,GeV/c$ at $\eta = 0$		steel absorber: $L \approx 70\,cm$ muon detectors
ECal	Photons, jets	large acceptance		Pb-Sci sampling calorimeter
ECal	χ_c	high-resolution segment		$PbWO_4$ calorimeter
Soft photon detection	Ultra-soft photons		measurement of photons in p_T range 1–50 MeV/c	Forward conversion tracker based on silicon pixel tracker

	Inner TOF	Outer TOF	Forward TOF
Radius (m)	0.19	0.85	0.15–1.5
z range (m)	–0.62–0.62	–2.79–2.79	4.05
Surface (m^2)	1.5	30	14
Granularity (mm^2)	1×1	5×5	1×1 to 5×5
Hit rate (kHz/cm^2)	74	4	122
NIEL (1 MeV n_{eq}/cm^2) / month	1.3×10^{11}	6.2×10^{9}	2.1×10^{11}
TID (rad) / month	4×10^{3}	2×10^{2}	6.6×10^{3}
Material budget ($\%X_0$)	1–3	1–3	1–3
Power density (mW/cm^2)	50	50	50
Time resolution (ps)	20	20	20

(with MIPs)

ALICE3 detector concept

Industry demonstrates extraordinary capabilities in terms of **volumes**, **technology nodes**, **stitching**, and **integration**

Compared to mainstream electronics, **High-Energy Physics (HEP) applications** require **moderate to small volumes,** which are **not beneficial in term of costs**.

What is a Legacy Technology ?

- **The CHIPS and Science Act of 2022 defines legacy devices as those produced using 28nm technology or larger**
- Application-Dependent Node Selection:
  - Process node choice depends on application requirements.
  - Some applications do not need nodes requiring extreme ultraviolet (EUV) lithography.
- Market Dynamics:
  - Porting designs to newer/smaller nodes may not add incremental market value.
  - Many foundries and IDMs have stable business on older nodes.
  - "More advanced" nodes are not always more appealing in the market.
  - For example, a 65 nm node could be discontinued while the 130 nm node remains in demand, or vice versa, based on specific market needs.

Conclusion: Technology is available; what truly matters are the **application requirements** and the **budget**!

Image credits © ST Microelectronics and Sphere Entertainment Co.

CEREBRAS
Wafer-Sized Chip
Source : https://cerebras.ai/product-chip/