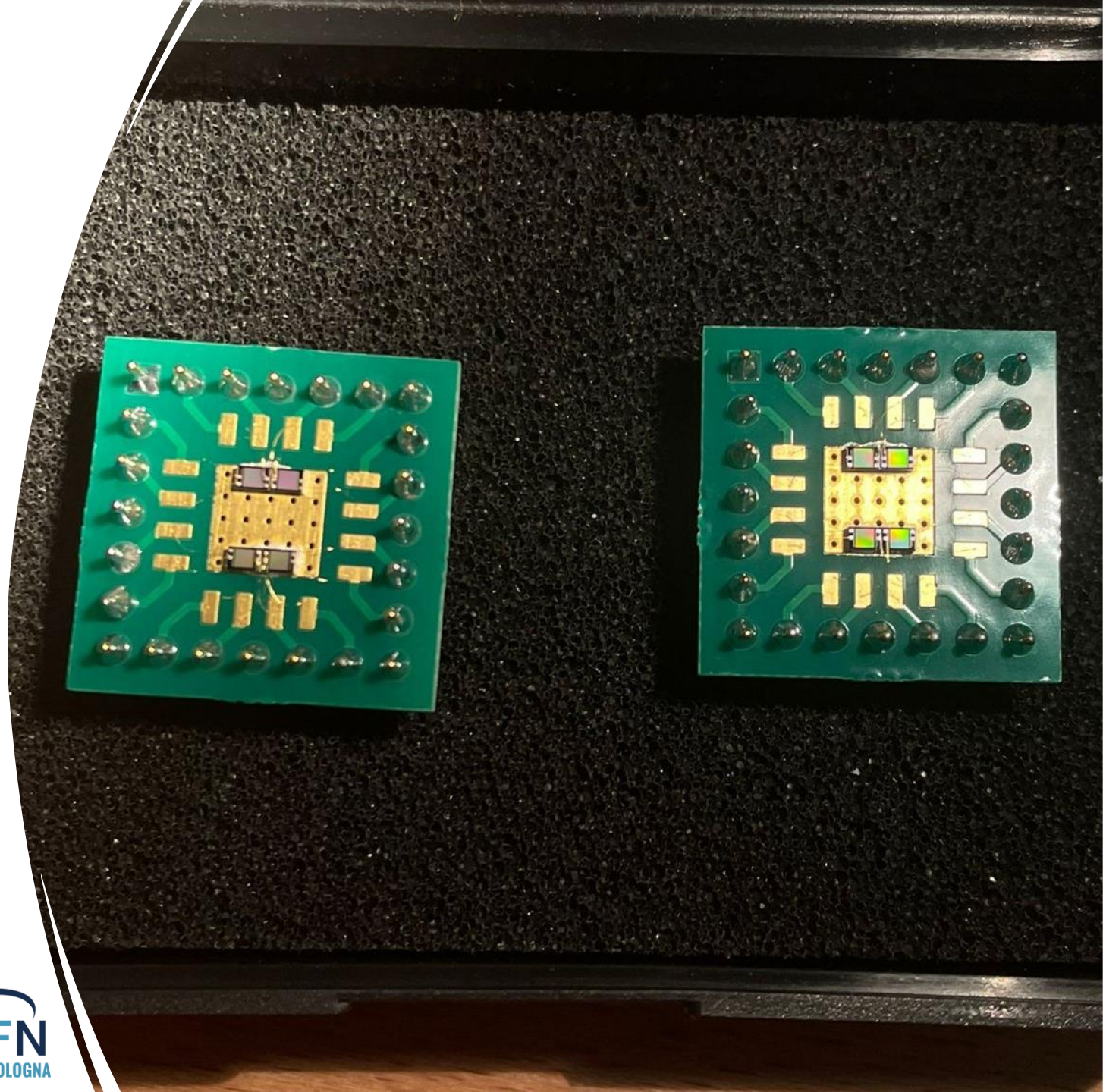
Status of R&D on the Backside Illuminated Silicon PhotoMultipliers

Elisabetta Montagna
AdS 16-12-2024

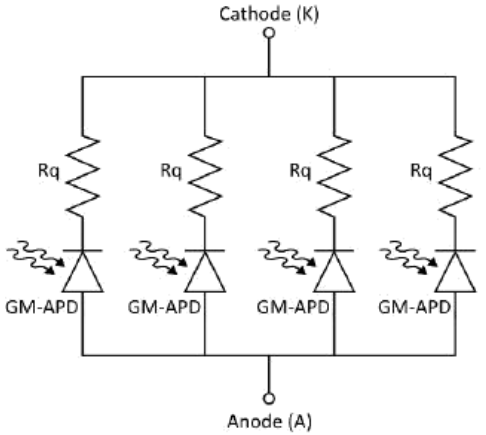


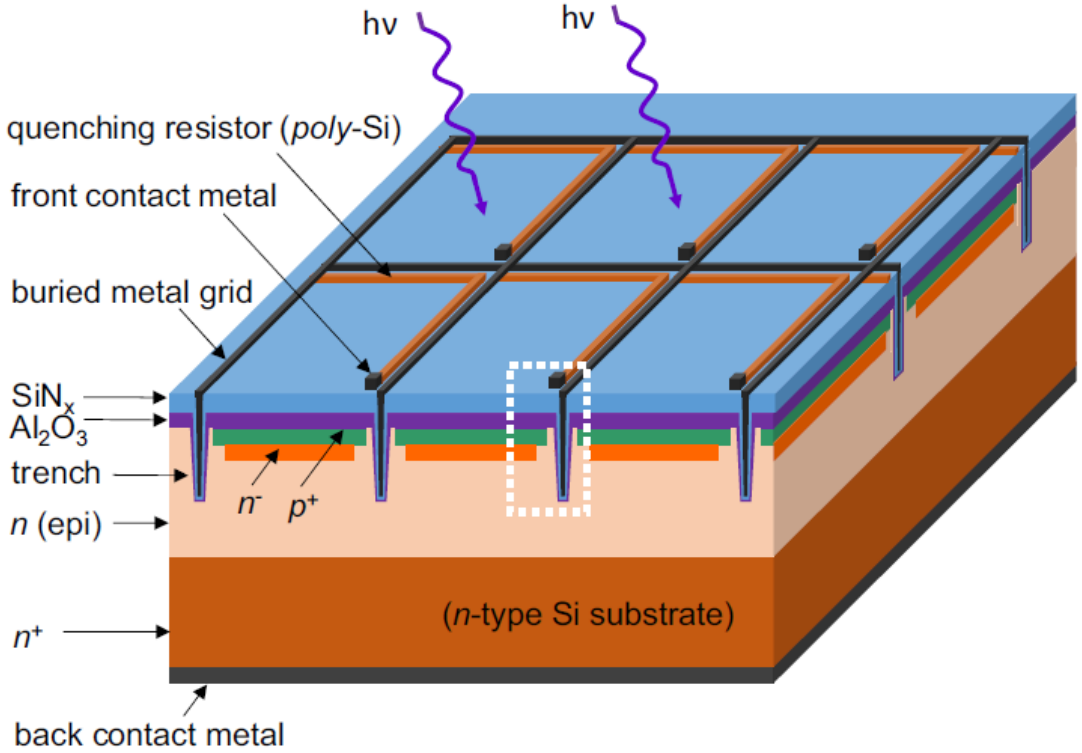
INFN BOLOGNA

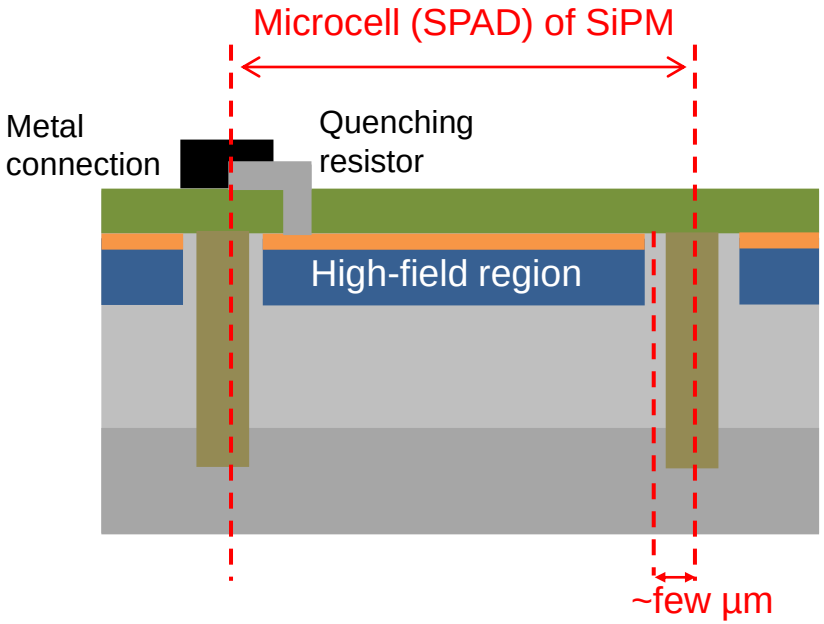
The standard SiPM

Array of Geiger-mode avalache photodiodes (SPAD) connected in parallel on a common Silicon substrate:

→ analog signal «linearly» proportional to number of impinging photons

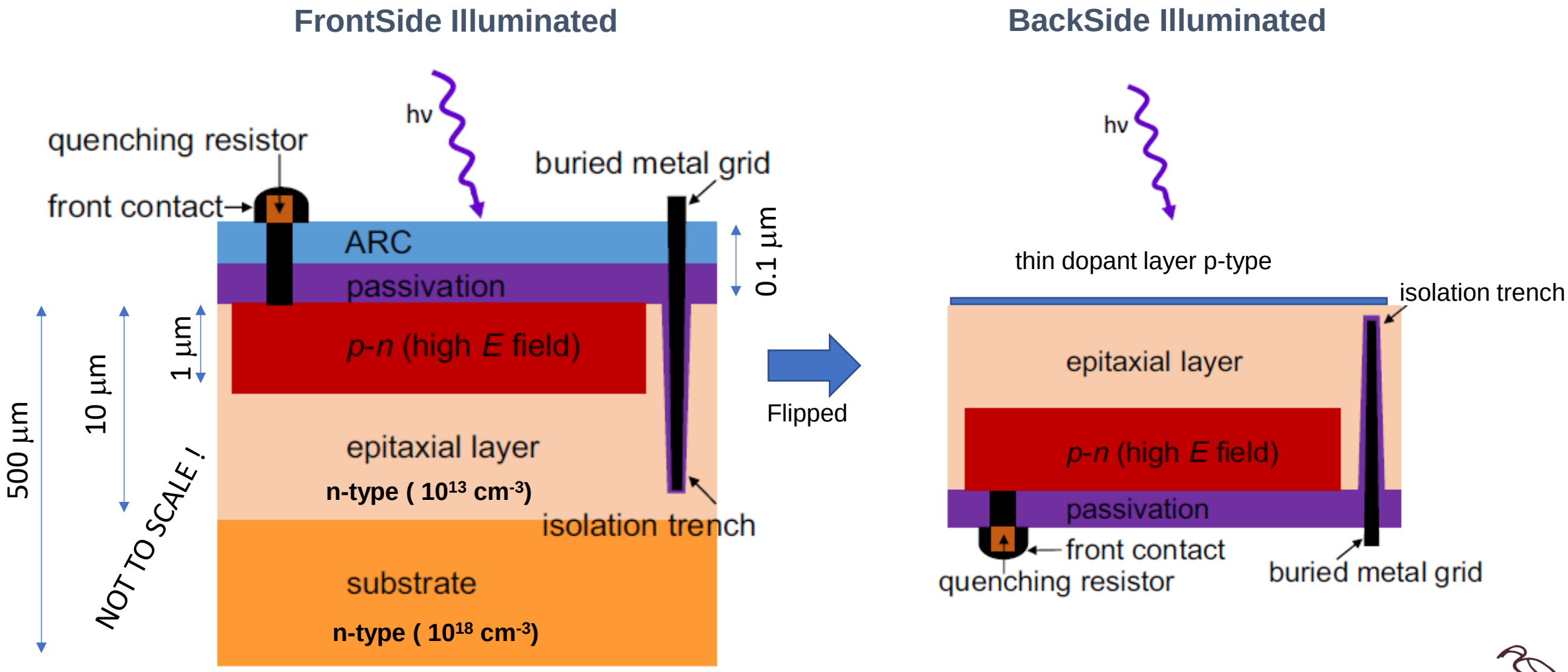






Sci Rep **12**, 13906 (2022)

What is a Backside Illuminated SiPM?



BSI SiPMs

Advantages:

- Entrance window free of metal grid, quenching resistance, Through Silicon Vias
  → **Enanched Fill Factor** (up to 100%)
  Enables more advanced surface treatments to improve optical properties

- No need for Vias allows smaller SPAD size:
  →**High Dynamic range**

- Direct coupling of individual pixels (or small group of pixels) to readout chip by bump bonding
  →Extremely high performance **cameras**

Possible disadvantages:

- More difficult to control CrossTalk and AfterPulse

State of the art

A lot of interest about Backside Illuminated:

- Max Plank Institute: no news since prototype built in 2007
- TCAD simulations, but no prototype
- Innovative Anti Reflective Coating (ARC) for Backside, but no prototype
- A matrix of BSI-SiPM for LiDAR
- Canon's SPAD sensors

PROCEEDINGS OF SCIENCE

31 January 2020

64x48 pixel backside illuminated SPAD detector array for LiDAR applications

Jennifer Ruskowski, Charles Thattil, Jan H. Drewes, Werner Brockherde

www.nature.com/scientificreports

o Electronics and Photonics XVII; 1128805 (2020)

ited States

Development of Back Illuminated SiPM at the MPI Semiconductor Laboratory

H.-G. Moser*, S. Hass, C. Merck, J. Ninkovic, R. Richter, G. Valceanu
Max-Planck-Institut für Physik, Föhringer-Ring 6, D-80805 Munich, Germany
MPI Halbleiterlabor, Otto-Hahn-Ring 6, D-81739 Munich, Germany

scientific reports

Check for updates

OPEN **Advanced antireflection for back-illuminated silicon photomultipliers to detect faint light**

Nuclear and Radiological Engineering, Georgia Institute of Technology, Atlanta, GA, USA. email: yuguo.tao@gatech.edu

IEEE Sensors Council IEEE SENSORS JOURNAL, VOL. 22, NO. 16, 15 AUGUST 2022 16089

Advanced Back-Illuminated Silicon Photomultipliers With Surrounding P+ Trench

Haifan Hu, Ying Wang, *Senior Member, IEEE*, Penghao Liu, Xiubo Qin, Junpeng Fang, Hongming Zhao, Zhe Ma, and Jiatong Wei

IBIS project

Main goal of the **I**nnovative **B**ackside **I**lluminated **S**ingle photon detector (**IBIS**) project is the production of **different devices** tailored **for several applications**

- Activities started in 2021, project proposed to CSN5 (Resp. Naz.: Alessandro Montanari)
- Units involved:
  - INFN-**Bo** (DUNE, EIC, ALICE3) – 2.3 FTE,
  - INFN-**To**,
  - INFN-**MiB**,
  - Fondazione Bruno Kessler (**FBK**)

Initial activities delayed over 1 year wrt original plan due to:

- COVID
- upgrade of FBK clean room
- Queue of projects at FBK

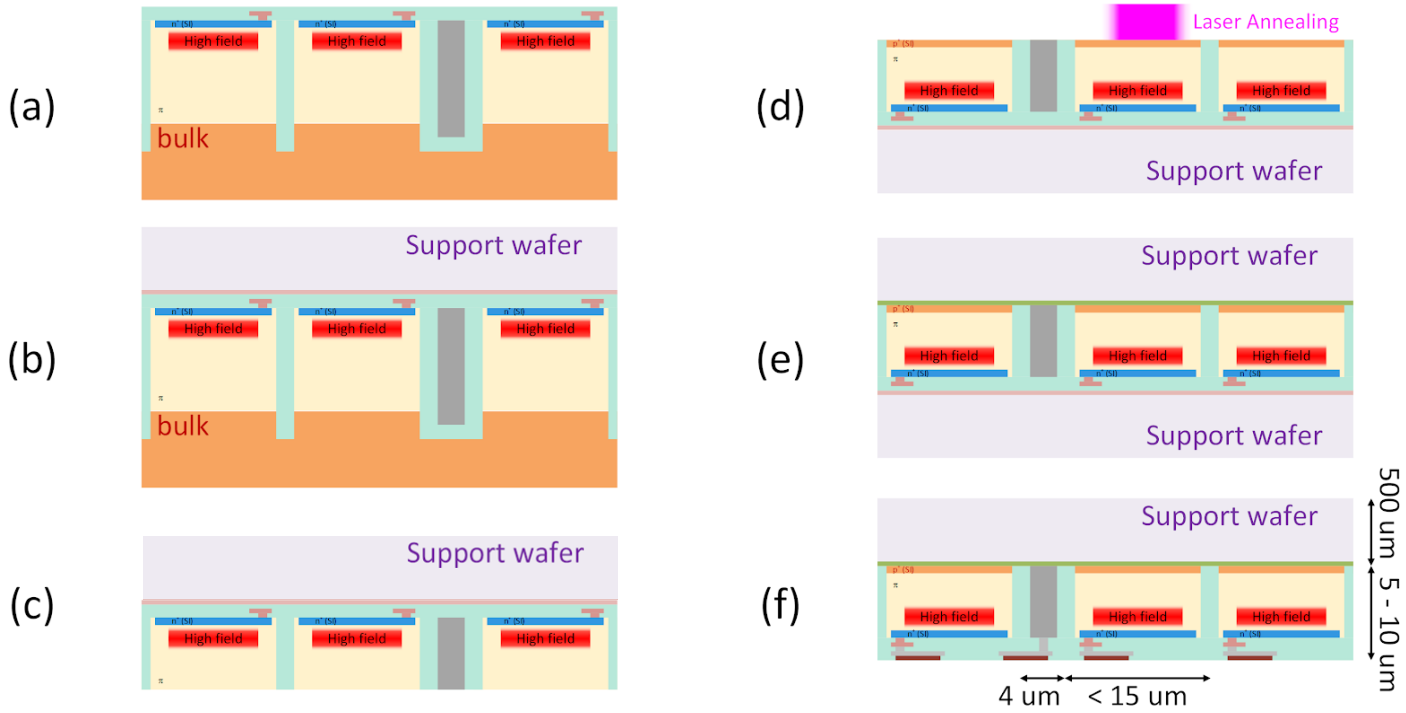
IBIS project

Goals:

- **Characterization** of the first prototypes samples of BSI SiPMs
- Test **Radiation tolerance**
- Test MIPs detection capability and **timing**
- Study Cherenkov application
- Study application to novel **imaging** technique to Liquid Argon detectors
- Design of a vertically integrated readout electronics (Read Out Chip bump bonded)

  →**INFN Torino** already has in hand an **ASIC** for SiPM readout with a matrix of 32 channels **ready for bump bonding**: mini-SiPMs backside illuminated with matched size (440 um) can be coupled with the existing ASIC with bump bonding…first step towards vertical integration

BSI Sensor Development at FBK



a) **Build new cell**
b) Attach Support Wafer on Front side
c) **Remove completely Silicon bulk + Plasma doping on backside**
d) **Laser annealing** on backside thin dopant
e) Attach Support Wafer on Back side
f) Remove Support wafer from Back side, from contacts

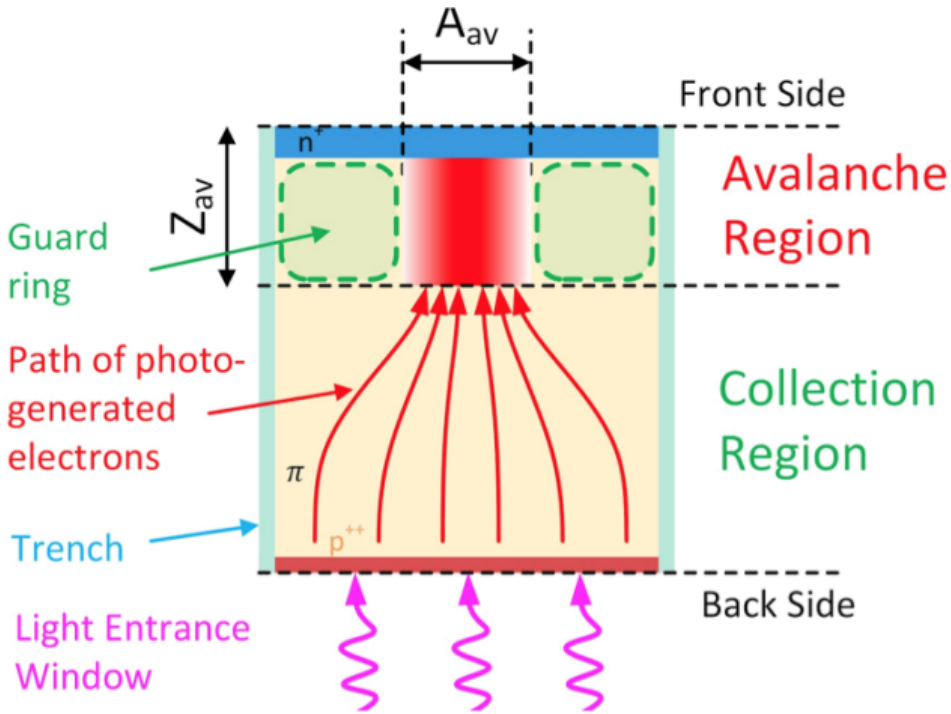
Development status at FBK

FBK, throughout 2021-2025, focused on the development of an innovative cell design, resulting in the production of first prototypes samples for BSI SiPMs

Significant advantage of the BSI innovative cell design by FBK is the **clear separation between charge collection and multiplication regions** → **charge focusing**

→**Better Radiation Tollerance**

area sensitive to radiation damage is smaller than the light sensitive area

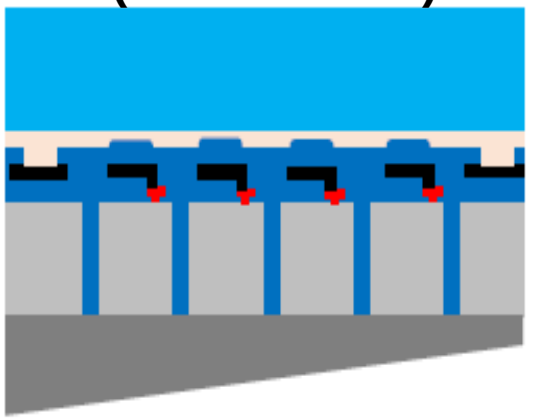


S. Enoch et al 2021 JINST 16 P02019

Development status at FBK

FBK dedicated a first learning cycle on mechanical tests and improvement of the process flow (wafer thinning - bulk removal, grinding)

Wafer thinning (bulk removal)



One important challenge in developing the NUV-BSI process flow is **achieving small total thickness variation (TTV)** after wafer thinning

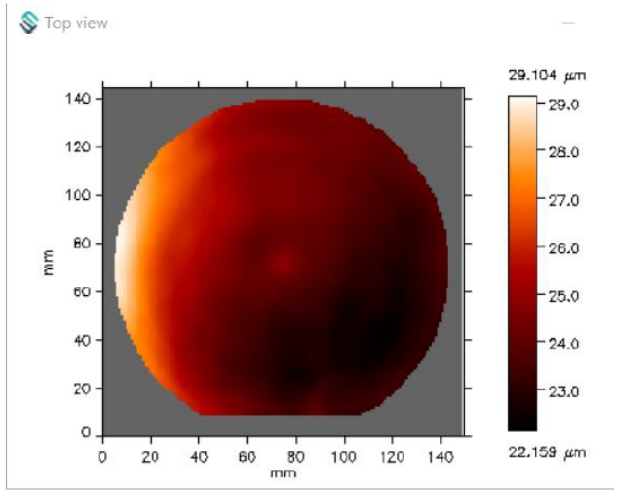
→ in order to ensure **consistent SPAD performance across the wafer**

Development status at FBK

Too high Total Thickness Variation **(TTV)** evaluated after chemical mechanical polishing
→**study of additional TTV reduction process**

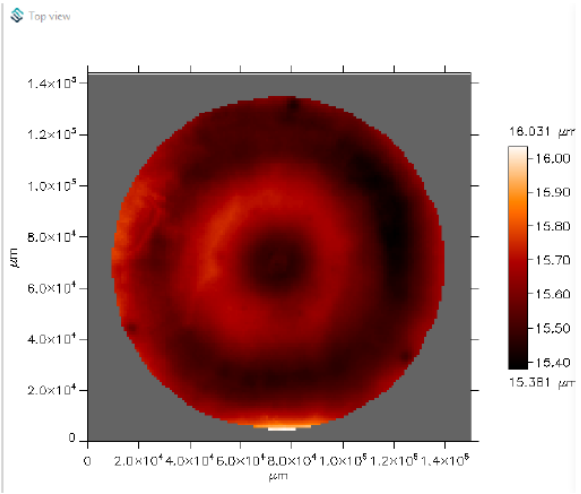
Results obtained after optimization of recipes and procedures :
→ a **TTV of less than 1 um** achieved with additional etching step

Grinding



TTV = 7 um
(worst case)

Grinding + TTV reduction

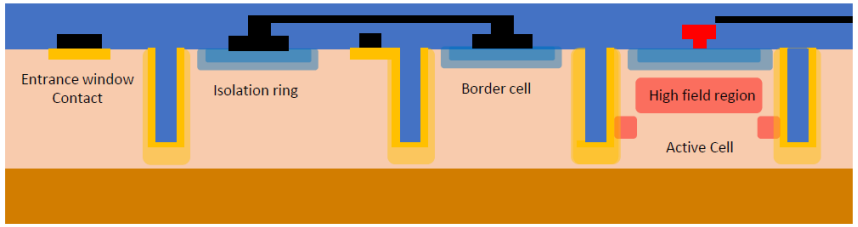


TTV = 0.8 um

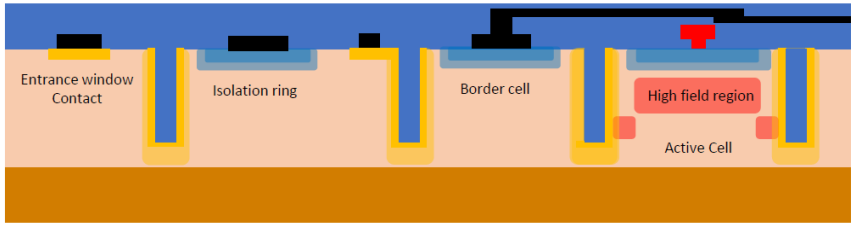
Sample testing

Production of 12 wafers with several split differing in: cell dimensions, bulk contact, biasing etc.

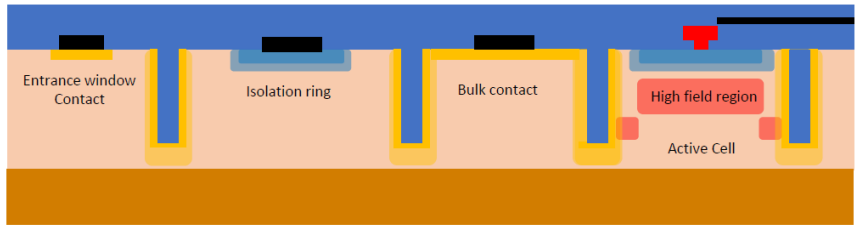
A split - border cell and isolation ring biased together



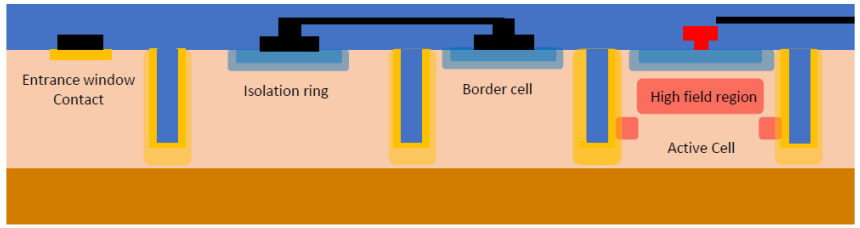
B split - active cell and border cell biased together



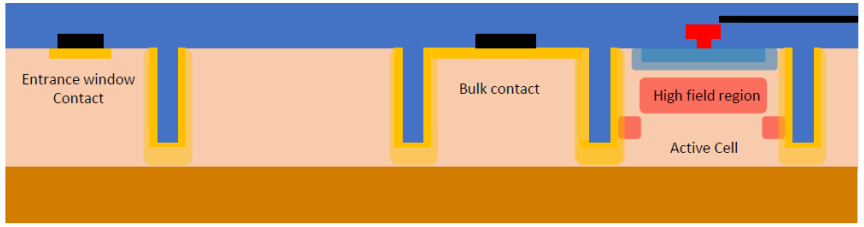
C split - independent bias for active cell and isolation ring



D split - border cell and isolation ring biased together unbiased trench

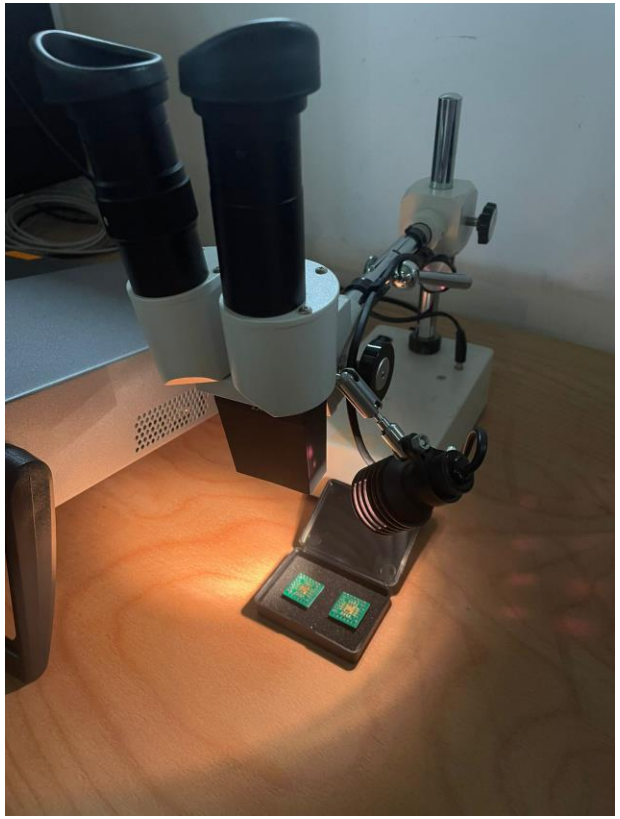


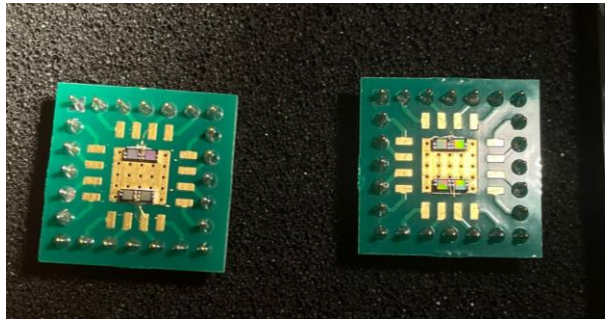
E split - no isolation ring

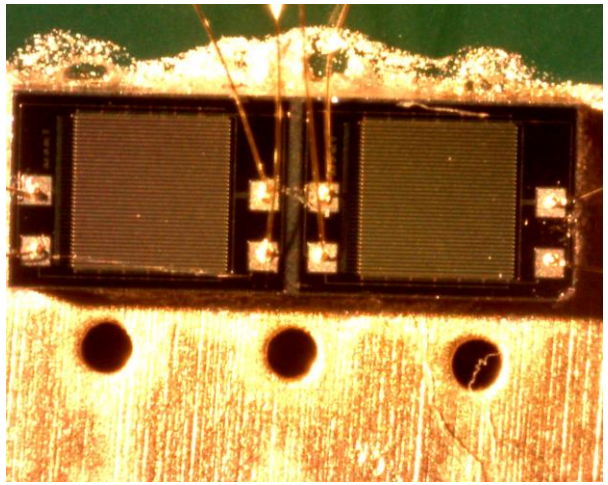


INFN Bologna received samples belonging to the **B** and **E** splits

Sample testing





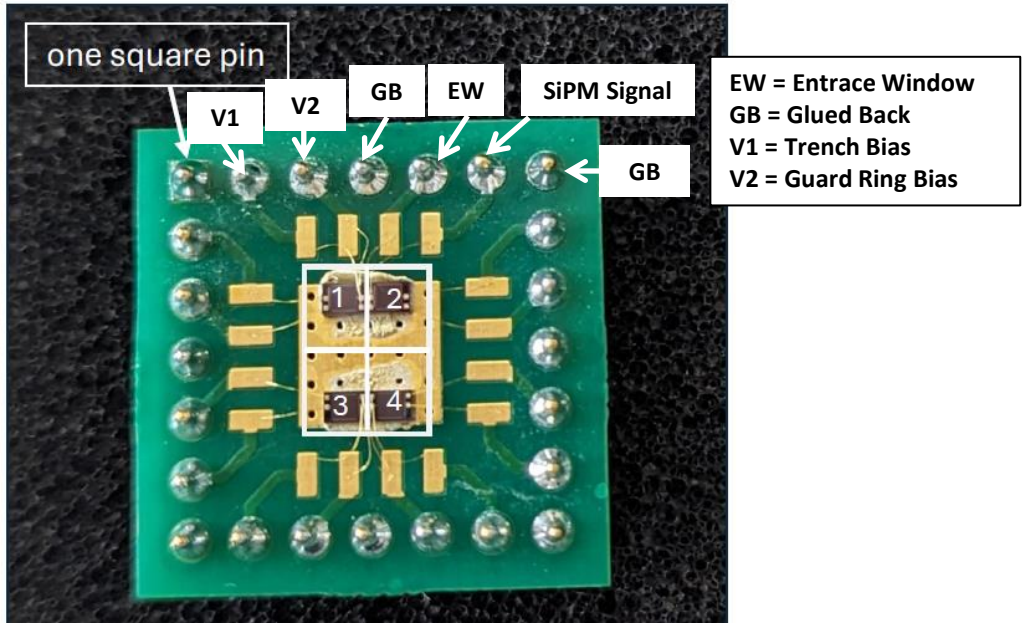


Visual inspection at the microscope

Setup used for the I-V measurements:

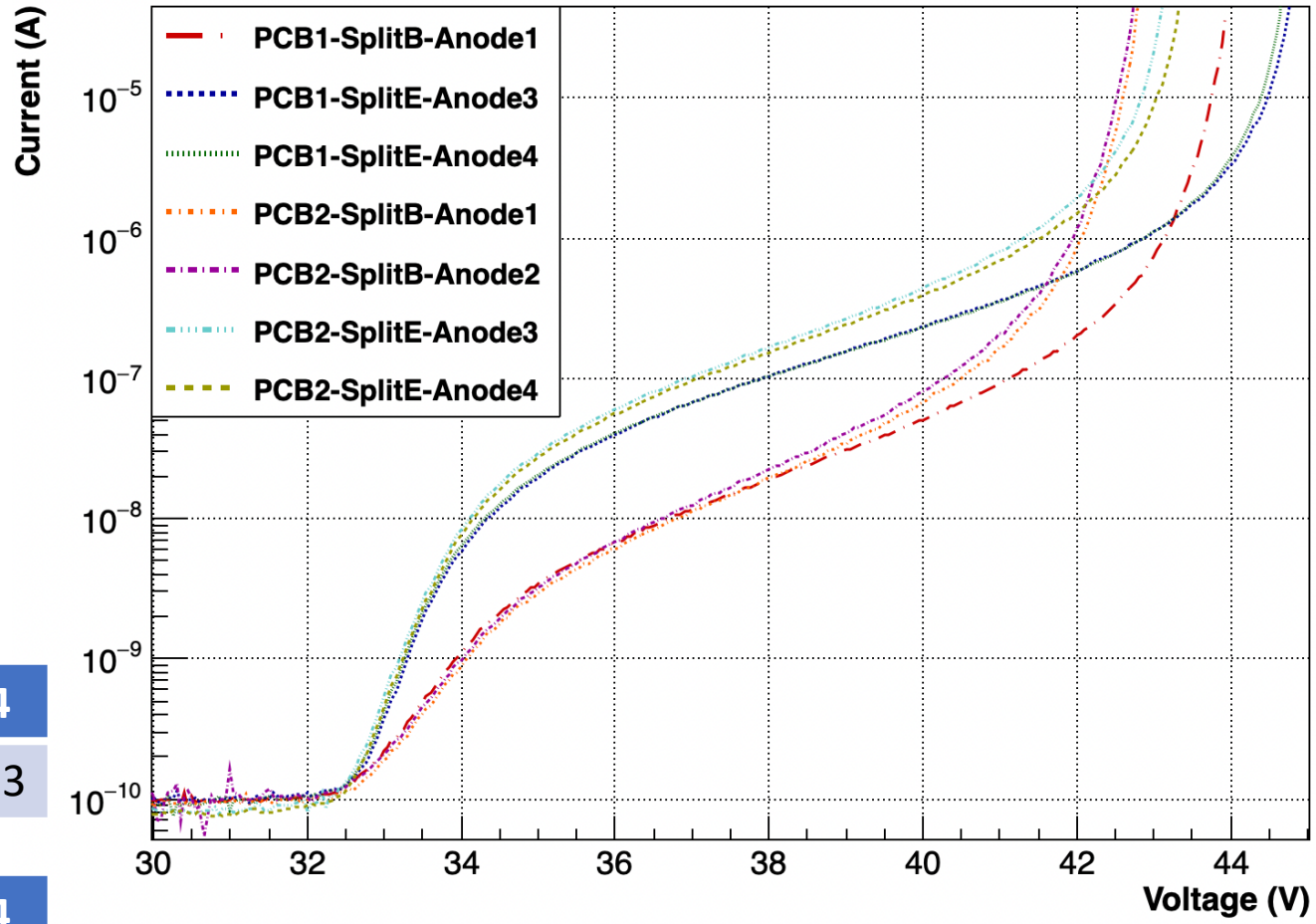
- **Source Measure Unit** to bias the SiPM in reverse polarization
- **Black box** for the light shield

Results of the very preliminary tests



PCB1	anode 1	anode 2	anode 3	anode 4
V_{bd}	32.6 ± 0.4	n.c.	32.5 ± 0.5	32.5 ± 0.3

PCB2	anode 1	anode 2	anode 3	anode 4
V_{bd}	32.6 ± 0.6	32.6 ± 0.4	32.4 ± 0.5	32.5 ± 0.3



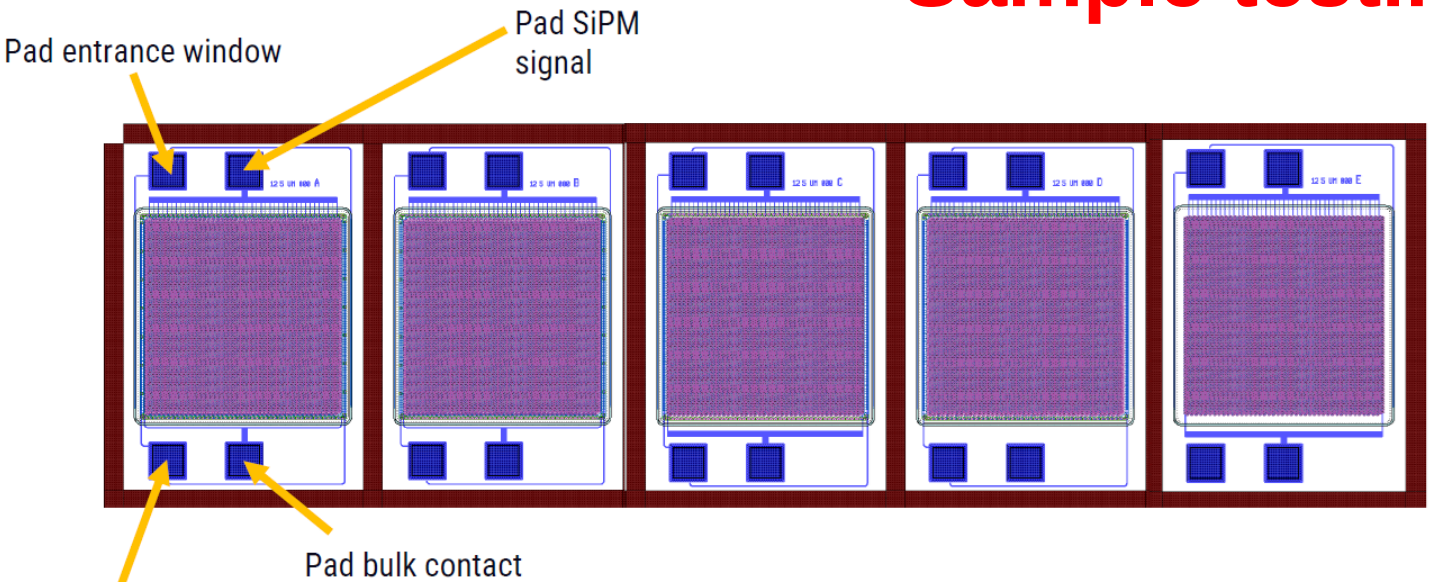
Analysis performed by IBIS PhD student Edoardo Rovati

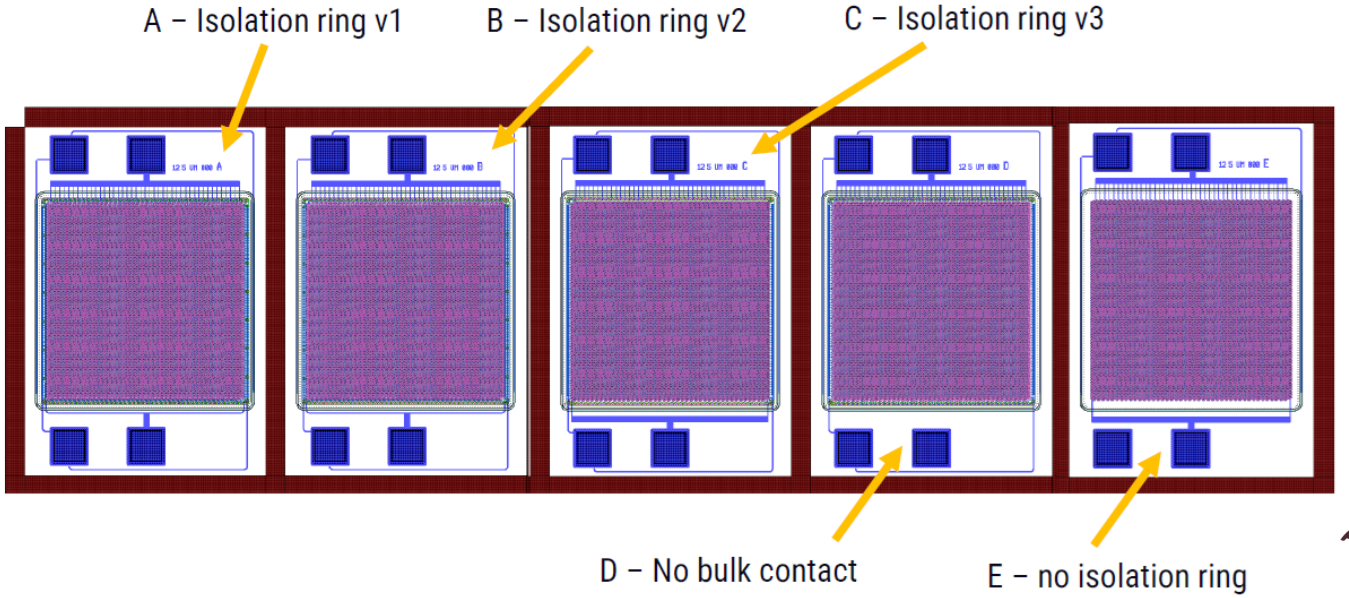
Future plans and perspectives

- First preliminary tests on samples proved **correct functioning of the cell**, break down voltage extracted from the analysis agrees with the expected value
- Tests on the **temperature dependence** of the samples are ongoing
- Tests at **cryogenic temperature** are scheduled for January
- Test for **radiation tolerance**
- In **spring 2025** new BSI SiPM samples should be delivered from FBK

Back up

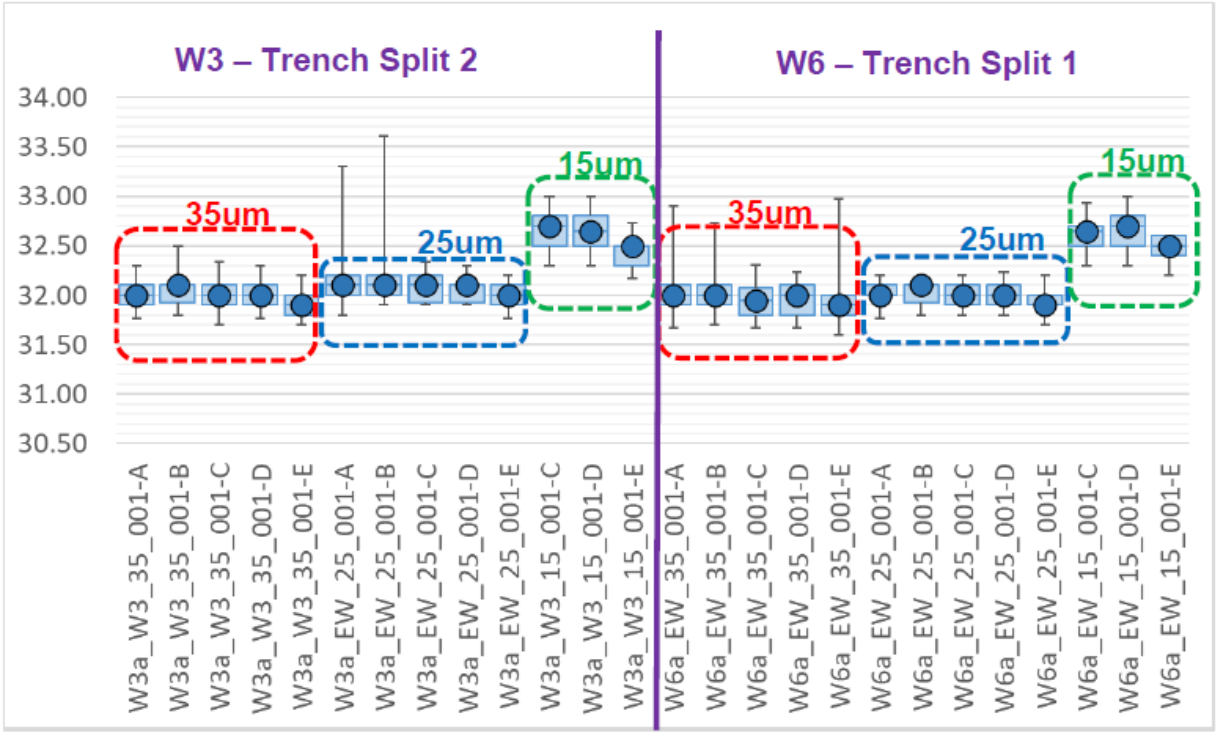
Sample testing



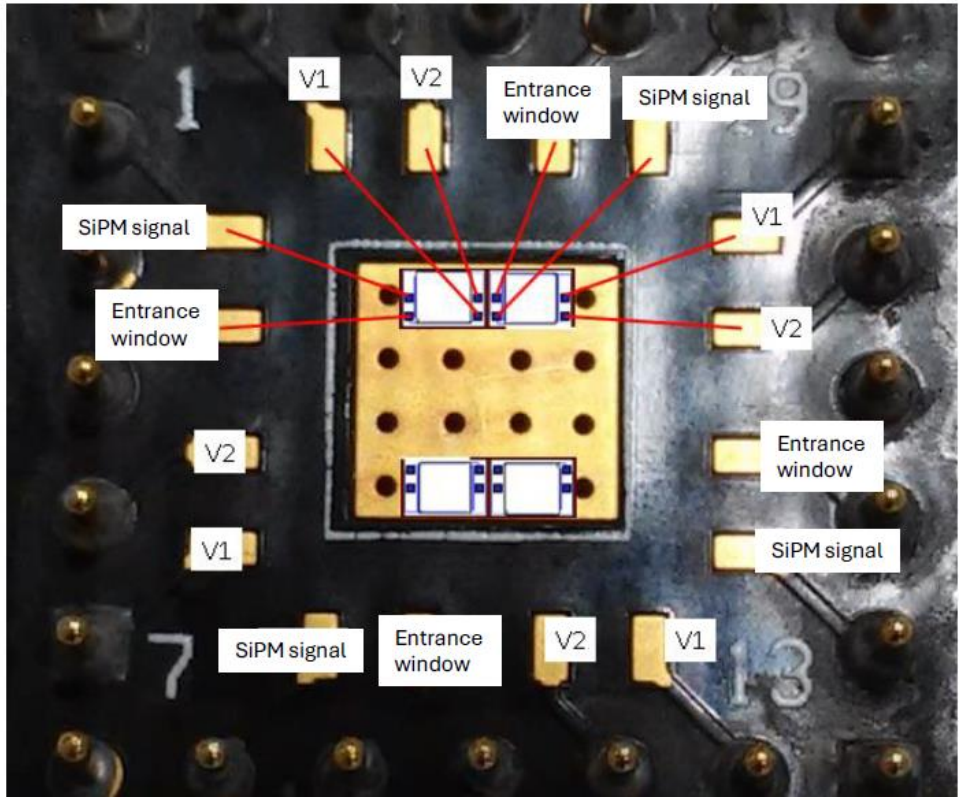


SiPM parameters statistics on IBIS1
Breakdown Voltage

W3 – Trench Split 2 (Trench depth medium-)
W6 – Trench Split 1 (Trench depth medium+)



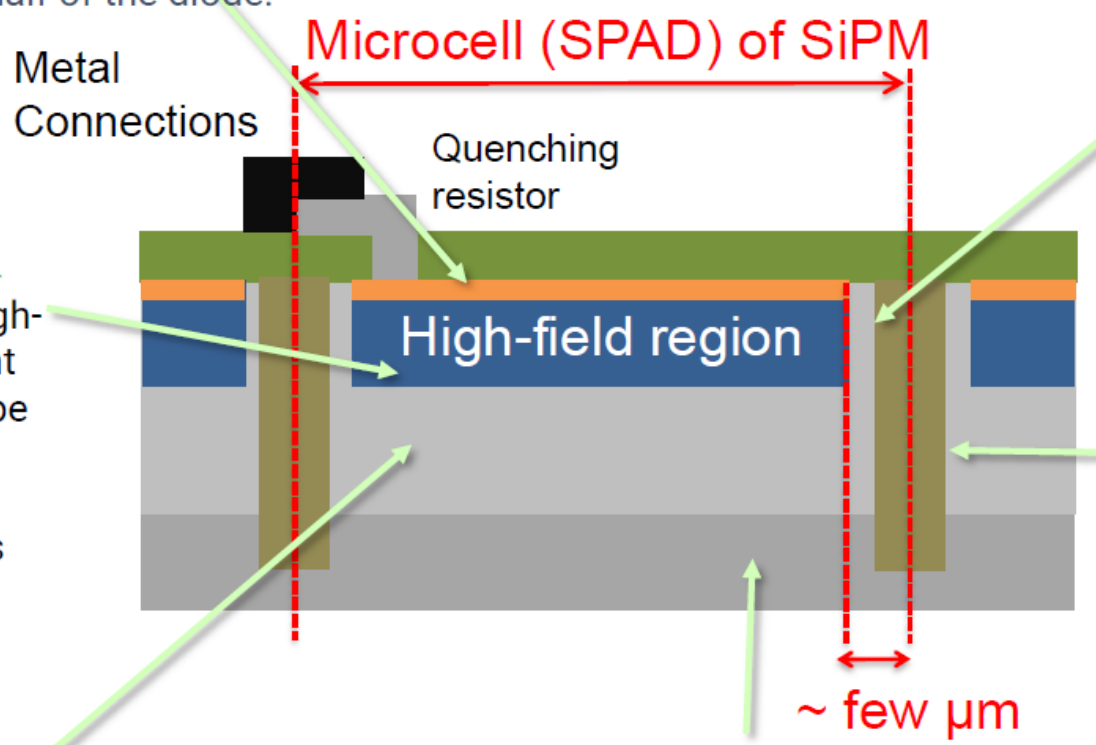
Quite uniform breakdown voltage between same splits and different wafers


1
V1
V2
Entrance window
SiPM signal
9
SiPM signal
V1
Entrance window
V2
V2
Entrance window
V1
SiPM signal
7
SiPM signal
Entrance window
V2
V1
13

SiPM structure

Superficial implant (SI):

Very thin, constitutes the entrance window for the light into the SPAD. High-dose, opposite dopant polarity compared to the epitaxial layer, partially undepleted. Constitutes one half of the diode.



Virtual Guard Ring:

Dead border around the high-field region, necessary to prevent edge breakdown.

High-field region:

is defined with a high-energy deep implant **(DI)** of the same type as the epi layer. Avalanche multiplication takes place here.

Deep trench Isolation:

are used to isolate adjacent microcells electrically. Optical isolation depends on filling material.

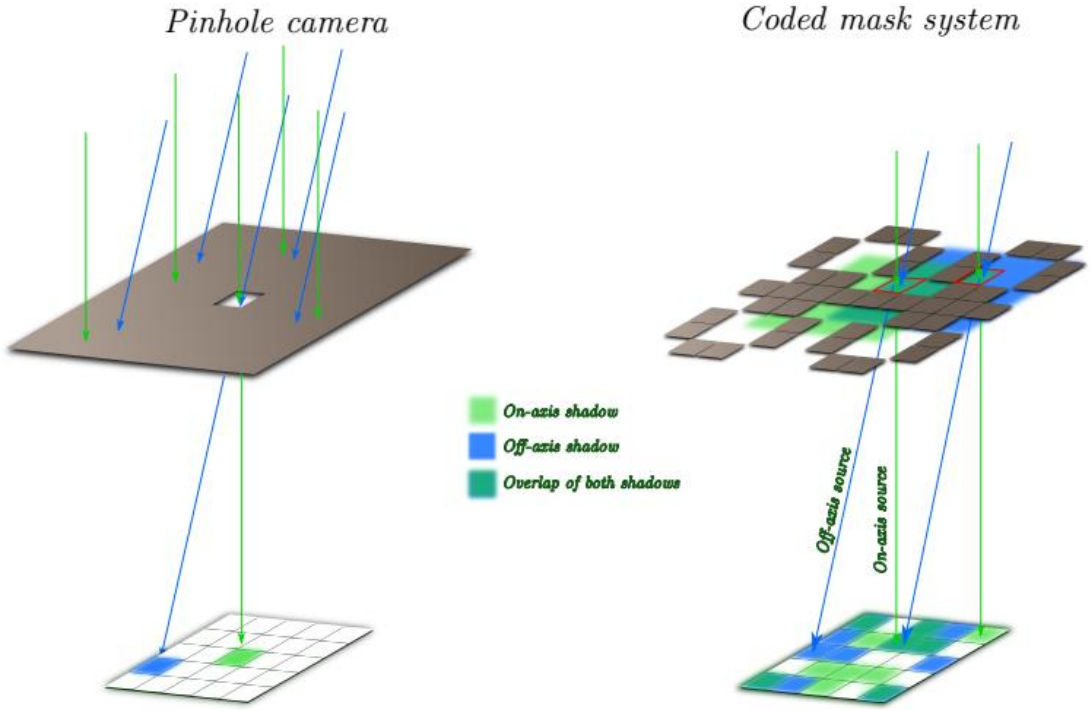
Epitaxial layer:

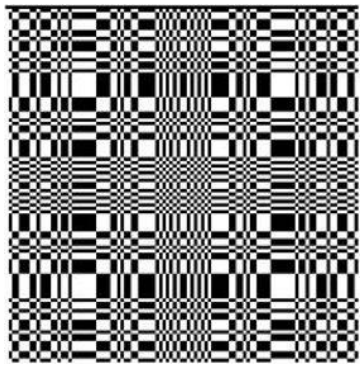
The high-resistivity region in which the SiPM cells are built. Few um thick. Almost fully depleted at breakdown. Close to the interface with the bulk, part of it is undepleted. Constitutes one half of the diode.

Bulk:

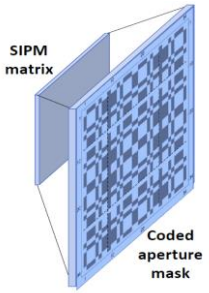
(Very) highly doped region upon which the epitaxial layer is built. Never depleted.

Optics development



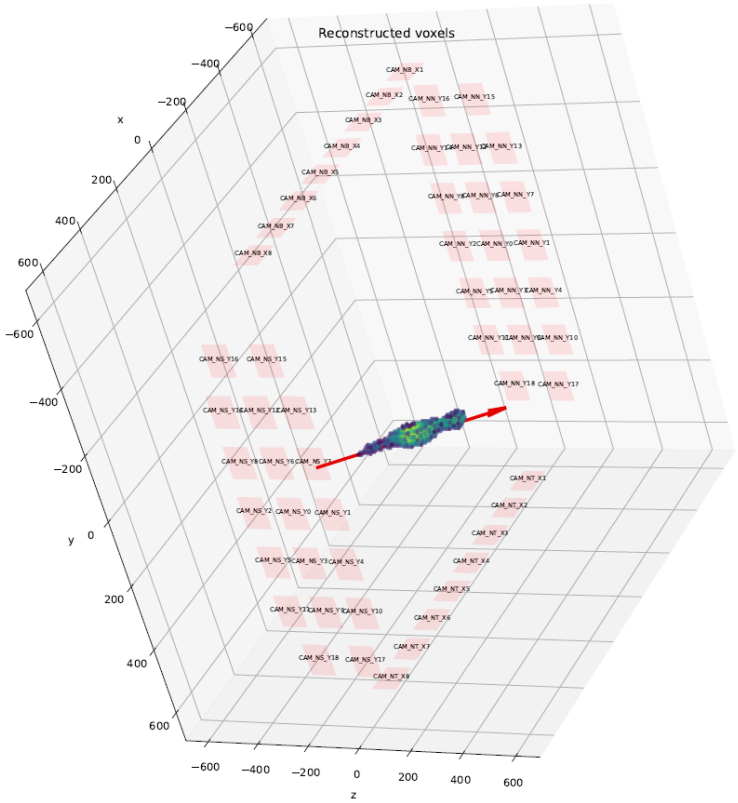


- Coded Aperture mask techniques were developed as the evolution of a single pinhole camera
  - matrix of multiple pinholes to improve light collection and reduce exposure time
- Image formed on sensor is the superimposition of multiple pinhole images.
- Advantages
  - Good light transmission (50%)
  - Good depth of field
  - Small required volume

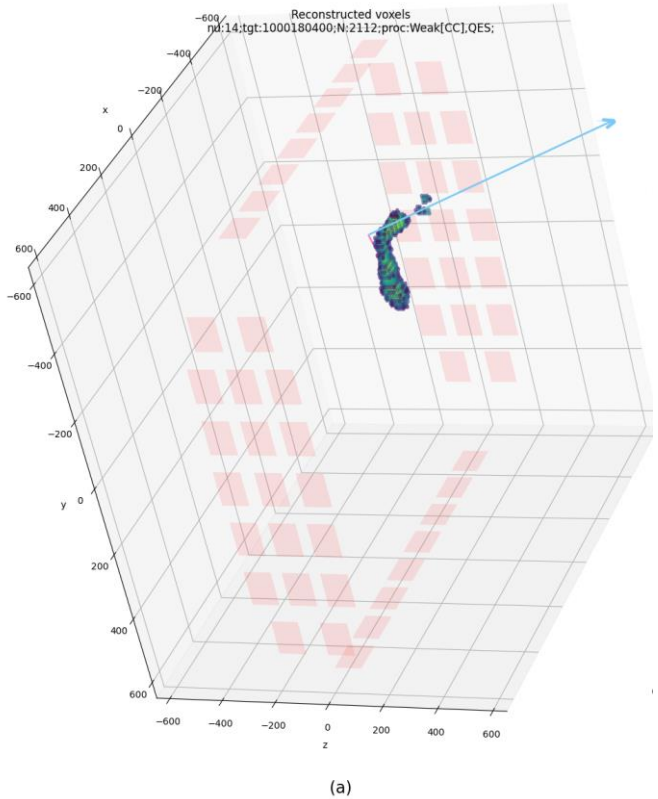


Examples

- Simulations of Coded Aperture masks with 3D reconstruction algorithm in LAr:



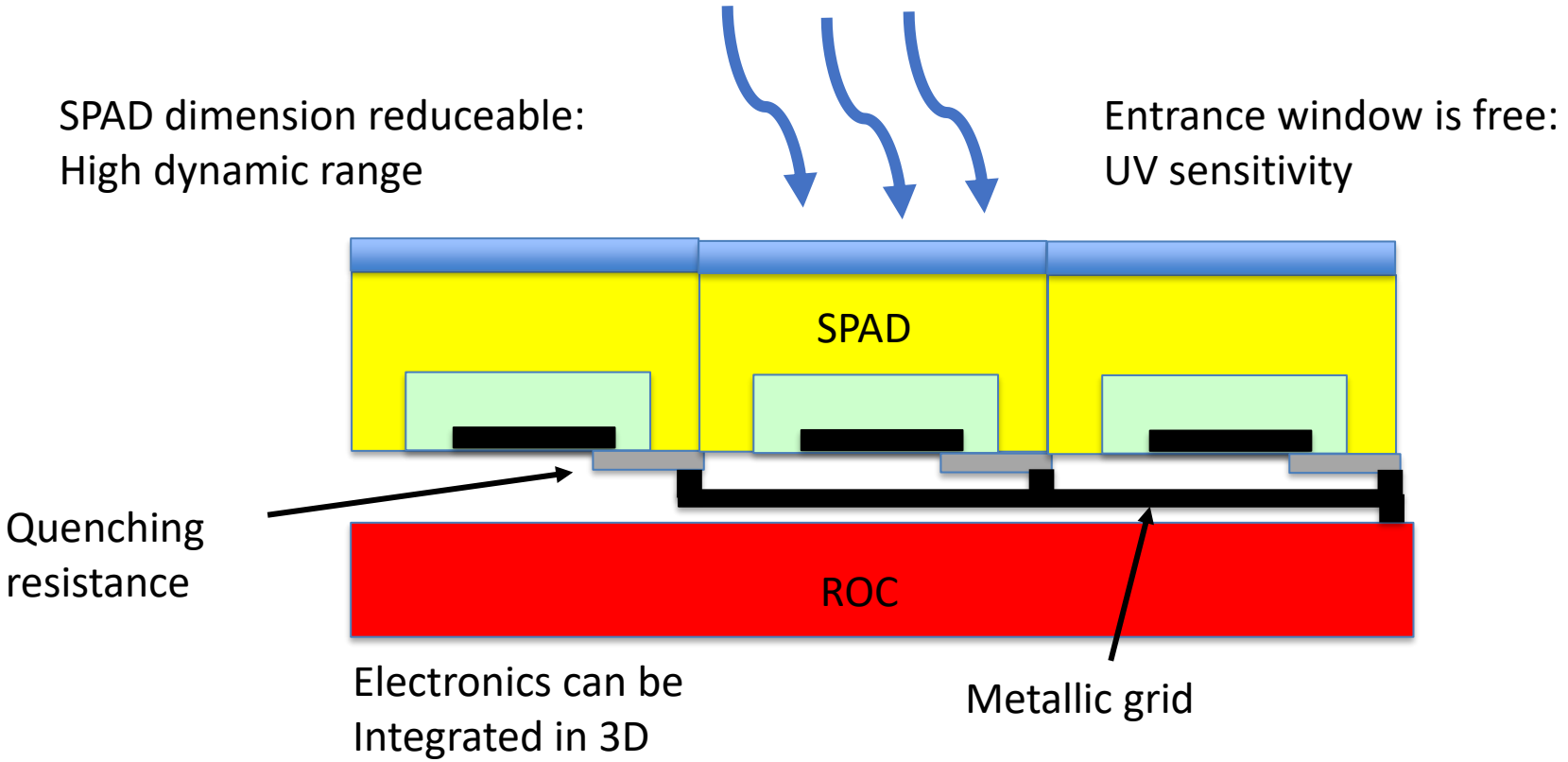
Cosmic Muon



Neutrino Interaction (proton + muon)

Electronics

- As a first step of 3D integration, the design of INFN-Torino foresee a ReadOut Chip (ROC) based on the “Alcor” ASIC:
  - one channel in 440x440 um2
  - mini-SiPM by grouping SPADS so that the size correspond to one channel
  - chip bonding



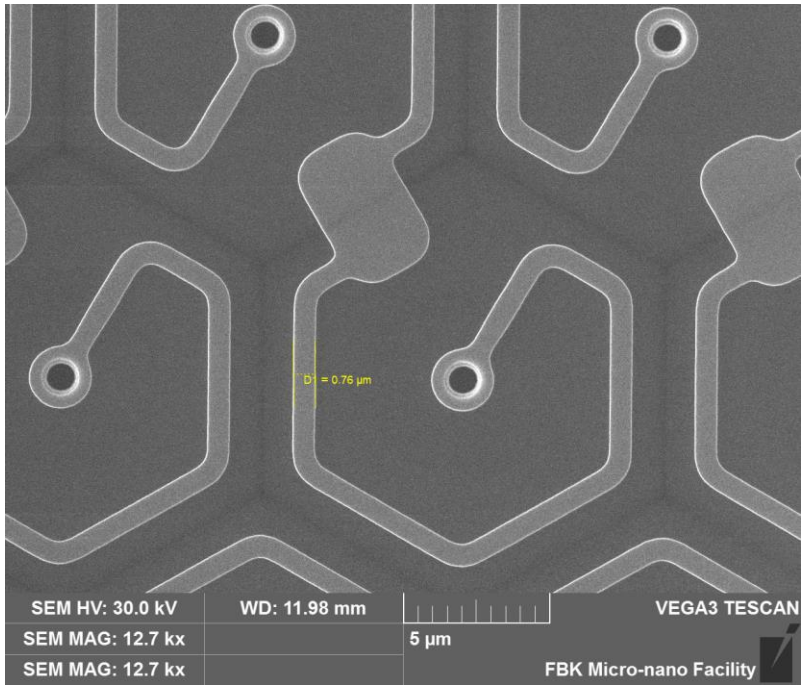
IBIS Run#1:
Process split table

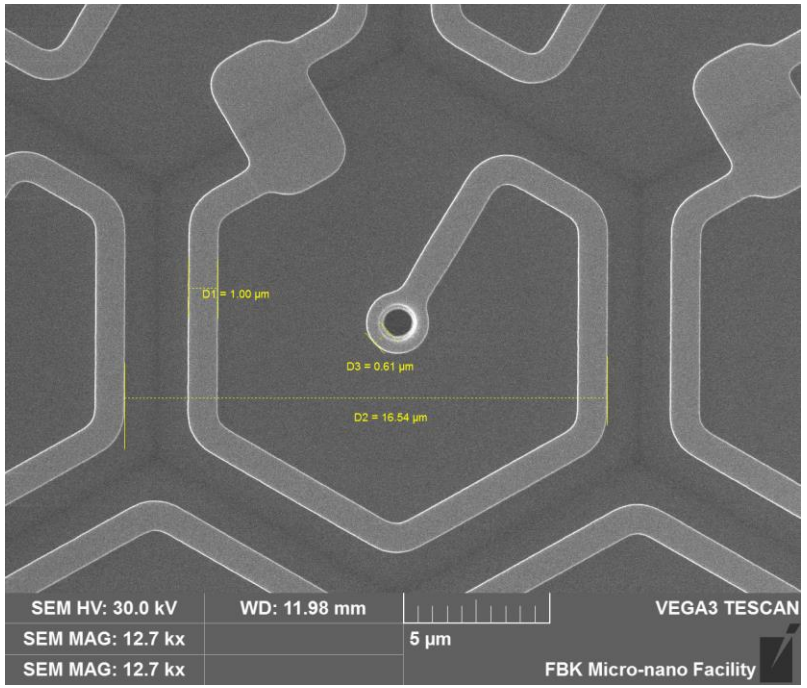
Wfs	Epi thickness	Wafer vendor	Trench	Plasma Doping	Annealing	note
1	split 1	Vendor 2	Split 1	Dose 1	Split1	
2	split 1	Vednor 2	Split 2	Dose 1	Split1	
3	split 1	Vendor 2	Split 2			Test Front Side
4	split 1	Vednor 2	Split 1	Dose 1	Split2	
5	split 1	Vendor 2	Split 2	Dose 1	Split2	
6	split 1	Vednor 2	Split 1			Test Front Side
7	split 1	Vendor 2	Split 1	Dose 2	Split1	
8	split 1	Vednor 2	Split 2	Dose 2	Split1	
9	split 1	Vendor 2	Split 2	Dose 2	Split1	
10	split 1	Vednor 2	Split 1	Dose 2	Split2	
11	split 1	Vendor 2	Split 2	Dose 2	Split2	
12	split 1	Vednor 2	Split 2	Dose 2	Split2	
13	split 1	Vendor 1	Split 1			Test Front Side
14	split 1	Vendor 1	Split 2			Test Front Side

1 epi thickness
2 vendors (standard vs new vendor)
2 trench depths: split1 deeper than split 2

IBIS Run#1:
Process Report – Example of in-line quality controls

Poly Resistor Litho Inspection

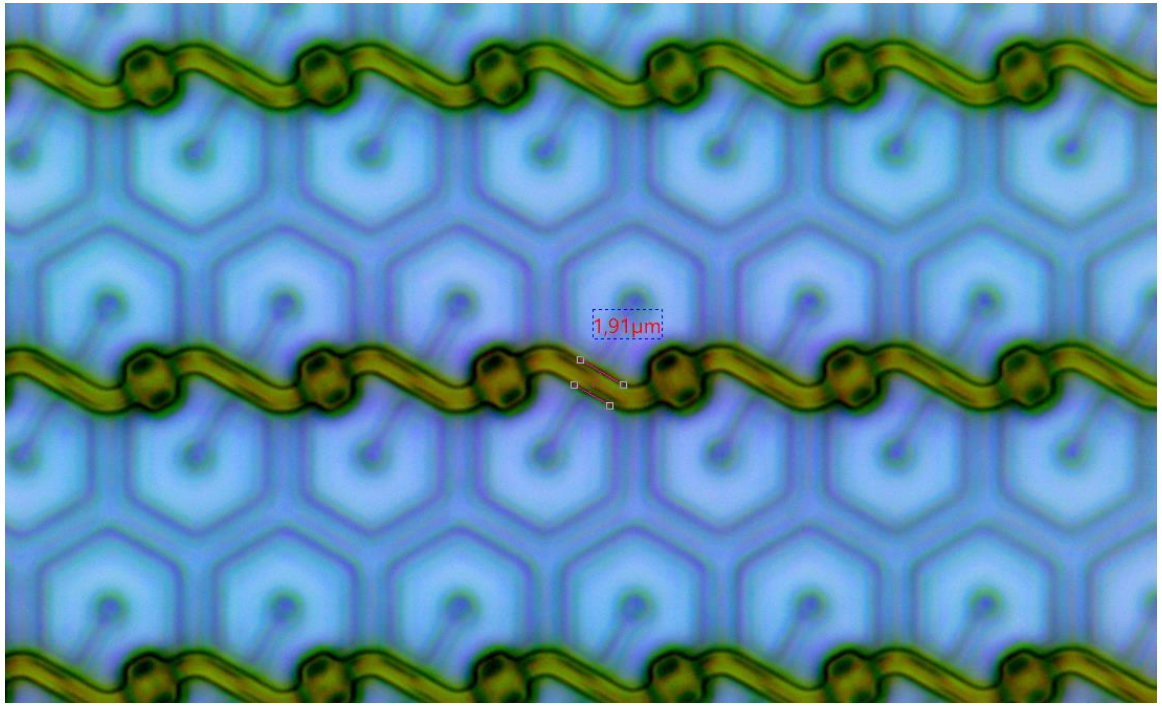




	Designed (um)	Measured (um)
Poly Width 1	0.75	0.76
Poly Width 2	1	1

IBIS Run#1:
Process Report – Example of in-line quality controls

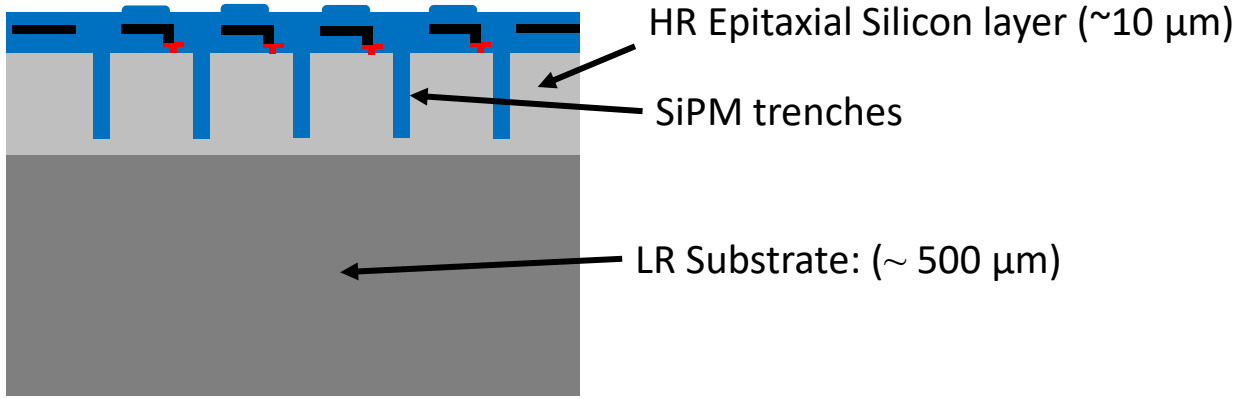
Metal Litho Inspection



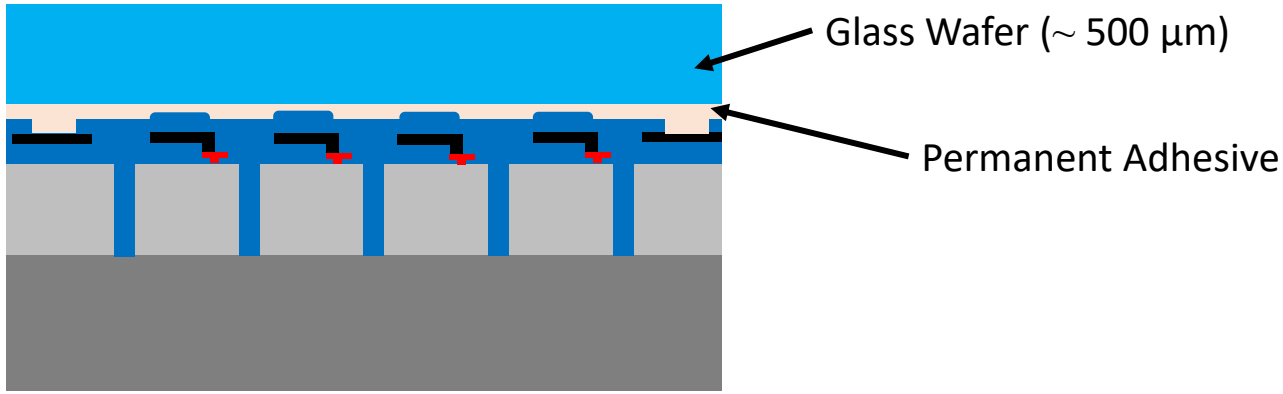
	Designed (um)	Measured (um)
Metal Strip width	2	1.9

IBIS Run#1:
BEOL Process Flow

1. Starting Wafer (6”)

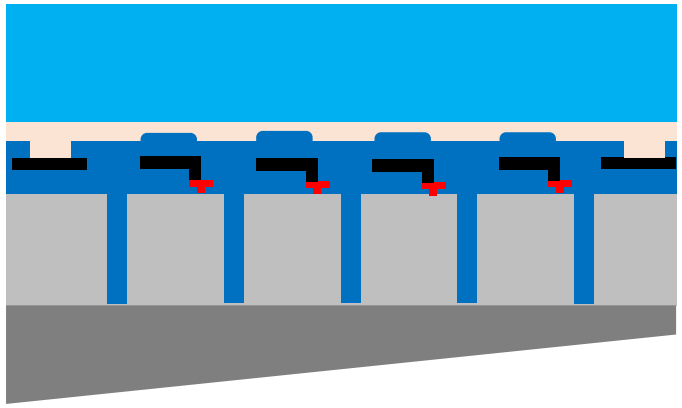


2. Adhesive Permanent Bonding to Glass Wafer



IBIS Run#1:
BEOL Process Flow

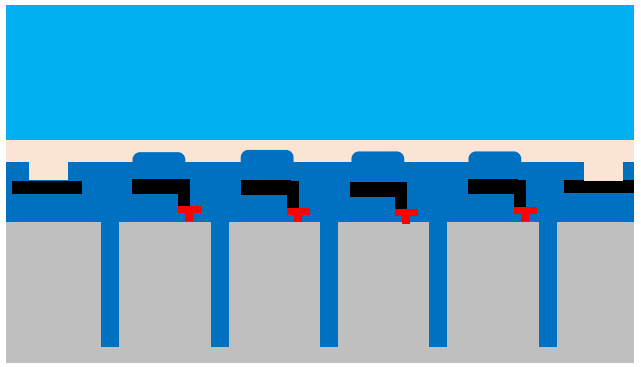
3. Wafer thinning (Substrate Removal)



Remaining Substrate buffer after grinding: ~ 10 µm

Expected total thickness variation (TTV): 2-4 µm

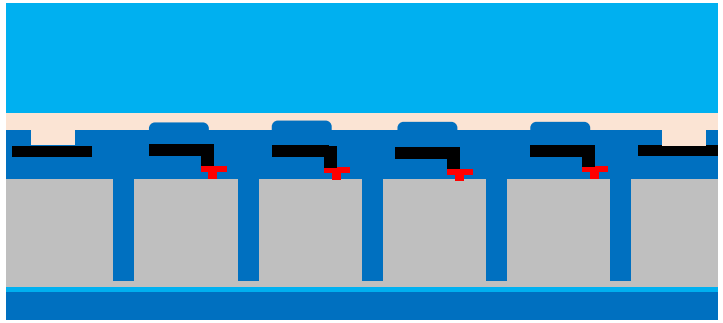
4. Etching of highly doped Silicon substrate using doping selective etching



Doping Selective WET etching is used to complete the substrate removal and to reach the epi/sub interface by reducing the final TTV

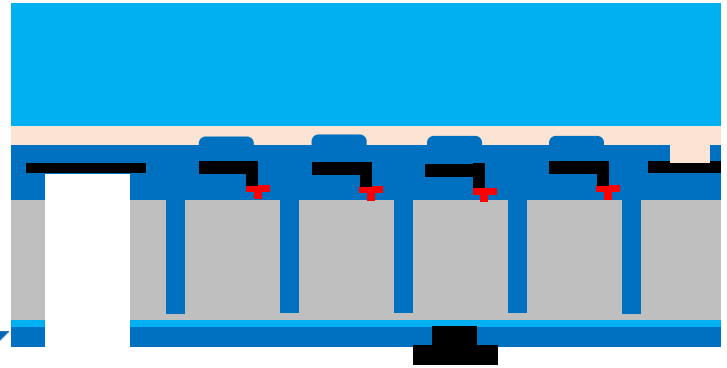
IBIS Run#1:
Latest tests: HNA for substrate Removal

5. Back junction Formation



- Final Polishing (tbd)
- Plasma Ion Implantation and laser annealing
- ARC deposition

7. Contact formation

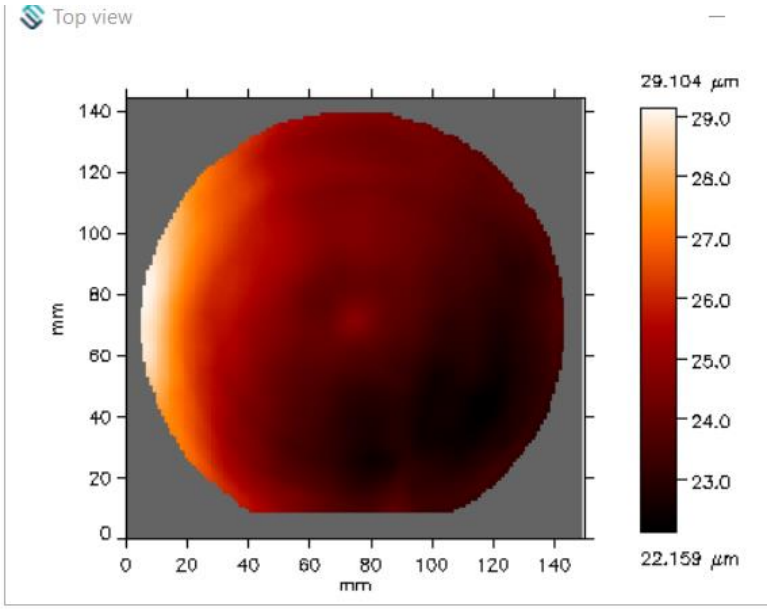


Anode and cathode contacts form the backside

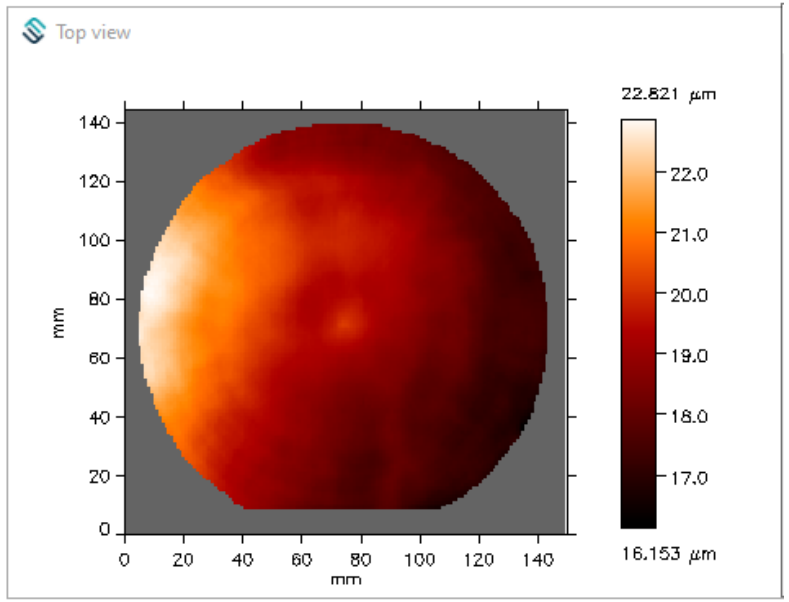
IBIS Run#1:
Latest tests: HNA for substrate Removal

Just After grinding

Ave: 24.3um
TTV: 7 um



Partial HNA Etching
Ave: 19.1 um
TTV: 6.7 um



Complete HNA Etching
Ave: 15.6 um
TTV: 0.7 um