Silicon tracker development from ALICE towards FCC-ee

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INFN Trieste in the European Strategy
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Outline

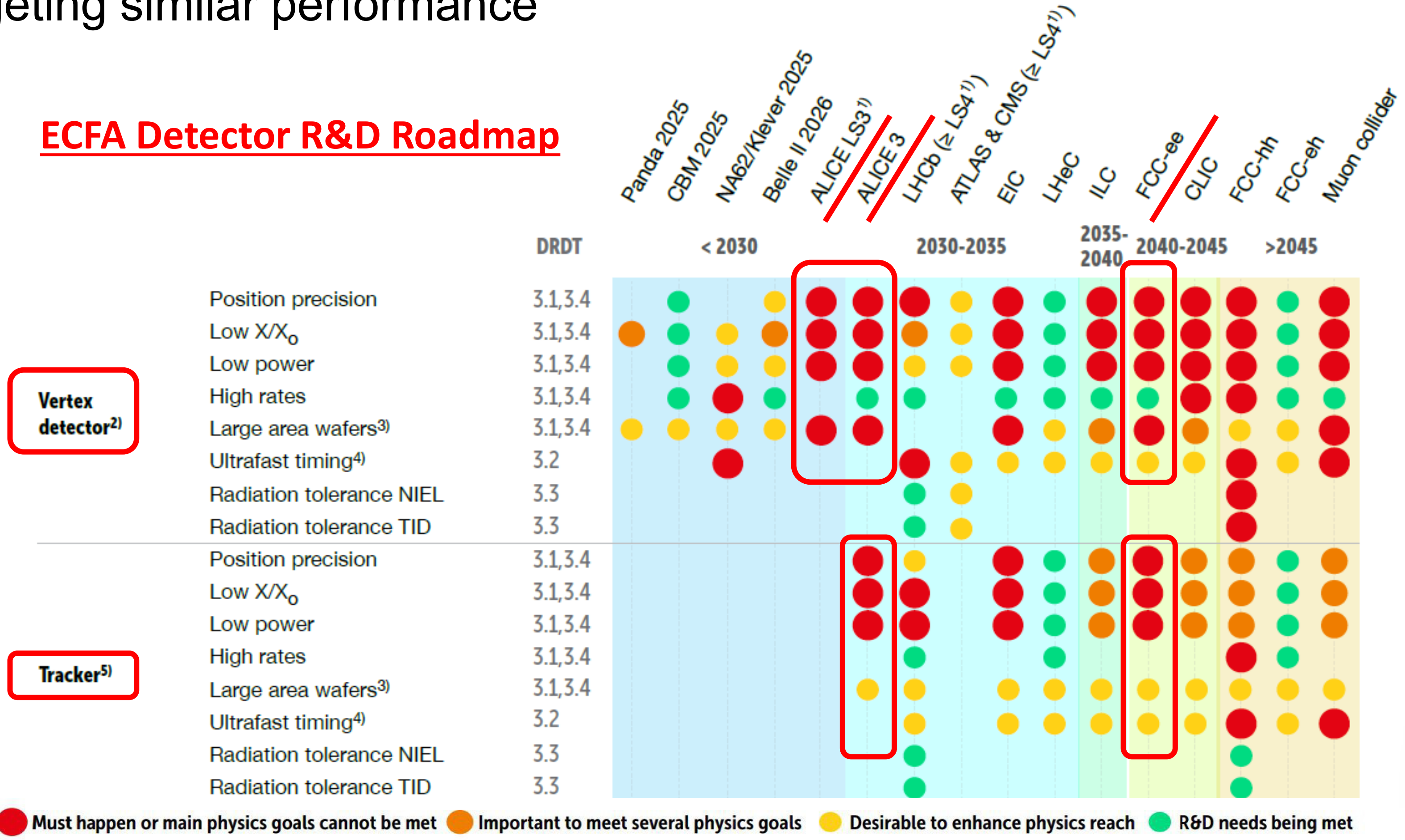
- ALICE Upgrades and FCC-ee **common challenges**
- **ITS3**: ALICE vertex detector upgrade for **LHC Run 4**
  - Ultra-thin, truly cylindrical, wafer-scale MAPS
- **ALICE 3**: future heavy-ion experiment for **LHC Run 5** and beyond
  - Compact all-silicon MAPS tracker
- Conclusions and outlook

ALICE Upgrades and FCC-ee common challenges

- The ALICE silicon upgrades planned for LHC LS3 and LS4 and the FCC-ee vertex and tracker detectors are targeting similar performance

Can the R&D for ITS3 and ALICE 3 serve as a stepping stone for FCC-ee vertex and tracker detectors?

ECFA Detector R&D Roadmap



		DRDT	Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3 1)	ALICE 3	LHCb (≥ LS4 1))	ATLAS & CMS (≥ LS4 1))	EIC	LHeC	ILC	FCC-ee	CLIC	FCC-hh	FCC-eh	Muon collider
			< 2030					2030-2035					2035-2040	2040-2045		>2045		
Vertex detector2)	Position precision	3.1,3.4		🟢		🟡	🔴	🔴	🔴	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low X/X_0	3.1,3.4	🟠	🟢	🟡	🟠	🔴	🔴	🟠	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low power	3.1,3.4		🟢	🟡	🟡	🔴	🔴	🟡	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	High rates	3.1,3.4		🟢	🔴	🟢		🟢	🟢		🟢	🟢	🟢	🟢	🔴	🔴	🟢	🟢
	Large area wafers3)	3.1,3.4	🟡	🟡	🟡	🟡	🔴	🔴			🔴	🟡	🟠	🔴	🟠	🟡	🟡	🔴
	Ultrafast timing4)	3.2			🔴				🔴	🟡	🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢	🟡						🔴		
	Radiation tolerance TID	3.3							🟢	🟡						🔴		
Tracker5)	Position precision	3.1,3.4						🔴	🟡		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low X/X_0	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low power	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	High rates	3.1,3.4							🟢			🟢				🔴	🟢	
	Large area wafers3)	3.1,3.4						🟡	🟡		🟡	🟡	🟡	🟡	🟡	🟡	🟡	🟡
	Ultrafast timing4)	3.2							🟡		🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢							🟢		
	Radiation tolerance TID	3.3							🟢							🟢		

🔴 Must happen or main physics goals cannot be met 🟠 Important to meet several physics goals 🟡 Desirable to enhance physics reach 🟢 R&D needs being met

ALICE Upgrades and FCC-ee common challenges

- The ALICE silicon upgrades planned for LHC LS3 and LS4 and the FCC-ee vertex and tracker detectors are targeting similar performance

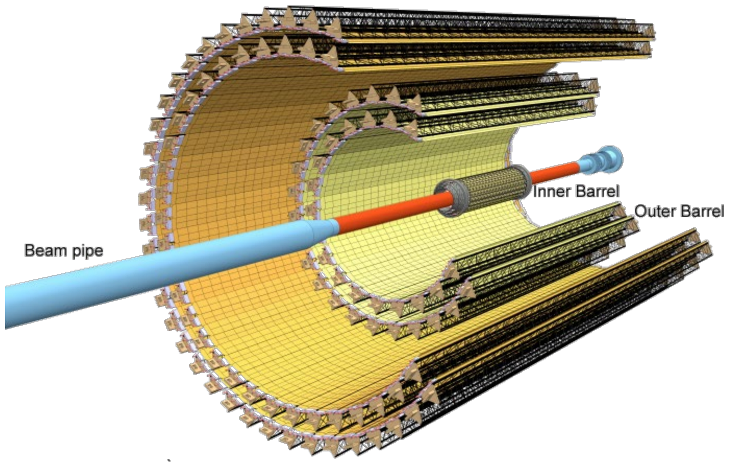
Target performance	ITS3	ALICE 3	FCC-ee
Position precision	5 μm	2.5 μm	3 μm
X/X_0 per layer	0.09% *(average)* 0.07% *(most of active region)*	0.1 %	0.15 - 0.3 %
Power consumption	40 mW/cm^2 *(active region)*	20 mW/cm^2	50 mW/cm^2
NIEL	10^{13} 1MeV n_{eq} $/cm^2$	10^{16} 1MeV n_{eq} $/cm^2$ *(LOI, *)*	$\sim 6 \times 10^{12}$ 1MeV neq $/cm^2$/year
TID	1 Mrad	300 Mrad *(LOI , *)*	~3.4 Mrad/year
Maximum hit rate	$<$ 10 MHz/cm^2	94 MHz/cm^2	400 MHz/cm^2 *(*)*
Time resolution	$\mathcal{O}$(1000 ns RMS)	$\mathcal{O}$(100 ns RMS)	~ 20 ns RMS

** being revised*

ALICE silicon tracker development path

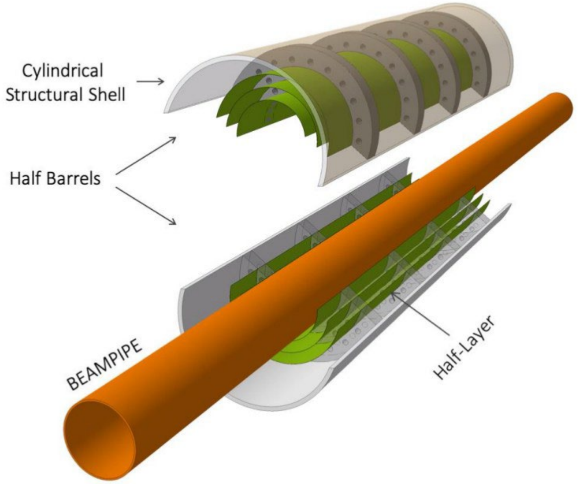

ALICE 2
ALICE 2.1
ALICE 3
LHC Run 3
LHC LS3
LHC Run 4
LHC LS4
LHC Run 5
2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041

ITS2



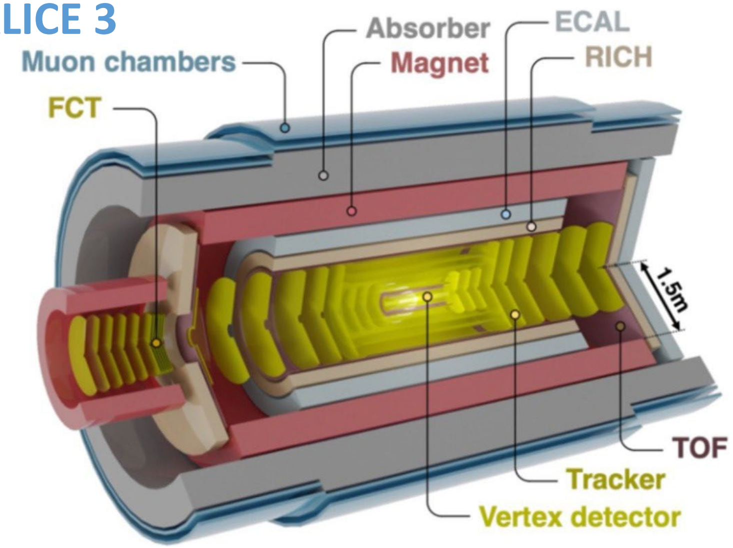
ALICE Upgrades during LHC LS2

ITS3



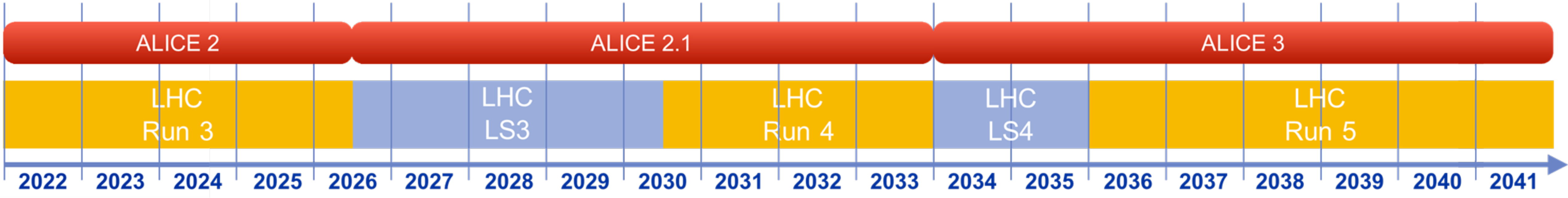
LOI: CERN-LHCC-2019-018
TDR: CERN-LHCC-2024-003

ALICE 3

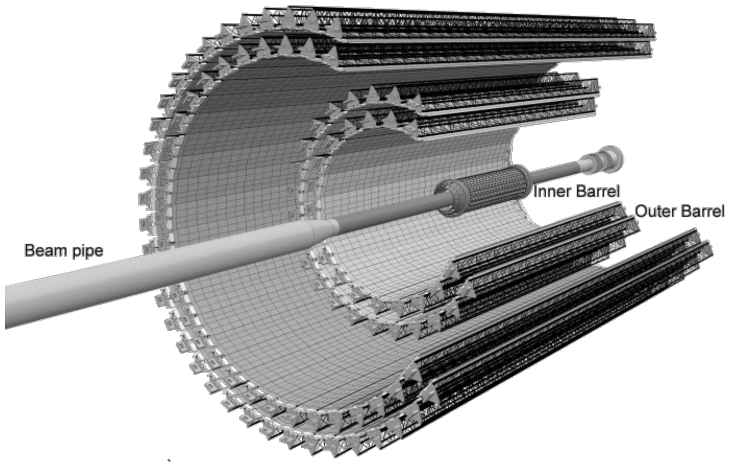


LOI: CERN-LHCC-2022-009
Scoping Document submitted to LHCC

ALICE silicon tracker development path



ITS2



ALICE Upgrades during LHC LS2

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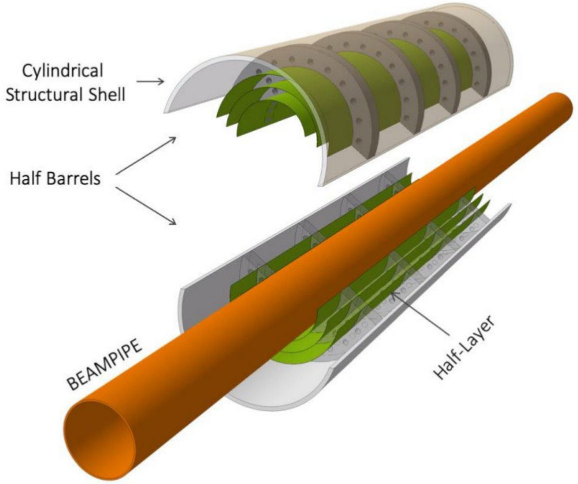

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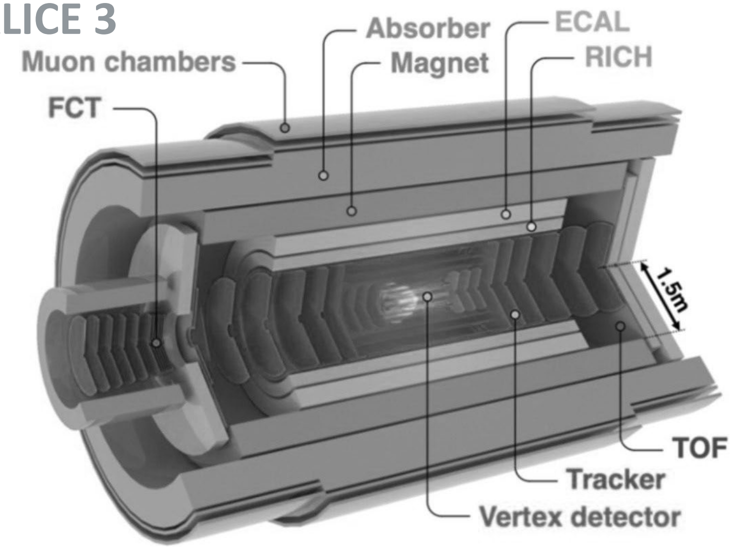

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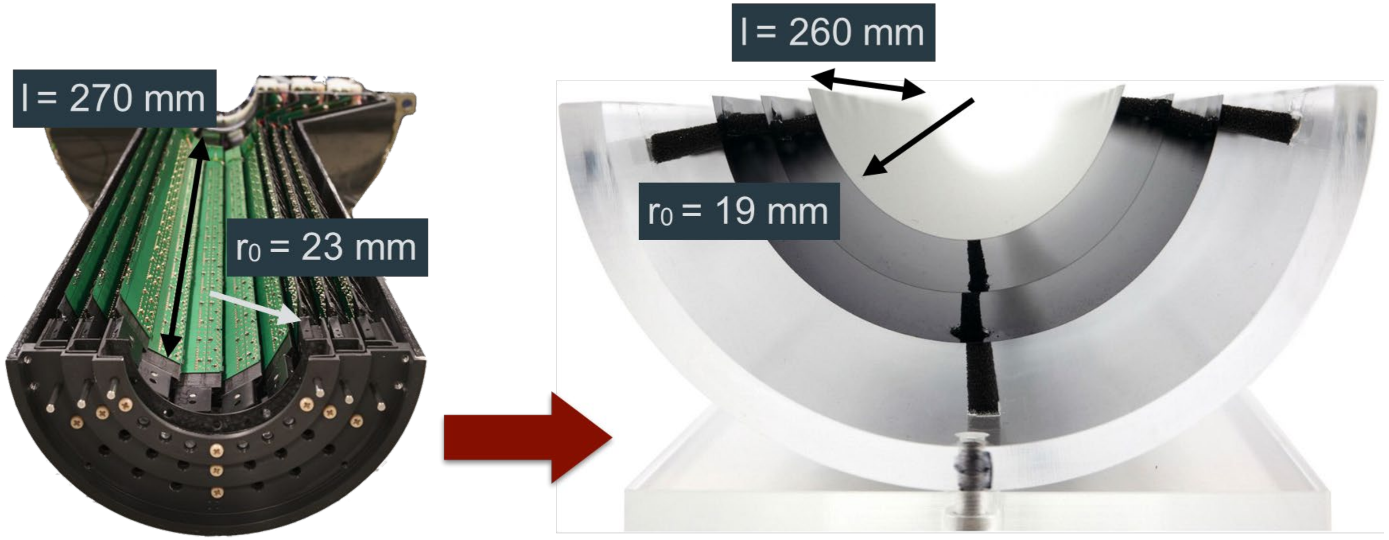
ITS3 layout and material budget

- **3 layers of curved wafer-scale MAPS in TPSCo 65 nm CMOS process**
  - Replacing ITS2 Inner Barrel (innermost radius reduced from 24 mm to **19 mm**)
  - Each half-layer made of one wafer-size **flexible sensor**
  - **In-silicon** data transmission and power distribution
  - Minimal **carbon foam** support structures
  - **Air cooling**



ITS2 Inner Barrel **ITS3 Engineering Model 1**

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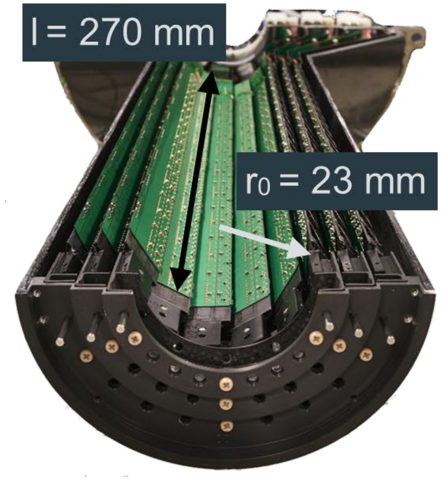
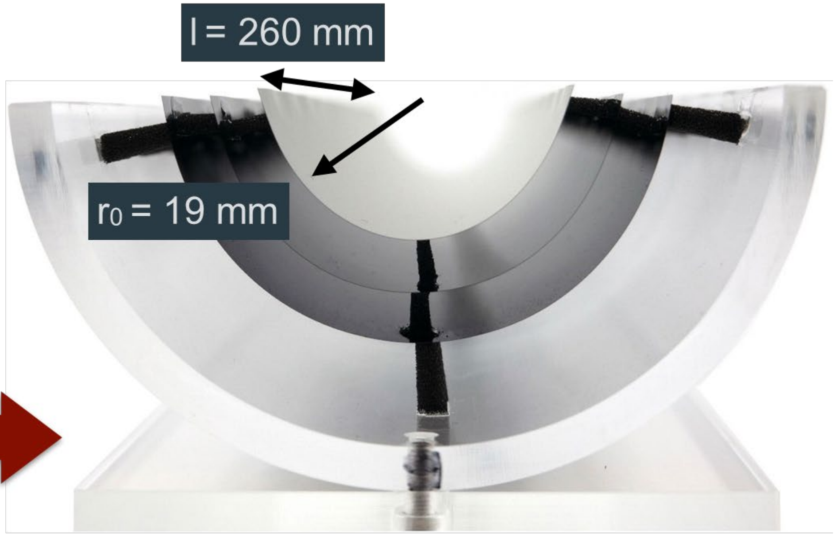
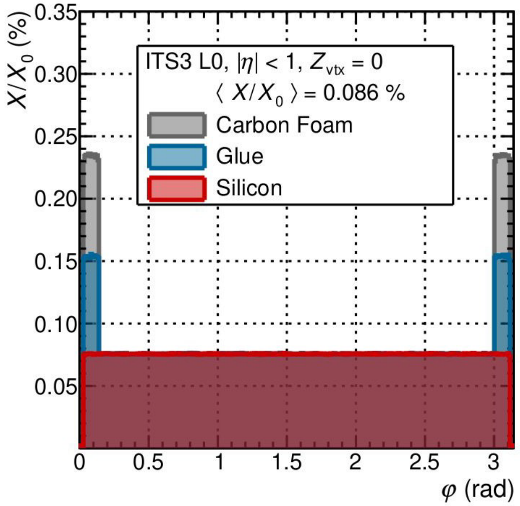


ITS2 Inner Barrel



ITS3 Engineering Model 1



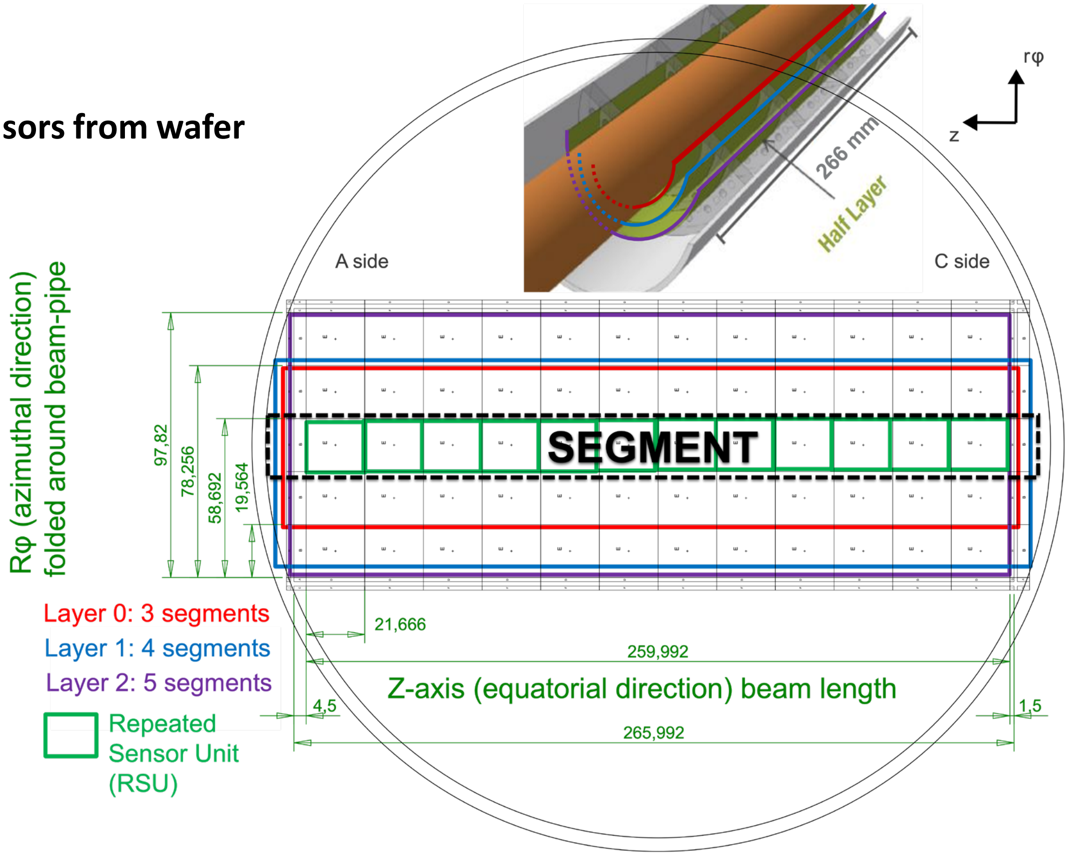
Minimal material budget:

~0.09% X_0 on average

ITS3 layout and material budget

- **3 layers of curved wafer-scale MAPS in TPSCo 65 nm CMOS process**

ITS3 sensors from wafer

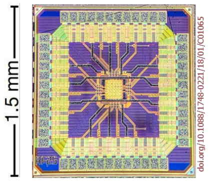


ITS3 Engineering Model 2

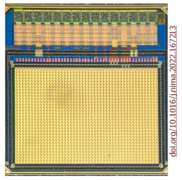
ITS3 chip development plan

PAST

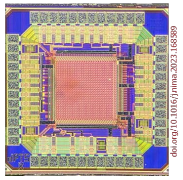
- Multi-Layer Run 1 (MLR1): **first MAPS in TPSCo 65 nm** CMOS
  - Transistor test structures
  - Analog and digital test structures
  - Achieved goal: **full process qualification**



APTS



CE65



DPTS

- Engineering Run 1 (ER1): **first large area sensors**
  - Main goals: **excercize and validate stitching**
  - Chips work, main yield issue understood
  - Full characterization currently ongoing

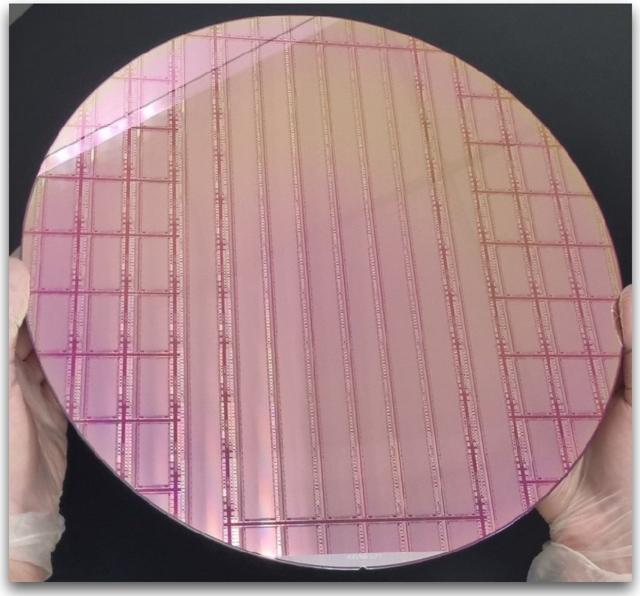
PRESENT

- Engineering Run 2 (ER2): **first ITS3 sensor prototype**
  - Now: **specifications frozen**, design being finalized
  - Submission to foundry planned for early 2025

we are here!

FUTURE

- Engineering Run 3 (ER3): **ITS3 sensor production**



ER1 wafer

65 nm CMOS process validation and radiation hardness

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TPSCo **65 nm CMOS process validated** on MLR1 test structures:

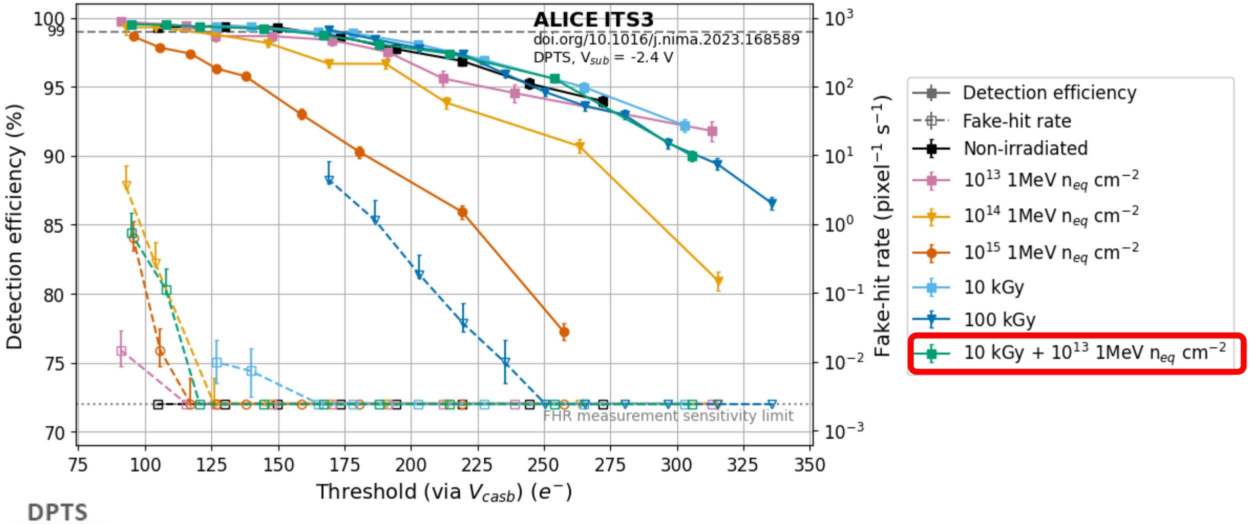
FCC-ee

$\sim 6 \times 10^{12}$ 1MeV neq /cm^2/year

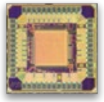
- Efficiency > 99%
- Fake-hit rate < $2 \cdot 10^{-3}$ pix^{-1} s^{-1}

over a wide operating range

- Radiation hardness demonstrated beyond **10 kGy + 10^{13} 1MeV n_{eq} cm^{-2}** *ITS3 requirement*
  - Still efficient with 10^{15} 1MeV n_{eq} cm^{-2} at room temperature



DPTS



Detection efficiency and fake-hit rate Vs threshold and irradiation levels, as measured on 15 μm pitch **Digital Pixel Test Structures (DPTS)**

ITS3 sensor performance: spatial resolution

- ITS3 **spatial resolution requirement: 5 µm**
  - Test beam measurements on APTS with different pixel pitches
  - Requirement met for pitch ≤ 20 µm at standard operating settings
  - Projected resolution with (20.8 µm x 22.8 µm) **ITS3 target pixel pitch meets the requirement**

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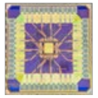
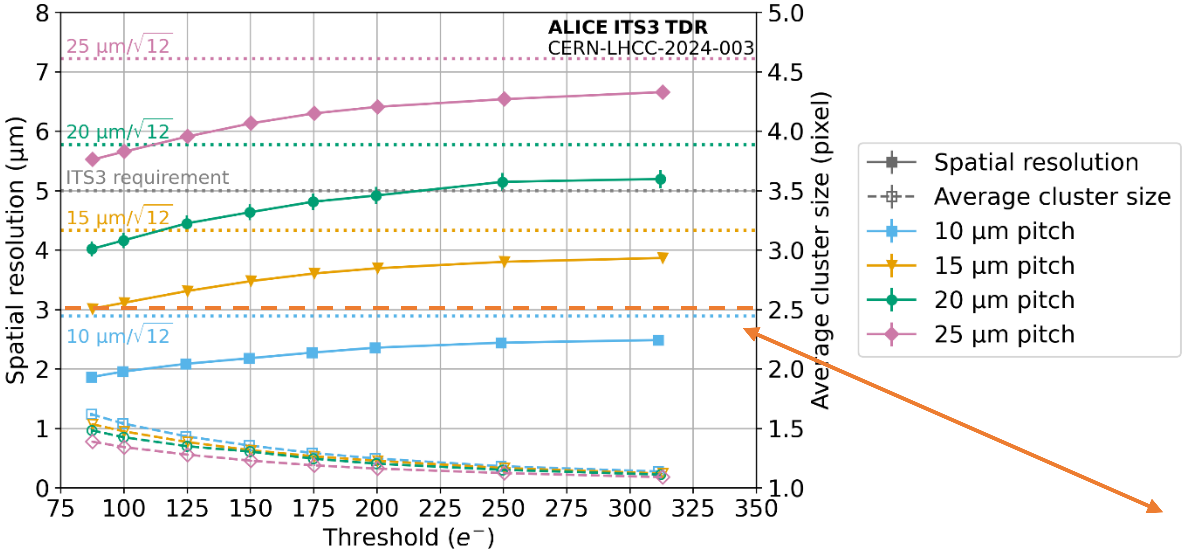
APTS



Spatial resolution Vs threshold and pixel pitch, as measured in testbeams on **APTS**



FCC-ee

3 µm

- Sensor **position stability** required to be within 2 µm

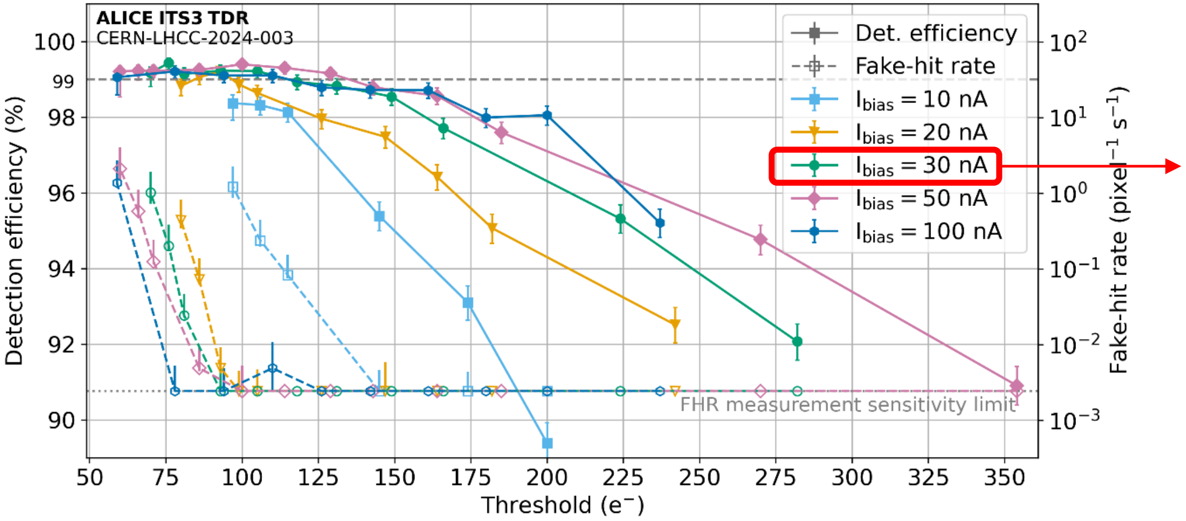
ITS3 sensor performance: power consumption

- ITS3 maximum **power density: 40 mW/cm^2** in the pixel matrix
- In-pixel power consumption minimization studied on DPTS by optimizing front-end settings
  - 16 mW/cm^2 as measured on 15 μm pixel
  - 7.6 mW/cm^2 if projected to the final ITS3 sensor pixel pitch

to be measured on stitched sensor matrix

FCC-ee

50 mW/cm^2



= 16 mW/cm^2 on DPTS

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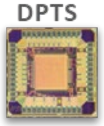
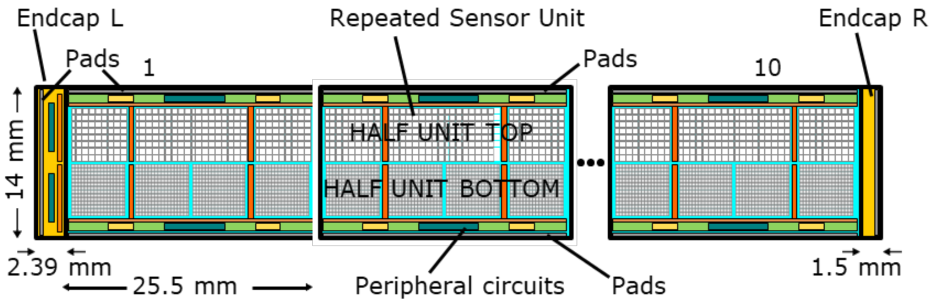
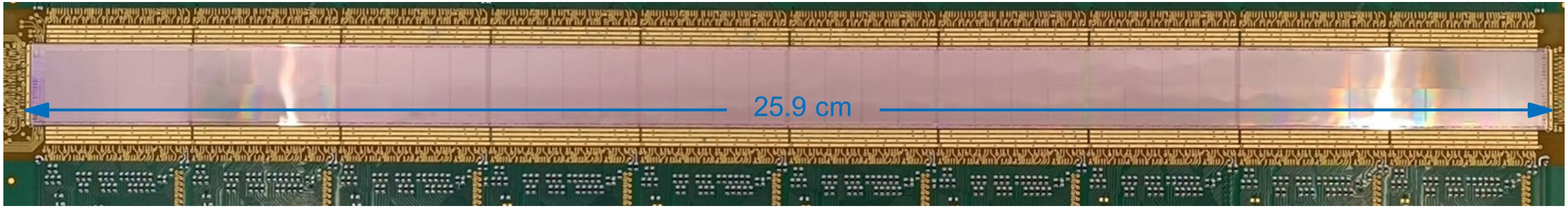


Detection efficiency and fake-hit rate Vs threshold and amplifier biasing current as measured on 15 μm pitch **DPTS**

ITS3 sensor performance: stitching

- **MOnolithic Stitched Sensor (MOSS):**
  - 10 Repeated Sensor Units (RSU) stitched together
  - **25.9 cm x 1.5 cm** – 18 µm and 22.5 µm pitch – 5 FE variants
  - **Stitched backbone** allows to control and read out from left edge
  - Each unit can be powered and tested separately
  - **Main yield issue understood**





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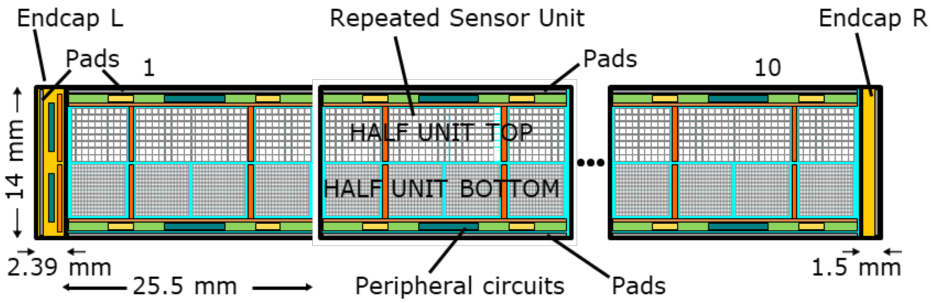

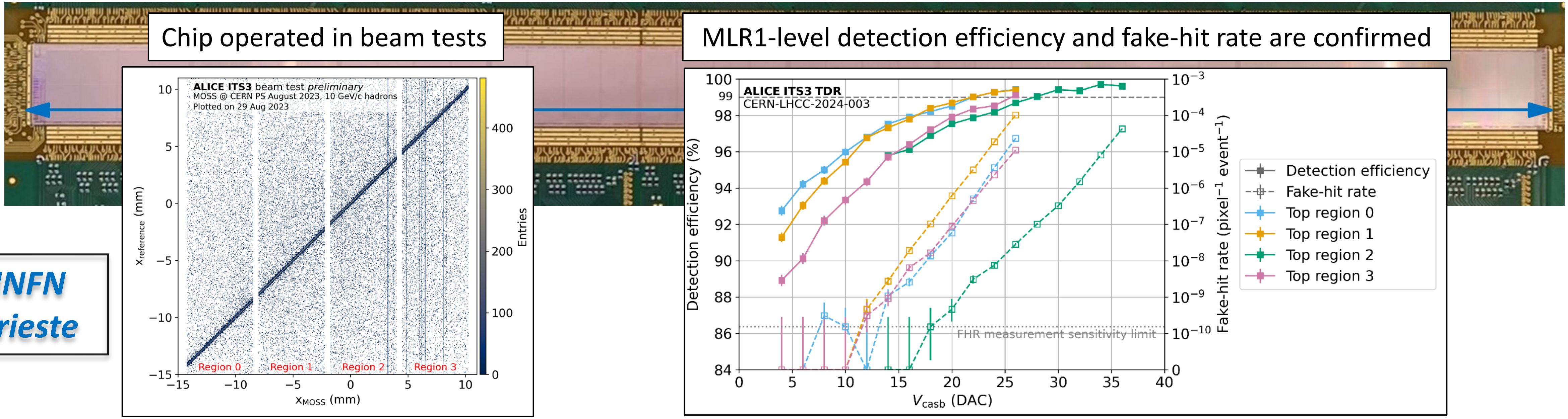

Chip operated in beam tests

MLR1-level detection efficiency and fake-hit rate are confirmed

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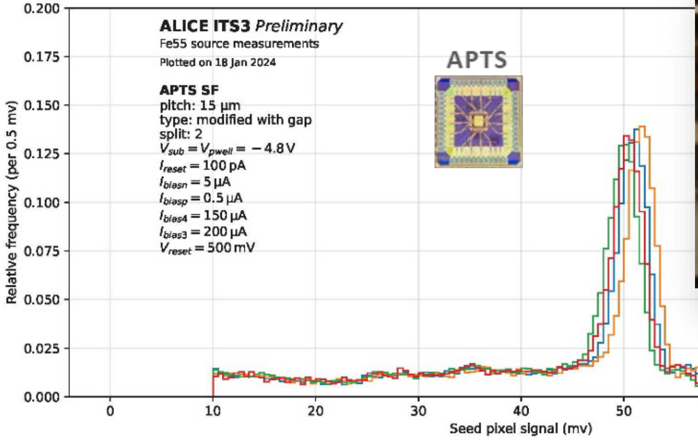
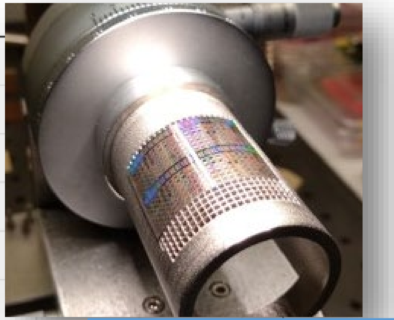
Bent MAPS: performance validation

- MAPS performance in **curved geometry** has been validated
  - Efficiency preserved on bent ALPIDE (180 nm CMOS sensors)
  - Charge collection properties preserved on bent APTS (65 nm CMOS)





Seed pixel signal response to ^{55}Fe as measured by flat and bent **APTS**

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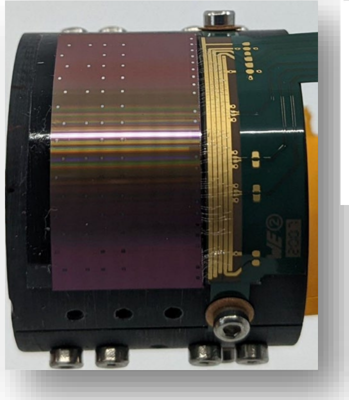
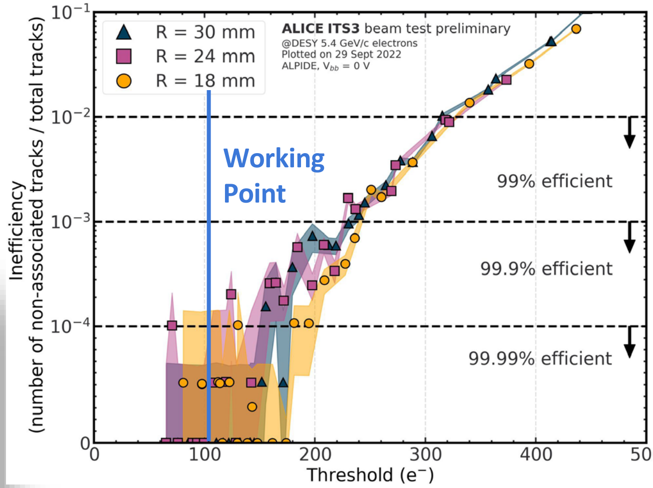
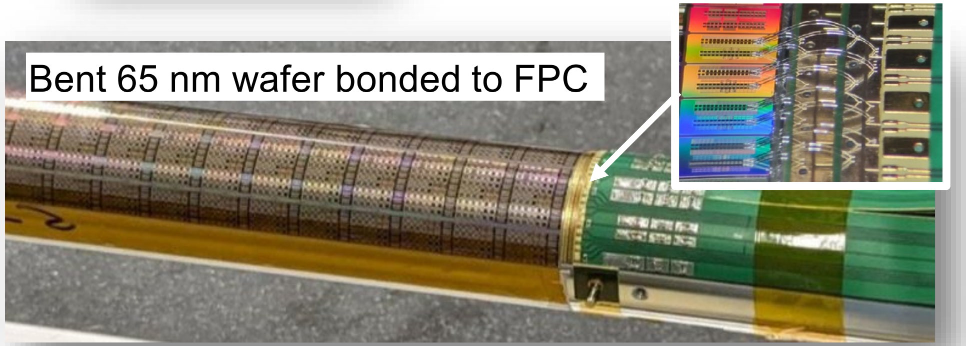




Detection inefficiency Vs threshold for curved 180 nm CMOS sensors (**ALPIDE**), bent beyond the ITS3 radii

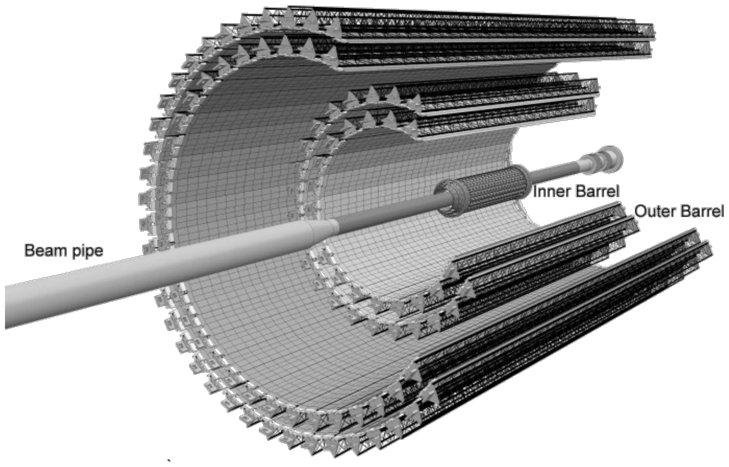
- **Large-area** sensor bending
  - Technique and procedure have been mastered
  - Tests on functional bent stitched sensors in preparation



Bent 65 nm wafer bonded to FPC

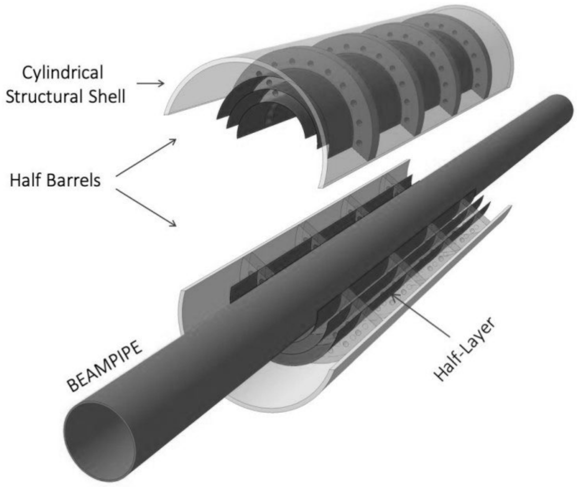
ALICE silicon tracker development path

ITS2



ALICE Upgrades during LHC LS2

ITS3



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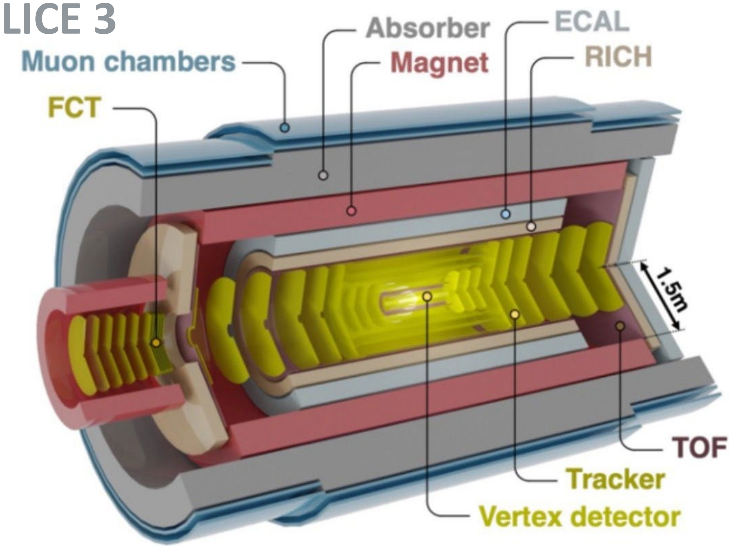
ALICE 3



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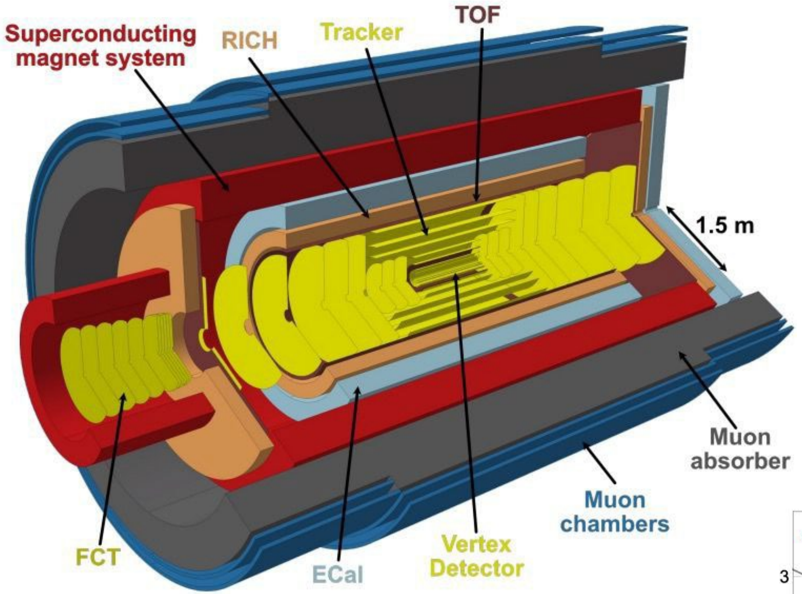
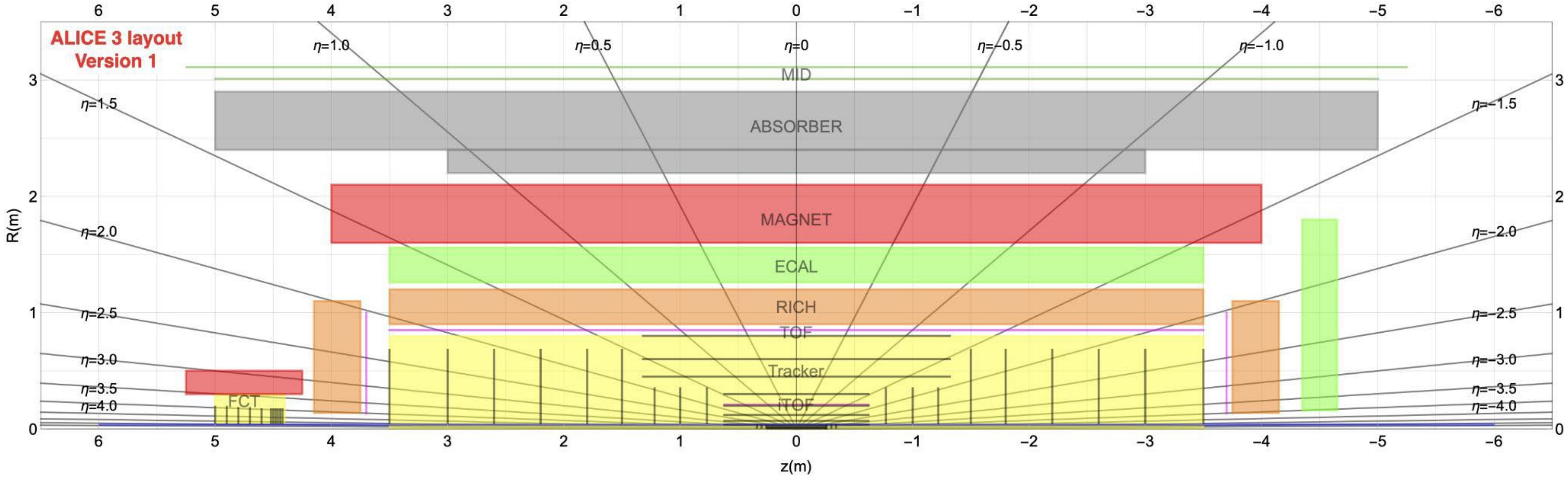
ALICE 3



Next generation **compact experiment for LHC Run 5** and beyond

- **60 m^2** low-mass **all-silicon tracker** fully made of MAPS
- Retractable vertex detector for **unprecedented pointing resolution**
- **Large acceptance:** $-4 < \eta < 4$
- Specific **INFN R&D for Vertex Detector and Middle Layers**

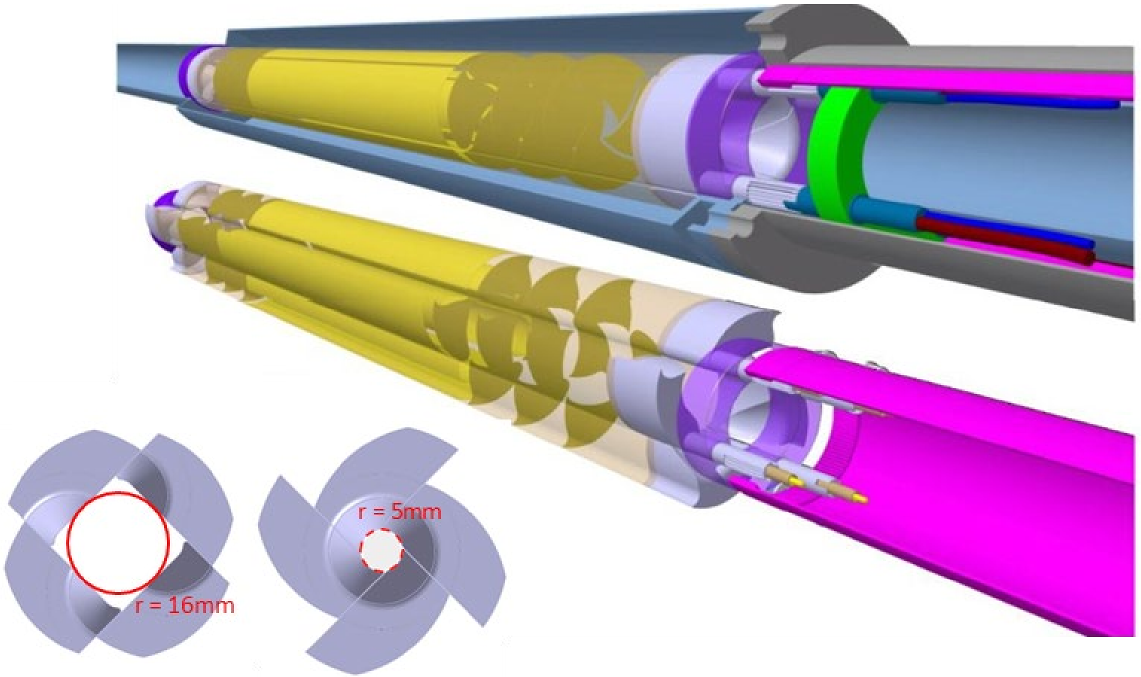


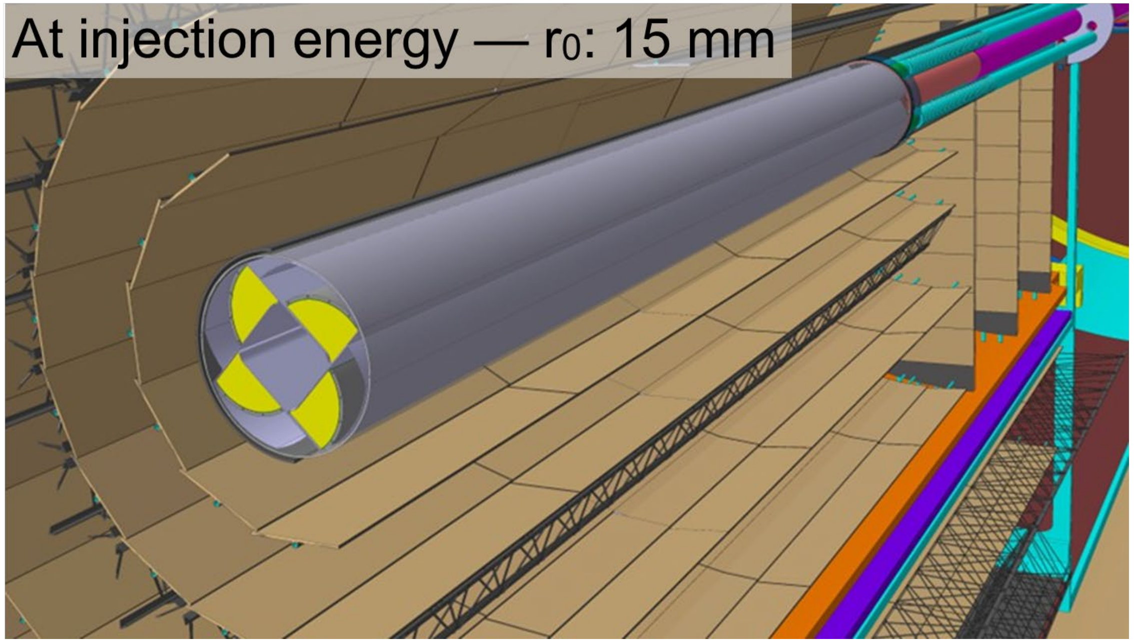
- **LOI** approved in 2022
- **Scoping Document** submitted to LHCC
- Specific **R&D has started**

ALICE 3 Vertex Detector

3 barrel layers of ultra-thin, curved, wafer-scale MAPS

- Retractable structure inside the beam pipe secondary vacuum
- First detection layer at **5 mm from the interaction point**
- Completed by 2 x 3 end-cap disks for high |η| coverage





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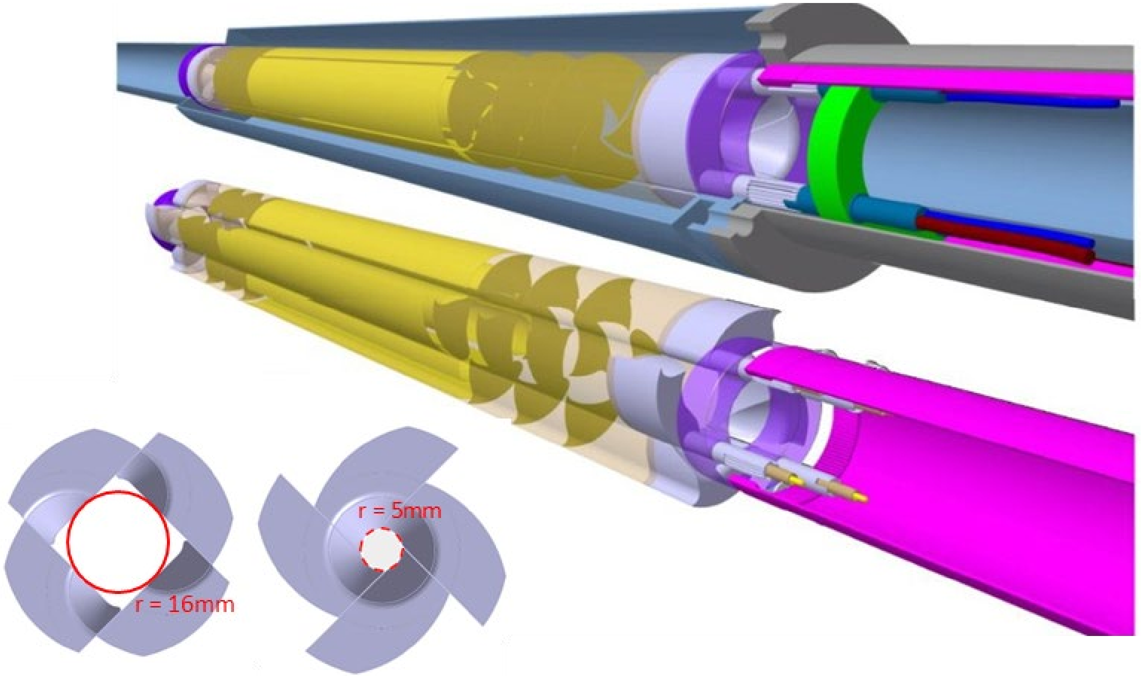

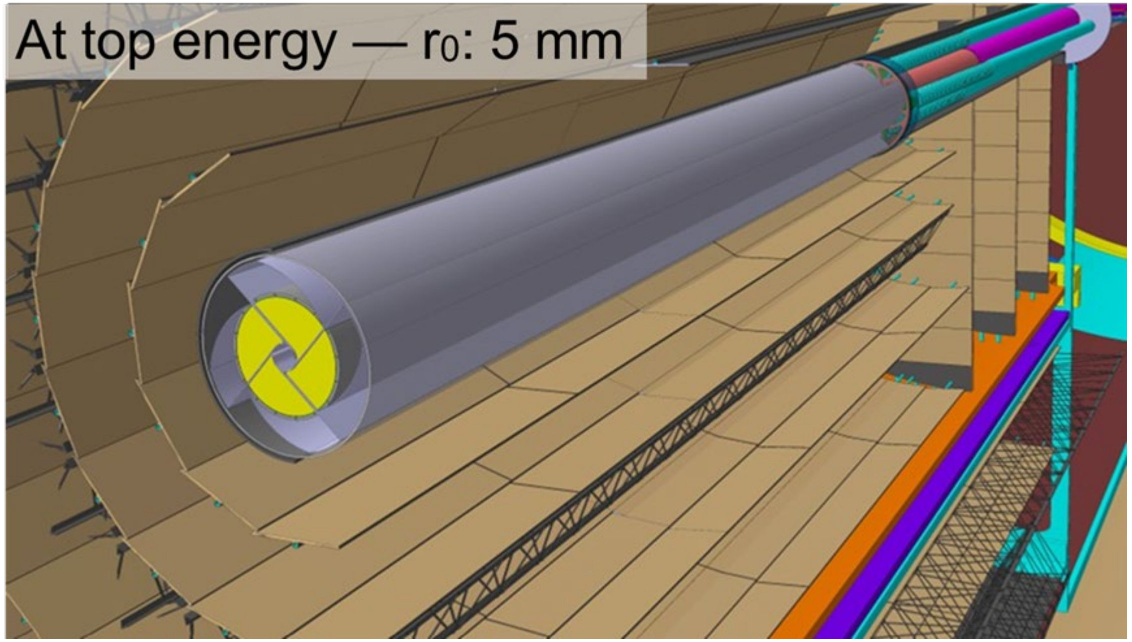

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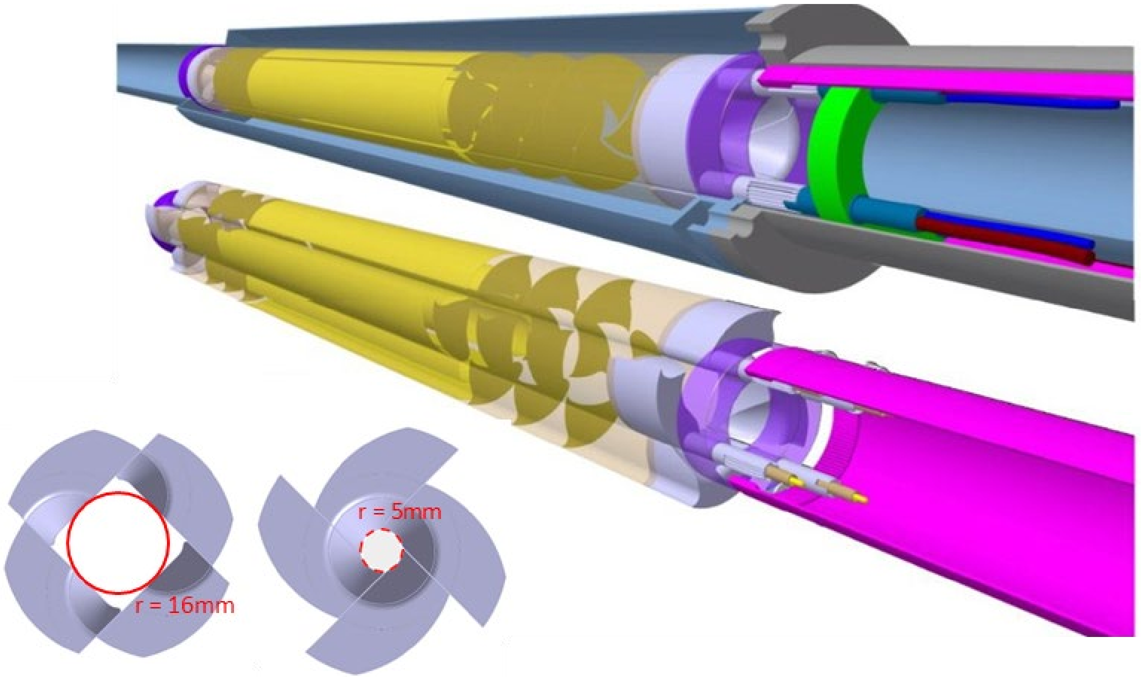

- Unprecedented **spatial resolution: 2.5 μm**
- Extremely low **material budget: 0.1%** X_0/layer
- **Hit rate: up to 94 MHz cm^{-2}**
- **Main R&D challenges:**
  - Radiation hardness
    - **10^{16} 1MeV n_{eq} cm^{-2} + 300 Mrad** *(LOI values)*
  - In-vacuum mechanics and cooling
  - **10 μm pixel pitch**
  - Data and power distribution

ALICE 3 Middle Layers and Outer Tracker

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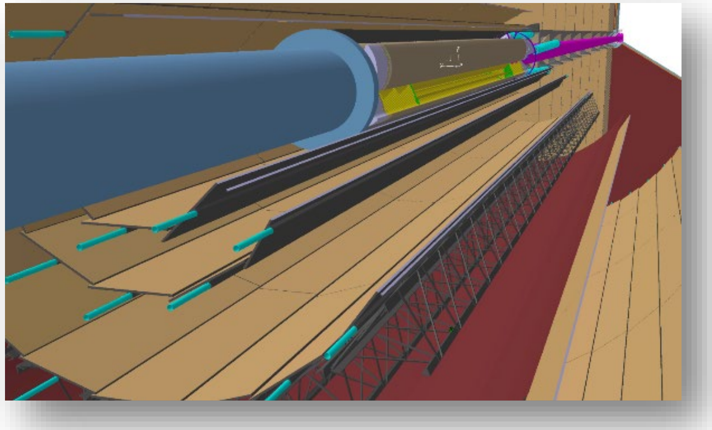
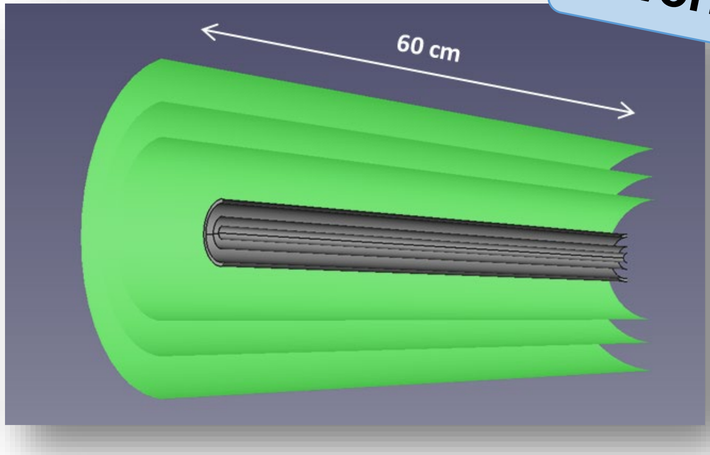
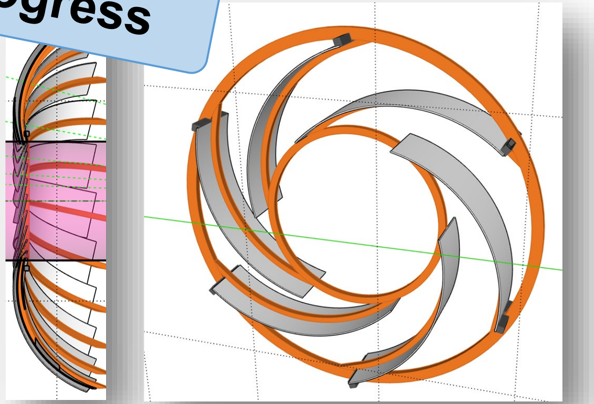
- Specific layouts being proposed for **Middle Layers**
  - 3-4 layers **outside the beam pipe** (r < 20 cm)
  - **Material budget reduction** from 1% to 0.1% beneficial for secondary particles and soft e^-

Work in progress


Standard staves/module layout (LOI)



ITS3-like bent large-area sensors


Blade/wheel barrels and disks

- Vertex Detector, Middle Layers and Outer Tracker need **specific sensor optimizations:**
  - Towards a common, versatile R&D path forking into two separate chips
  - Easier for other applications like FCC-ee to build on it

DRD3 and DRD7

Conclusions and Outlook

- **ALICE Upgrades** for LS3 and LS4 targeting ambitious detector performance
- **ITS3:** ultra-thin, truly cylindrical, wafer-scale MAPS vertex detector for Run 4
- **ALICE 3**, future LHC heavy-ion collider experiment for Run 5 and beyond
- ITS3 and ALICE 3 upgrades can serve as **stepping stones towards FCC-ee**

- Constant effort to **encourage collaboration** and exchange of information…

Regular occasions for discussion in 2024

ALICE tracker experts invited to several workshop to investigate MAPS silicon technology application to FCC-ee vertex and tracker:

RD_FCC WP-Silicon Mini-workshop 22–23 Apr '24 - Torino

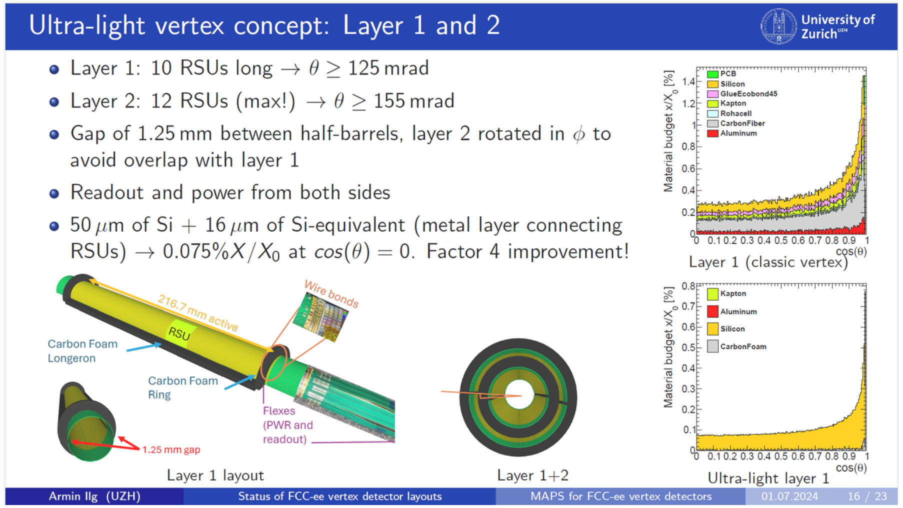
FCC Week 2024 10–14 Jun '24 - San Francisco (USA)

MAPS detectors technologies for the FCC-ee vertex 1 Jul '24 - CERN

2nd FCC Italy & France Workshop 4–6 Nov 2024 - Venezia

…

ITS3/ALICE3 now inspiring FCC-ee vertex concepts



Ultra-light vertex concept: Layer 1 and 2

- Layer 1: 10 RSUs long $\rightarrow \theta \geq 125\,\mathrm{mrad}$
- Layer 2: 12 RSUs (max!) $\rightarrow \theta \geq 155\,\mathrm{mrad}$
- Gap of 1.25 mm between half-barrels, layer 2 rotated in ϕ to avoid overlap with layer 1
- Readout and power from both sides
- 50 μm of Si + 16 μm of Si-equivalent (metal layer connecting RSUs) $\rightarrow 0.075\% X/X_0$ at $cos(\theta) = 0$. Factor 4 improvement!

Layer 1 layout

Layer 1+2

Layer 1 (classic vertex)

Ultra-light layer 1

Armin Ilg (UZH) Status of FCC-ee vertex detector layouts MAPS for FCC-ee vertex detectors 01.07.2024 16 / 23

➢Next steps:

- ➢Expressions of Interest in preparation
- ➢Couple DRD3 and DRD7 activities with ALICE 3 MAPS development

Thank you for your attention!

Backup

ALICE Upgrades' motivations and requirements

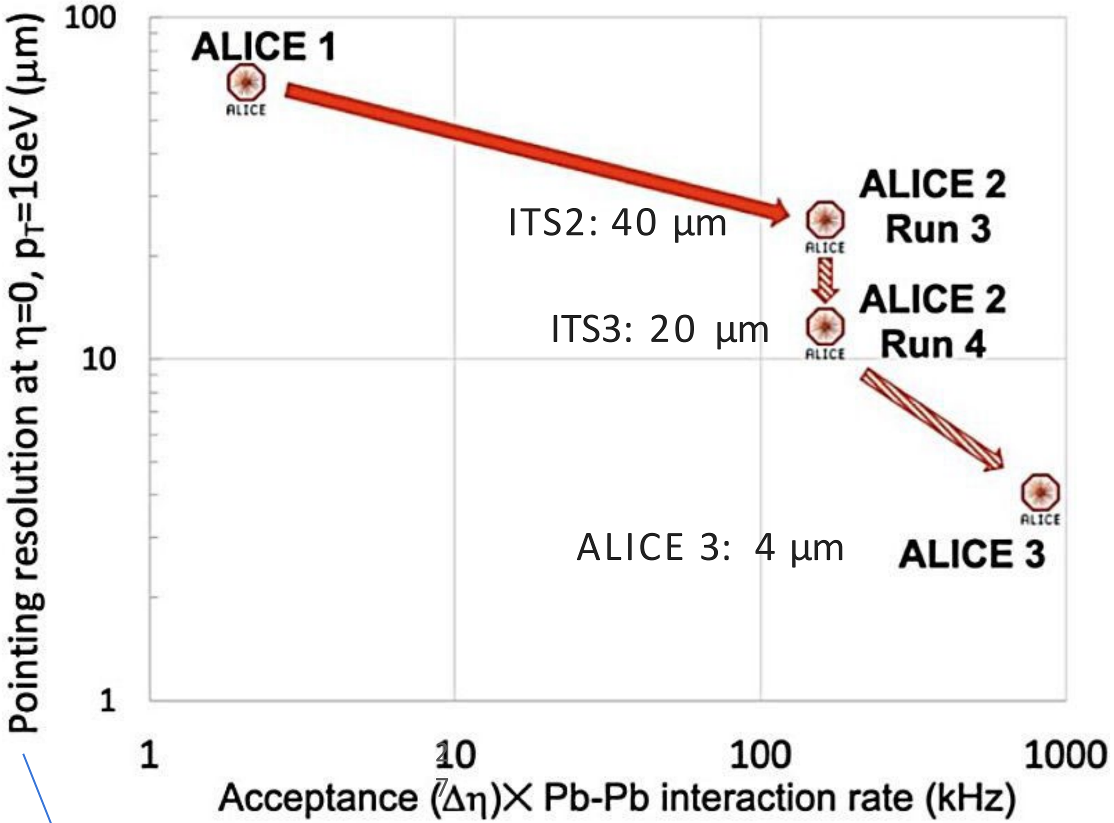
Physics Motivations:

Study of QGP in ultra-relativistic heavy-ions collisions → search for rare, low momentum probes, reconstruction of displaced decay topologies:

- Heavy flavour hadrons at low p_T
- Thermal dileptons
- Precision measurements of light (hyper)nuclei and searches for charmed hypernuclei

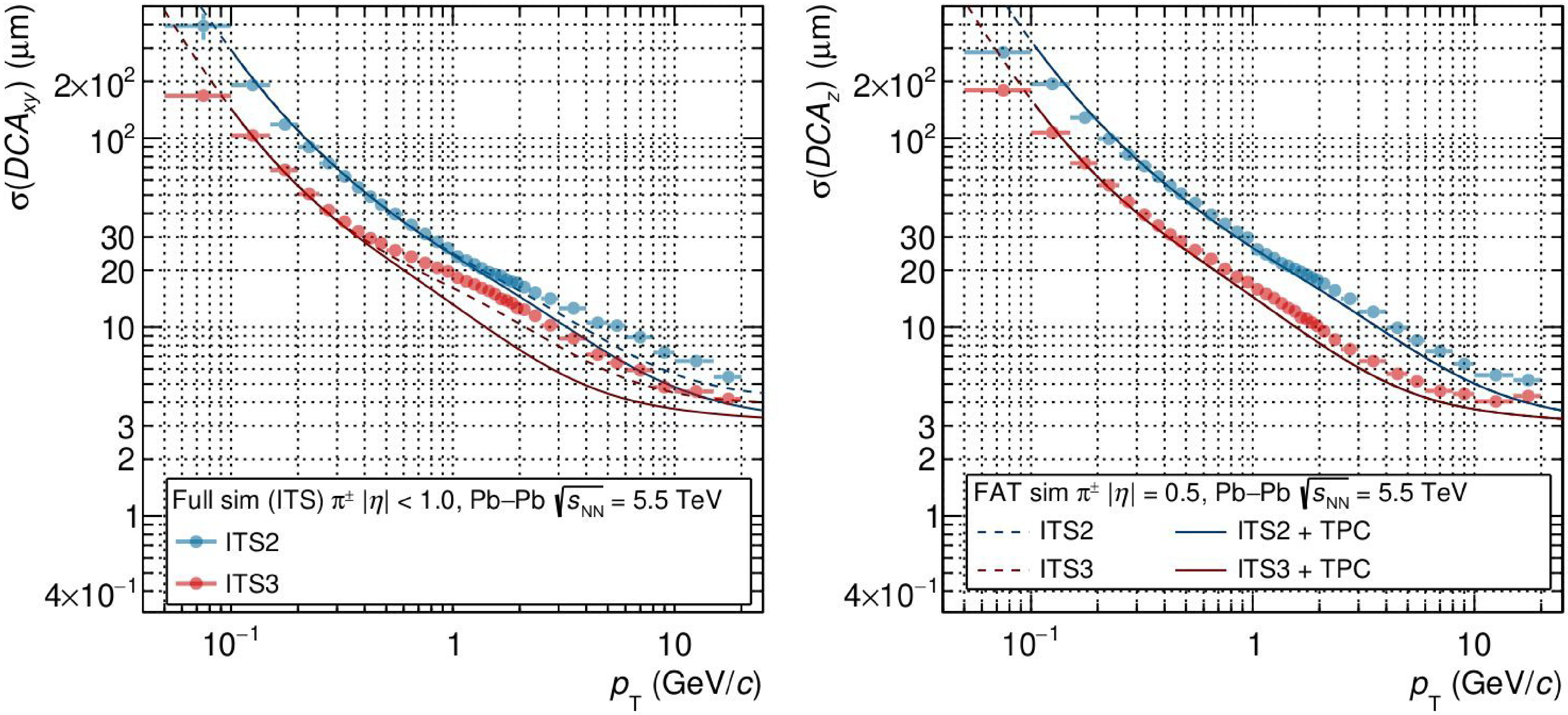
Tracker upgrade requirements:

- Increase of effective acceptance (acceptance x readout rate)
- Improve tracking and vertexing performance low p_T for combinatorial background suppression
  →Excellent **spatial resolution**, minimal **inner radius** and low **material budget** are needed

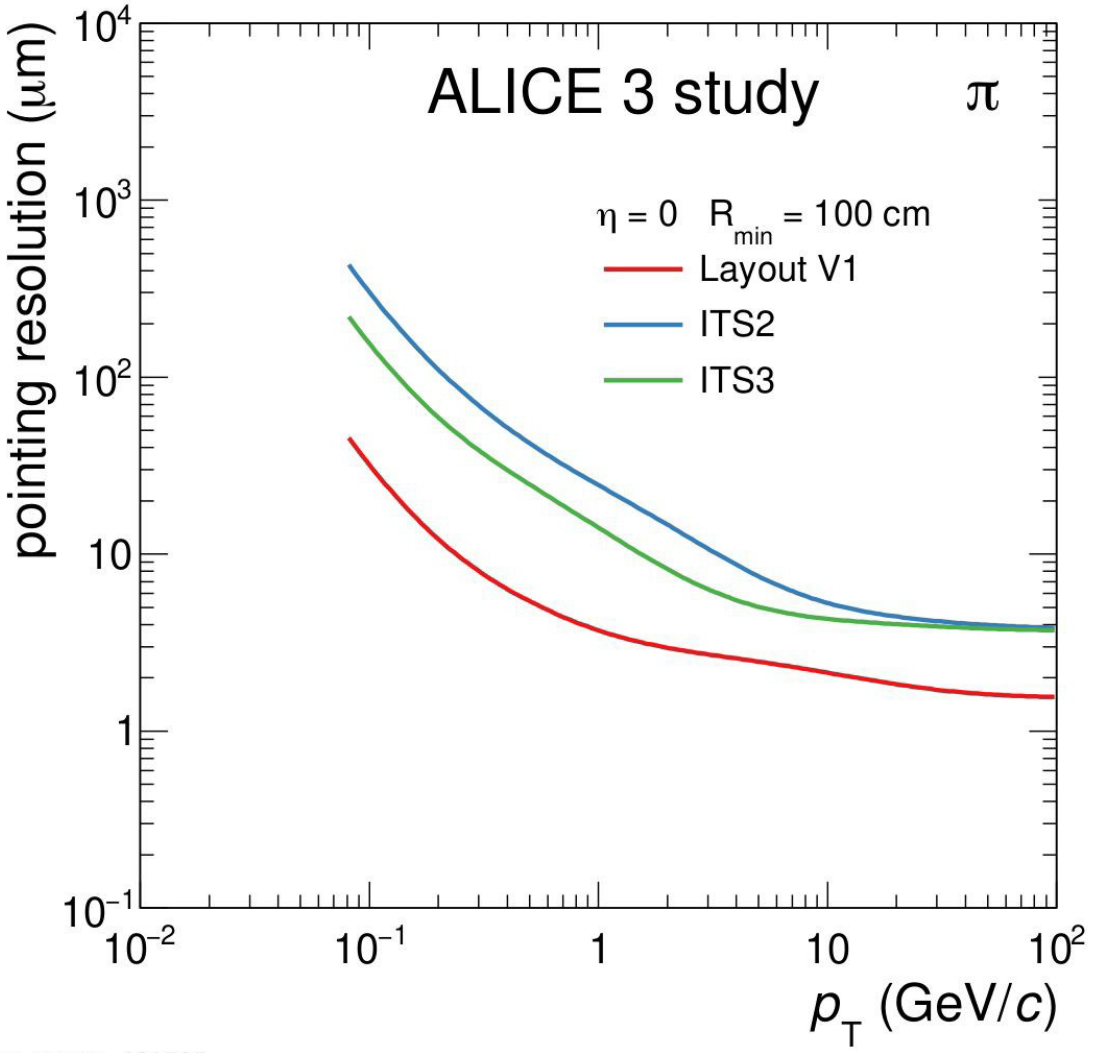


$$\sigma_{DCA} \approx A\,\sigma_{xyz} \oplus B\,\frac{r_0}{p}\sqrt{\frac{X}{X_0}}\cosh\eta$$

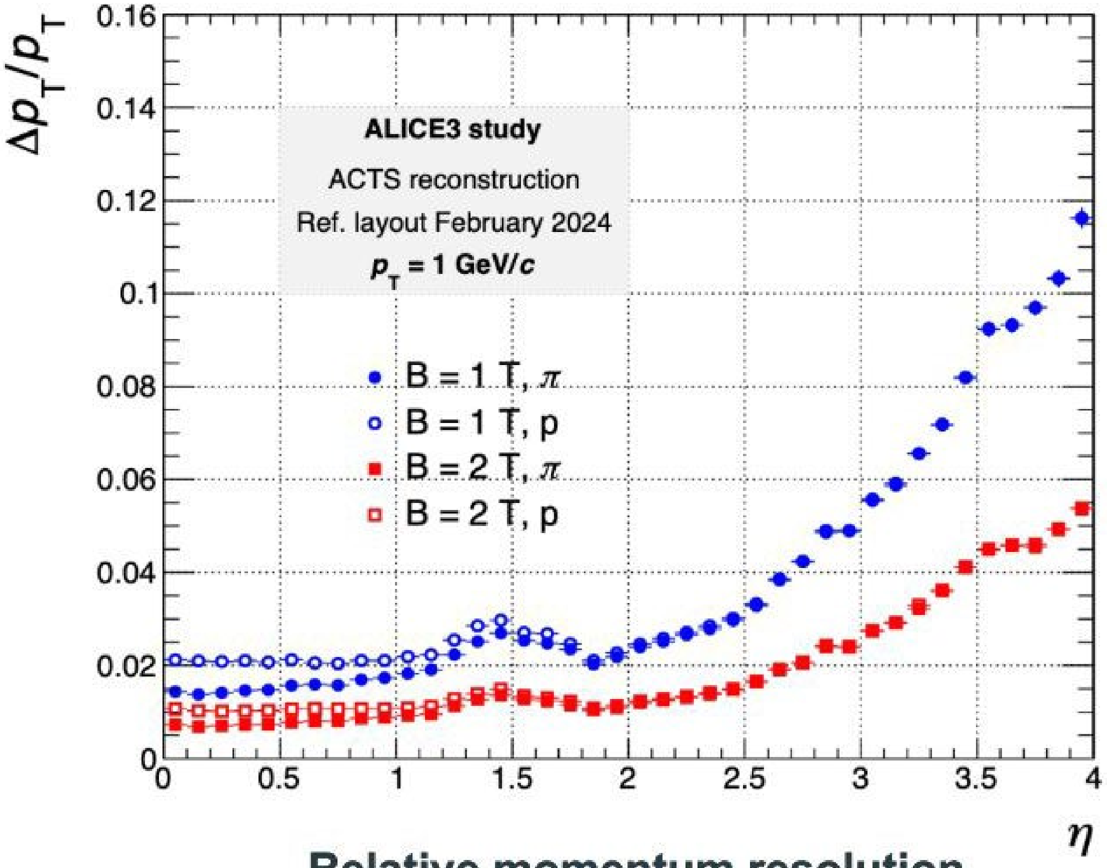
ITS3 pointing resolution



ALICE 3 tracking performance



ALI-SIMUL-491785



Relative momentum resolution

65 nm CMOS process validation and radiation hardness

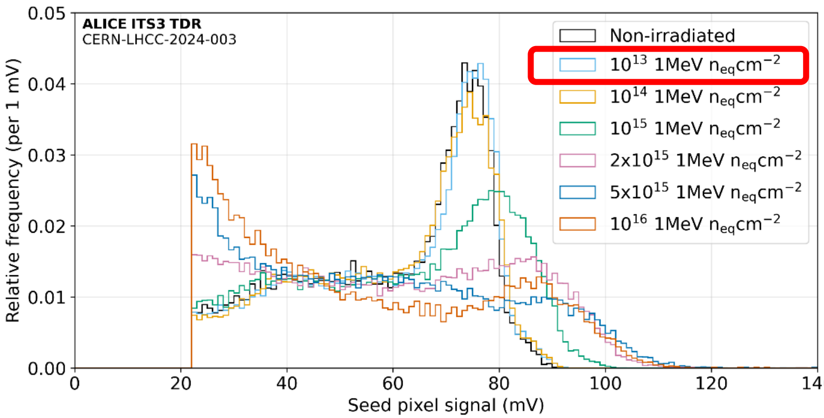
TPSCo **65 nm CMOS process validated** on MLR1 test structures:

INFN Trieste

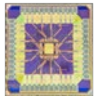
FCC-ee

$\sim 6 \times 10^{12}$ 1MeV neq $/\mathrm{cm}^2/$year

- Efficient charge collection
- Radiation hardness demonstrated beyond **10 kGy + 10^{13} 1MeV n_{eq} cm^{-2}** *ITS3 requirement*
  - Still efficient with 10^{15} 1MeV n_{eq} cm^{-2} at room temperature



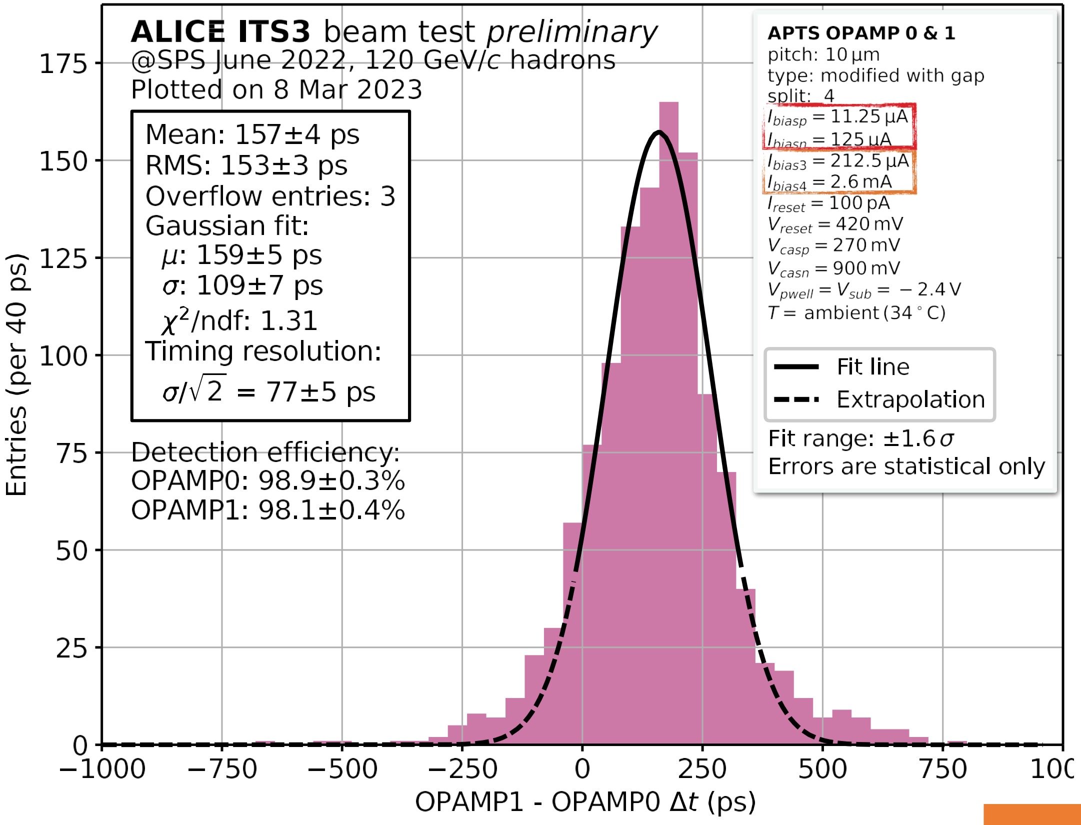
APTS



Seed **pixel signal response to ^{55}Fe** Vs irradiation levels, as measured on 15 μm pitch **Analog Pixel Test Structures (APTS)**

ITS3 sensor performance: intrinsic time resolution

Sensor only



~80 ps timing resolution

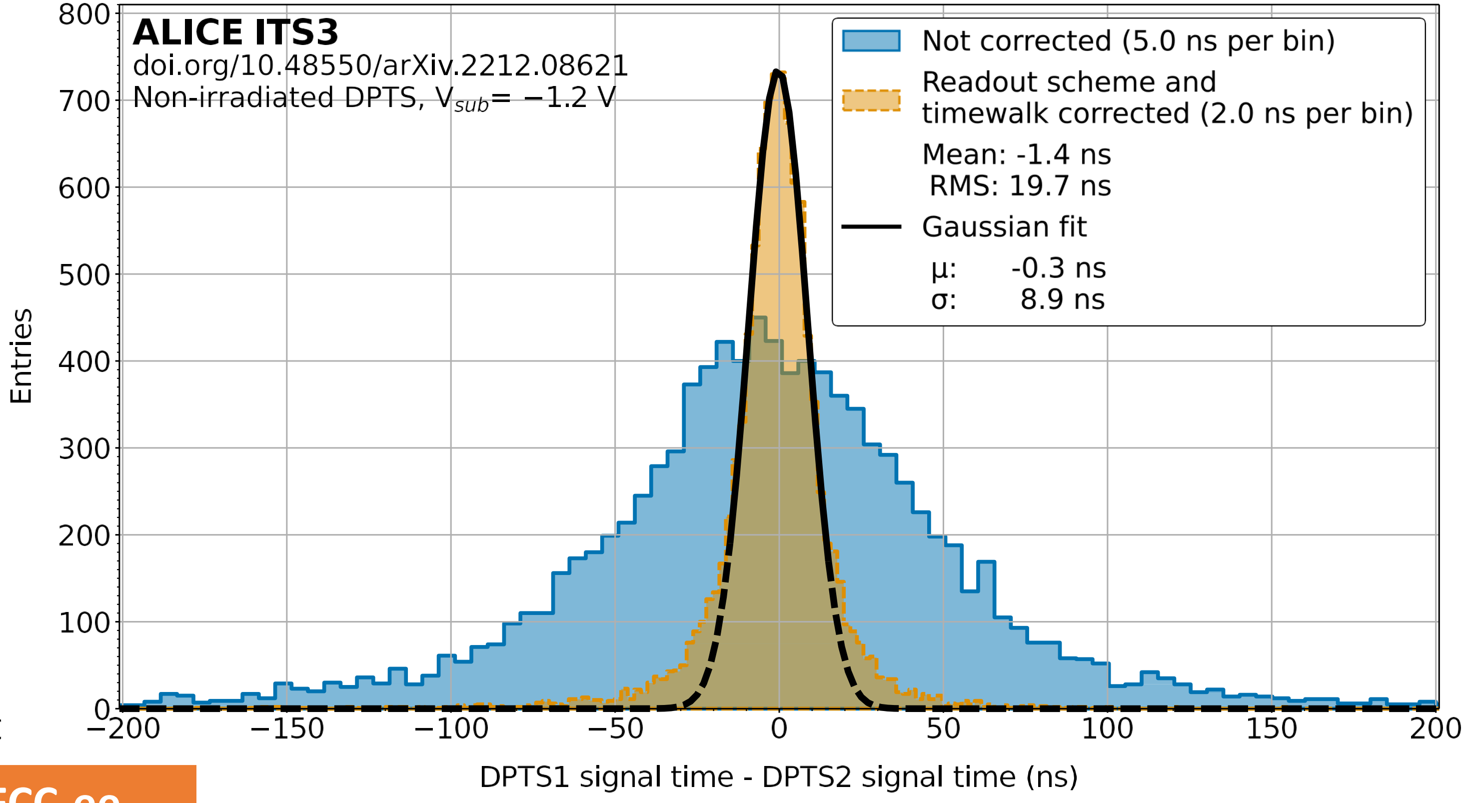
~3 µW in-pixel

~3 mW in-chip

FCC-ee

~ 20 ns RMS

With front-end



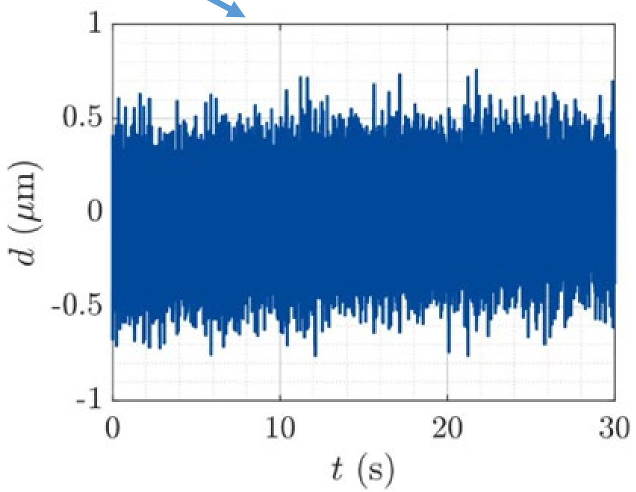
~6 ns timing resolution

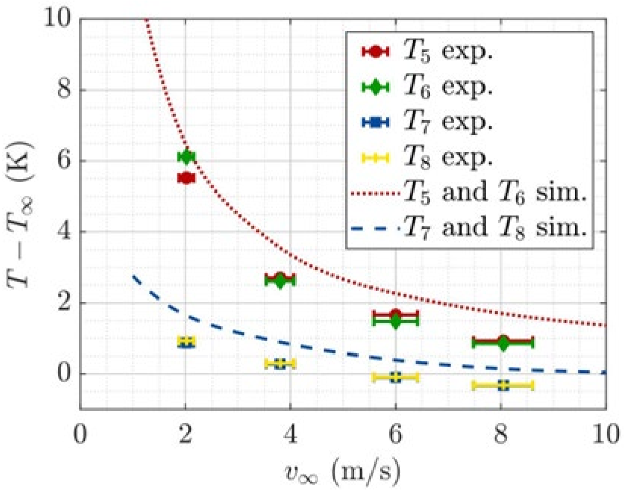
(~30 ns not corrected)

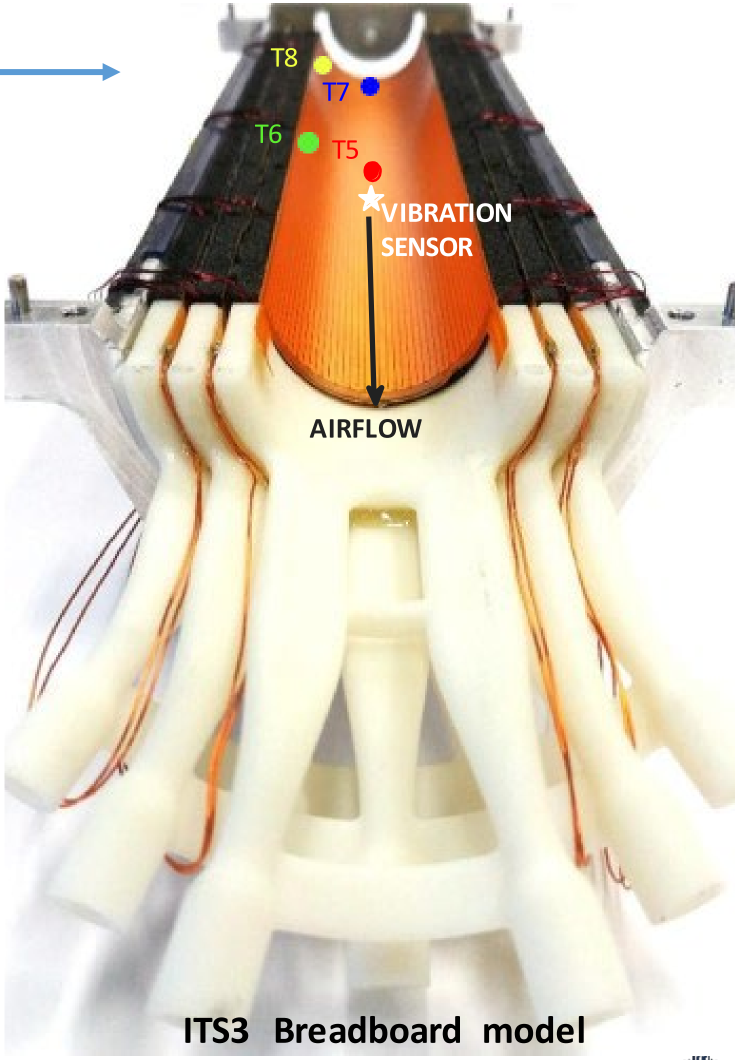
~120 nW in-pixel

ITS3 air cooling studies

- **Tests in wind tunnel** on breadboard model
  - Dummy silicon sensor with copper serpentine heater
  - Thermal load: 25 mW cm^{-2} in matrix, 1000 mW cm^{-2} in end-caps
- **Temperature difference** from inlet and within the sensor **< 5°C with 8 m/s airflow** between the layers
- Mechanical assembly with carbon foam half rings keeps **vibrations within ± 0.5 µm** with 8 m/s airflow







ITS3 Breadboard model

ALICE 3 Middle Layers and Outer Tracker

60 m^2 of silicon

  - 8 barrel layers (3.5 cm < radius < 80 cm)
  - 2 x 9 end-cap disks
- Material budget: 1% X_0/layer
- Position resolution: 10 μm (~ 50 μm pixel pitch)
- **Low power consumption < 20 mW/cm^2**
- **100 ns time resolution** to mitigate pile-up

Main R&D challenges:

- Module design for **industrialized production**
- **Low power consumption** while preserving timing performance