Contribution ID: **101** Type: **Parallel talk**

Using AI on FPGAs for the CMS Overlap Muon Track Finder for the HL-LHC

In view of the HL-LHC, the Phase-2 CMS upgrade will replace the entire trigger and data acquisition system. The L1T system has been designed to process 63 Tb/s input bandwidth with state-of-the-art commercial FPGAs and high-speed optical links reaching up to 28 Gb at a fixed latency below 12.5 μs. In view of the upgraded trigger system and in preparation for the HL-LHC, a GNN has been trained to reconstruct displaced muon signatures in the transition region between barrel and endcap and its implementation in FPGAs within the strict latency requirements imposed by the system will be discussed in this presentation. The process of adapting such machine learning models to hardware will also be described in detail. Additionally, other recent muon reconstruction algorithms developed for the HL-LHC will be reviewed.

AI keywords

FPGAs;real-time signal identification,ultra fast processing

Primary author: SPEAKER, CMS

Presenter: SPEAKER, CMS

Track Classification: Real-Time Data Processing