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Pulse pile-up reconstruction using 1D-CAE for signal discrimination in nuclear experiments

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Abstract

Pulse pile-up in detection systems can degrade energy and time resolution, especially in high-rate environments. While traditional rejection methods discard overlapping events, some of these signals may still contain valuable physical information. We present a novel reconstruction method based on a one-dimensional convolutional autoencoder (1D-CAE), trained on data acquired for our first experience, from the Neutron Detector Array (NEDA). This method reconstructs pile-up events, allowing further analysis such as Pulse Shape Analysis (PSA) neutron-gamma discrimination using the Charge Comparison method (CC). As part of ongoing work, we have executed the model on a 32-bit microprocessor and are currently implementing the solution on FPGA hardware. Using the HLS4ML library, we have generated a hardware IP core, although successful simulation of the IP remains an open task. These developments aim to enable real-time, on-detector pulse reconstruction in future high-throughput experiments.

Introduction

Building on previous work on pulse pile-up reconstruction[1], the objective is to implement this reconstruction model in FPGA hardware for real-time processing. Although originally developed for NEDA[2], the approach is relevant for other detectors using PSA, such as GRIT[3].

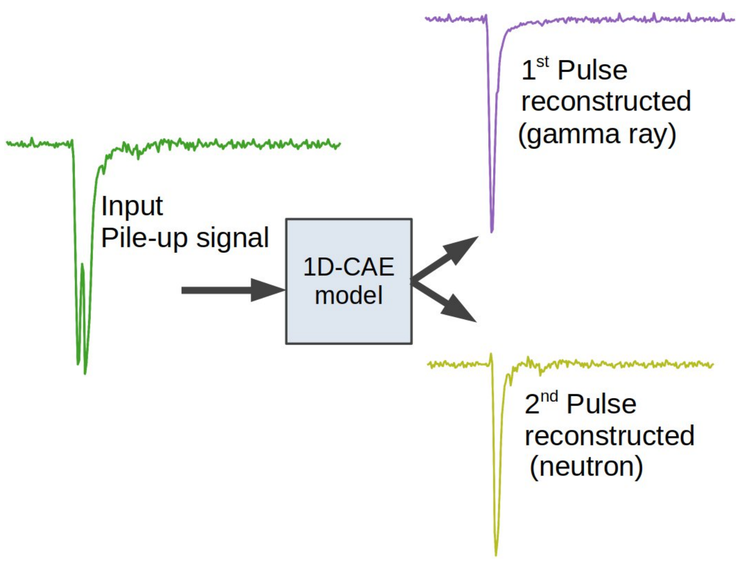

Figure 1. Example of using 1D-CAE trained model for the reconstruction of pile-up signals from detector.

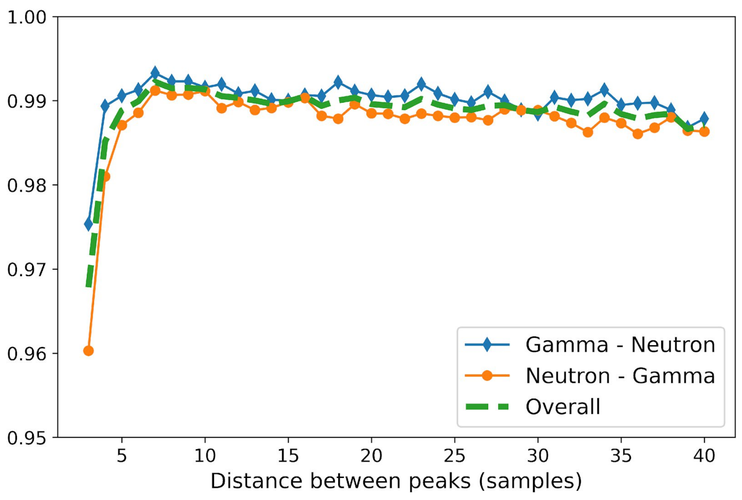

Figure 2. Correlation coefficient between original and reconstructed signals depending on the distance between pulses. Average correlation between original signal and reconstructed signal of 0.988.

Real-Time pulse pile-up reconstruction

The trained model has been successfully deployed on a Raspberry Pi using TensorFlow Lite, demonstrating real-time inference on a mini PC. Current work focuses on FPGA implementation using the HLS4ML[4,5] library to generate synthesizable HDL code. As an intermediate step, model inference has already been achieved with HLS4ML libary, paving the way for full integration on the Xilinx ZCU104 board with a UltraScale+ FPGA.

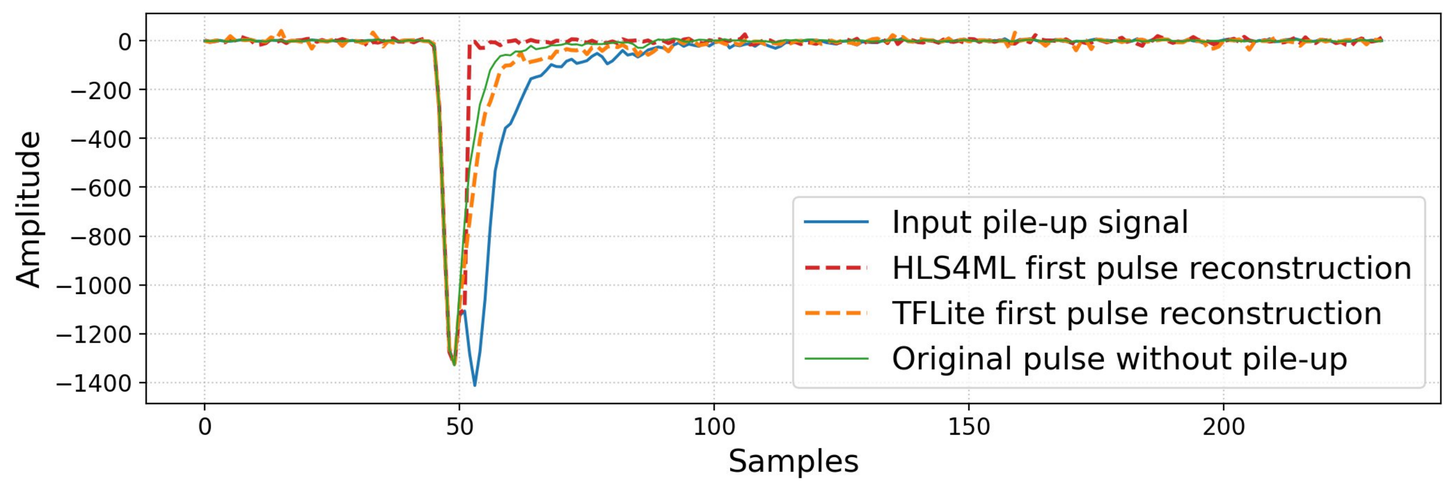

Figure 3. Output signals reconstructed with TFLite and HLS4ML model.

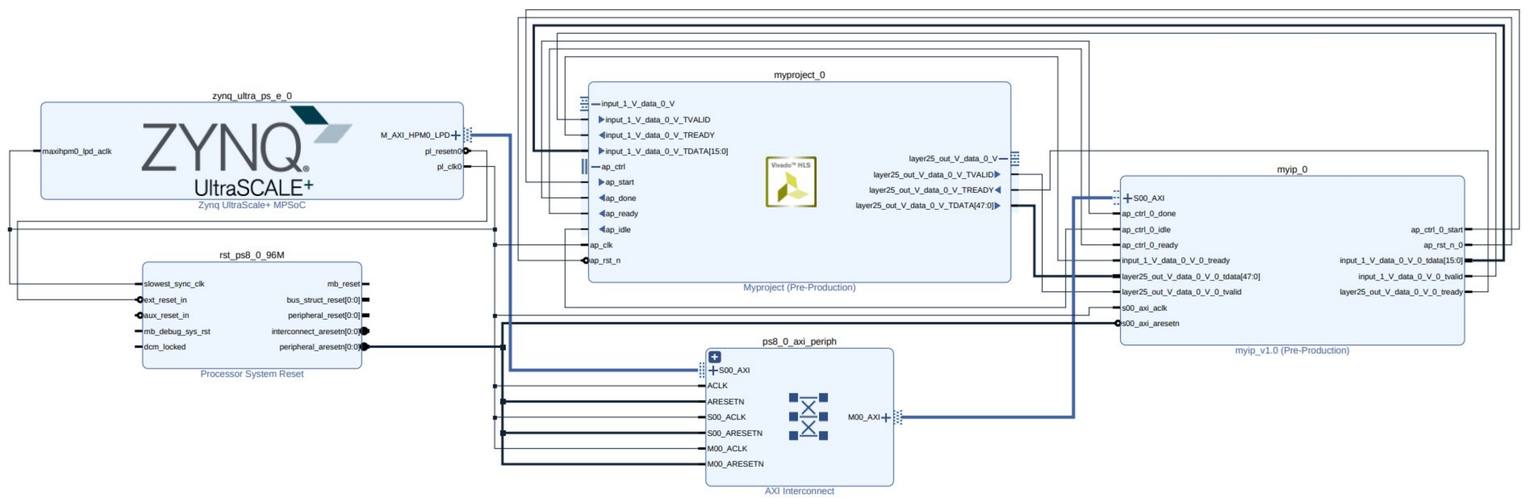

Figure 4. Block diagram of the implementation in Xilinx ZCU104 board with UltraScale+ FPGA.

Problems encountered

- **Single Output in HLS4ML:** Limited to one output, restricting model designs.
- **TensorFlow Layer Issues:** Some TensorFlow layers incompatible with HLS4ML conversion.
- **Linux-Only Support:** HLS4ML works only on Linux, not Windows.
- **Vivado Version Conflicts:** Incompatibilities between HLS4ML and some Vivado versions.
- **High Resource Use in RTL:** RTL conversion increases resource demands due to complex layers.

Conclusions

- Machine learning enables recovery of pile-up events in detectors like NEDA and GRIT
- The inference has been successfully demonstrated on a Raspberry Pi using TensorFlow Lite.
- FPGA implementation is in progress using HLS4ML, with model inference already achieved in HLS.
- This work represents a key step toward integrating real-time pile-up reconstruction into experimental data acquisition systems.

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