RD_FCC

Silicon and Gas Detector R&D for the IDEA

Manuel Rolo, Michela Greco,

on behalf of the **RD_FCC Torino.**

FUTURE CIRCULAR COLLIDER

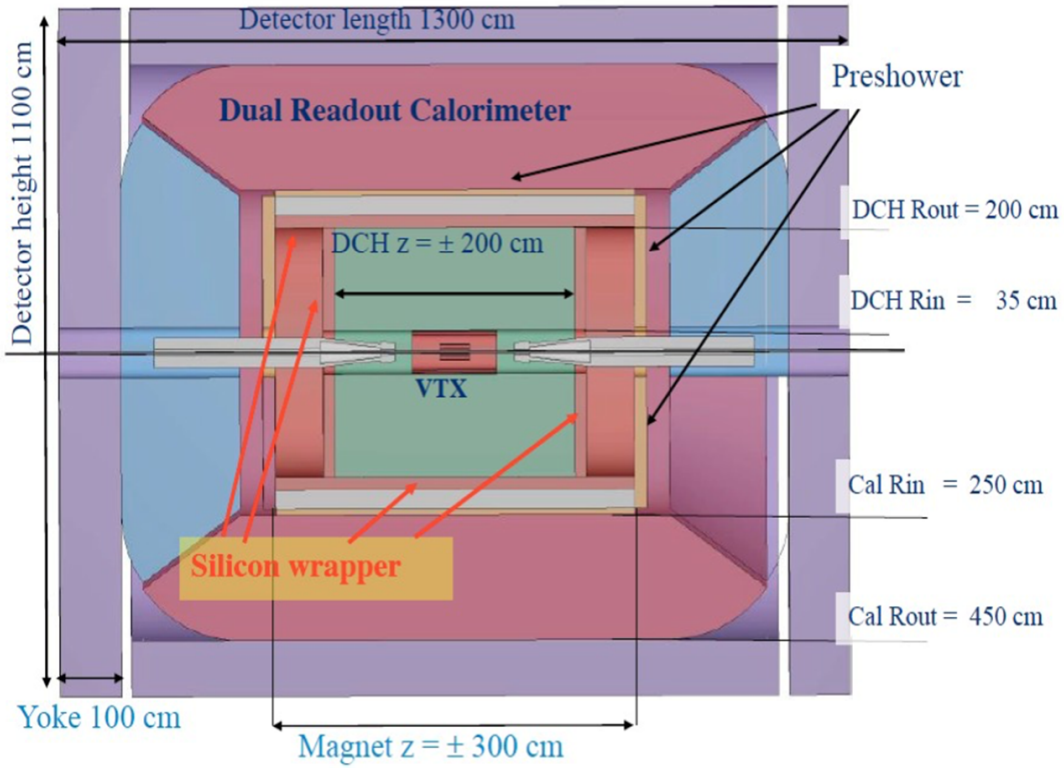
Discussione su

EU Strategy on Particle Physics

October 17th 2024, Torino

Innovative Detector for e+e- Accelerator

- **The Innovative Detector for e^+e^- Accelerator (IDEA) was originally proposed a detector concept for a large circular e^+e^- collider**
- **Could be an excellent choice for one of the FCC-ee IPs**



- Central tracking device:
  - light Drift Chamber
- Silicon detectors for precision measurements
  - inner vertex detector
  - outer vertex detector
  - silicon wrapper/TOF
- Thin solenoid with 2T field (according to MDI limits)
- Dual readout calorimeter
- Muon chambers in the solenoid return yoke
- Pre-shower and Muon system to be instrumented with μ-RWELL technology and custom ASIC

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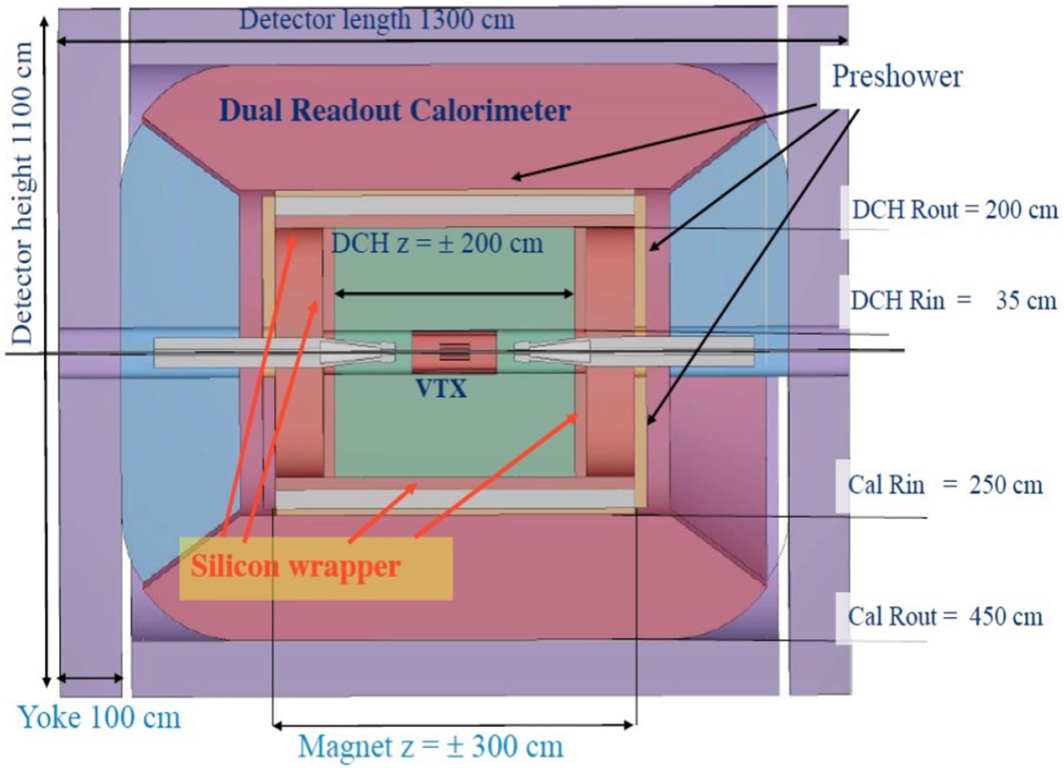

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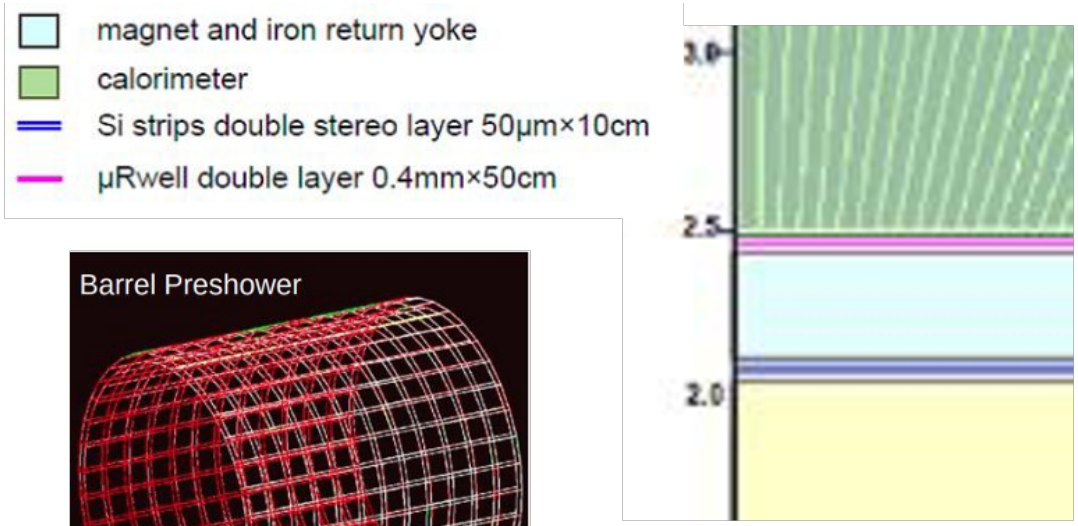
The IDEA pre-shower

BOLOGNA/FERRARA/LNF



High resolution after the magnet to maximise the energy resolution of the dual readout calorimeter and tag π0 and γ

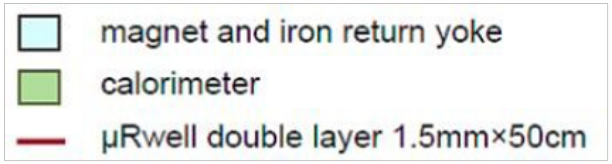
pitch = 0.4 mm
FEE capacitance = 70 pF

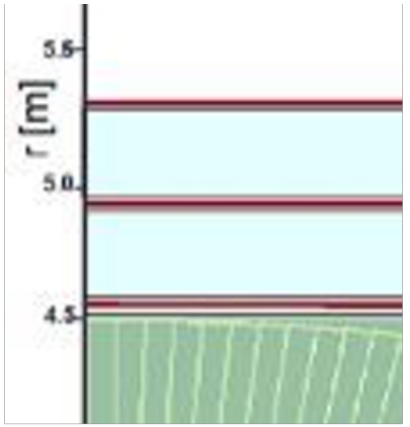
50x50 cm² 2D tiles to cover about 130 m²

- Efficiency > 98%
- Space Resolution < 100 μm
- 1.3 million channels: optimisation of FEE channels/cost

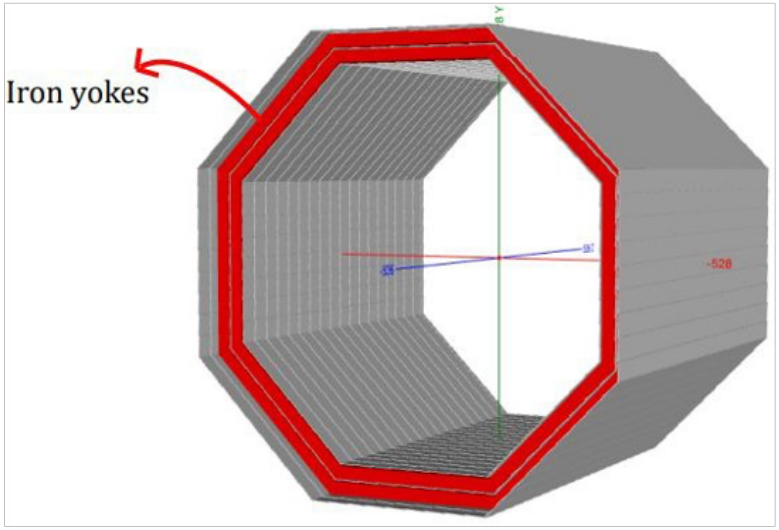
The IDEA muon detector

BOLOGNA/FERRARA/LNF





Reconstruct and tag the muon with three layers in between the iron return yoke and reconstruct LLP



pitch = 1.5 mm
FEE capacitance = 270 pF

- Efficiency > 98%
- Space Resolution < 400 μm
- 5 million channels: optimisation of FEE channels/cost

50x50 cm2 2D tiles to cover about 1525 m^2

The μ-RWELL technology

G. Bencivenni et al., 2015 JINST 10 P02008

The μ-RWELL is composed of only two elements:

- μ-RWELL_PCB amplification and resistive stage
- cathode defining the gas gap

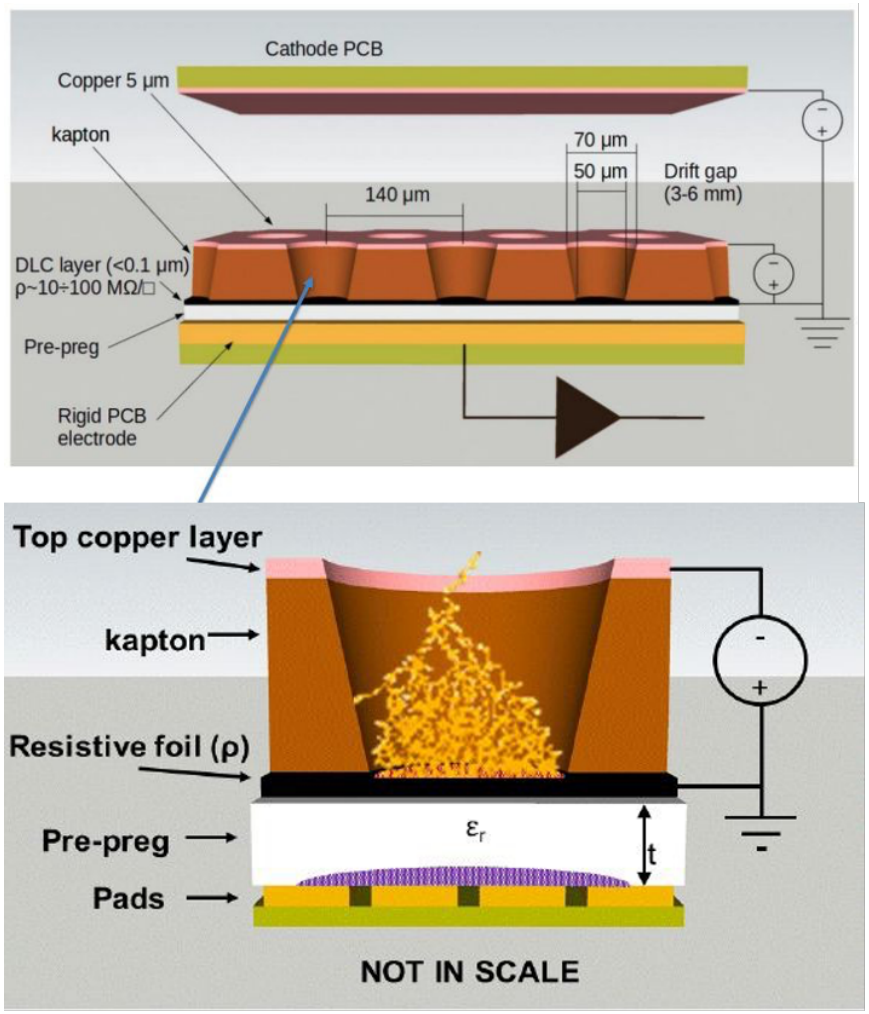
μ-RWELL operation:

1.A charged particle ionises the gas between the two detector elements

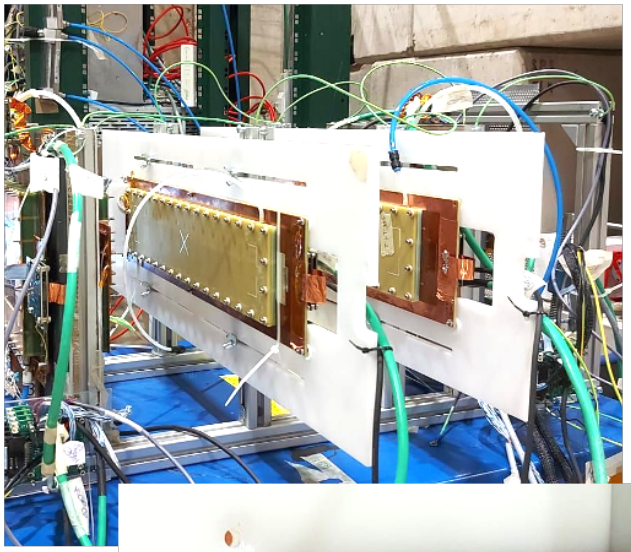
2.Primary electrons drift towards the μ -RWELL_PCB (anode) where they are multiplied, while ions drift to the cathode or to the PCB TOP

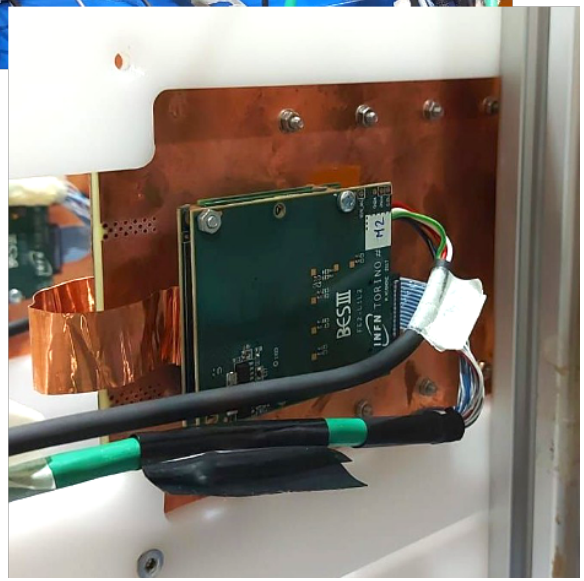
3.The signal is induced capacitively, through the DLC layer, to the readout PCB

4.only two HV for the drift region (cathode-drift wrt PCB TOP) and the amplification region (PCB TOP wrt resistive stage)



TIGER for μ-RWELL readout





Detector under test:

-4 μRWELL w/ 40 cm strip length
1D strip pitch of 0.4/0.8/1.2/1.6 mm

Readout under test, developed for the BESIII CGEM-IT

- TIGER FEE (INFN-TO)
- GEMROC FPGA (INFN-FE)

Goals of the testbeam:

-Define the state of art of μRWELL+TIGER for IDEA Muon system optimisation studies
-Compare the APV-25 performance studies with TIGER
-Performance in Ar:CO2 and Ar:CO2:CF4 comparison
-Collect data to compare experimental measurement and simulation

Measurements:

-Gain scan to evaluate the amplification/saturation/performance
-Drift scan to evaluate the signal collection
-Threshold scan to optimize S/N

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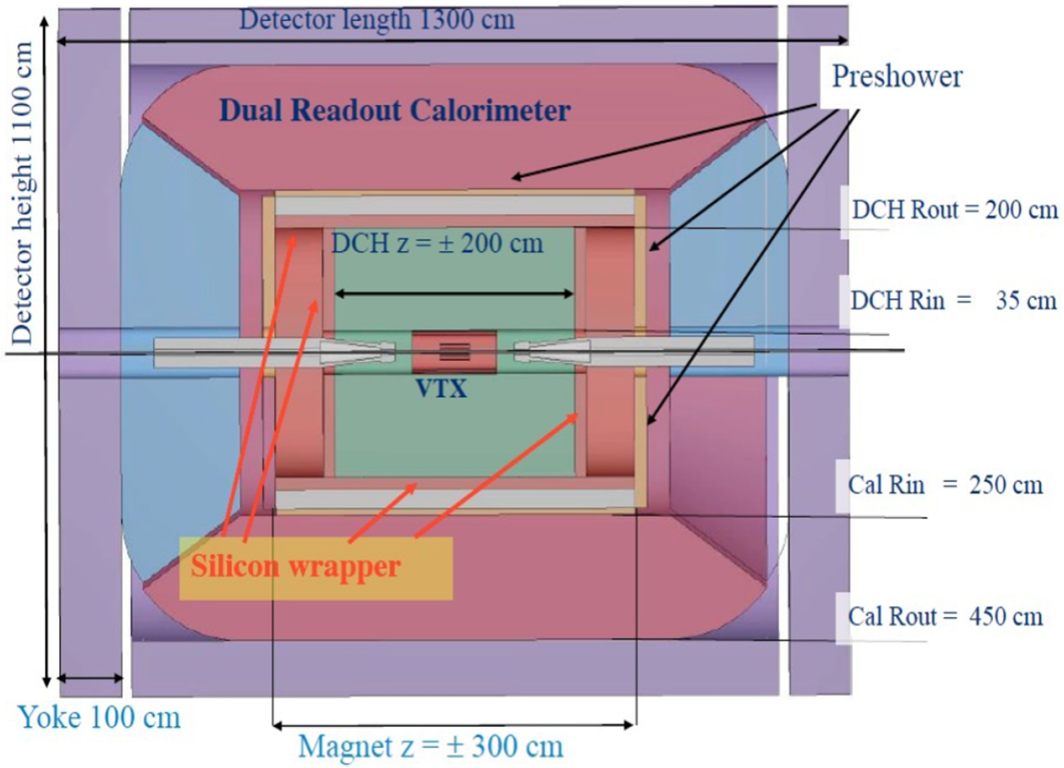

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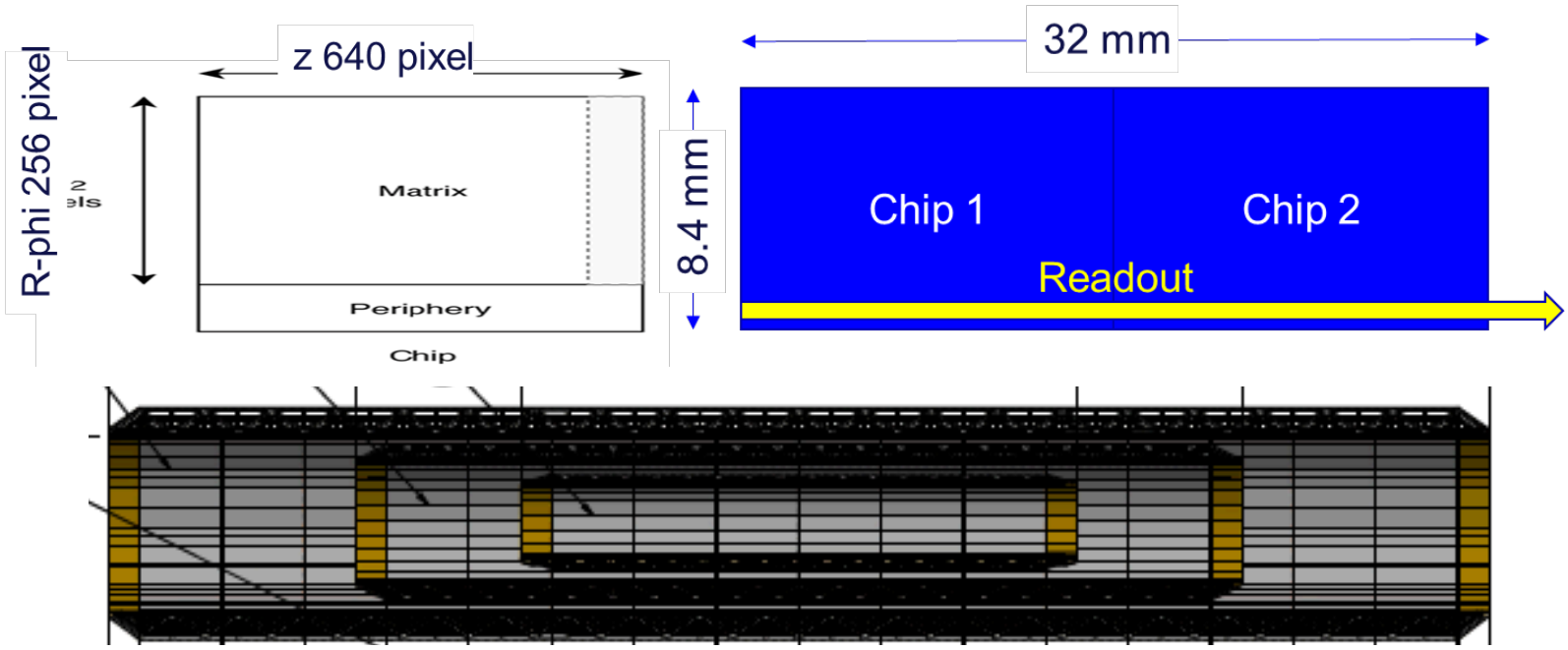
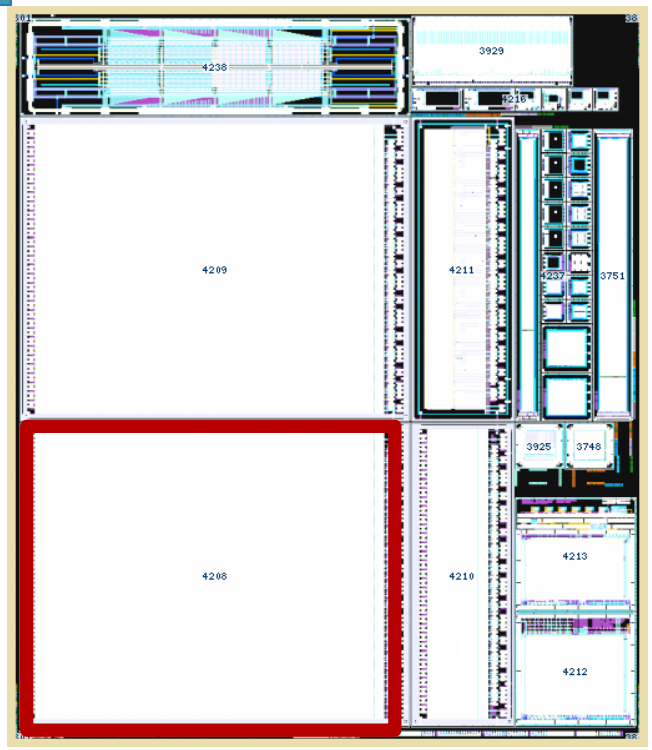
Inner Vertex Layout

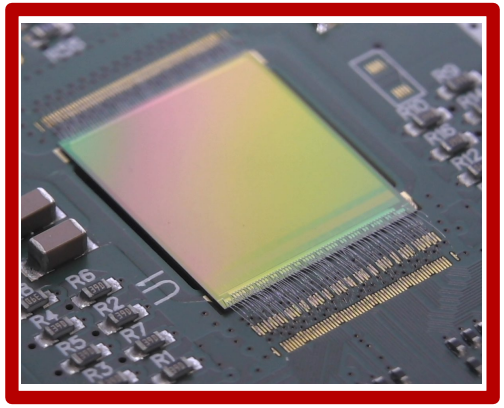


- Module based on ARCADIA MD3 layout
- 3 barrel layers: 13.7, 23.7, 34/35.6 mm radii
- Sensor loaded on thin carbon-carbon support and flex PCB for powering and readout
  - Alice/Belle2 like stave approach
- Light truss structure to provide mechanical rigidity to the stave

PERUGIA/PISA/LNF

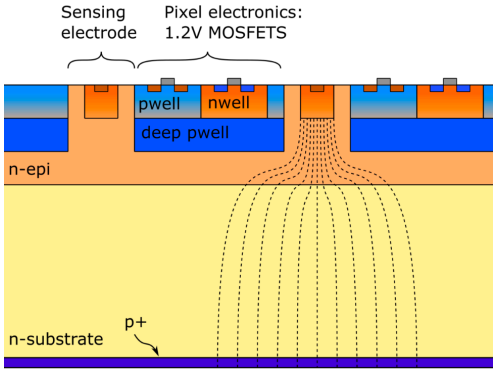
ARCADIA Technology demonstrators



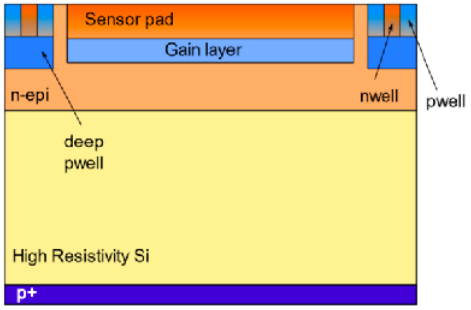


- ARCADIA-MD3 Main Demonstrator (512 x 512 pixels)
- MAPS and test structures for PSI (CH)
- MATISSE Low Power (ULP front-end for space instruments)
- pixel and strip test structures down to 10µm pitch
- ASTRA 64-channel mixed signal ASIC for Si-Strip readout
- 32-channel monolithic strip and fully-functional readout electronics
- (ER2) HERMES: small-scale demonstrator for fast timing
- (ER3) Small-scale demonstrator of a X-ray multi-photon counter
- (ER3) Wafer splits with timing layer, new R&D towards <<50 ps timing performance: test structures and
- (ER3) MADPIX: multi-pixel active demonstrator chip for fast timing

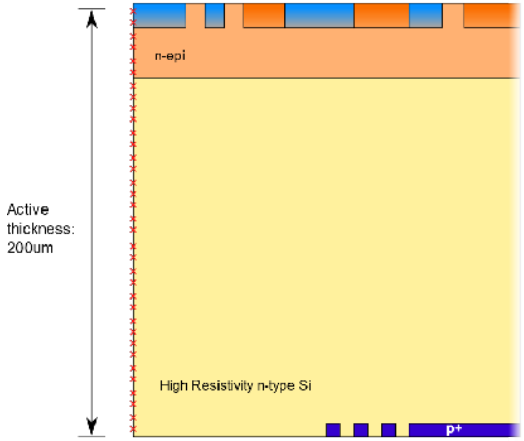
ARCADIA Sensor Concepts



- n-type high resistivity active region + n-epi layer (reduces punch-through current between p+ and deep pwells)
- sensing electrodes can be biased at low voltage (< 1V)
- BSI Reverse-biased junction: depletion grows from back to top
- Ongoing R&D: Fully Depleted PAD sensors with gain layer



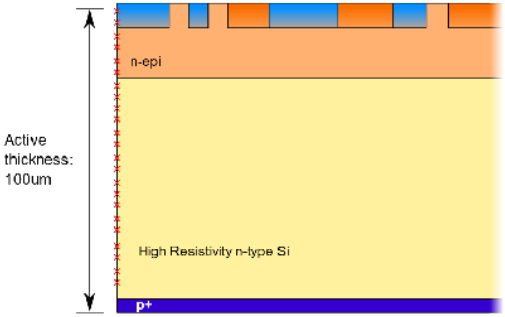
HR wafers - backside litho



Masked backside implantation

- thinning, lithography, backside p+ implantation and laser annealing, insulator and metal deposition to create backside guardring structures

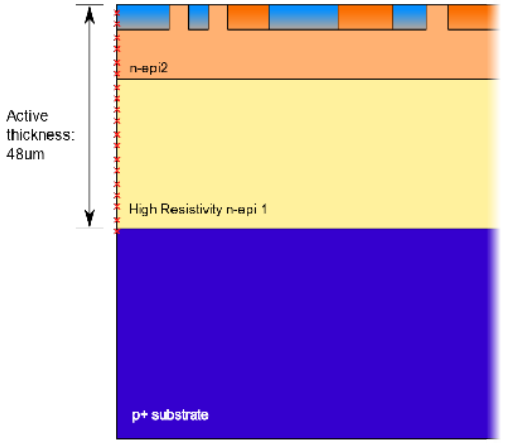
HR wafers - no backside lithio



Maskless backside implantation

- thinning, backside p+ implantation and laser annealing, no patterning on backside

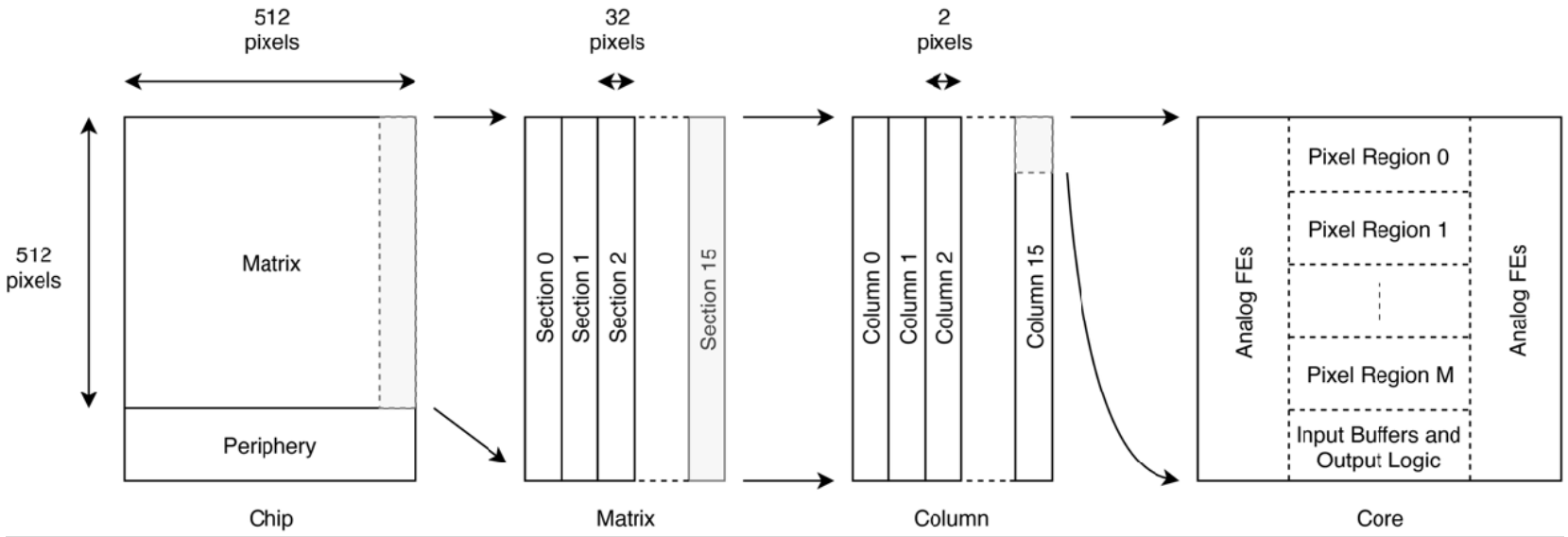
p+ wafers - double epi



Total thickness: 300um

- thinning down to 100μm total thickness on a p+ starting substrate, active thickness below 50μm

ARCADIA-MD3: Chip Architecture

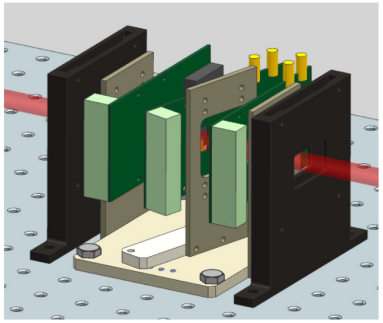


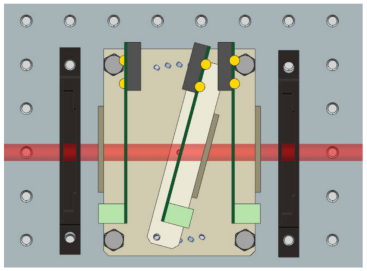
A. Paternò, S. Garbolino

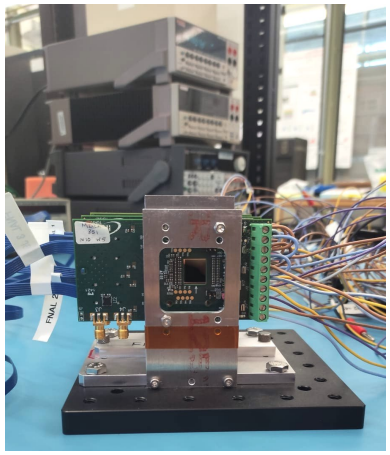
- Pixel size 25 µm x 25 µm, Matrix core 512 x 512, 1.28 x 1.28 cm^2 silicon active area, "side-abuttable"
- Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
- Event rate up to 100 MHz/cm^2 (design post-layout simulations)
- High-rate operation (16 Tx): 17-30 mW/cm^2 depending on transceiver driving strength (measured)
- Low-power operation (1 Tx): **10 mW/cm^2** (all data conveyed in 1 transceiver, others turned-off)

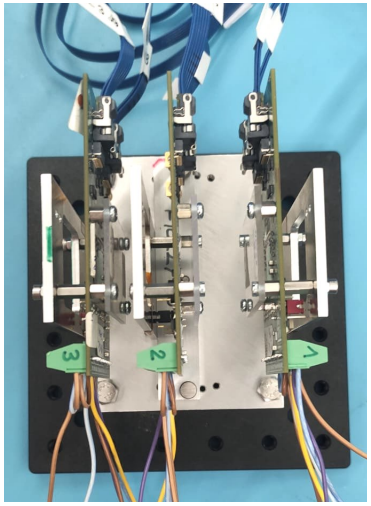
Test beam with ARCADIA-MD3

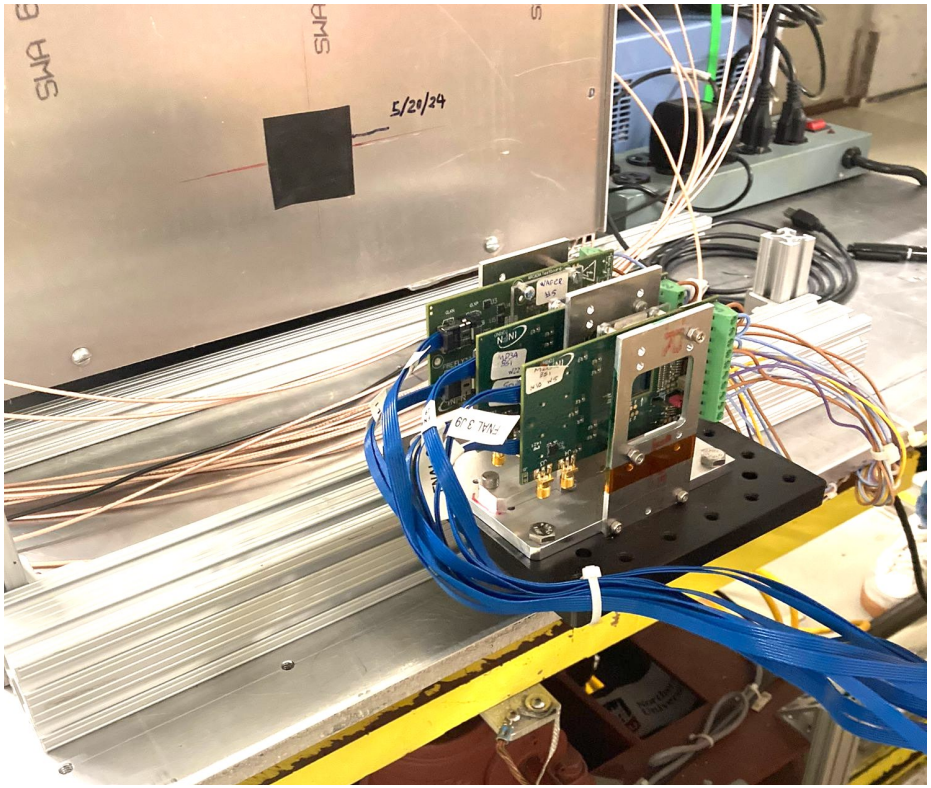
- Test beam at FNAL (120 GeV protons): very good results from data analysis ongoing
- mini-telescope with 3 ARCADIA-MD3 sensors
- Threshold, sensor HV and incidence angle parametrisation: study of cluster size, collection efficiency, spatial resolution







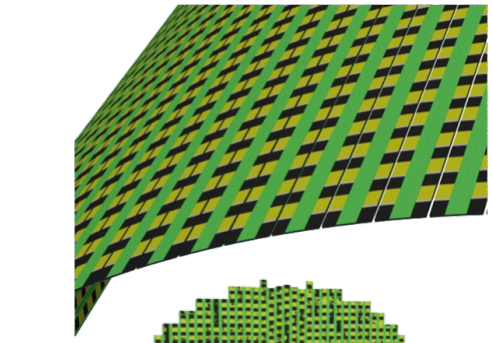




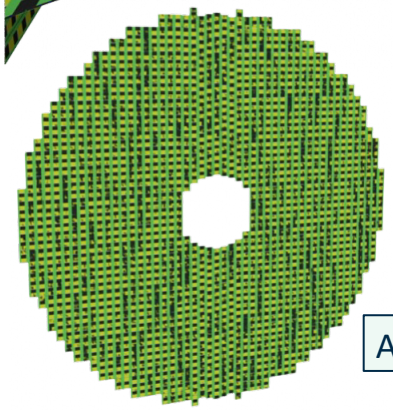
Si Wrapper

- **Precision silicon layer around the central tracker**
  - improve momentum resolution
  - extend tracking coverage in the forward/ backward region by providing an additional point to particles with few measurements in the drift chamber
  - precise and stable ruler for acceptance definition
  - *it may provide TOF measurement*

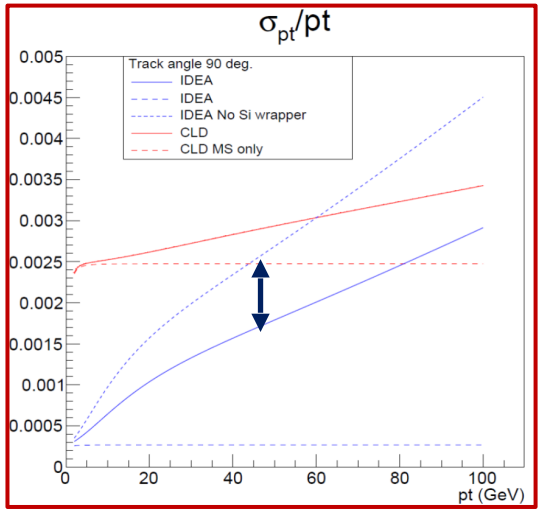
- Covered area ~100 m²
  - important impact on services
  - technology suitable for large size production



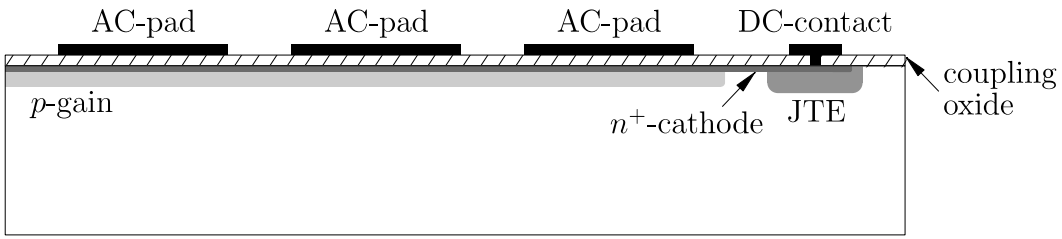
Endcap

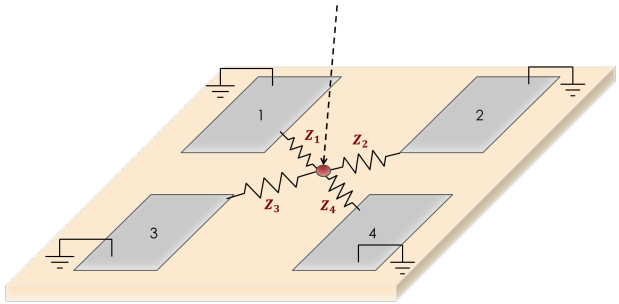


A. Ilg's



Si Wrapper: RSD option





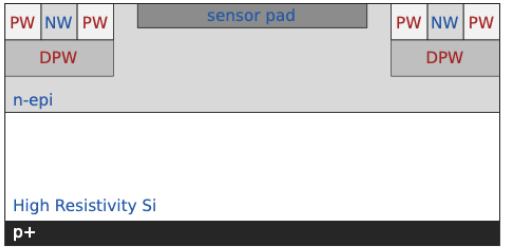
More info on RSD: project, 10.48550/arXiv.2003.04838, 10.1016/j.nima.2021.165319

- LGAD detector with continuous gain layer, charge collection through resistive n-layer and readout by induction on AC coupled pads, for a
- fully active detector, avoiding inefficient regions due to the insulation between pixels in LGAD sensors
- Sharing is deterministic (in low pitch pixel detectors sharing is dominated by Landau fluctuations)
- Timing resolution approximatively independent from pixel pitch
- CMOS integration of the LGAD technology already demonstrated (in LF11is) with the ARCADIA project
- Up next for CMOS AC-LGAD: Demonstrate the compatibility between the RSD readout scheme and the CMOS process flow

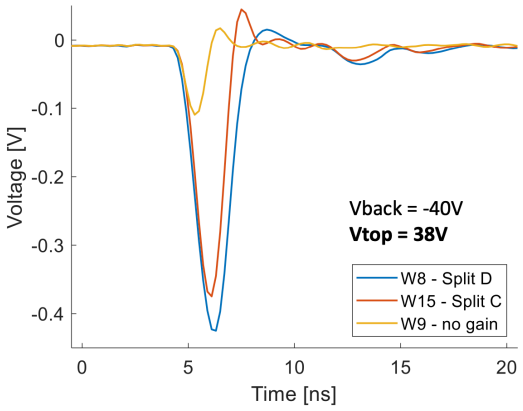
Monolithic CMOS LGAD technology

M. Mandurrino

development of fully-depleted MAPS

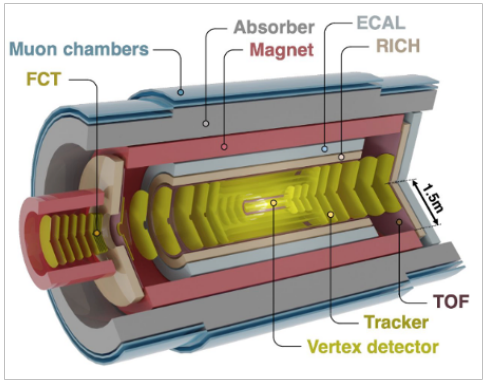


Standard 110 nm CMOS process at **LFoundry**



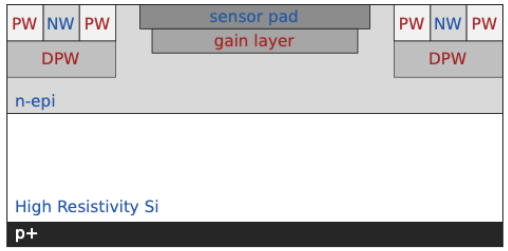
ALICE3 TOF detector:

- high-resolution **tracking**
- **particle ID** with low $p_T \Rightarrow \sigma_t \sim 20$ ps

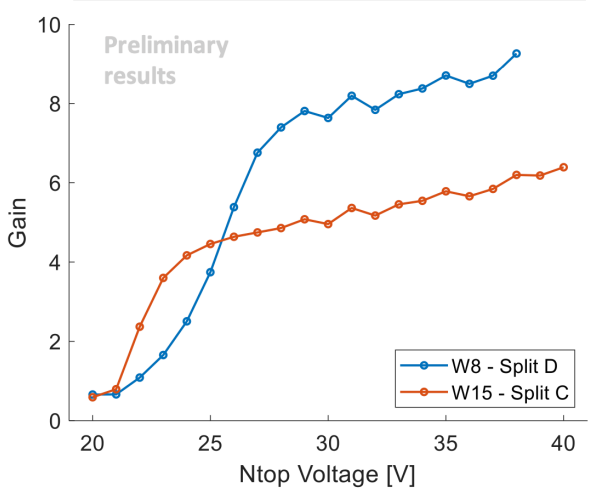


First results on monolithic CMOS detector with internal gain:
https://indico.cern.ch/event/1415726/contributions/6144007/attachments/2942716/5170665/Pancheri_ALICE_UpgradeWeek_8Oct2024_v2.pdf

CMOS-LGAD



Add-on ***p*-gain** implant (**gain target: 10 – 30**)



- Add-on p-gain implant underneath the n+ collecting electrode to push the timing performances
- Productions on ARCADIA-ER3 (25 wafers), ER4 (16 wafers) and ER5 (TB ongoing, 16 wafers)
- Gain layer implemented (5-15) with very good matching with TCAD simulation framework

Open items and Outlook

Attilio Andreazza (MI)

- **Inner vertex**
  - Improve readout rate and speed of ARCADIA architecture
  - On-chip intelligence to suppress background hits
  - Improvement on services layout
  - Option: Development of curved layout (based on TPSCo technology)
- **Outer vertex**
  - Design of endcap disks, optimisation of module sizes
  - Integrate missing features: chip-to-chip data transfers, serial powering, command decoder…
- **Silicon wrapper**
  - Mechanical layout still need to be defined
  - Define where timing is needed:
    - forward region may have low number of drift chamber hits for dE/dx measurement

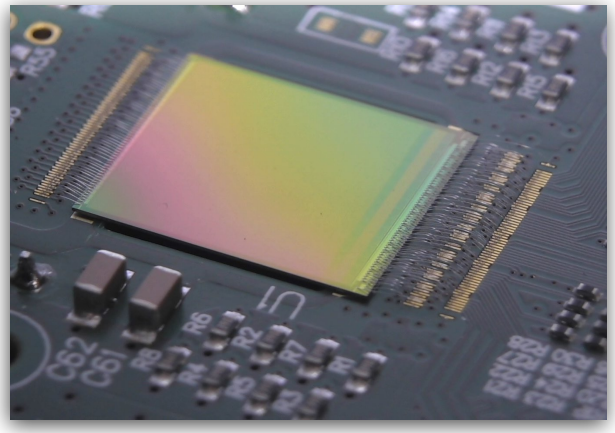
Plenty of fascinating electronic design and sensor development will be needed to arrive to build a state-of-art detector within the time scale of future e^+e^- factories

LF11is FDMAPS development through DRD7

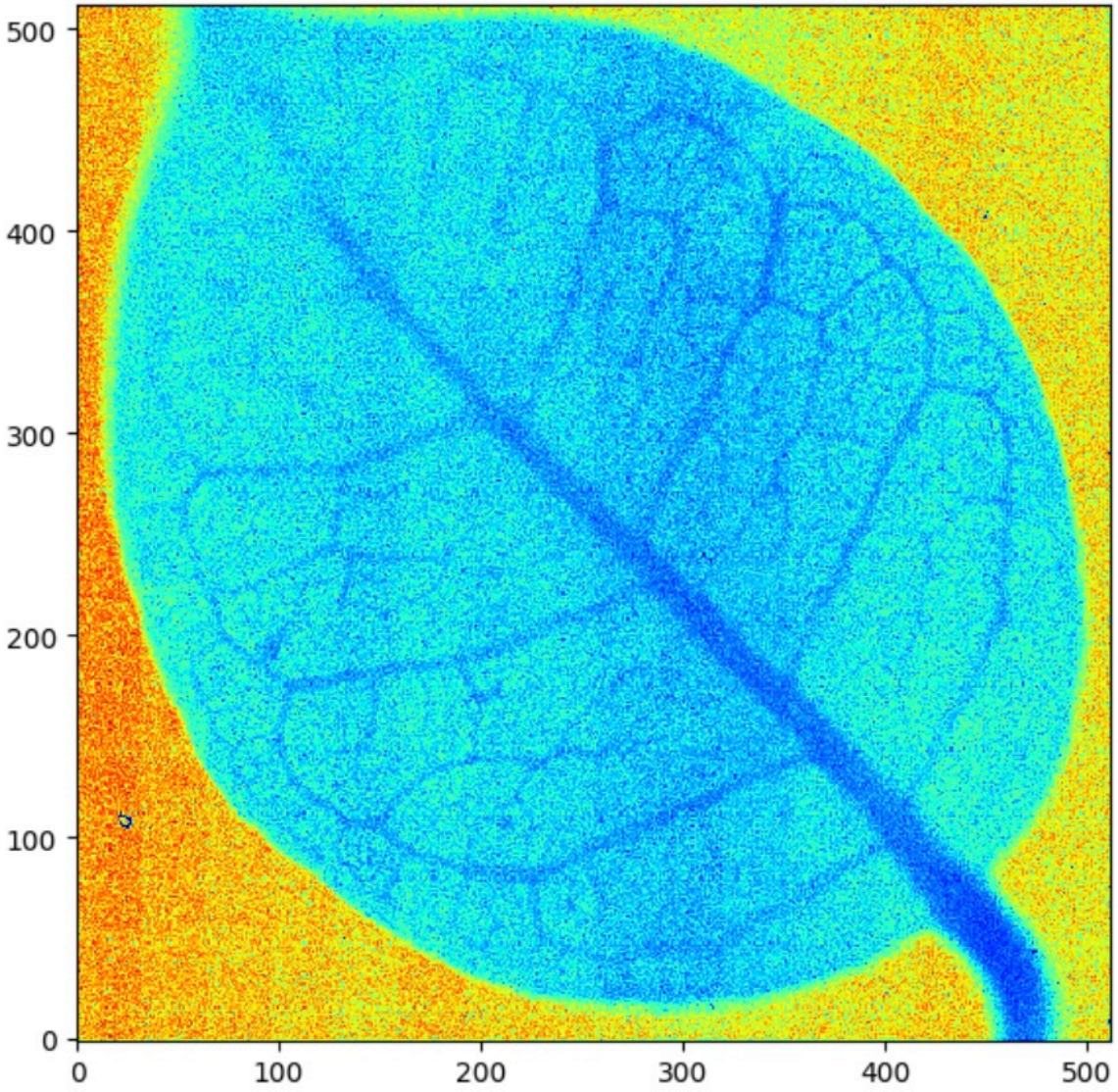
DRD7.6 – Complex Imaging ASICs and Technologies

- Possibility to explore multiple wafer splits: n-epi thickness, n-type or p-type starting substrate, substrate resistivity, FSI or BSI process on different wafer thicknesses, use of a gain layer for the implementation of monolithic CMOS LGADs.
- INFN and LFoundry agree on the terms to allow for the participation of third-party design groups to joint LF11is production runs, enabling straightforward and low-risk ramp-up of the R&D on FDMAPS using LF11is technology for new design teams.
- Silicon-proven IP available (Serialisers, c-LVDS Transceivers, bandgap/LDO, SPI, DAC/ADCs).

Further information on DRD7 workshop 25-26 September 2023: https://indico.cern.ch/event/1318635/



Grazie!



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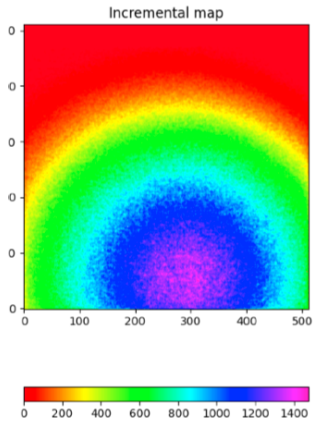
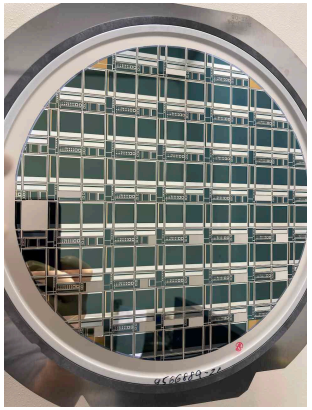
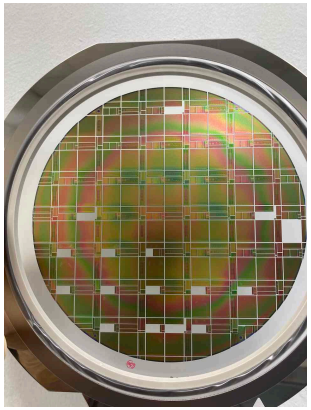
ARCADIA DMAPS R&D at INFN

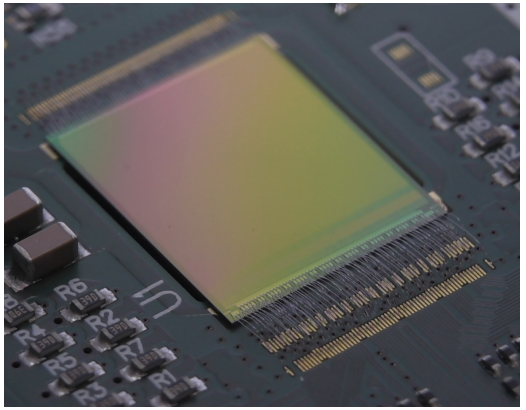
Advanced **R**eadout **C**MOS **A**rchitectures with **D**epleted **I**ntegrated sensor **A**rrays

- **ARCADIA:** CMOS sensor design and fabrication platform on LF11is technology
  - Sensor R&D and Technology, CMOS IP Design and Chip Integration, Data Acquisition
  - MD3: demonstrator full-chip FDMAPS for Medical (pCT), Future Leptonic Colliders and Space Instruments
  - Scalable FDMAPS architecture with very low-power: **10 mW/cm²**
  - Fully-depleted monolithic active micro strips with fully-functional embedded readout electronics
  - Ongoing R&D for the implementation of monolithic CMOS sensors with gain layer for fast timing
  - Custom BSI process allow to develop fully-depleted thick sensors (400µm) for X-ray imaging









ARCADIA-MD3: Chip Floorplan

Top Padframe

Auxiliary supply, IR Drop Measure

Matrix

512x512 pixels, Double Column arrangement

End of Sector (x16)

Reads and Configures 512x32 pixels

Sector Biasing (x16)

Generates I/V biases for 512x32 pixels

Periphery

SPI, Configuration, 8b10b enc, Serializers

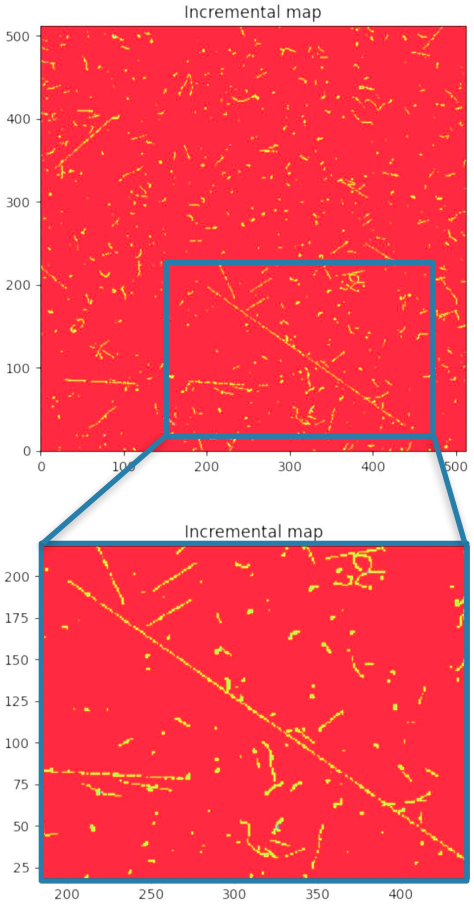
Bottom Padframe

Stacked Power and Signal pads

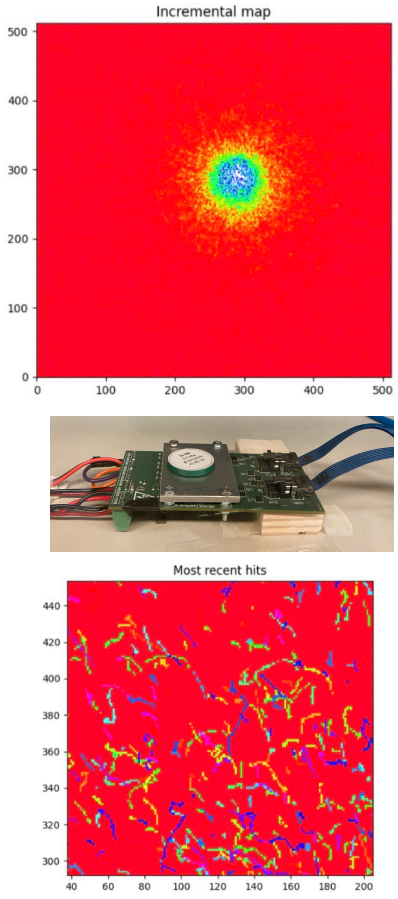
A. Paternò

ARCADIA-MD3: charged particles

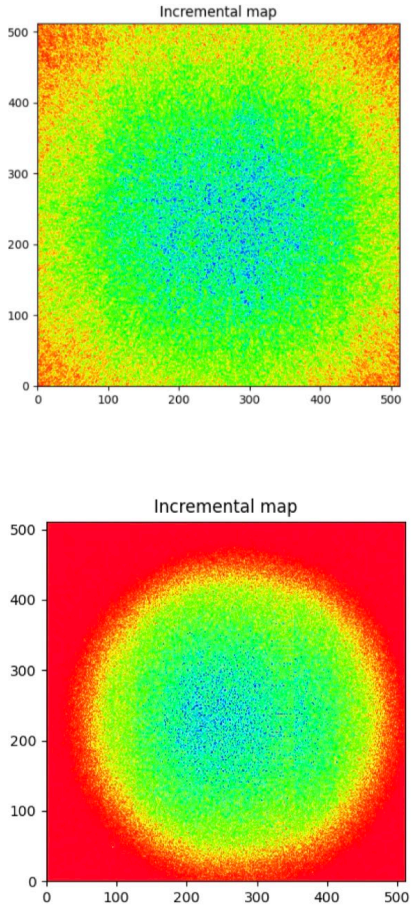
Cosmic rays
(tilted sensor)



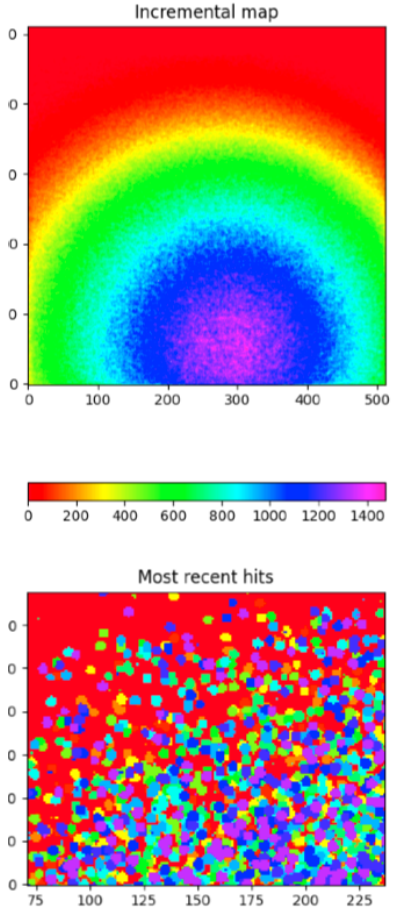
^{90}Sr
(collimated 1mm)



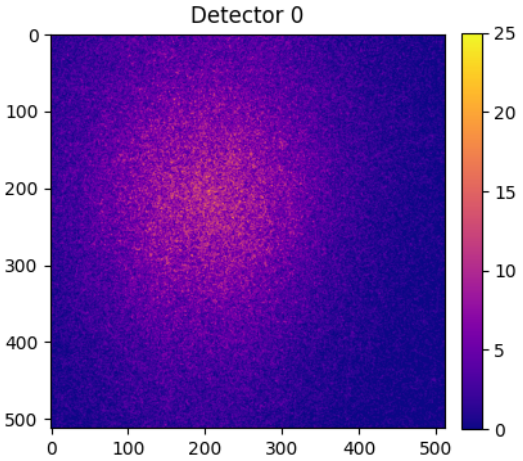
^{90}Sr
(uncollimated)

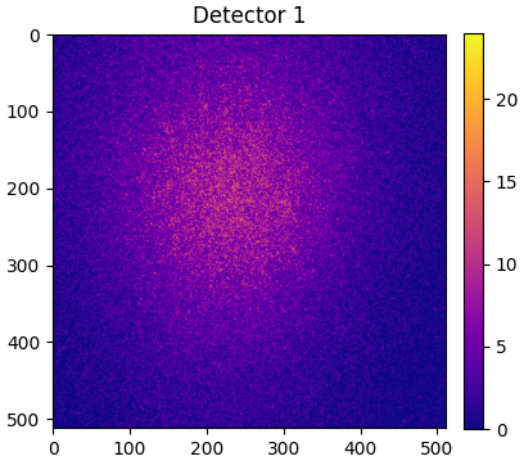


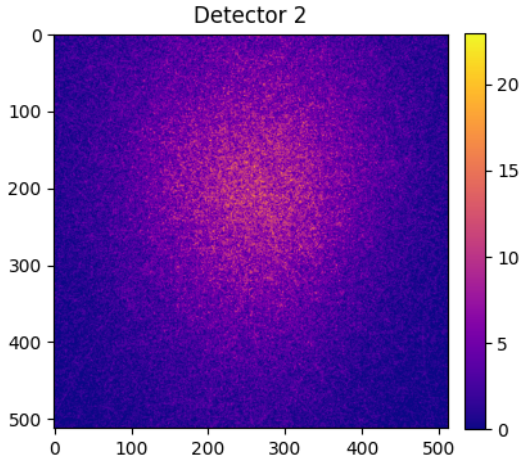
^{241}Am



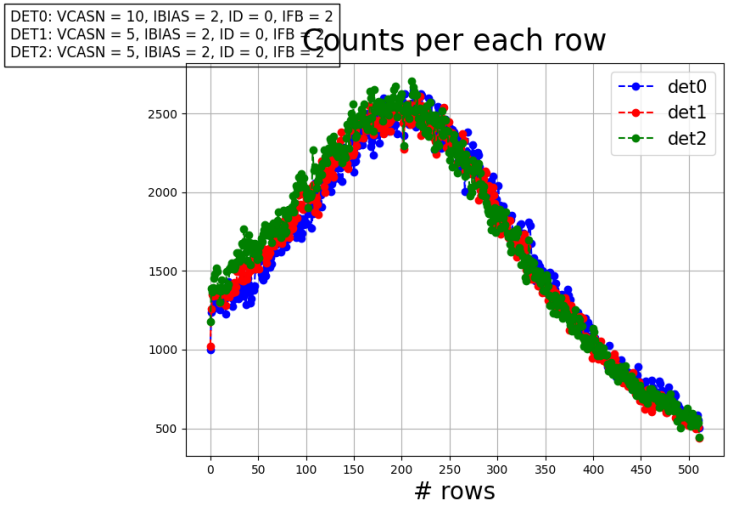
Test beam with ARCADIA-MD3

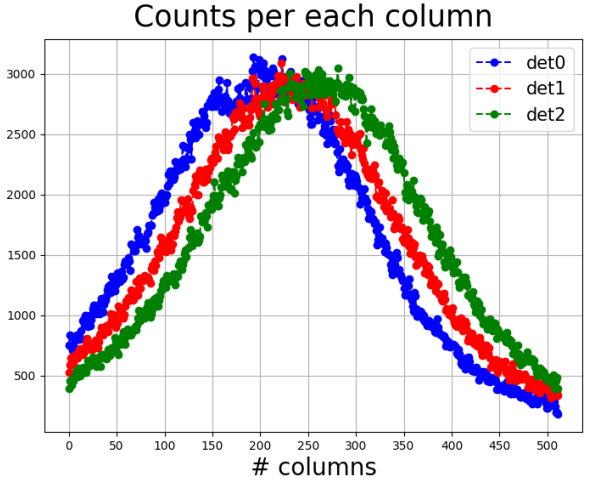




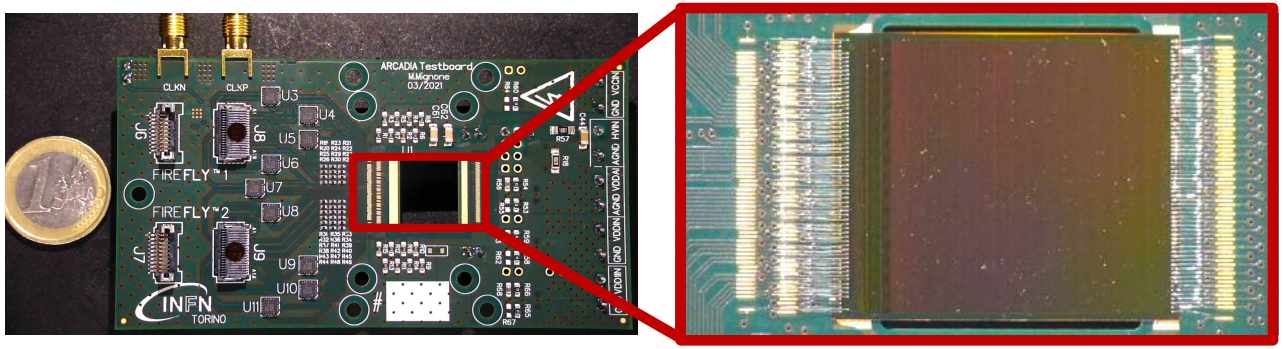


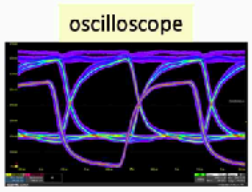
PRELIMINARY

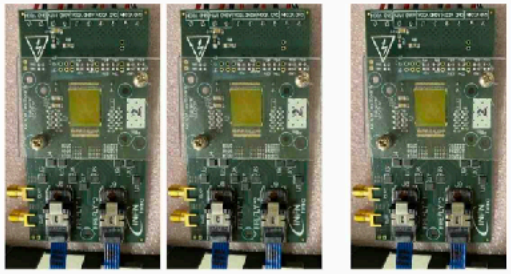


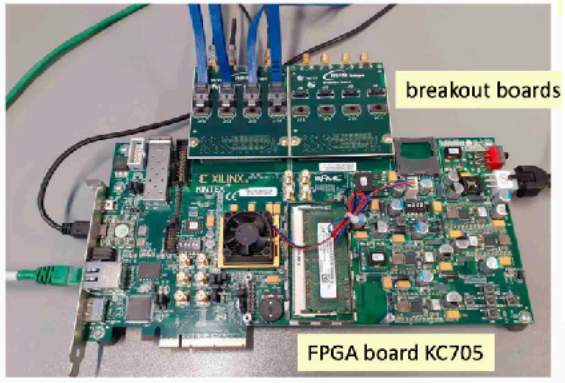


Front-end FEB-MD3 and DAQ





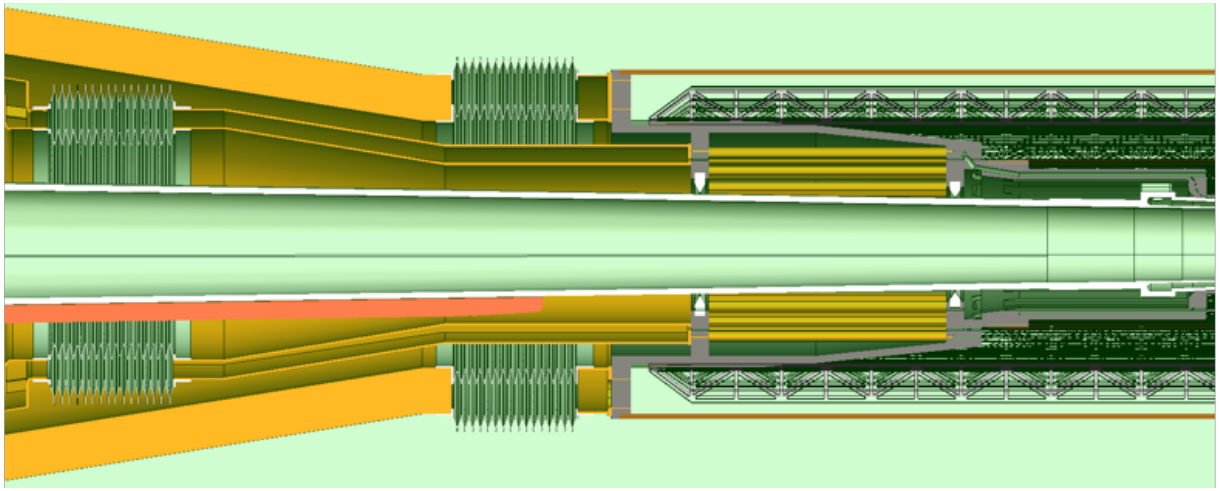




- 2 Samtec FireFly connectors for ASIC signals (Clock, SPI, Data)
- Connection to external low jitter Clock (via SMA connectors)
- Bias to the DMAPS backside or (wirebonded) to top pads
- Independent LDOs for IO Buffers, Analog Core, Digital Core
- PCB through-hole for matrix BSI
- custom FMC-to-Firefly breakout board

D. Falchieri, B. Balbi, M. Mignone

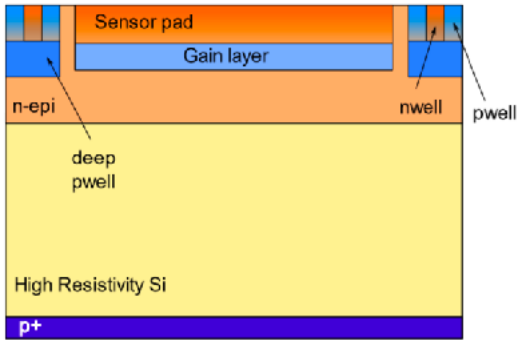
Inner Vertex Layout



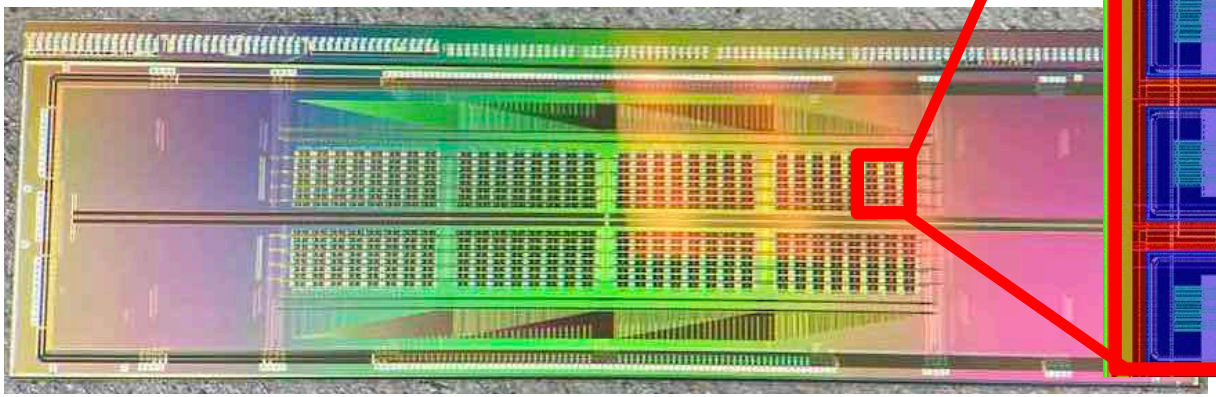
- Total detector weight 285 g
- 0.25% X0 thickness per layer
- Chips ~0.05% X0, readout and power bus ~0.06% X0
- Total power consumption 121 W
- Air cooling is possible
- Mockup construction and testing of the concept ongoing (LNF, Pisa, Perugia)

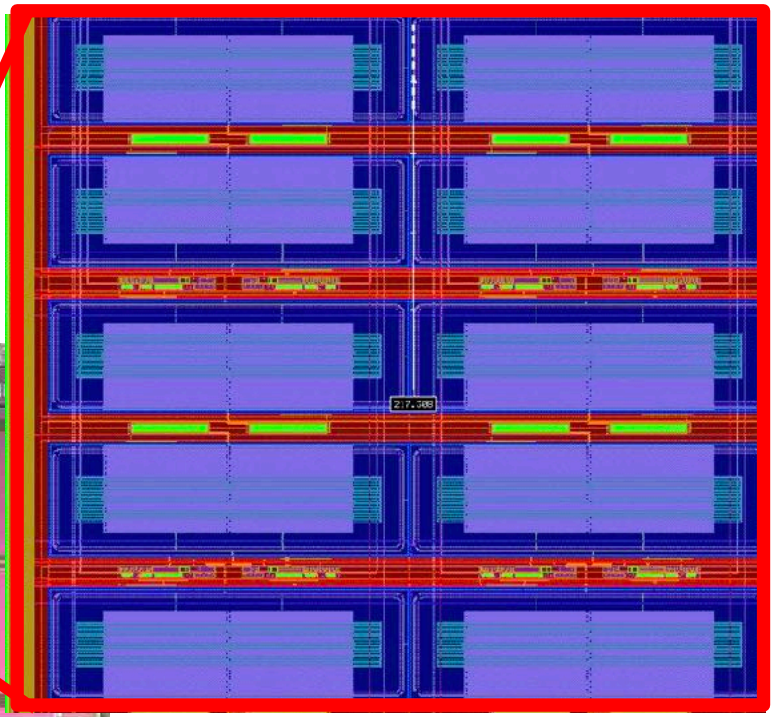
MadPix CMOS LGAD multi-pixel prototype

- MadPix prototype with gain layer and integrated electronics
- first small-scale demonstrator 4 x 16 mm^2;
- 8 matrices (64 pixel pads each) implementing different sensor and front-end flavours;
- 250 x 100 µm^2 pixel pads;
- 64 analogue outputs on each side, rolling shutter of single matrix readout;



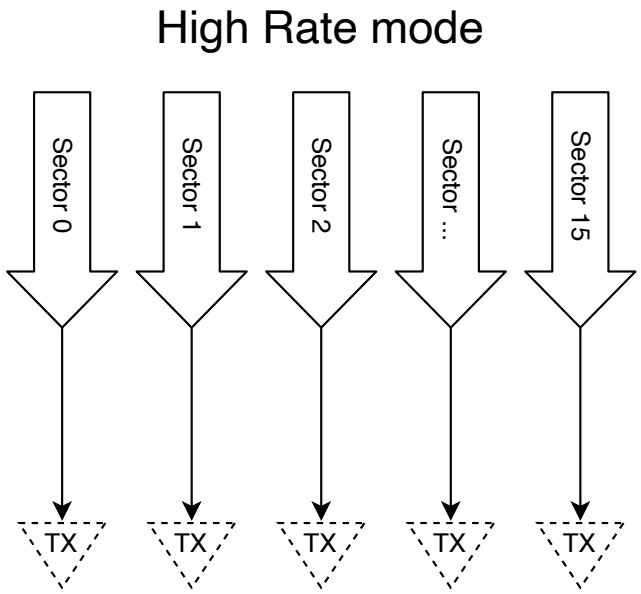
U. Follo, S. Durando, G. Gioachin, C. Ferrero

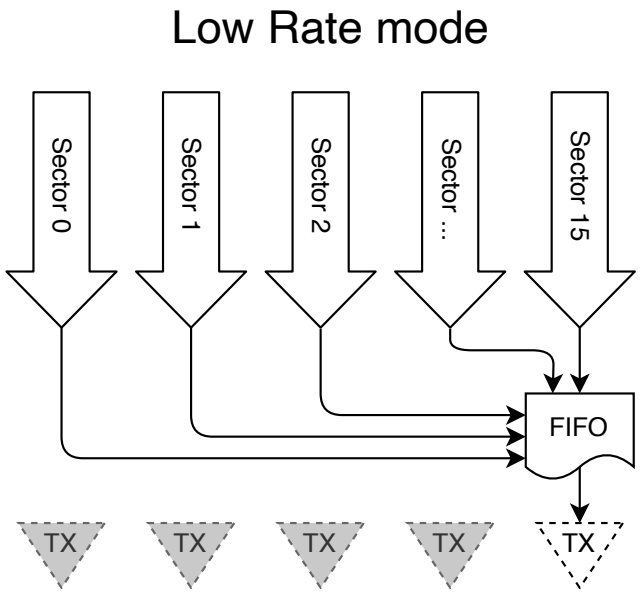




ARCADIA-MD3: Peripheral Dataflow

- Each sector has an independent readout and output link when operating in High Rate Mode
- Sector data is sent out (8b10b encoded) via dedicated 320MHz DDR Serialisers
- In Low Rate Mode, the first serialiser processes data from all the sections. The other serialisers and C-LVDS TXs(*) are powered off in order to reduce power consumption.

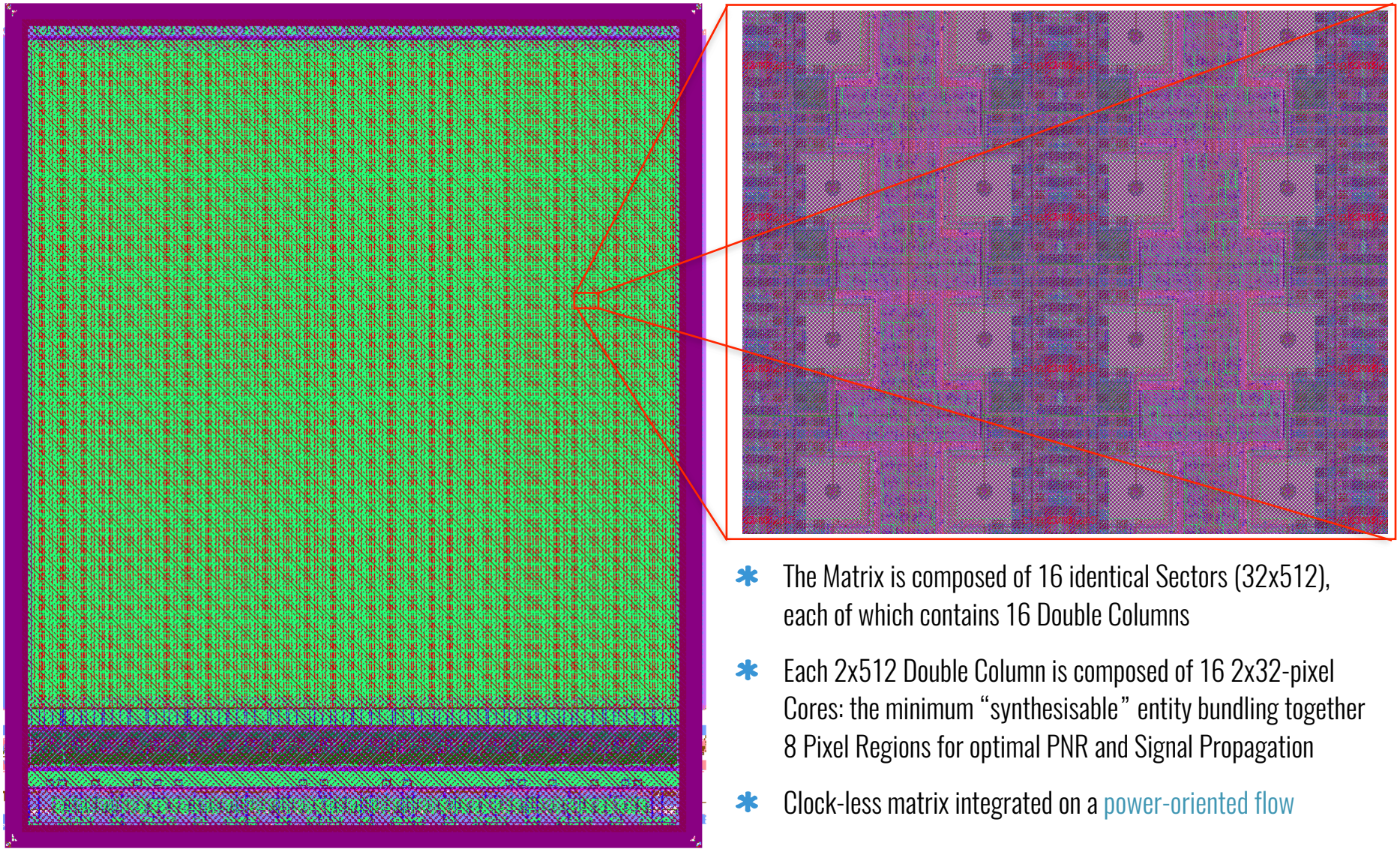




M. Pezzoli, G. Traversi, L. Ratti

* "A 2 Gbps custom LVDS transceiver for the ARCADIA project", talk at IEEE NSS-MIC 2021

ARCADIA-MD3: Integration



- The Matrix is composed of 16 identical Sectors (32x512), each of which contains 16 Double Columns
- Each 2x512 Double Column is composed of 16 2x32-pixel Cores: the minimum “synthesisable” entity bundling together 8 Pixel Regions for optimal PNR and Signal Propagation
- Clock-less matrix integrated on a power-oriented flow

ARCADIA MD3 DAQ Hardware: Telescope

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B. Balbi,
M. Mignone