INFN/AExxx, LAL-xxx, SLAC-R-xxx

Super$B$ Detector Technical Design Report

Abstract

This report describes the technical design detector for Super$B$.

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6 Silicon Vertex Tracker

Rizzo. Pages ??

6.1 Vertex Detector Overview G.Rizzo - 12 pages

6.2 Backgrounds R.Cenci - 4 pages

6.3 Detector Performance Studies N.Neri - 6 pages

6.3.1 Introduction *(about 1/2 page)*

- write some considerations about the main differences between BaBar and SuperB (i.e. luminosity, boost, beampipe, beamspot);
- describe the main idea behind the new detector design focusing on performances;
- cite BaBar TDR and BaBar NIM paper as reference for strip detectors.

6.3.2 Impact of Layer0 on detector performances *(about 2 pages)*

- definition of Layer0 requirements for physics (material budget, inner radius vs boost, outer radius, intrinsic resolution, coverage);
- B^0 decay and tag vertex and B^0 proper time resolution for different solutions;
- baseline solution performances;
- discussion of pro and cons.

6.3.3 Sensitivity studies for time-dependent analyses *(about 2 pages)*

- studies of benchmark channels $B^0 \to \phi K^0_S$, $B^0 \to \pi^+\pi^-$, etc.;
- include time-dependent sensitivity studies at charm threshold?
- impact of background on detector performances.

6.3.4 Vertexing and Tracking performances *(about 1 pages)*

- track parameter resolutions;
- considerations for pattern recognition, efficiency vs numbers of layers, reconstruction capabilities for low momentum tracks, K^0_S reconstruction.

6.3.5 Particle Identification *(about 1/2 pages)*

- dE/dx resolution and relevance for QED pairs suppression.
- discussion of relevance of ToT information and number of bits of the FEE.

6.4 Silicon Sensors L. Bosisio - 8 pages

(Striplets will be discussed together with the other sensors)

Short introduction (a few lines).

6.4.1 Requirements

6.4.1.1 Efficiency

6.4.1.2 Resolution

6.4.1.3 Radiation hardness

6.4.2 Sensor design

6.4.2.1 Technology choice

6.4.2.2 Optimization of strip layout

6.4.2.3 Wafer sizes and quantities

6.4.3 Prototyping and tests

6.5 Fanout Circuits L.Vitale - 4+4 pages

(Layer0 will be treated separately from the other ones)

6.5.1 Fanouts for layer0

6.5.1.1 Requirements

6.5.1.2 Technology

6.5.1.3 Design

6.5.1.4 Prototyping and tests

6.5.2 Fanouts for outer layers

6.5.2.1 Requirements

6.5.2.2 Technology

6.5.2.3 Design

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6.6.1 Readout chips V.Re - 10

6.6.2 Hybrid Design M.Citterio - 10

6.6.3 Data Transmission M.Citterio - 10

6.6.4 Power Supply - 2

6.7 Mechanical Support & Assembly S.Bettarini/F.Bosi - 14 pages

6.8 Layer0 Upgrade Options G.Rizzo/L.Ratti - 10 pages

With the machine operated at full luminosity, the layer 0 of the silicon vertex tracker may benefit from upgrading the layer0 to a pixellated detector. This solution can actually provide some significant advantages with respect to the baseline striplet option. In particular

- the occupancy per detector element from machine background is expected to fall to a few kHz, with a major impact on the speed specifications for the front-end electronics, mainly set by the background hit rate in the case of the striplet readout chip;
- better accuracy in vertex reconstruction can be achieved with a detector pitch of 50 μm or smaller; the shape of the pixel can be optimized in such a way to reduce the sensor pitch in the z direction while keeping the area in the range of 2500-3000 μm^2, which guarantees enough room for sparse readout functionalities.

A few technology alternatives for pixel detector fabrication are being investigated and R&D activity is in progress to understand advantages and potential issues of the different options.

6.8.1 Technology options

6.8.1.1 Hybrid pixels

6.8.1.2 Deep N-well CMOS monolithic sensors

Deep N-well (DNW) CMOS monolithic active pixel sensors (MAPS) are based on an original design approach proposed a few years ago and developed in the framework of the SLIM5 INFN experiment [4]. The DNW MAPS approach takes advantage of the properties of triple well structures to lay out a sensor with relatively

Figure 6.2: Resolution on the proper time difference of the two B mesons ($\beta\gamma = 0.28$), for different Layer0 radii, as a function of Layer0 thickness (in X_0 %).

large area (as compared to standard three transistor MAPS [9]) read out by a classical processing chain for capacitive detectors. The sensor, featuring a buried N-type layer with N-wells (NW) on its contour according to a typical deep N-well scheme, collects the charge released by the impinging particle and diffusing through the substrate, whose active volume is restricted to the uppermost 20-30 μm thick layer below the collecting electrode. Therefore, within this extent, substrate thinning is not expected to significantly affect charge collection efficiency, while improving momentum resolution performance in charged particle tracking applications. As mentioned above, DNW MAPS have been proposed chiefly to comply with the intense data rates foreseen for tracking applications at the future high energy physics (HEP) facilities. Based on the proposed solution, the MAPS detectors of the Apsel series (see Section 6.8.2.2), which are among the first monolithic sensors with pixel-level data sparsification [10, 11], have been developed and successfully tested at the Proton Synchrotron facility at CERN [12].

6.8.1.3 Monolithic pixels in CMOS quadruple well technology

In DNW MAPS, charge collection efficiency can be negatively affected, although to a limited extent, by the presence of competitive N-wells including PMOS transistors of the pixel readout chain, which may subtract charge from the collecting electrode.

6.8.2 R&D activity

6.8.2.1 The Superpix0 and Superpix1 hybrid pixel front-end chips

6.8.2.2 The Apsel DNW MAPS series

6.8.2.3 The Apsel4well quadruple well monolithic sensor

6.8.2.4 Radiation tolerance

6.9 Services, Utilities - 8 pages

Figure 6.1: Longitudinal section of the SVT

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