Tuesday Dec 13, 15-16:30

Introduction & TDR status	G. Rizzo	5	5
Update on background simulation	R. Cenci (phone)	15	5
Update on HDI design and periphel electronics	M. Citterio	15	5
Fastsim studies	N. Neri	15	5
SVT Mechanics	F. Bosi	15	5
subtotal		65	25

Tuesday Dec 13, 17-18:30

Pixel & inner layer strips analog FE in Pavia	M.Manghisoni/V.Re	15	5
Analog FE for outer layer strips in Milano	C. Fiorini	15	5
In-strip digital logic development in Pisa	R. Beccherle	15	5
FE chip readout architecture simulation in Bologna	F. Giorgi	15	5
Update on activities in Strasbourg	I.Ripp/Baudot	15	5
subtotal		75	25

Wednsday Dec 14, 9-10:30

Update on activities in Bari	V.Manzari	15	5
Update on activities in UK	A.Bevan/F.Wilson	15	5
Optimization of sensor and fanout in Trieste	L.Bosisio/L. Vitale	15	5
Testbeam results - Superpix0 Hybrid Pixel	A.Lusiani	15	5
Testbeam results - Analog MAPS	S.Bettarini/E.Paoloni	10	5
Testbeam results - Striplets	L.Fabbri	10	5
subtotal		80	30

Wednsday Dec 14, 11-13:30 - 15-18

SVT electronics meeting in aula Calcolo - edificio 14.