Master Panel

Schema di principio per regolazione VBias e VAnnealing

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The work of the MasterPanel

Dalla presentazione di Preghenella

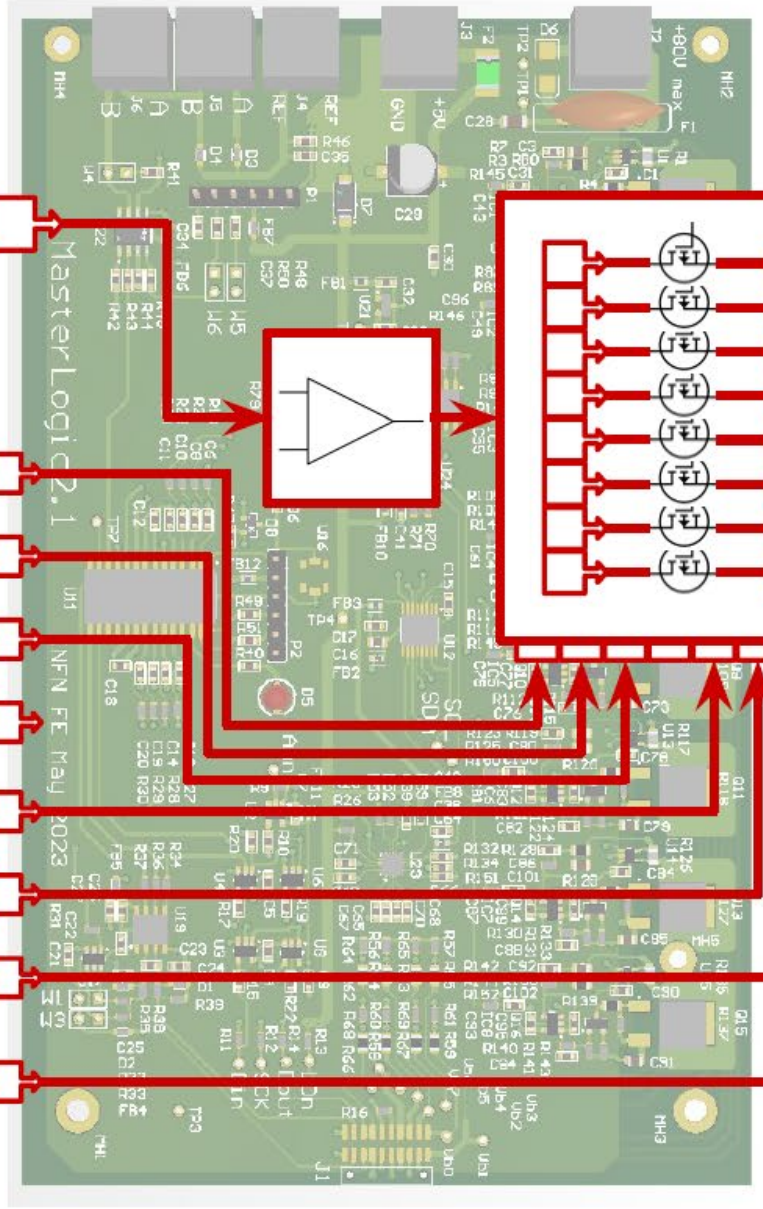
- **patch panel for the front-end electronics**
  - MP receives the input LV from the PS
    - 1.4 V analog, 1.4 V digital low, 2.7 V digital high
  - MP distributes the LV to the connectors to the FEE
    - 1 MP / 8 PDU scheme = 32 FEB + 8 RDO connectors on the MP output side
  - space considerations
    - 1 MP can not be bigger than 100 x 200 mm^2 (2 x 4 PDU) = 20000 mm^2
    - one FEB/RDO connectors is ~ 150 mm^2 → 150 x 40 = 6000 mm^2
    - assume similar space is taken by the input connectors
    - there are 8000 mm^2 for services: 100 x 80 mm^2
- **PDU services: NTC, Vbias, Vannealing**
  - MP receives 32 NTC voltages from PDU and converts into ADC
    - 1 32-channel ADC? 1 ADC + 32-channel multiplexer?
  - MP receives one input Vbias-in (64 V) from PS and generates 8 output regulated Vbias-out (40-60 V)
    - Vbias-out, one for each PDU
  - MP receives 8 input Vann-in (-12 V)

MasterPanel

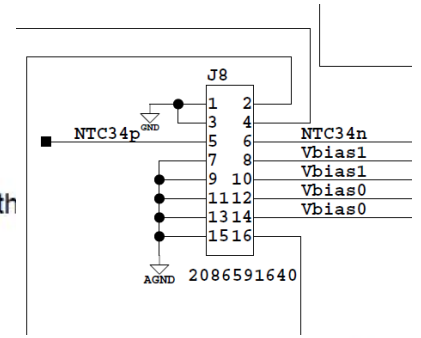
64 V
1.5 A

1 Vbias input

8 Vann inputs



for each PDU
- 1 linear regulator for Vbias
- 1 output stage with 8 bias lines with individual ON/OFF control



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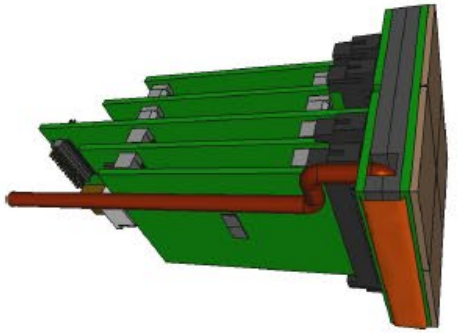


NORMAL operation
Vbias-in → regulator → 8x V-out

ANNEALING operation
8x Vann-in → 8x V-out

Dalla presentazione di Preghenella

Schema Vann. switch

Gate-Sector_7
Gate-Sector_1
Gate-Sector_0
x 8
+5V
CMOS signal
Vref 2.5V
U1A
LM324
GND
D3 DIODE
D1 DIODE
D2 DIODE
R1 10K
R2 10K
R3 10K
R4 10K
R5 10K
R6 10K
Q1 MOSFET N
Q2 MOSFET N
Q8 MOSFET N
Vann_0
Vann_1
Vann_2
Vann_7
-Vann_0
-Vann_1
-Vann_2
-Vann_7
PDU_0-Sector_0
PDU_1-Sector_0
PDU_7-Sector_0
PDU_0-Sector_1
PDU_1-Sector_1
PDU_7-Sector_1
PDU_0-Sector_7
PDU_1-Sector_7
PDU_7-Sector_7

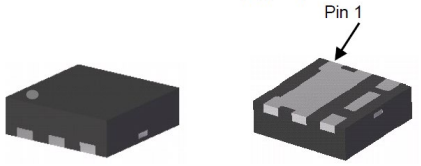
Da cambiare collegamento matrice...

MOSFET DMT6030LFCL

Product Summary

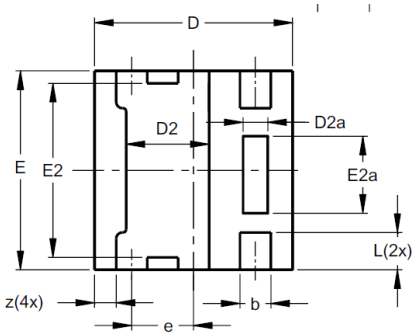
BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
60V	25mΩ @ V_{GS} = 10V	6.5A
	34mΩ @ V_{GS} = 4.5V	5.2A

U-DFN1616-6 (Type K)



Top View Bottom View

1,65 x 1,65 mm



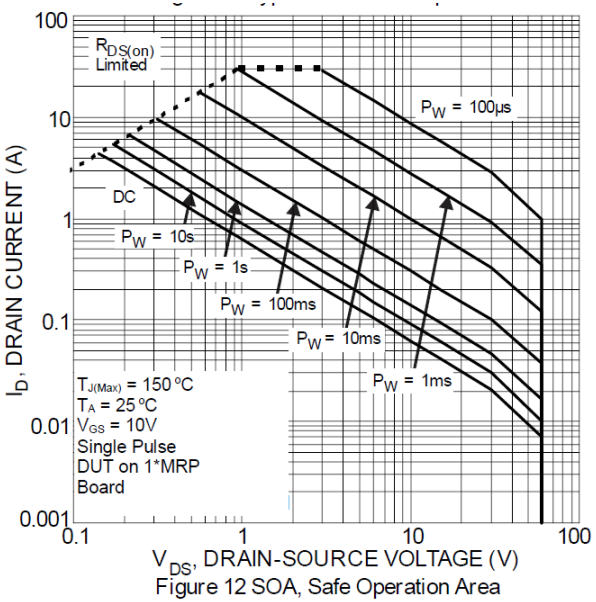


Figure 12 SOA, Safe Operation Area

Confronto MOSFET

Part Number	DMT6017LFDF	DMT8030LFDF	DMT6030LFCL
Data Sheet	https://www.diodes.com/assets/Datasheets/DMT6017LFDF.pdf	https://www.diodes.com/assets/Datasheets/DMT8030LFDF.pdf	https://www.diodes.com/assets/Datasheets/DMT6030LFCL.pdf
Spice Model	https://www.diodes.com//spice/download/4175/DMT6017LFDF.spice.txt	https://www.diodes.com//spice/download/4265/DMT8030LFDF.spice.txt	https://www.diodes.com//spice/download/4541/DMT6030LFCL.spice.txt
AEC Qualified	No	No	No
Compliance (Only Automotive(Q) supports PPAP)	Standard	Standard	Standard
Polarity	N	N	N
ESD Diodes (Y|N)	Yes	No	No
|VDS| (V)	**65**	**80**	**60**
|VGS| (±V)	16	20	20
|IDS| @TA = +25°C (A)	8.1	7.5	6.5
|IDS| @TC = +25°C (A)	-	-	-
PD @TA = +25°C (W)	1.76	2.2	1.58
PD @TC = +25°C (W)	-	-	-
RDS(ON)Max@ VGS(10V)(mΩ)	**18**	**25**	**25**
RDS(ON)Max@ VGS(4.5V)(mΩ)	**23**	**38**	**34**
RDS(ON)Max@ VGS(2.5V)(mΩ)	-	-	-
RDS(ON)Max@ VGS(1.8V)(mΩ)	-	-	-
|VGS(TH)| Min (V)	-	-	-
|VGS(TH)| Max (V)	2.3	2.5	2.5
QG Typ @ |VGS| = 4.5V (nC)	7.5	5.4	4.5
QG Typ @ |VGS| = 10V (nC)	15.3	10.4	9.1
CISS Typ (pF)	891	641	639
CISS Condition @|VDS| (V)	30	25	30
Packages	**U-DFN2020-6 (Type F)**	**U-DFN2020-6 (Type F)**	**U-DFN1616-6**

NHDTA114/124/144ET series

80 V, 100 mA PNP resistor-equipped transistors

Rev. 1 — 26 June 2020 Product data sheet

1. General description

PNP Resistor-Equipped Transistor (RET) family in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package.

Table 1. Product overview

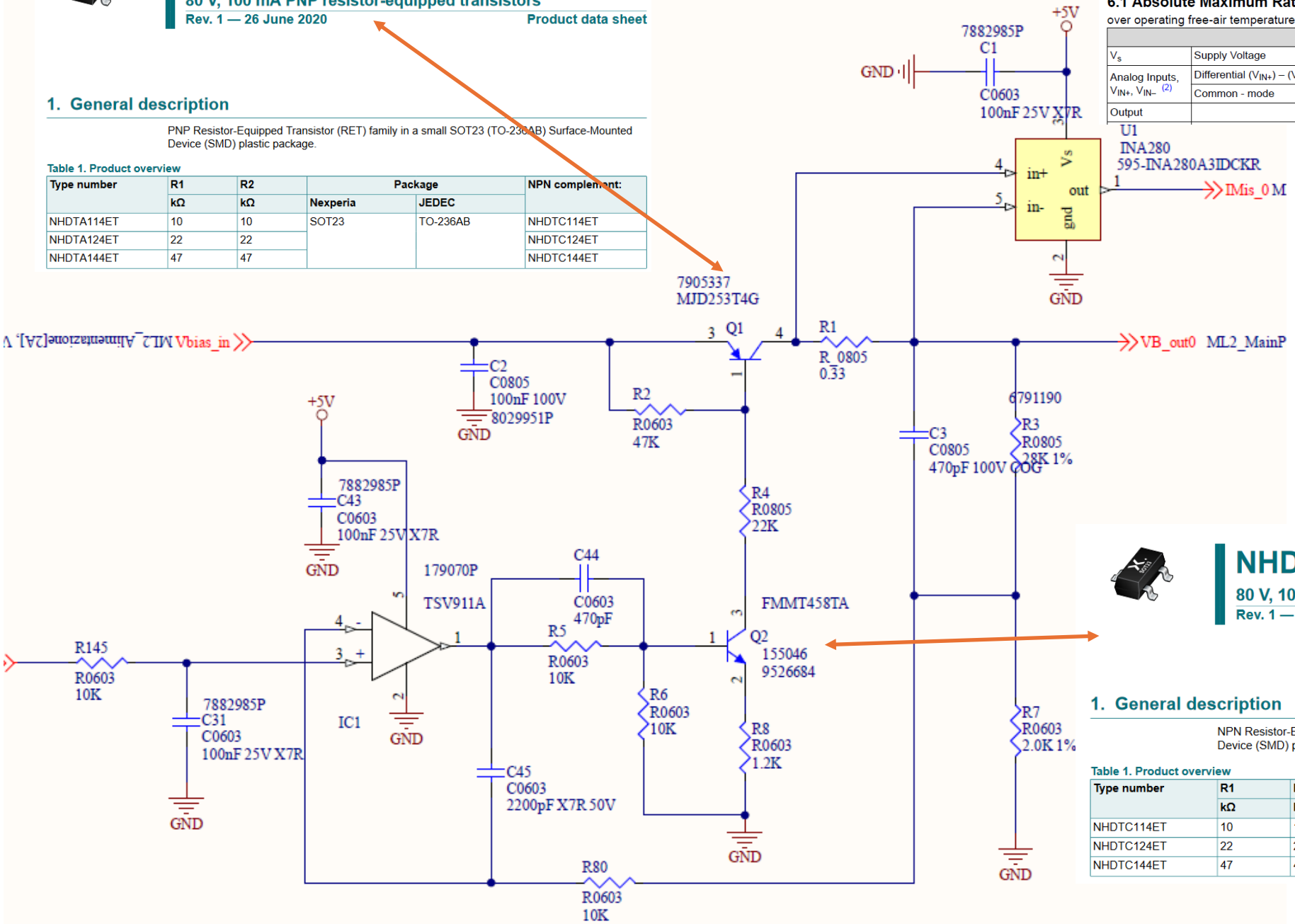
Type number	R1	R2	Package		NPN complement:
	kΩ	kΩ	Nexperia	JEDEC	
NHDTA114ET	10	10	SOT23	TO-236AB	NHDTC114ET
NHDTA124ET	22	22			NHDTC124ET
NHDTA144ET	47	47			NHDTC144ET

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply Voltage	–0.3	22	V
Analog Inputs, V_{IN+}, V_{IN-} (2)	Differential (V_{IN+}) – (V_{IN-})	–30	30	V
	Common - mode	–20	122	V
Output		GND – 0.3	Vs + 0.3	V



Schema regolatore Vbias

- Vin max = 64V
- Corrente di uscita max = 1.5mA

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Conclusioni

- Avere un solo regolatore Vbias reduce lo spazio del circuito ma richiede 8 diodi per collegare UNA Vbias a 8 canali di Vann.
- 8 regolatori VBias per PDU implica 64 regolatori su una MasterPanel ma semplifica il collegamento.
- Il misuratore di corrente in uscita ai regolatori VBias potrebbe non essere indispensabile.
- La misura della tensione in uscita (VBias e Vann) e' utile.
- Canale di comunicazione. RS485, a parere mio, e' il piu' indicato ma occorre vedere se compatibile con lo standard dell'esperimento