Digital SiPMs: Technology Potential and 4D-Tracking Applications

Characterization of CMOS SPADs

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Outlook

In this Presentation

- SiPMs analog & digital
- DESY dSiPM prototype in LFoundry-150 nm
 - Laboratory characterizations
 - Test beam of bare prototypes
 - Test beam of prototypes with thin LYSO coupling
- Recent development of dSiPM technologies
- Conclusion

Silicon Photomultipliers

State of the Art Solid State Photodetectors



Analog & Digital SiPMs

State of the Art Solid State Photodetectors





Analog SiPM

- SPADs array with analog output
- All SPAD read in parallel
- Charge and time measurements performed outside
- Well-known and widely diffused technology
- High-performance SPADs produced in specialized fabs

Digital SiPM

- Signal digitization at SPADs level
- In-pixel electronics (counting, hit position, etc.)
- Charge and time measurements can be on-chip
- Customised ASICs design using commercial processes
- Hybrid or monolithic approach

CMOS SPADs Possible Applications

Commercial and HEP Examples



LIDAR & 4D-imaging

- Automotive
- Industry
- Security

Images from: Fraunhofer IMS





Scintillating fibers readout

• Calorimetry, tracking





4D-Tracking of charged particles

• MIPs tracking and timing

https://dx.doi.org/10.1088/1361-6633/aa94d3

DESY dSiPM Prototype in LF-150 nm

DESY dSiPM Prototype

ASIC in LF 150 nm CMOS

Layout

- In LFoundry 150 nm CMOS technology
- Main matrix: 32 x 32 pixels (4 SPADs per pixel)
- Sensor area: 2.2 x 2.4 mm²
- Test structures in the chip periphery

Features

- Full hit matrix readout and timing measurements
- 4 x 12-bit Time to Digital Converters with ~95 ps bins
- Pixel masking & 2-bit in-pixel hit counting
- Quenching can be tuned (quenching transistor)
- Readout is frame-based (3 MHz frame rate)



DESY dSiPM in LFoundry 150 nm

For details: I. Diehl et al 2024 JINST 19 P01020

Readout Concept

The Quadrant Structure



Quadrant structure

Readout concept of a 16-by-16 pixel unit (Quadrant)

For details: I. Diehl et al 2024 JINST 19 P01020

DAQ System

Juli I

Caribou

 Versatile readout system developed by CERN, BNL, DESY and University of Geneva

Fast and Low-Cost Implementation

- Allows fast, simple and Low-cost implementation & tests of sensors
- Already used for ATLASPix, CLICTD, DPTS, FASTPIX, etc.

SoC Board

- An embedded CPU runs DAQ and control software
- An FPGA runs custom hardware for data handling and detector control

Control and Readout (CaR) Interface Board

- Provides physical interface from the SoC to the detector chip
- Contains all peripherals needed to interface and run the chip: power supplies, ADCs, voltage/current references, LVDS links, etc.

Chip Board

- Passive & detector-specific components only
- DSiPM here glued & bonded
- Enclosed in Aluminum case that acts as heat sink and light shield

http://dx.doi.org/10.22323/1.370.0100 https://gitlab.cern.ch/Caribou/







Chip Board

Chip Glued & Bonded

Laboratory Characterizations

IV Curves & Dark Count Rate

- Detailed characterization performed on several samples (Chip4 shown in figures)
- IV & Dark Count Rate studies performed with controlled temperature (from -25 to 20 °C) and humidity (~ 0 %) in a dark environment
- Measurements compatible with expectations (Foundry)





V_{Bias}

4 || SPADs

masking

Pixel

Effect of Masking

Dark count rate reduction by masking

- Any masking pattern can be used ٠
- Noisy pixels can be identified and masked ٠
- Masking reduces the sensor DCR ٠





Effect of masking on sensor IV

- IV shape above breakdown dominated by dark count discharges
- Masking allows to study the effect of individual pixels to sensor IV and power consumption

Laser Studies

Timing Performances

Setup

- DUT placed on an x-y stage
- Laser optical system on a z-stage
- 1064 nm pulsed laser (few ps jitter)
- Laser in sync with the DAQ Clock
- Spot size O(pix_pitch)
- Single pixel investigations

Timing resolution

- Analog Pixel/SPAD (TS): < 20 ps
- Digital Pixel + TDC: O(50 ps)

Propagation delay

- Delays up to 330 ps in pixels TOA
- Contribution can be corrected knowing the position of firing pixels



Laser Setup



Timing of analog SPAD/Pixel



y[pix]

Signal propagation delays

Tuning the Quenching Resistance

- Transistor used for avalanche quenching in the pixel
- The equivalent quenching resistance can be tuned
- This affects recovery time and power consumption
- Dead time is investigated using the laser setup
- Pulse duration can be tuned in the range 20-400 ns





Crosstalk Probability

- Optical crosstalk is one of the main correlated noise in SiPMs
- The digital nature of the sensor (masking and hitmap-readout) allows a measurement of the crosstalk of individual pixels
- The probability of crosstalk is measured using noisy pixels in a dark environment
- A non-uniform CT-probability is measured in adjacent pixels



https://doi.org/10.1016/j.nima.2018.11.119





Light Emission and Crosstalk Probability

- The probability of crosstalk can be correlated with the position of the noisy SPAD within the pixel
- The photons produced during SPAD discharges cause crosstalk but also escape from the sensor and can be detected
- Long-exposure images with a high-sensitivity camera in dark conditions can be used to identify the position of the defect within the pixel.







Crosstalk studies as a function of avalanche position

Test Beam on Bare Prototypes

dSiPM as Possible 4D-Tracker Candidate

Beyond Photon Detection Applications

MIP detection with analog devices

- SPAD/SiPMs already proved to be good MIPs detectors [1] [2]
- Excellent instrinsic timing performance O(10 ps)
- Photon detection is still possible (multipurpose detector)

Using CMOS dSiPM

- On-chip data processing and digitalization
- Tracking-like detector architecture possible
- High granularity with O(10 μm) spatial resolution
- Large area/volume production possible

Drawbacks

- Efficiency is limited by the fill factor
- High DCR compared to standard pixel detectors
- No distinction between signal and noise



MIP and photons interaction in a SPAD

DESY dSiPM Test Beam

Device Treated as a Particle Detector





DESY dSiPM test beam setup



- **EUDAQ** framework and AIDA TLU used for data acquisition and synchronization of devices.
- **Corryvreckan** Framework used for test beam data reconstruction and analysis



MBI for Alignment to the Trigger ROI

hitmap





Plastic scintillator with a hole used as VETO for trigger

- · Anticoincidence with other scintillators
- Trigger only in a ROI slightly larger than DUT
- · Allows to save disk space and maximize yield

Material Budget Image (AAD)





Material budget image for DUT positioning

Corryvreckan modules: [TrackingMultiplets] [AnalysisMaterialBudget]

DESY dSiPM Spatial Properties

Associated cluster size

Direct MIP Detection (Only Silicon)



Cluster size VS OV

DESY dSiPM Spatial Properties

Direct MIP Detection (Only Silicon)



Spatial Residuals

- Distance between dSiPM hit and track
- Shape due to in-pixel 4 SPADs structure
- Spatial resolution from signal RMS O(20 μm)
- Compatible with pitch/ $\sqrt{(12)}$



DESY dSiPM Timing

Direct MIP Detection (Only Silicon)



dSiPM pixel





- Time resolution in MIP detection measured using time residuals
- Model fitted to the data to extract timing components
- 85% of the entries fast (50 ps), 15% "slow" O(ns)
- Tracking allows spatial resolution O(5 μm)
- Selecting only "slow" events an in-pixel "ring" shape is visible
- Slow events come from SPAD edges
- This is probably due to drift in low E-field regions

DESY dSiPM Efficiency

Direct MIP Detection (Only Silicon)

in-pixel y_{track} µm 0.8 30 0.7 20 0.6 10 0.5 0 0.4 -10 0.3 -20 0.2 -30 0.1 10 20 30 in-pixel x_{track} [μm] -30-20 -10Ω

In-pixel efficiency

- Image resolution limited by tracking resolution (O 5µm)
- Maximum efficiency in the SPAD centre (close to 100%)
- Lower efficiency in SPAD edges (covered by SPAD isolation ore electronics well)
- MIP detection efficiency is higher than PDE peak (~15%)

Efficiency VS overvoltage



- Efficiency compatible with fill factor (~30%)
- Efficiency reported is noise corrected
- Small overvoltage dependence
- No temperature/sample dependence

Possible Solution to Increase Efficiency

And "Reduce" DCR Noise

MIP detection with analogue SiPMs

- High detection efficiency observed while detecting MIP
- High number of SPADs firing
- Correlation between MIP response and SiPM packaging
- Effects attributed to Cherenkov light produced in commercial SiPMs encapsulation materials (~0.6-1.5 mm Epoxy resin or Silicone)
- Benefits:
 - High efficiency of SiPM in direct MIP detection
 - Low DCR contamination (high threshold)
 - Multipurpose detector (single photon and MIP)

References

- F.Carnesecchi, G.Vignola et al. *Direct detection of charged particles with SiPMs, 2022*
- F.Carnesecchi, G.Vignola et al. Understanding the direct detection of charged particles with SiPMs, 2023

F.Carnesecchi, B.Sabiu et al. Measurements of the Cherenkov effect in direct detection of charged particles with SiPMs, 2023



Test Beam on Prototypes with thin LYSO Coupling

Thin Radiator Concept

Detecting Cherenkov & Scintillation Light





Coupling with 100, 200 and 500 μm Thin Scintillators



dSiPM + LYSO Sr-90 Data

Random Selection of events



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Cluster Size, Signal & Noise with Different Tagging







radiator coupling

Spatial Residuals, Good Spatial Performances Preserved







- Thinner LYSO has better spatial resolution
- Sigma ~32 μm (100μm LYSO) and ~38 μm (200μm LYSO)
- Small OV & temperature dependence

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Efficiency up to ~100%

In-pixel Efficiency with 100 µm - LYSO coupling



Timing Resolution

- Fast time residuals core in efficiency-enhanced dSiPMs
- Significant fraction of event in residuals tails (not log scale)
- Tail effect attributable to the LYSO's scintillation properties and low fill-factor
- Faster radiators or designs/technology with higer sensor fill-factor will improve timing



Time Residuals with bare dSiPMs



Recent Development of dSiPM Technologies

Microlenses to Increase Fill-Factor

Photon Focusing on Sensing Area, Es from LFoundry



https://indico.cem.ch/event/855527/attachments/1924667/3225909/adelmonte - Technology_development_of_CMOS_Image_sensors.pdf

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Step index polymeric lightguides

CFOUNDRY

3D Bonded Structures and Backside Illumination

To Furter Enanche SPAD Performances

- 3D stacking of silicon wafers/chips allows to produce SPADs and electronics separately
- SPAD performances can be optimized without interfering with electronics
- In combination with backside illumination and internal charge focusing, fill-factor reach almost 100% and DCR decrease (smaller avalanche region)
- Mega-pixels high-performance SPADs array already produced with this technology [2]



3D integrated LIDAR image sensor from [1]



BSI charge focusing SPAD array from [2]



Image from a megapixel SPAD image sensor [2-3]



1" SPAD sensor for ultra-high-sensitivity cameras [3]

[1] https://doi.org/10.3390/s16040495

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https://doi.org/10.1109/IEDM19574.2021.9720605

[3] https://global.canon/en/technology/high-sens-cam-2023.html

Summary & Outlook

dSiPM as 4D-Tracking Candidate

CMOS dSiPMs

- Combination of SPAD and CMOS electronics in the same silicon die opens new application possibilities
- Reduction of complexity & cost especially for large volumes

DESY dSiPM & MIPs 4D-Tracking

- dSiPM can be a possible candidate technology for 4D-tracking
- Spatial resolution down to ~20 µm and ~50 ps system timing
- Efficiency >99%, very low noise rate using thin LYSOs

CMOS dSiPMs R&D Potential

- dSiPM can play an important role in future HEP detector systems
- CMOS dSiPMs are a "young" technology, promising R&Ds ongoing
- Industry is rapidly improving CMOS-SPADs performances

DESY dSiPM 4D-Tracking Performances

	dSiPM	dSiPM+LYSO
Signal Cluster Size	~ 1	10 – 40
Spatial Resolution	~ 20 µm	~ 35 µm
Efficiency in MIP detection	~ 33 %	> 99 %
Noise Rate	O(MHz)	O(Hz)*
Time Resolution	~ 50 ps	< 1ns **

* While cutting on cluster-size

** Currently under investigation

Thank you.

References:

I. Diehl et al, Monolithic MHz-frame rate digital SiPM-IC with sub-100 ps precision and 70 µm pixel pitch S.Lachnit, Time Resolution of a Fully-Integrated Digital Silicon Photo-Multiplier F.Feindt et al, The DESY digital silicon photomultiplier: Device characteristics and first test-beam results

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The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

DESY dSiPM ASIC

More Details in the Reference Publication



Figure 3. Simplified equivalent circuits of: (a) the dSiPM pixel, (b) the TDC, and (c) the validation logic.

From: <u>I. Diehl et al 2024 JINST 19 P01020</u>

DAQ System in Test Beam

AIDA TLU Core



TestBeam data reconstruction

Using Corryvreckan Framework

- Corryvreckan use hit (pixels above threshold) and Clusters (groups of adjacent hits) to reconstruct particle trajectories.
- DUT response is then investigated on associated events



Telescope Planes





https://project-corryvreckan.web.cern.ch/project-corryvreckan/

Timing Performances

- The timing is worse when the MIP does not hit the SPAD
- Tail effect attributable to the LYSO's scintillation properties and low fill-factor
- Faster radiators or designs/technology with higer sensor • fill-factor will improve timing



In-pixel map of time residuals Std Dev

time [ns]

0.9

0.8

0.7

0.6

0.5

0.4

Example of LYSO(Ce) scintillation



LYSO Timestamp: Fast if we catch one prompt ph



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Analog SiPM + Thin LYSO

Confirm that Fill-Factor and Scintillator Properties Affect Timing

- Thin LYSOs coupled to a commercial analog SiPM
- Investigation of the effect of higher fill-factor
- With low threshold exelent timing measured









Analog SiPM + Thin LYSO

Confirm that Fill-Factor and Scintillator Properties Affect Timing



Analog SiPM+LYSOs