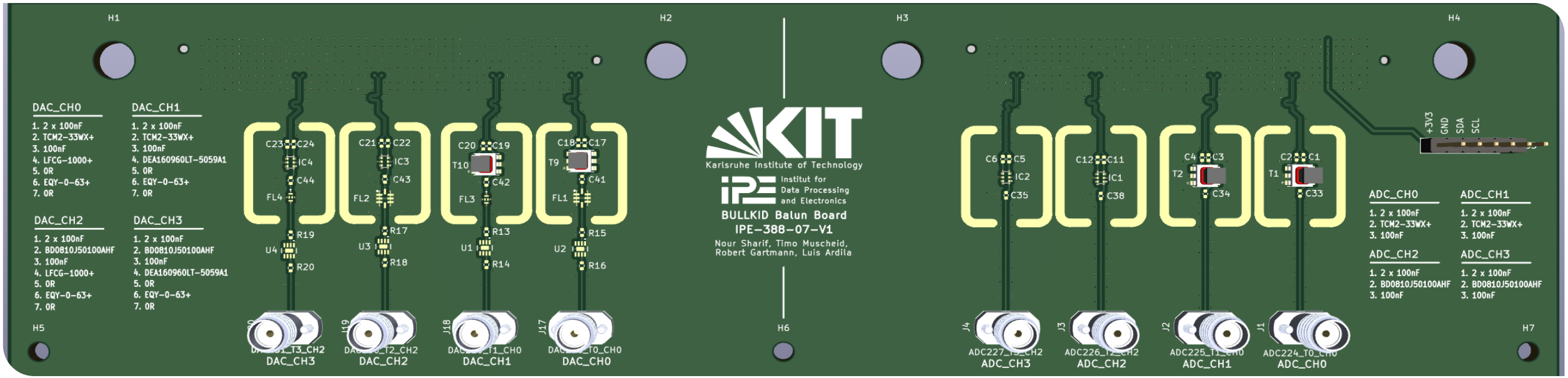
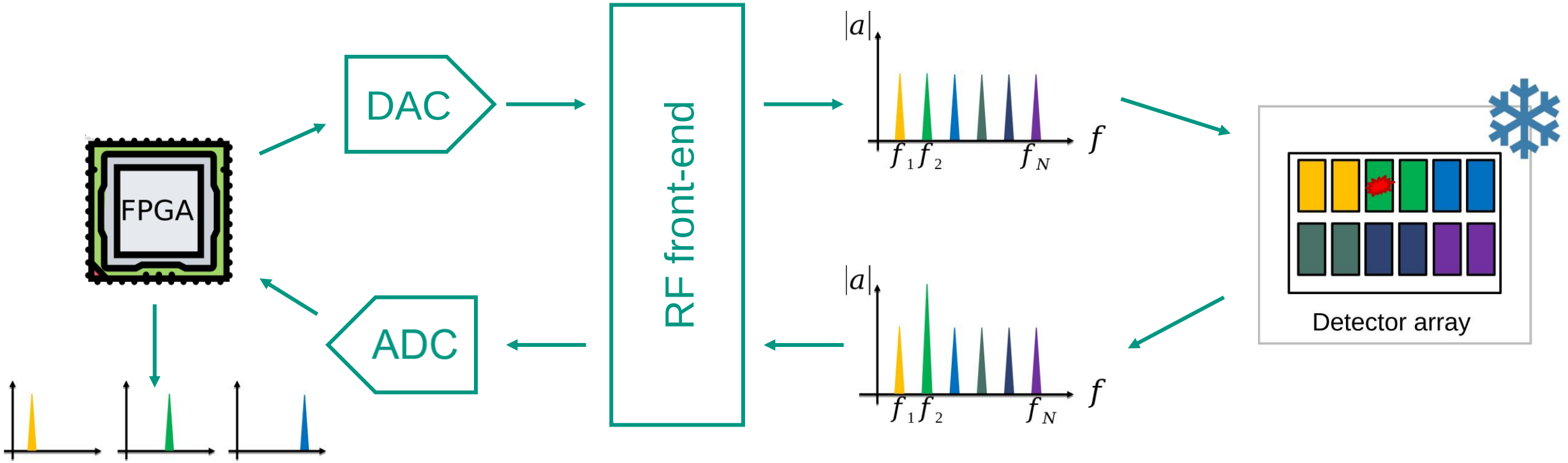
Karlsruhe Institute of Technology

Readout Electronics

BULLKID Digest 02.10.2024



Reminder: SDR readout concept

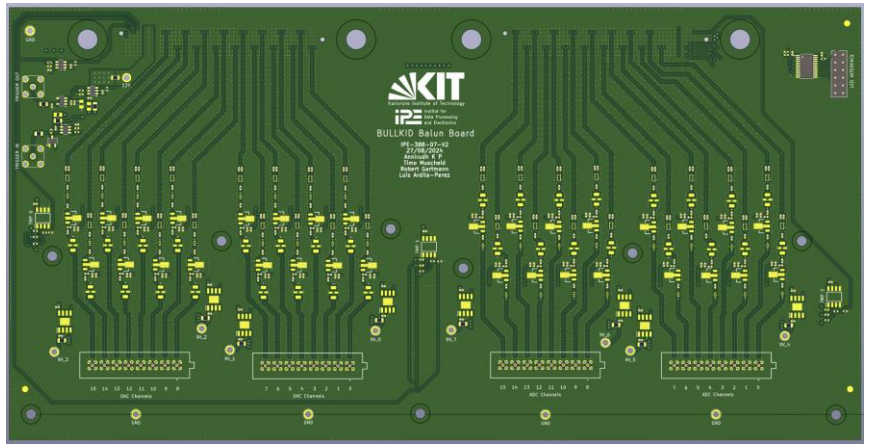


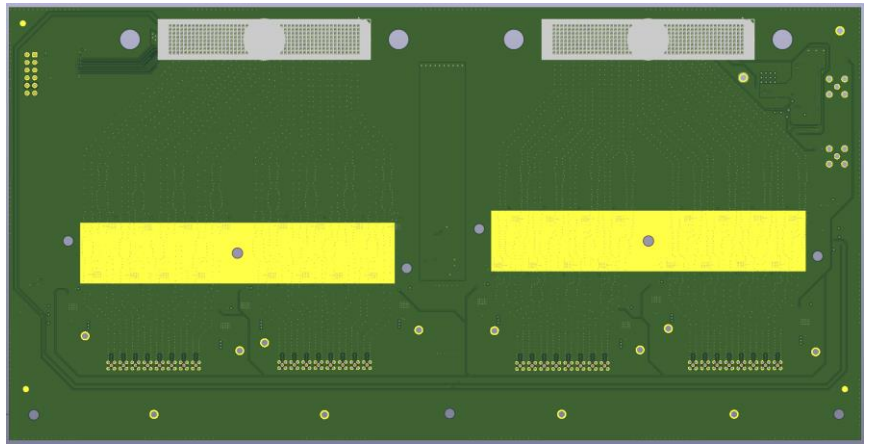
room-temperature

cryogenic domain

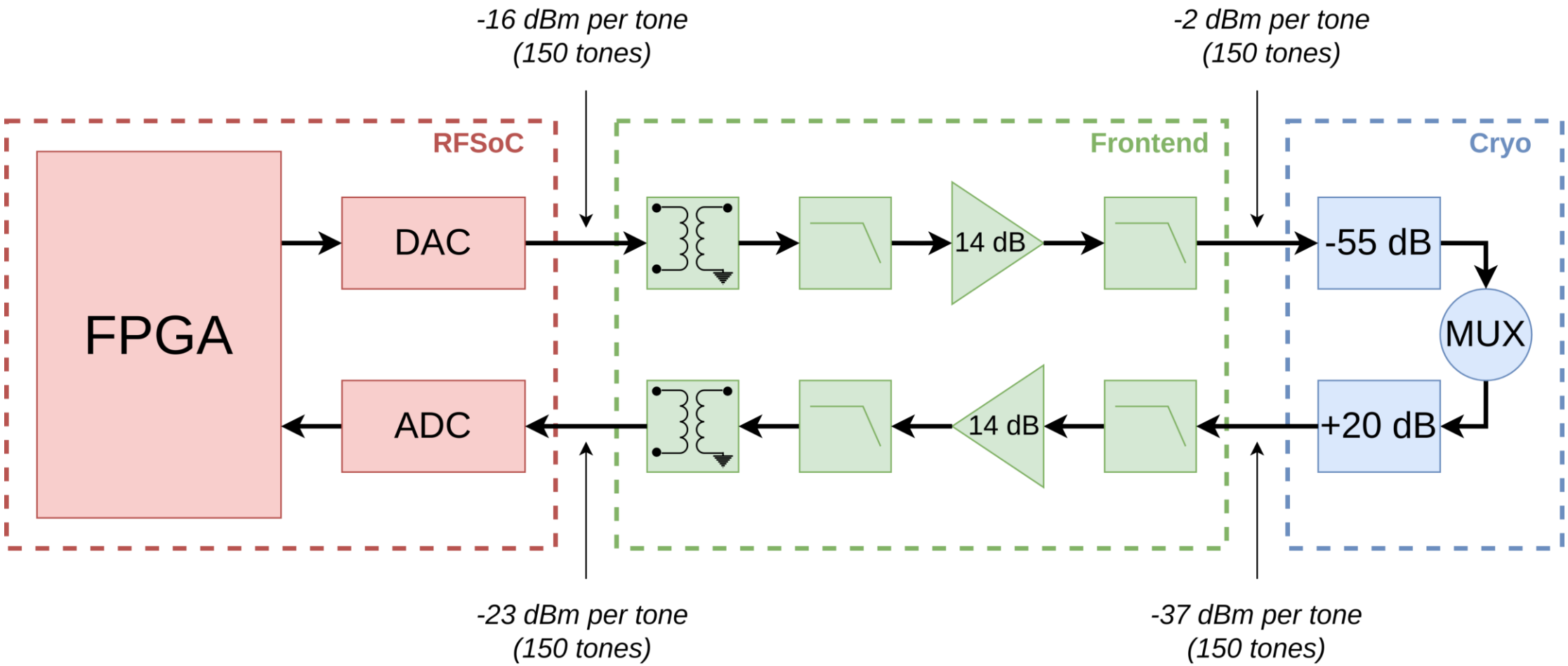
Custom frontend v2

- Supports all 16 cryogenic lines (TX and RX)
- Includes transformer, LP filters, amplifier on each line
- Additional feature
  - Temperature sensors
  - Trigger input/output for calibration





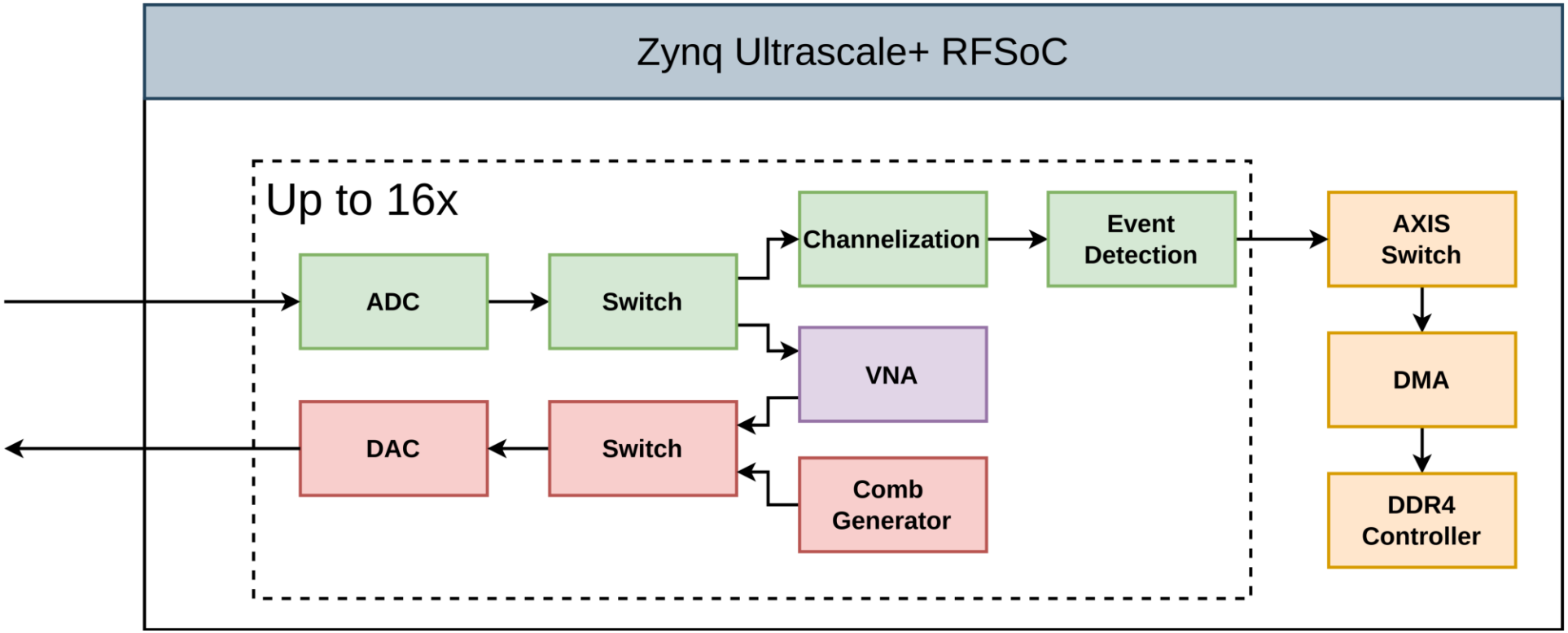
Signal flow


-16 dBm per tone
(150 tones)
-2 dBm per tone
(150 tones)
RFSoC
Frontend
Cryo
FPGA
DAC
ADC
14 dB
14 dB
-55 dB
MUX
+20 dB
-23 dBm per tone
(150 tones)
-37 dBm per tone
(150 tones)

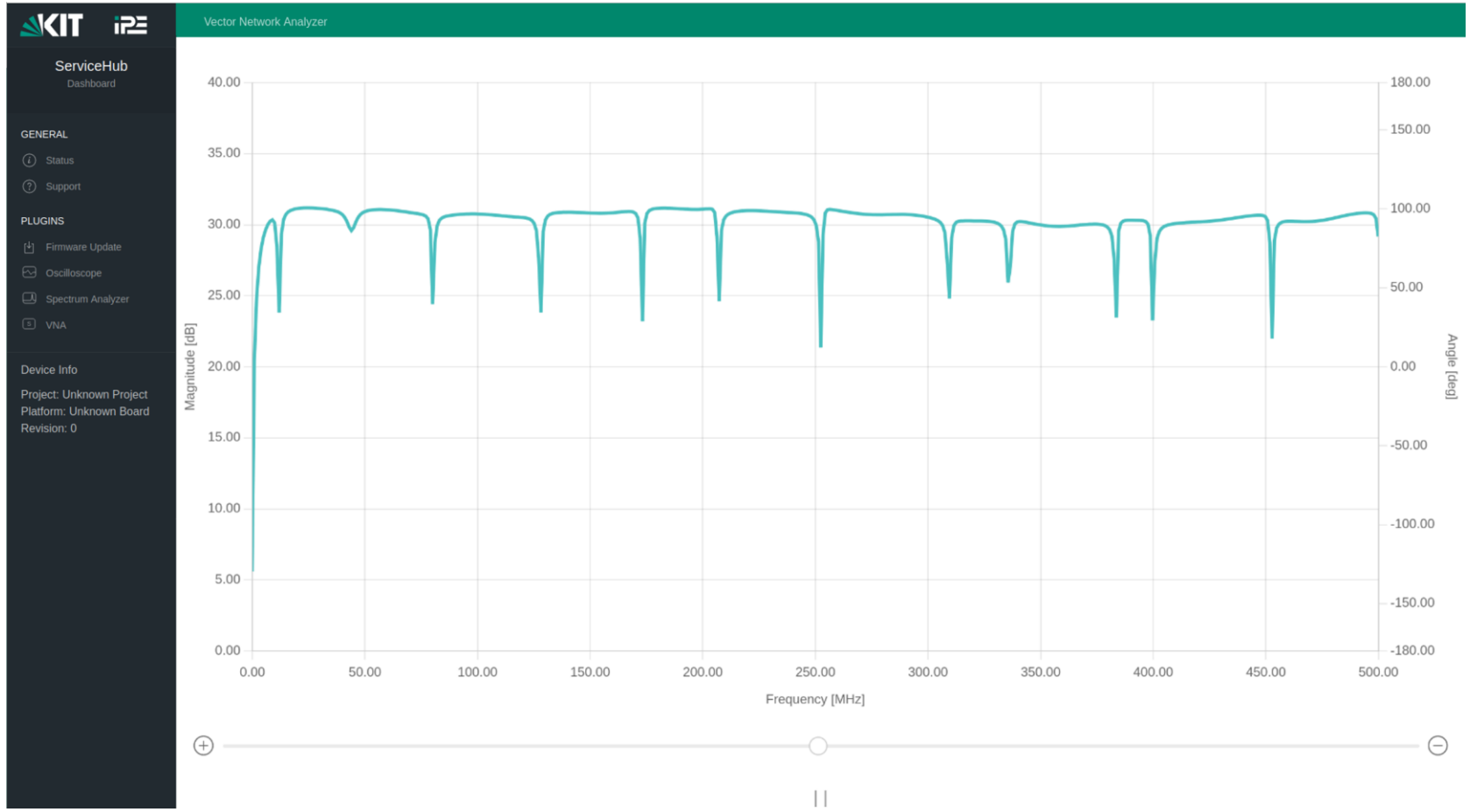
System to be installed in Rome

- Partially assembled frontend (4 channels TX+RX)
- Final preparations of the box for shipment
- Funding for a full hardware system secured
- Next measurement campaign: 23.10.2024 – 25.10.2024 in Rome

Firmware overview



VNA



- Use-case: Resonator search
- Automatic script for peak finding
- Data taking via Python API or web interface

Ongoing work

- Hardware
  - Characterization measurements of new frontend-board
  - Integrate trigger output for LED calibration system
- FPGA-Firmware
  - Properly include VNA module into all readout lines
  - Channelization (tone separation) for 145 detectors per MUX
- Software
  - Conversion from binary to h5 file format

Time schedule

- 2024: Operation of one prototype wafer with 60 MKIDs
  - Firmware of room-temperature readout system ready with simple trigger
  - Custom frontend v2 to be installed
- 2025: Operation of one fullscale wafer with 145 MKIDs
  - First tests in the cavern at Gran Sasso
  - Change parameters of channelization module
  - Implement complex trigger to reduce background noise
- 2026: Operation of full experiment with 15 wafers à 145 MKIDs
  - Scale firmware up to support multiple cryogenic lines