MasterPanel

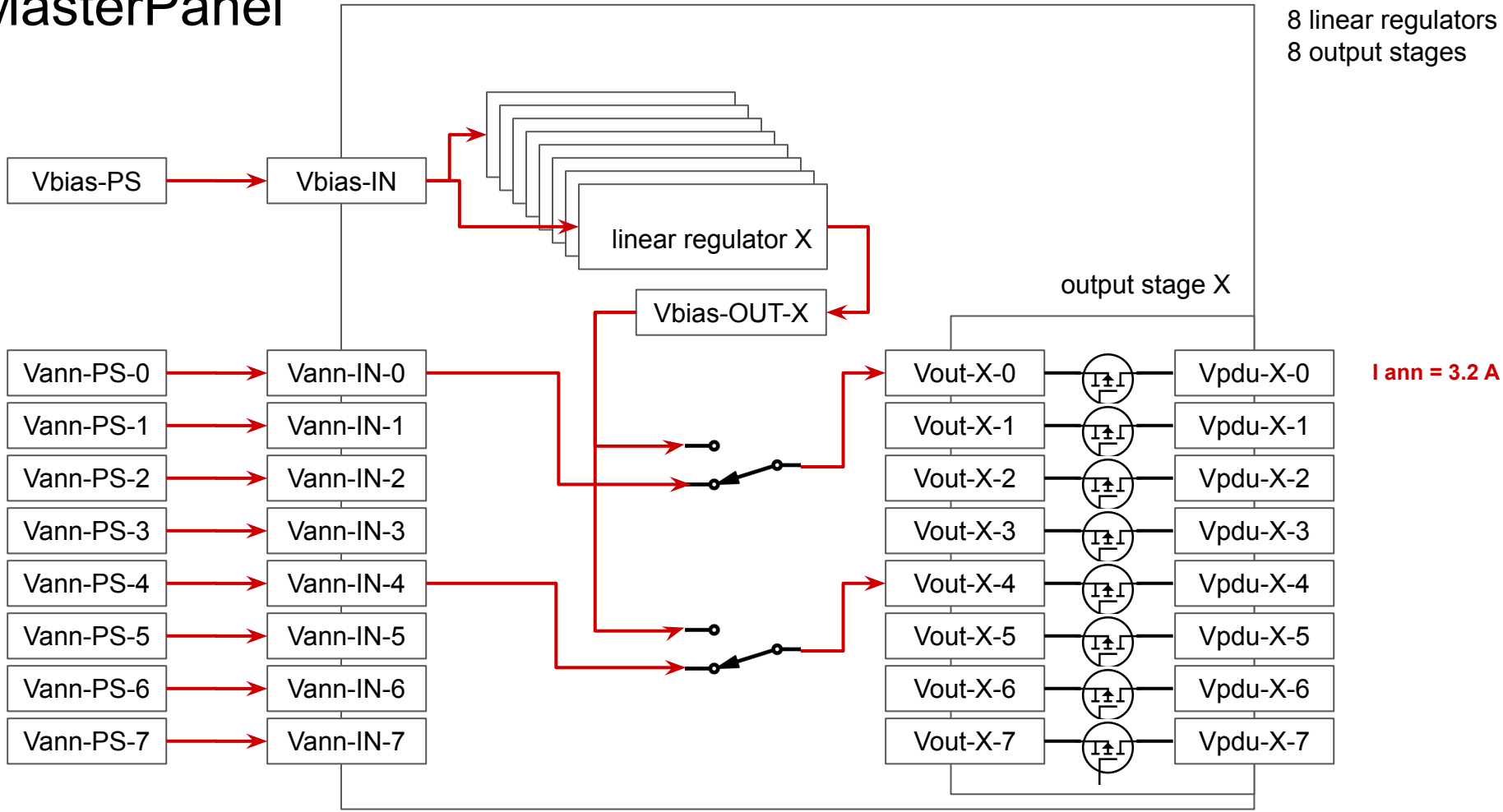
SiPM elettronica, 23 settembre 2024

The work of the MasterPanel

- **patch panel for the front-end electronics**
  - MP receives the input LV from the PS
    - 1.4 V analog, 1.4 V digital low, 2.7 V digital high
  - MP distributes the LV to the connectors to the FEE
    - 1 MP / 8 PDU scheme = 32 FEB + 8 RDO connectors on the MP output side
  - space considerations
    - 1 MP can not be bigger than 100 x 200 mm^2 (2 x 4 PDU) = 20000 mm^2
    - one FEB/RDO connectors is ~ 150 mm^2 → 150 x 40 = 6000 mm^2
    - assume similar space is taken by the input connectors
    - there are 8000 mm^2 for services: 100 x 80 mm^2
- **PDU services: NTC, Vbias, Vannealing**
  - MP receives 32 NTC voltages from PDU and converts into ADC
    - 1 32-channel ADC? 1 ADC + 32-channel multiplexer?
  - MP receives one input Vbias-in (64 V) from PS and generates 8 output regulated Vbias-out (40-60 V)
    - Vbias-out, one for each PDU
  - MP receives 8 input Vann-in (-12 V)

MasterPanel

X = 0 … 7
8 linear regulators
8 output stages



I ann = 3.2 A

Vbias distribution

summary table

ne avevamo discusso tempo fa, anche a riunione ePIC-DAQ
avevo mostrato possibili opzioni, ma quella che troverei più appetibile / realizzabile è quella in cui abbiamo un regolatore Vbias MasterPanel per ogni PDU
assumendo che una scheda MasterPanel serve 8 PDU = 8 regolatori per scheda MasterPanel (che è quello che abbiamo nella scheda MasterLogic v2)

	1 main 4 PDU	**1 main 52 CAEN 4 PDU**	**1 main 52 ML3 4 PDU**	**1 main 208 ML3 4 PDU**
$N_{primary}$	312	6	6	6
$N_{primary}$ / sector	52	1	1	1
$V_{primary}$ (V)	64	12	64	64
$I_{primary}$ (A)	< 1 mA	2	2	1
Granularity	1024	1024	1024	256
uController	no	yes	yes	yes

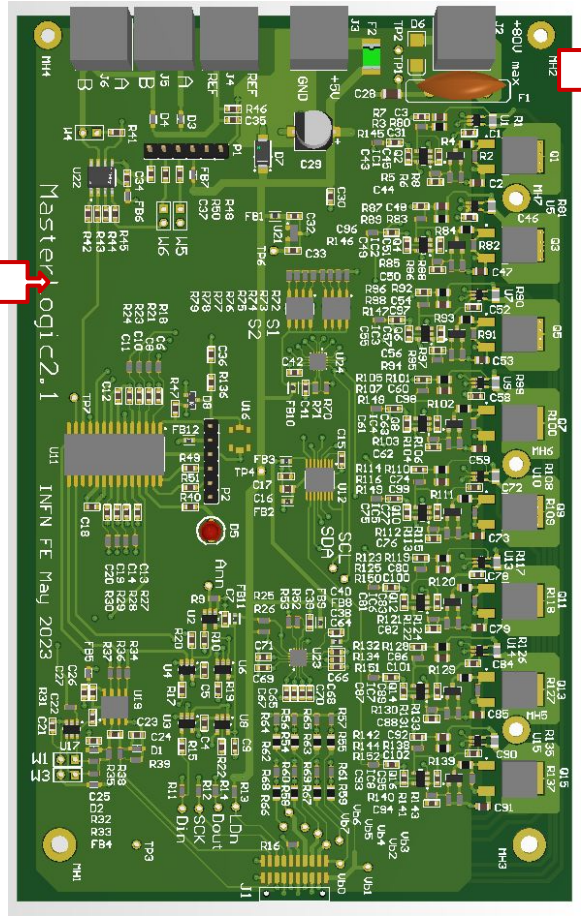
i numeri non sembrano tutti corretti al 100% in questa tabella

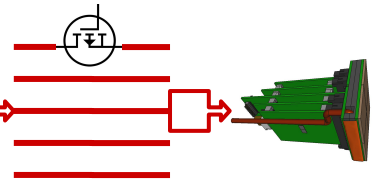
Vbias distribution

MasterPanel board

64 V
1.5 A

30 mA





1 MasterPanel
8 PDU

per ogni PDU
- 1 regolatore lineare
- 8 MOSFET per capacità di spegnere indipendentemente

regolazione Vbias comune a 256 SiPM
capacità di spegnere a 32 SiPM

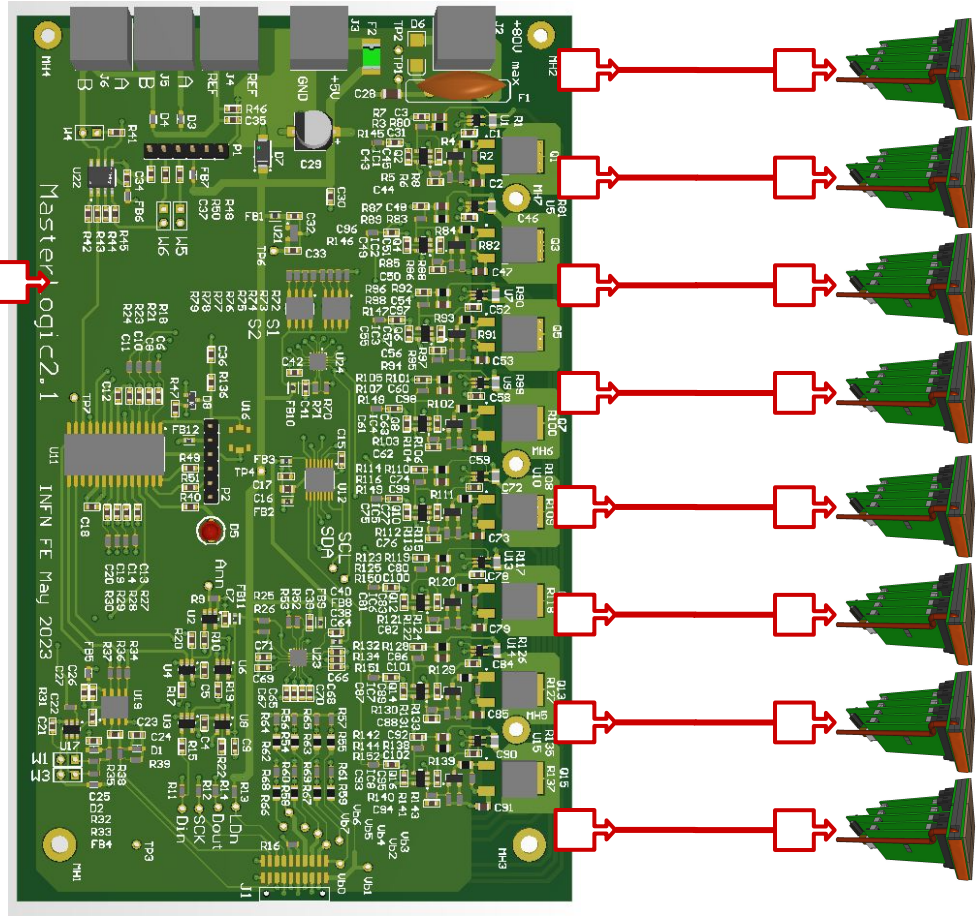
quindi in totale sulla MasterPanel
- 8 regolatori lineari
- 64 MOSFET

Vbias distribution

MasterPanel board

64 V
1.5 A

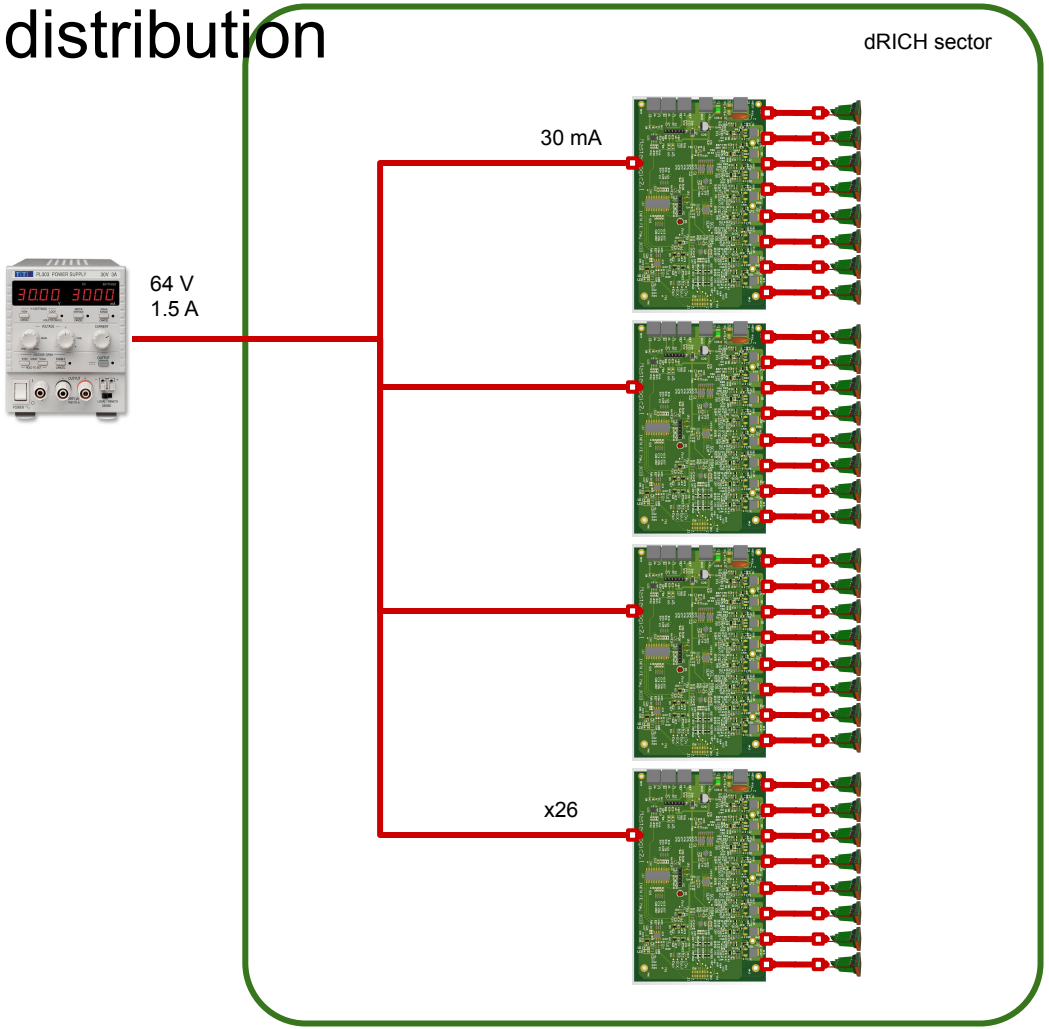
30 mA



sulla MasterLogic v2 i regolatori consumano ognuno 3.3 mA quando l'uscita è a 50 V

8 canali sono circa 30 mA

Vbias distribution



una MasterPanel per 8 PDU
in un settore ci sono 208 PDU

→ in un settore ci sono 26 MasterPanel

se ogni MasterPanel consuma 30 mA

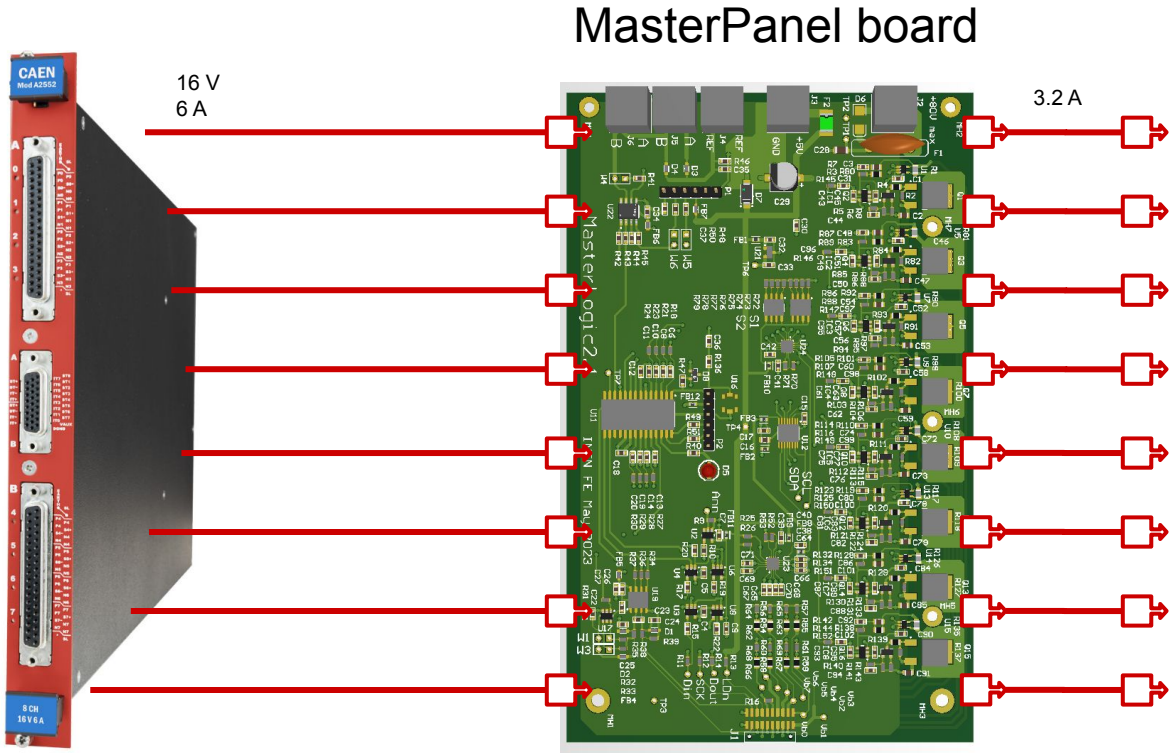
30 mA per 26 MasterPanel
= 0.8 A dal canale primario

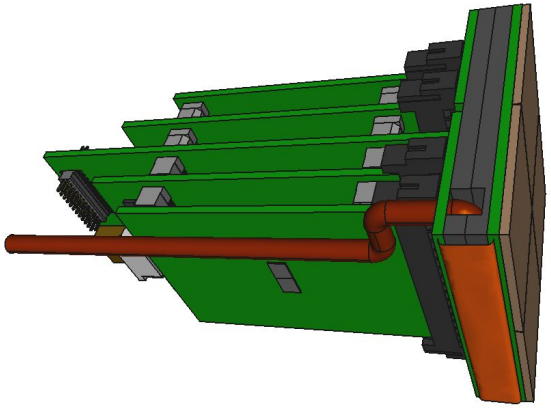
al momento la CAEN una scheda così non ce l'ha,
ma sta facendo una scheda 64 V 1.5 A

esistono
8 V 12 A
16 V 6 A
32 V 3 A
quindi la prossima è la 64 V 1.5 A

Vannealing distribution

2 Vbias input lines for each FEB
32 SiPM / Vbias input line
= 3.2 A for each line during annealing (max)

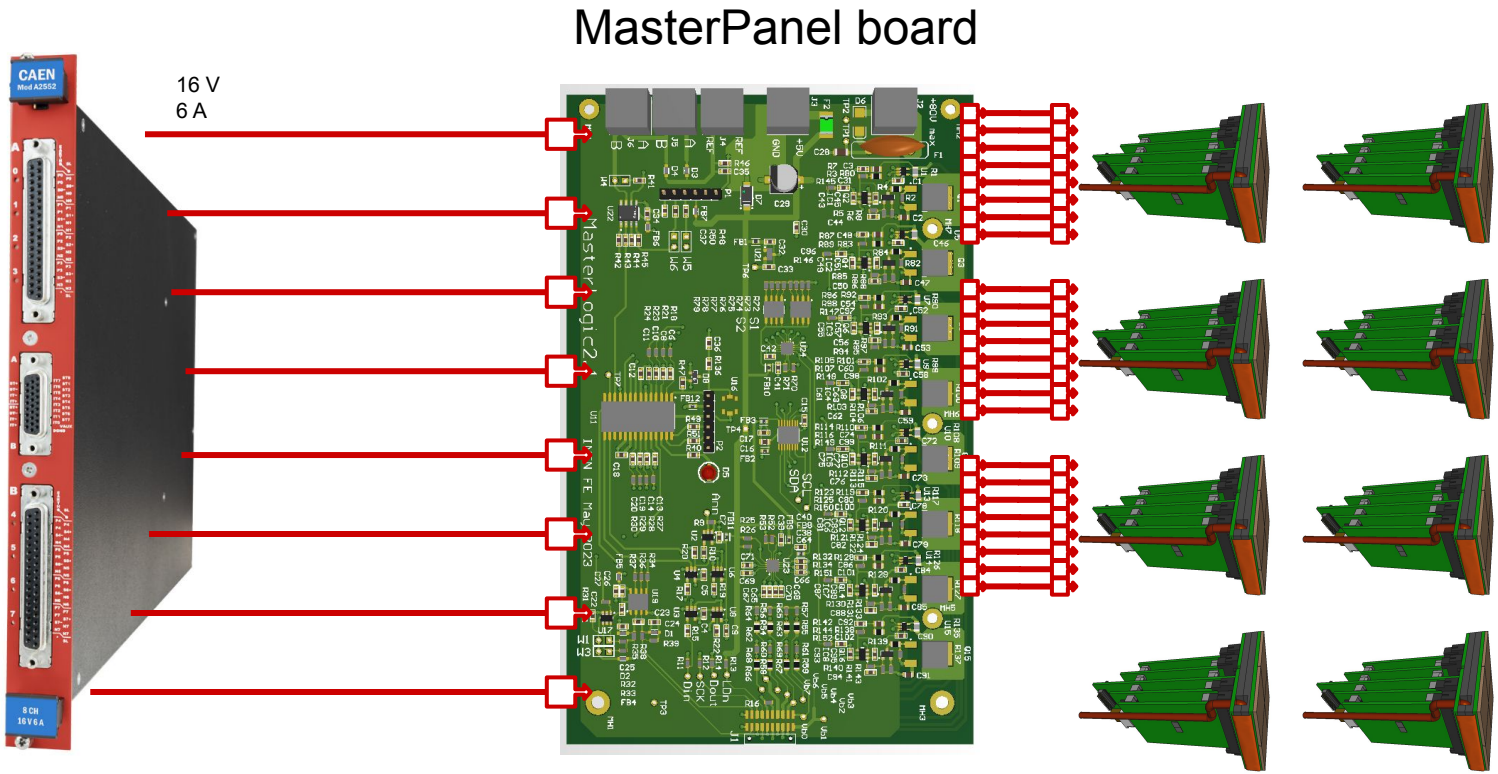




but, 1248 8-channel CAEN boards ar e a bit too much and are not needed given that we do not do annealing all at the same time
(that would be 150-300 kW)

fan-out to 8 PDUs

Vannealing distribution

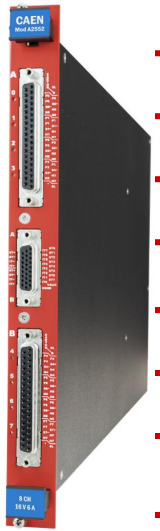


fan-out to 8 PDUs with MOSFETs to select which PDU is doing annealing
note: we want to do annealing of a full PDU

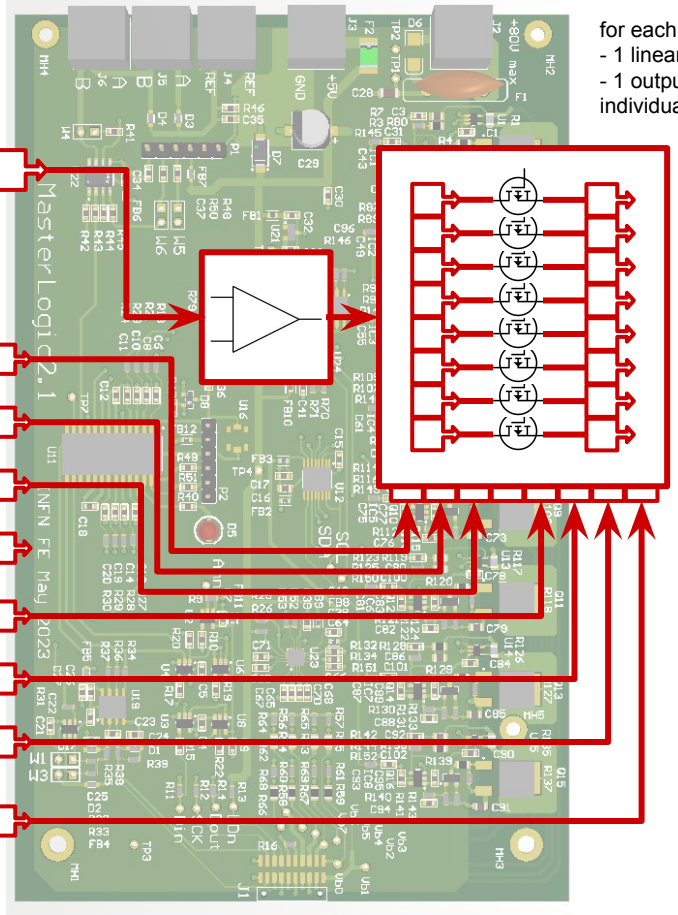
MasterPanel

64 V
1.5 A

1 Vbias input

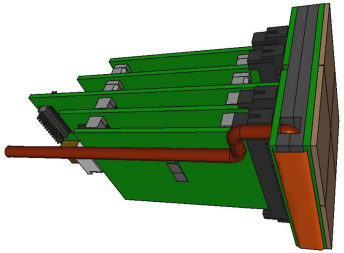


8 Vann inputs



for each PDU
- 1 linear regulator for Vbias
- 1 output stage with 8 bias lines with individual ON/OFF control

cable



NORMAL operation
Vbias-in → regulator → 8x V-out

ANNEALING operation
8x Vann-in → 8x V-out