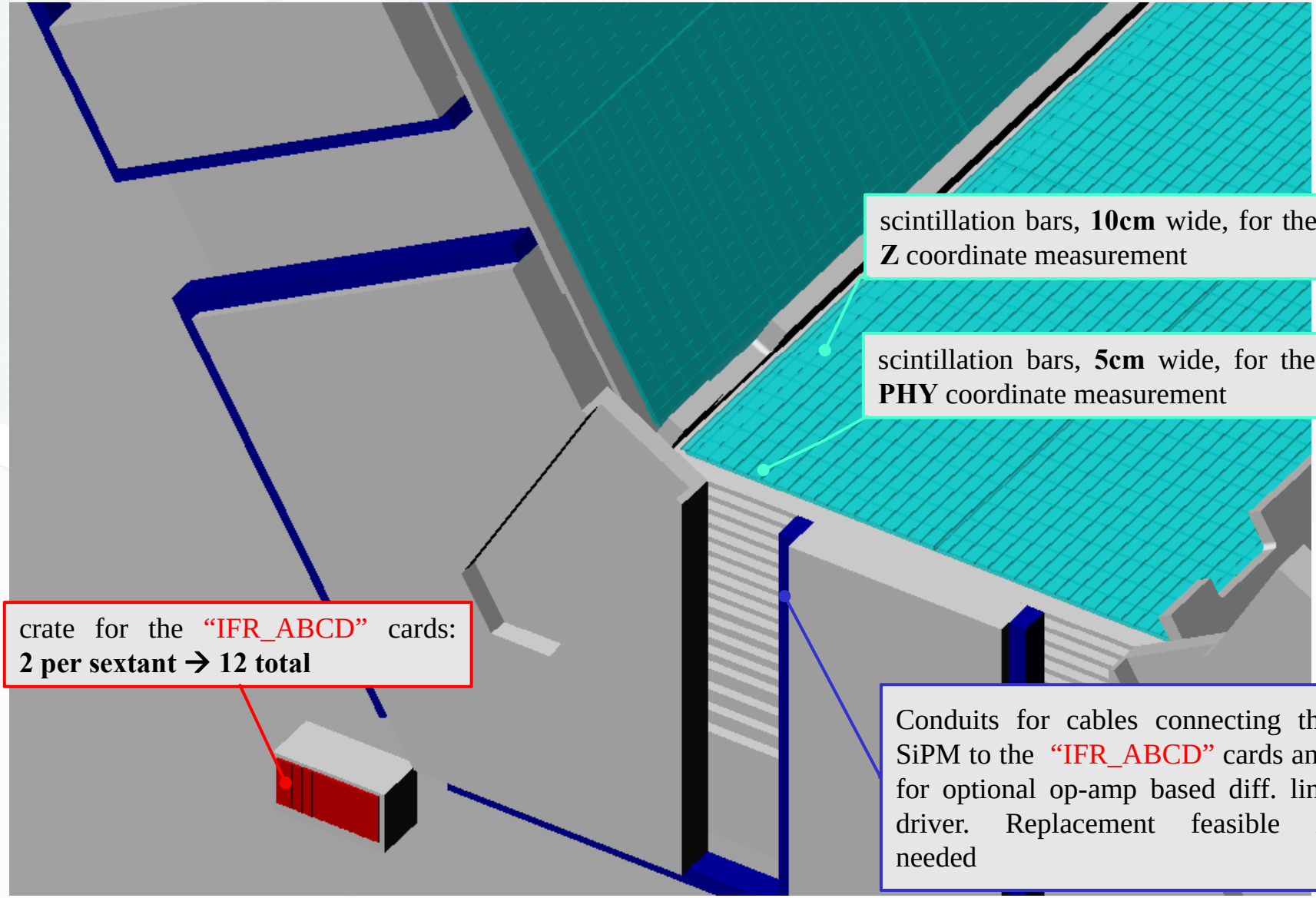
SuperB IFR electronics: report at the SuperB ETD meeting

SuperB IFR electronics: report at the SuperB ETD meeting

- features of the current baseline IFR detector design with "binary mode" readout
  - layout of the detector elements in the barrel
  - layout of the detector elements in the endcaps
  - passive Single Ended vs active Differential options for "picking-up" the signals from SiPM
  - block diagram of the "IFR_ABCD" front end card
- channel number estimation
  - barrel
  - endcaps
- data rate / data link count estimation
  - at nominal conditions (trigger rate 150KHz)
  - at higher luminosity (trigger rate 500KHz)
- addressing the radiation issues
  - background rates estimates at the location of IFR front end electronics
  - measurement of neutron induced SEE in FPGA at the INFN Laboratori Nazionali di Legnaro (exploiting beam time scheduled for SiPM test; thanks to Roberto Stroili, Flavio Dal Corso, INFN Padova)
  - measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro (being planned)

features of the current baseline IFR detector design with "binary mode" readout: barrel



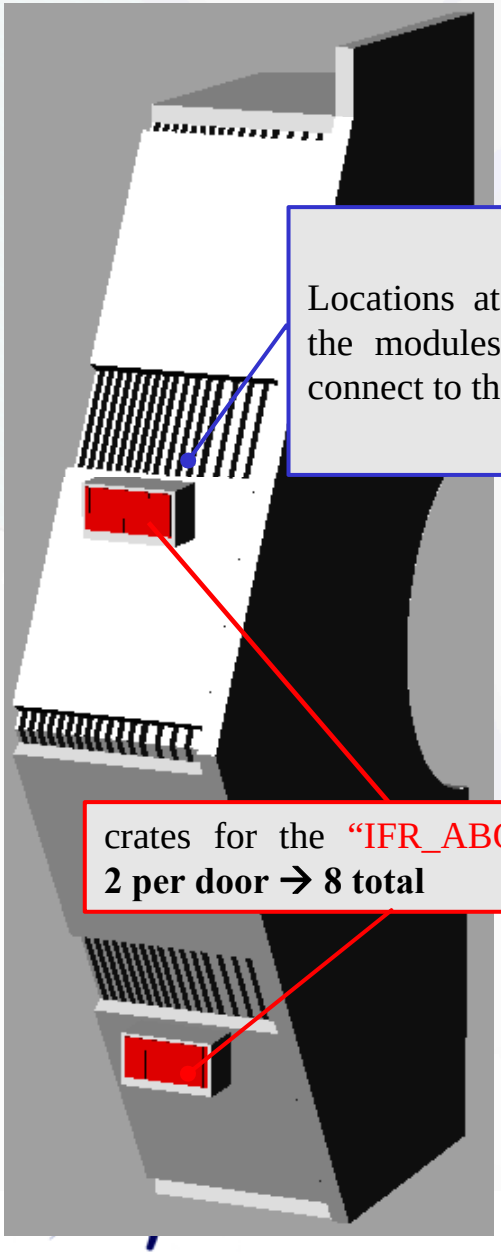
scintillation bars, **10cm** wide, for the **Z** coordinate measurement

scintillation bars, **5cm** wide, for the **PHY** coordinate measurement

crate for the "IFR_ABCD" cards: **2 per sextant → 12 total**

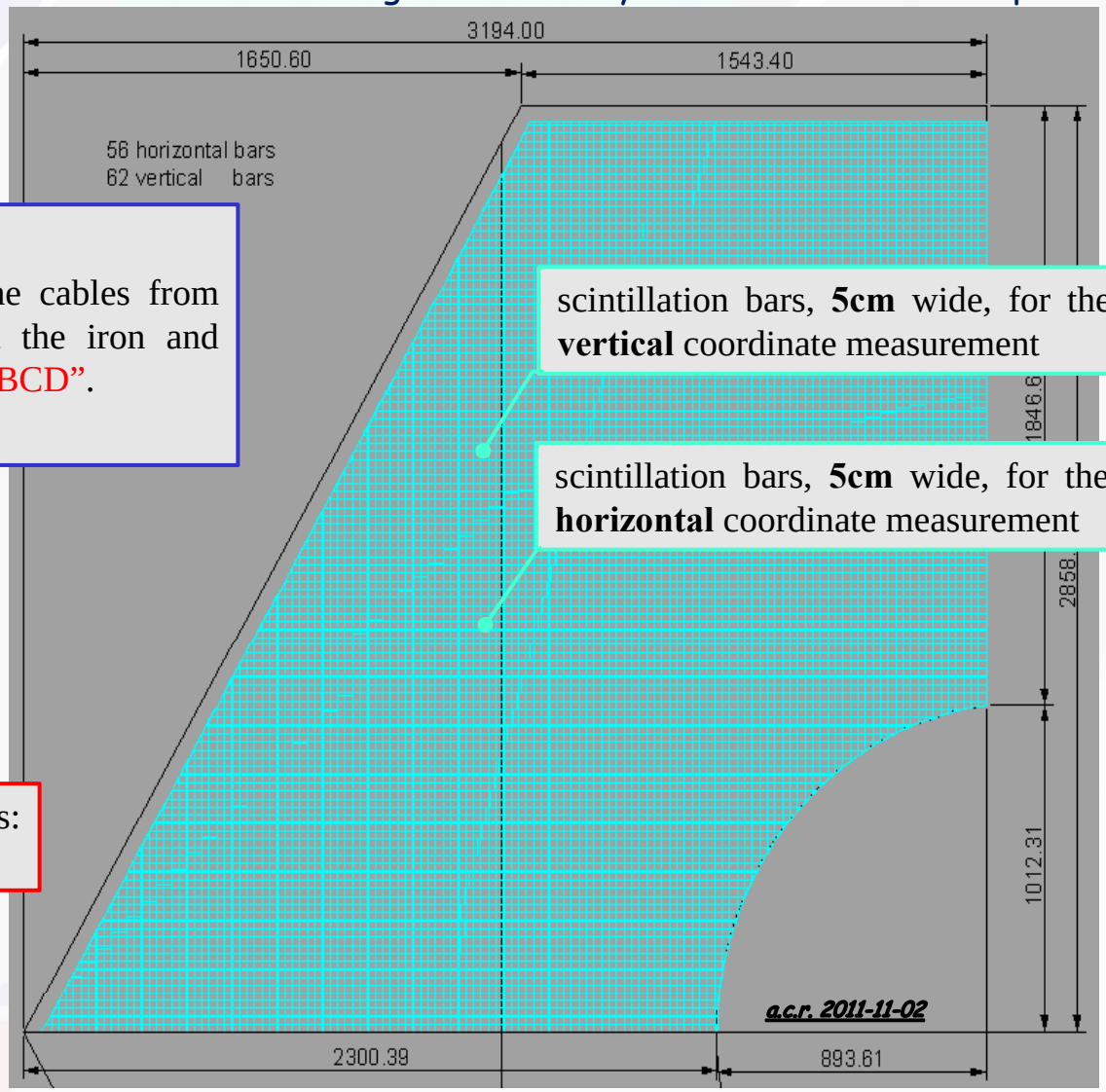
Conduits for cables connecting the SiPM to the "IFR_ABCD" cards and for optional op-amp based diff. line driver. Replacement feasible if needed

features of the current baseline IFR detector design with "binary mode" readout: endcaps



Locations at which the cables from the modules can exit the iron and connect to the "IFR_ABCD".

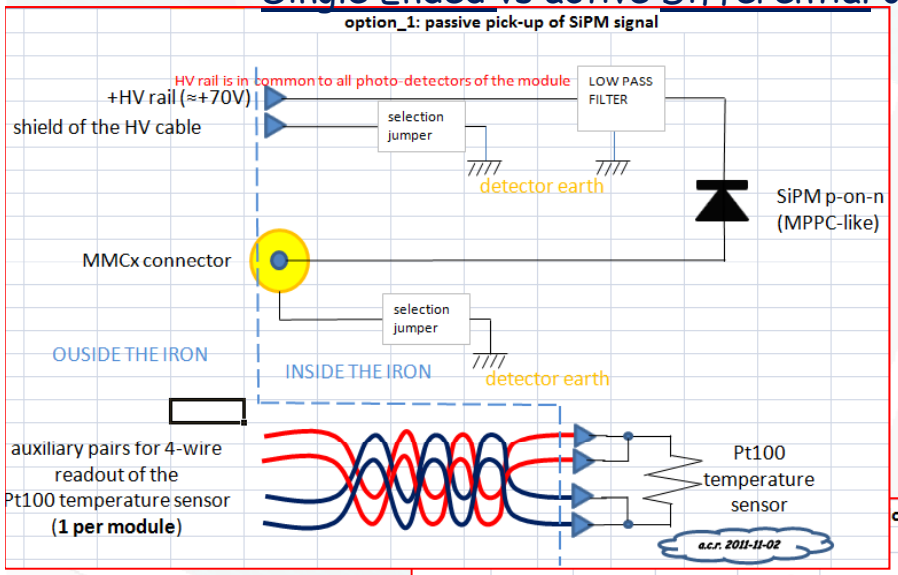
crates for the "IFR_ABCD" cards: **2 per door → 8 total**

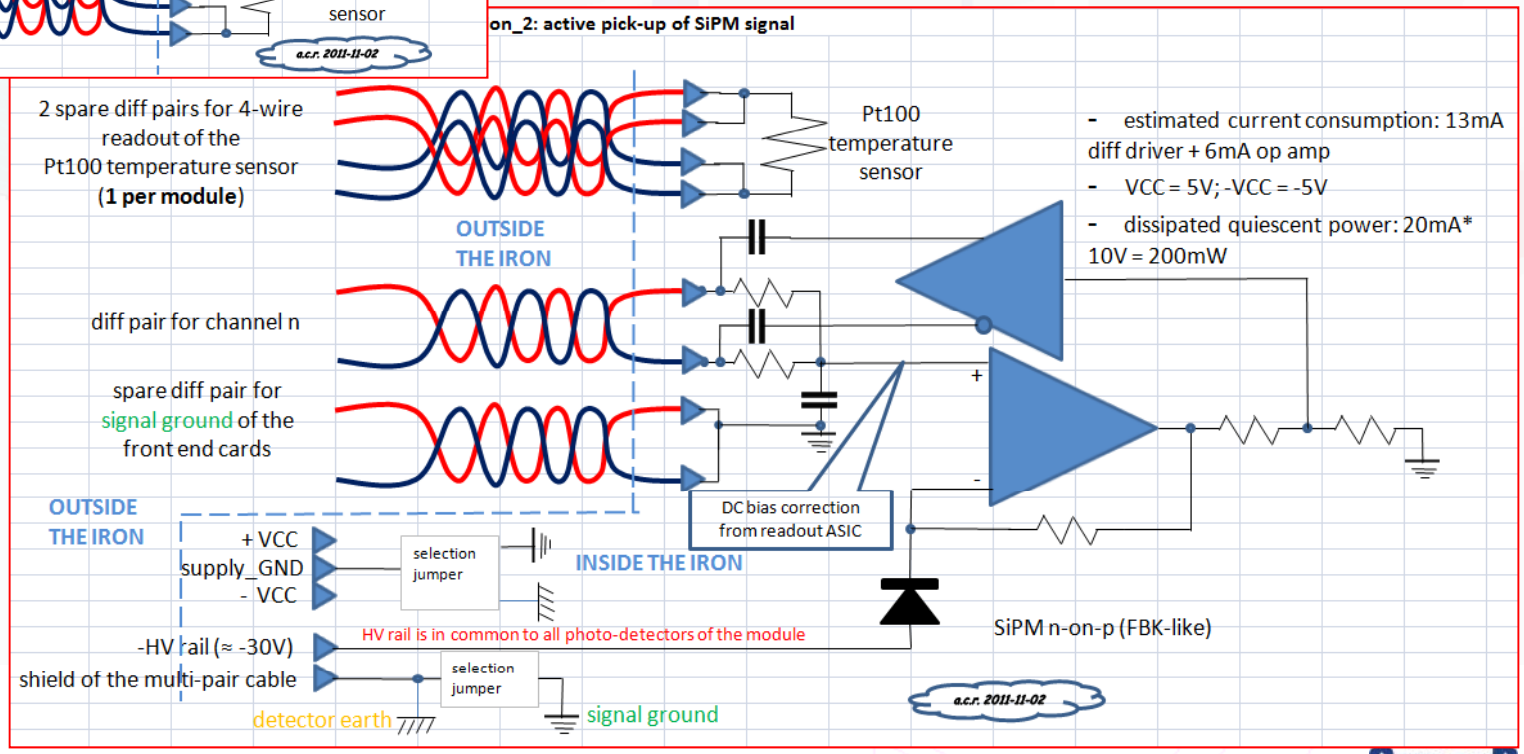


scintillation bars, **5cm** wide, for the **vertical** coordinate measurement

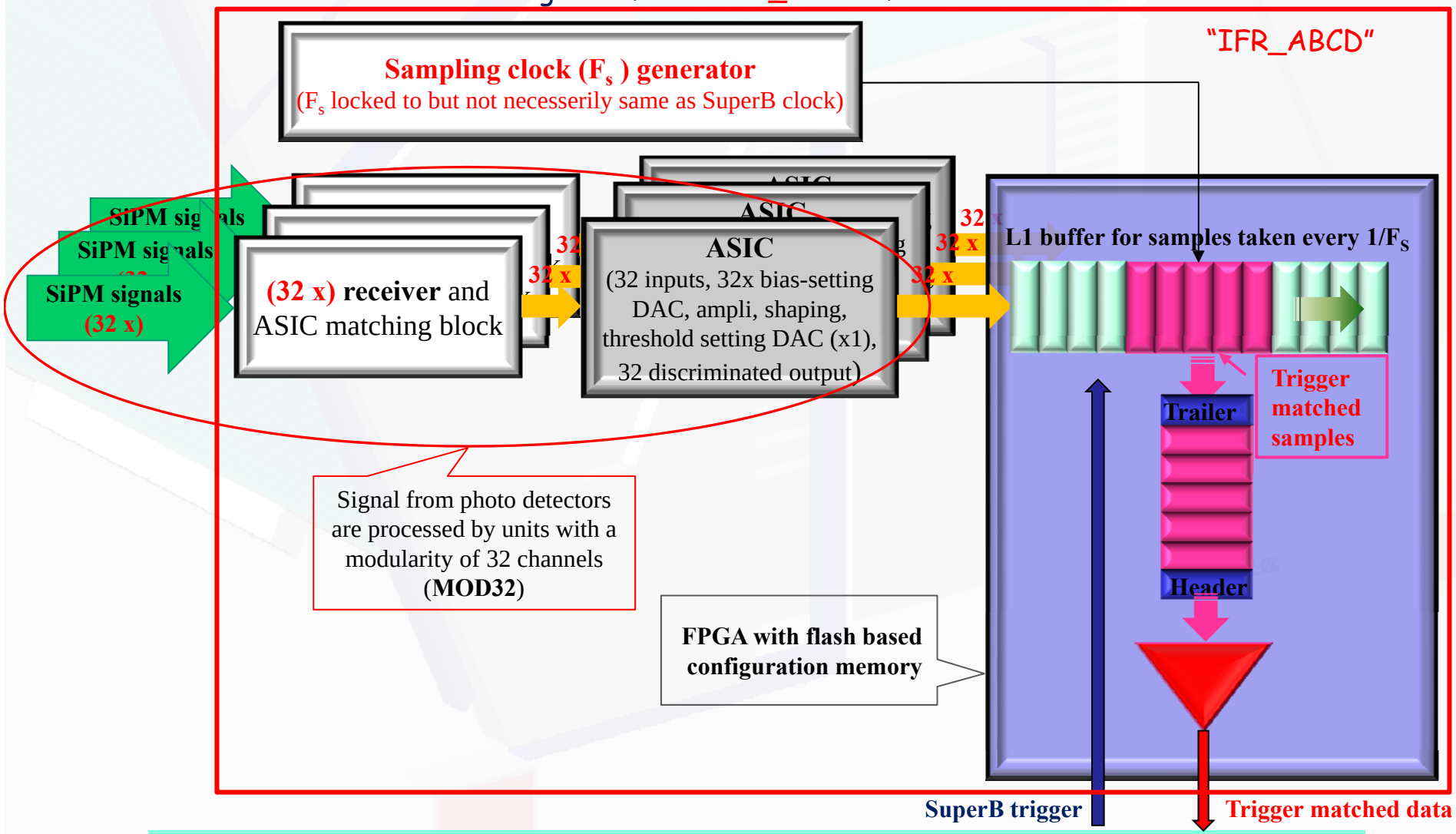
scintillation bars, **5cm** wide, for the **horizontal** coordinate measurement

features of the current baseline IFR detector design with "binary mode" readout:
Single Ended vs active Differential options for "picking-up" the signals from SiPM





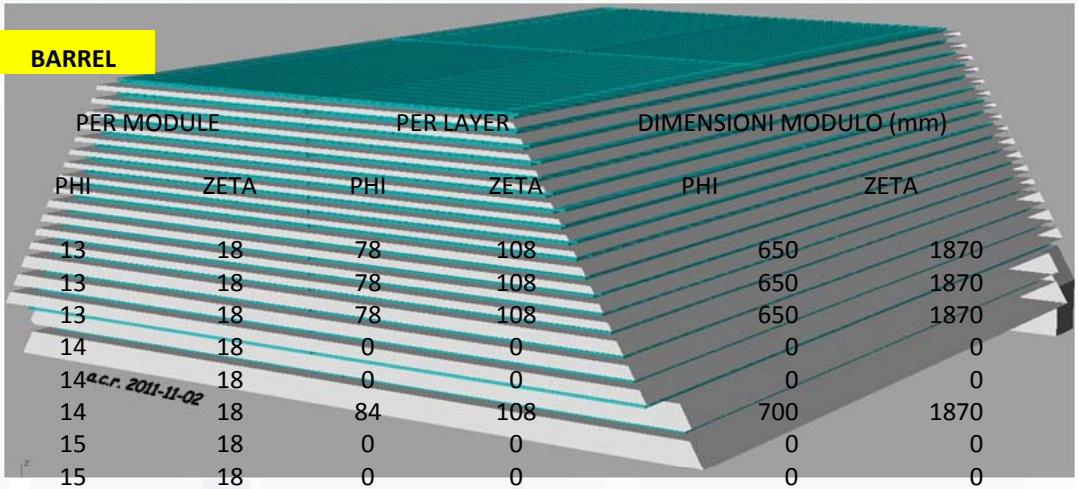
features of the current baseline IFR detector design with "binary mode" readout: block diagram of the "IFR_ABCD" front end card



Two "CONCENTRATOR / DATA LINK DRIVER" cards in the "IFR-ABCD" front end crates are connected to the FCTS and to the ROM: they distribute the trigger to the "IFR_ABCD" cards, collect the matched data, merge the streams into the de-randomizer FIFO and drive the data link (1 or 2 per concentrator) toward the ROMs

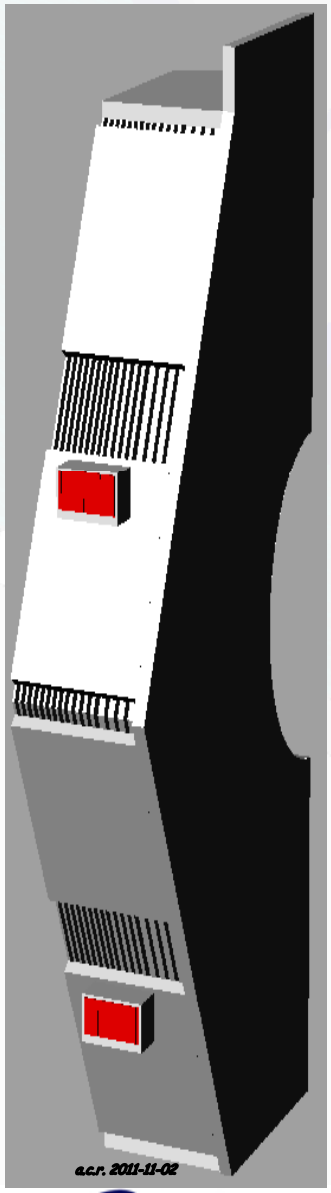
channel number estimation: barrel

BARREL



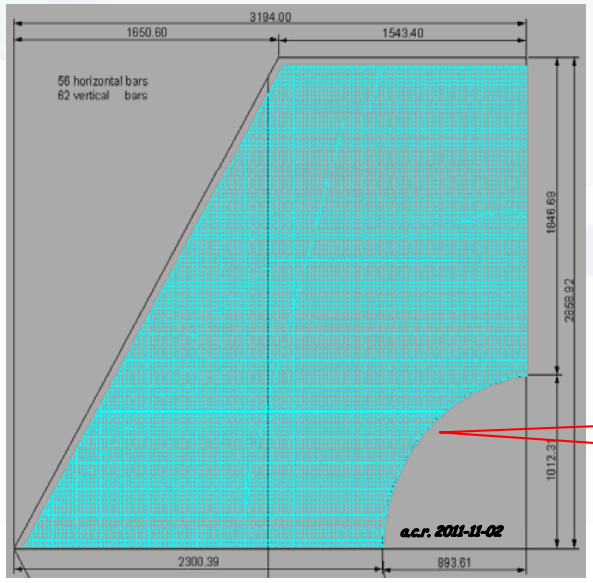
				PER MODULE		PER LAYER		DIMENSIONI MODULO (mm)	
LAYER WIDTH	LAYER	No.Modules per layer	LAYER ENABLE	PHI	ZETA	PHI	ZETA	PHI	ZETA
1963	1	6	1	13	18	78	108	650	1870
1987	2	6	1	13	18	78	108	650	1870
2050	3	6	1	13	18	78	108	650	1870
2113	4	6		14	18	0	0	0	0
2176	5	6		14	18	0	0	0	0
2240	6	6	1	14	18	84	108	700	1870
2304	7	6		15	18	0	0	0	0
2367	8	6		15	18	0	0	0	0
2431	9	6		16	18	0	0	0	0
2494	10	8	1	12	18	96	144	600	1870
2569	11	8		12	18	0	0	0	0
2641	12	8		13	18	0	0	0	0
2712	13	8	1	13	18	104	144	650	1870
2784	14	8		13	18	0	0	0	0
2879	15	8	1	14	18	112	144	700	1870
2973	16	8		14	18	0	0	0	0
3068	17	8		15	18	0	0	0	0
3144	18	8	1	15	16	120	128	750	1870
3296	19	8	1	16	16	128	128	800	1870
NUMBER OF MODULES per sextant:	134	**TOTAL NUMBER OF MODULES**	**804**						
		TOTAL PER SEXTANT	9	TOTAL PER SEXTANT	1998	878	1120		
NUMBER OF SEXTANTS	6	TOTAL PER BARREL	54	**TOTAL CHANNELS PER BARREL**	**11988**	5268	6720		

channel number estimation: endcaps



ENDCAP

horizontal bars per module:	56
vertical bars per module:	62
channel count per module:	118
NO_OF_MOD_PER_LAYER_EC:	2
horizontal bars per layer	112
vertical bars per layer	124
NUMBER OF LAYER PER DOOR	9
NUMBER OF DOORS IN ENDCAPS	4



TOTAL NUMBER OF MODULES IN ENDCAPS:	**72**
horizontal bars per door:	1008
vertical bars per door:	1116
TOTAL HORIZONTAL BARS:	4032
TOTAL VERTICAL BARS:	4464
TOTAL CHANNELS IN ENDCAPS:	**8496**

Dimensions of one endcap module

data rate / data link count estimation: at nominal conditions (trigger rate 150KHz)

BARREL

NUMBER OF CRATES PER SEXTANT	2	NUMBER OF CHANNELS PER CRATE	999
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNEL PER BOARD	83,25
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	2	NUMBER OF 32-CHANNEL PROCESSING UNITS	3
TRIGGER RATE (kHz)	150		
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)	150		
n:NUMBER OF SAMPLES PER TRIGGER	8		
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (**MOD32**)	10		
EVENT SIZE IN BYTES PER EACH **MOD32** UNIT	40	TOTAL NUMBER OF **MOD32** UNITS	432
	BARREL EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL **MOD32** UNITS)	**17280**	
TOTAL BARREL BANDWIDTH (MB/s)	2592	TOTAL BARREL BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	25,92
TOTAL NUMBER OF DATA LINK	**24**	bandwidth per link (Gbps)	**1,08**

ENDCAP

NUMBER OF CRATES PER DOOR	2	NUMBER OF CHANNELS PER CRATE	1062
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNELS PER BOARD	88,5
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	2	NUMBER OF 32-CHANNEL PROCESSING UNITS (**MOD32**) PER BOARD	3
TRIGGER RATE (kHz)	150		
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)	150		
n:NUMBER OF SAMPLES PER TRIGGER	8		
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (**MOD32**)	10		
EVENT SIZE IN BYTES PER EACH **MOD32** UNIT	40	TOTAL NUMBER OF **MOD32** UNITS	288
	ENDCAP EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL **MOD32** UNITS)	11520	
TOTAL ENDCAP BANDWIDTH (MB/s)	1728	TOTAL ENDCAP BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	17,28
TOTAL NUMBER OF DATA LINK	16	bandwidth per link (Gbps)	1,08

data rate / data link count estimation: at higher luminosity (trigger rate 500KHz)

BARREL

NUMBER OF CRATES PER SEXTANT	2	NUMBER OF CHANNELS PER CRATE	999
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNEL PER BOARD	83,25
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	4	NUMBER OF 32-CHANNEL PROCESSING UNITS	3
TRIGGER RATE (kHz)	500		
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)	150		
n:NUMBER OF SAMPLES PER TRIGGER	8		
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (**MOD32**)	10		
EVENT SIZE IN BYTES PER EACH **MOD32** UNIT	40	TOTAL NUMBER OF **MOD32** UNITS	432
		BARREL EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL **MOD32** UNITS)	**17280**
TOTAL BARREL BANDWIDTH (MB/s)	8640	TOTAL BARREL BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	86,4
TOTAL NUMBER OF DATA LINK	**48**	bandwidth per link (Gbps)	**1,8**

ENDCAP

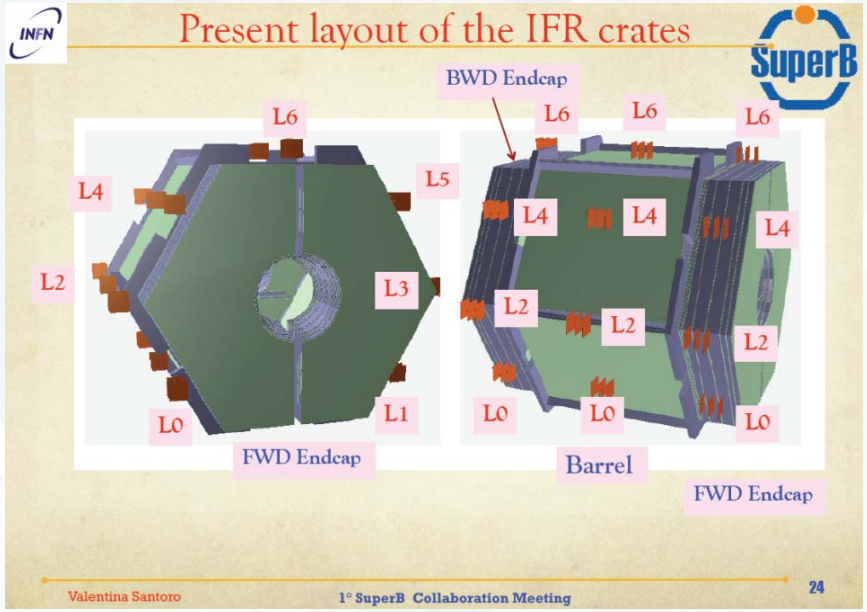
NUMBER OF CRATES PER DOOR	2	NUMBER OF CHANNELS PER CRATE	1062
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNELS PER BOARD	88,5
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	4	NUMBER OF 32-CHANNEL PROCESSING UNITS (**MOD32**) PER BOARD	3
TRIGGER RATE (kHz)	500		
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)	150		
n:NUMBER OF SAMPLES PER TRIGGER	8		
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (**MOD32**)	10		
EVENT SIZE IN BYTES PER EACH **MOD32** UNIT	40	TOTAL NUMBER OF **MOD32** UNITS	288
		ENDCAP EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL **MOD32** UNITS)	**11520**
TOTAL ENDCAP BANDWIDTH (MB/s)	5760	TOTAL ENDCAP BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	57,6
TOTAL NUMBER OF DATA LINK	**32**	bandwidth per link (Gbps)	**1,8**

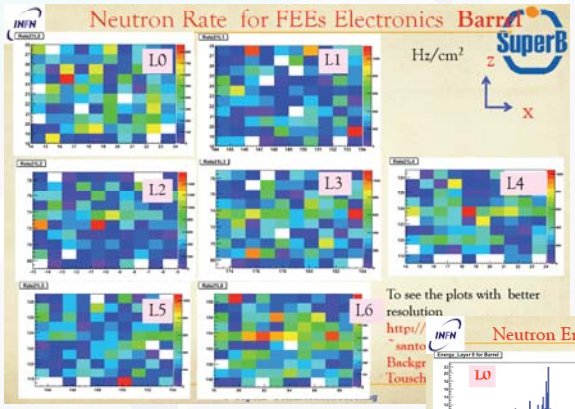
a.c.r. 2011-11-02

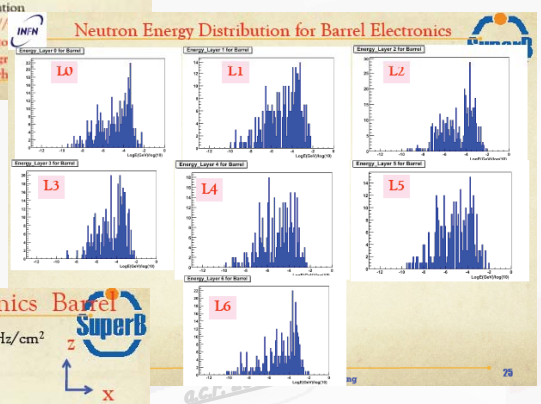
addressing the radiation issues:

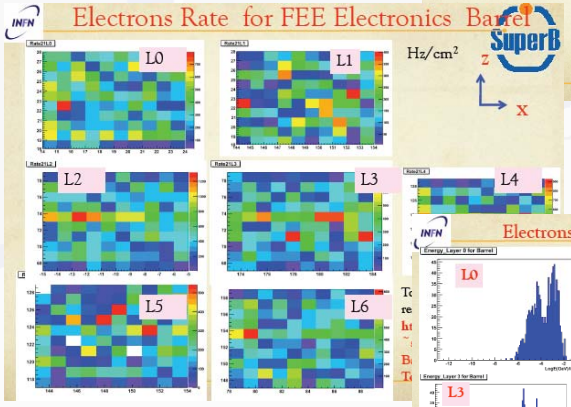
background rates estimation at the location of IFR front end electronics

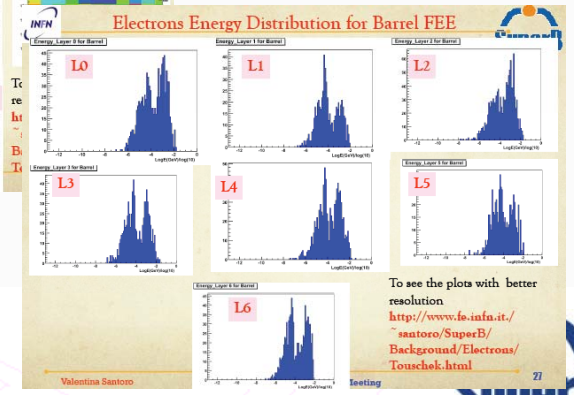
From: "IFR Background Status" Valentina Santoro INFN Ferrara







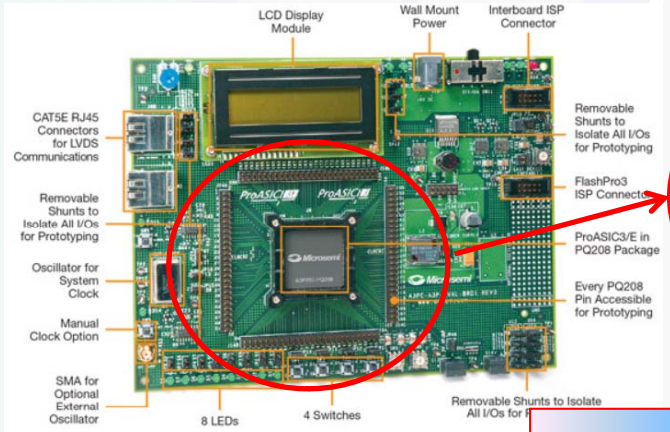




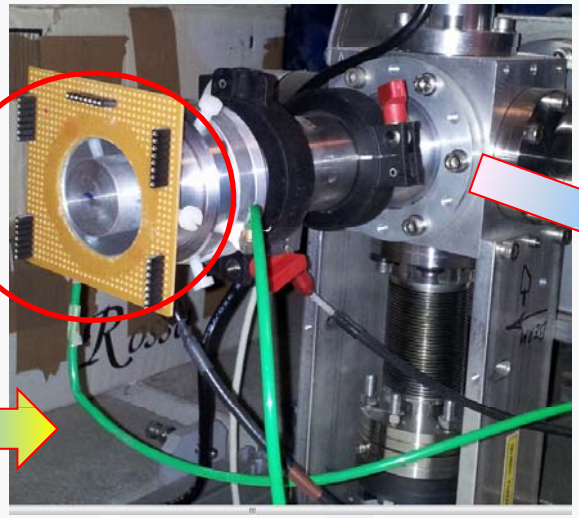
Thanks to this work we have now an estimate of the expected radiation doses at the locations of the front end electronics crates, according to the baseline design.

This will allow us to properly plan the irradiation tests of the "compact" front end design based on the EASIROC.

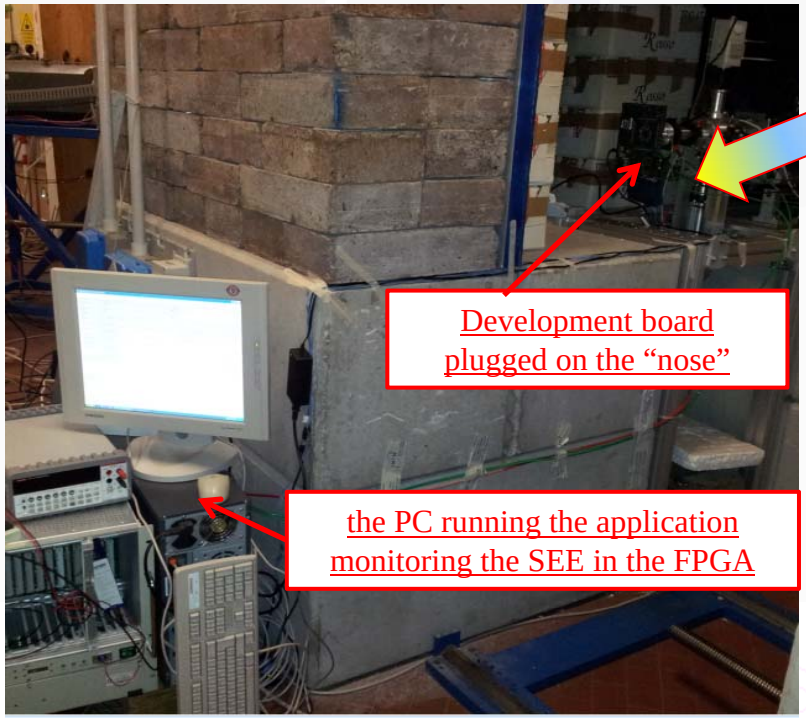
addressing the radiation issues:
measurement of neutron induced SEE in FPGA at the INFN Laboratori Nazionali di Legnaro



Evaluation board with an A3PE1500-PQ208 FPGA




Development board plugged on the "nose"

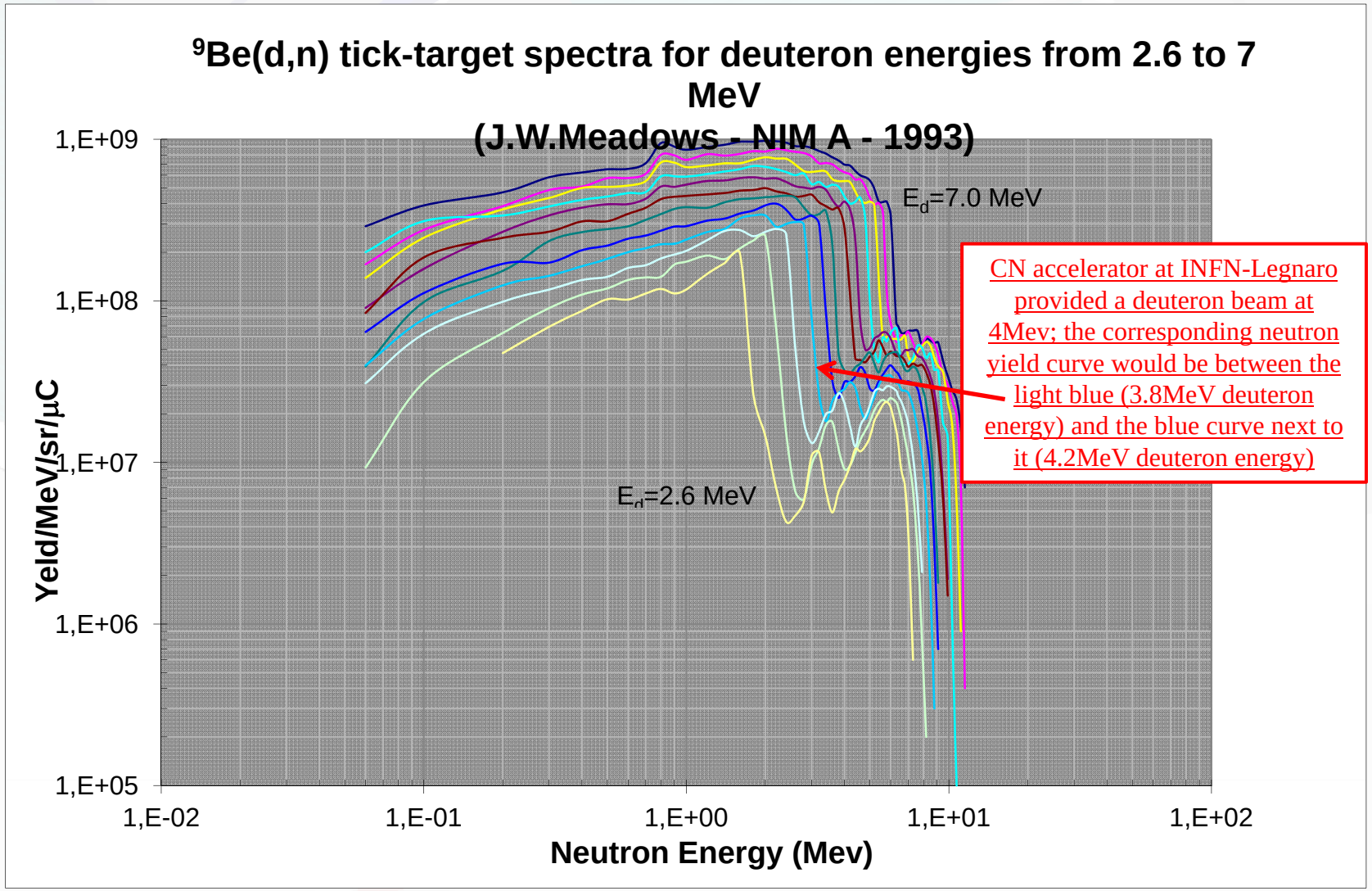

Development board plugged on the "nose"

the PC running the application monitoring the SEE in the FPGA

Acknowledgements:

We exploited beam time which had been allocated by our colleagues Roberto Stroili and Flavio Dal Corso who also provided the information needed to estimate the neutron flux.

addressing the radiation issues:
measurement of neutron induced SEE in FPGA at the INFN Laboratori Nazionali di Legnaro



CN accelerator at INFN-Legnaro provided a deuteron beam at 4Mev; the corresponding neutron yield curve would be between the light blue (3.8MeV deuteron energy) and the blue curve next to it (4.2MeV deuteron energy)

(excel file by Flavio Dal Corso)

addressing the radiation issues:
measurement of neutron induced SEE in FPGA at the INFN Laboratori Nazionali di Legnaro

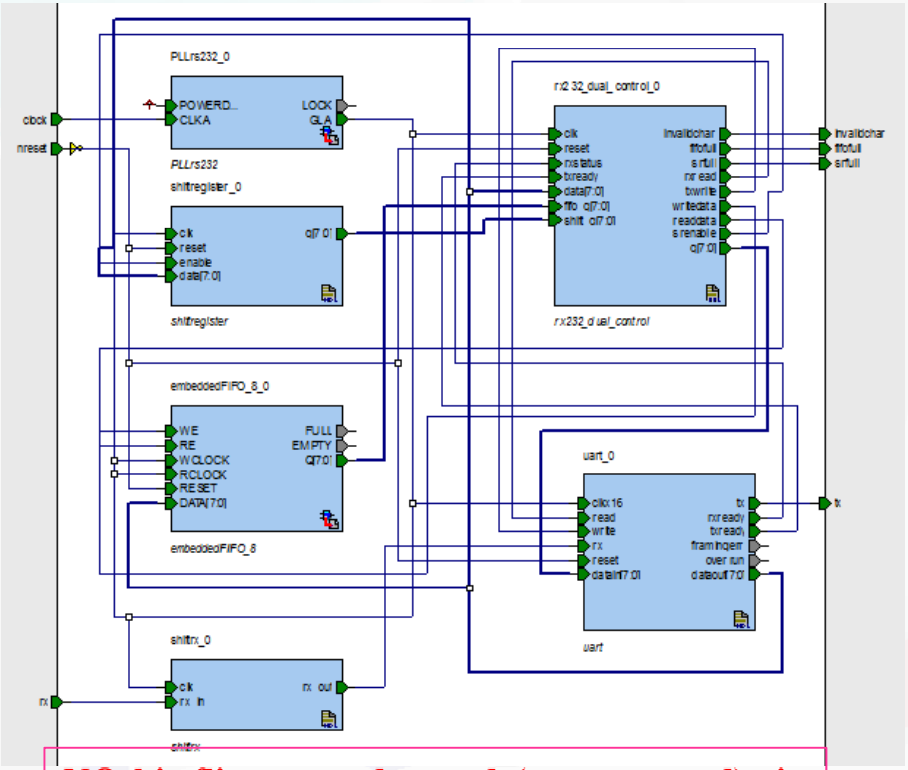
Acknowledgements:

The test design developed as his undergraduate thesis work by **Lorenzo De Santis** (University of Ferrara) in the ACTEL device occupied the FPGA for about 98%.

It implemented:

- an embedded FIFO 4096 x 8 based on SRAM cellsm, for a total of **32768 SRAM bits**
- a shift register with 728 cells 8bit wide, for a total of **5824 Flip Flops**
- a UART to load and read back the memory blocks

A PC running a Labview application also provided by Lorenzo was used to repeatedly run the routine of loading known patterns into the structures and reading them back after the test interval.



NO bit flips were detected (nor expected) in the configuration memory (flash-based) of the FPGA: the functionality of the chip was never found impaired

A typical outcome of the test was that in ½ hour run with 4MeV deuteron energy and 40nA average current we would detect:

- **around 36 SRAM bit flip**
- **between 0 and 2 FLIP FLOP upsets**

If our estimation of neutron flux at the test facility are correct then for each ½ hour run at 40nA the FPGA has been irradiated with ≈ order of 1*10^10 neutrons →

- **we could use a flash based FPGA to handle L1 buffering**
- **we should protect the state machines with TRM** but not necessarily the L1 buffer itself: data corruption rate is low

addressing the radiation issues:
measurement of neutron induced SEE in FPGA at the INFN Laboratori Nazionali di Legnaro

FIFO depth:	4096	number of bits:	32768
Shift Reg. Depth:	728	number of FF:	5824
word width:	8		
fluenza teorica at LNL per deutoni 4MeV (Flavio Dal Corso):	a.c.r.: provo a usare 1e8 che mi sembra piu' appropriato dato lo spettro	1,02E+08	neutroni/sterad * uC
IPOTESI: h - distanza tra sorgente e silicio FPGA (mm):		7,00E+00	mm
IPOTESI: a - spigolo del die della FPGA (mm):		1,00E+01	mm
angolo solido del Si dalla sorgente (Lorenzo): 4 * arcsin[a^2 / (a^2 + 4 * h^2)]		1,38E+00	sterad
corrente di fascio (nA)		4,00E+01	nA
tempo di misura (s)		1,80E+03	s
numero di neutroni attraverso FPGA in 1/2 ora. E' uguale alla fluenza se assumo che area FPGA = 1 cm^2		1,01E+10	neutrons thru FPGA in 1/2 hour
<numero di bit flip in FIFO> :		37,0000	
per Mb:		1129,1504	
<numero di bit flip in Shift Reg> :		1,5000	
per Million Flip Flop:		257,5549	

If our estimation of neutron flux at the CN facility in Legnaro are correct then for each ½ hour run at 40nA the FPGA (assuming 1cm^2 area) has been irradiated with ≈ order of 1*10^10 neutrons.

So,
according to current background simulations results (see Valentina Santoro's http://www.fe.infn.it./~santoro/SuperB/Background/Neutrons/Touschek.html), **we got a few upset with neutron fluxes corresponding to many months of SuperB operation at the locations where the FPGA will sit.**

vedi: "Overview of iRoC Technologies Report "Radiation Results of the SER Test of Actel FPGA December 2005"

da: "Radiation Results of the SER Test of Actel, Xilinx and Altera FPGA instances"

cross section per chip: Sigma_C = No_of_errors / (fluence * C) with C= number of chips

reference fluence: fluence at ground level in New York City: fluence_NYC = 14 n/cm^2/hour

FIT: Failure In Time: failures in 10^9 hours. FIT = Sigma_C * fluence_NYC * 10^9

nel nostro caso:

misure del 24/10 a 40nA **a3p250**	Sigma_C	ref_fluence	FIT
	3,900E-10	1,400E+01	5,460E+00

definisco: cross section per FIFO Mb: Sigma_Mb = No_of_errors * 10^6 / (fluence * N_FIFO_bit)

our test at LNL

misure del 24/10 a 40nA **a3p250 Fifo errors in 1 hour(avg):**	Sigma_Mb	ref_fluence	**FIT per million bit of embedded RAM**	**IROC test result per confronto**
	78			
	1,176E-07	1,400E+01	**1,646E+03**	**1580**

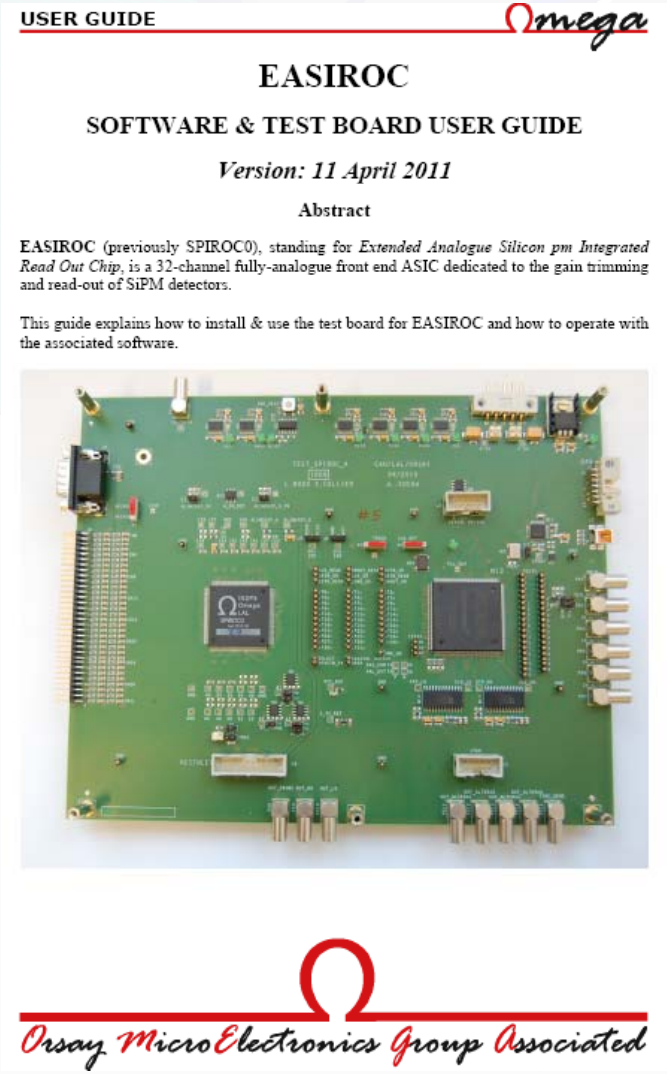
definisco: cross section per M flipflops: Sigma_Mff = No_of_errors * 10^6 / (fluence * N_flipflops)

misure del 24/10 a 40nA **a3p250 FlipFlop errors in 1 hour(avg):**	Sigma_Mff	ref_fluence	**FIT per million flip flop**	**IROC test result per confronto**
	2			
	1,696E-08	1,400E+01	**2,375E+02**	**889**
ratios RAMbit errors/FF errors			**6,932E+00**	**1,77727784**

INFN Istituto Nazionale di Fisica Nucleare

SuperB

addressing the radiation issues:
measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro (being planned)


USER GUIDE

Omega

EASIROC

SOFTWARE & TEST BOARD USER GUIDE

Version: 11 April 2011

Abstract

EASIROC (previously SPIROC0), standing for *Extended Analogue Silicon pm Integrated Read Out Chip*, is a 32-channel fully-analogue front end ASIC dedicated to the gain trimming and read-out of SiPM detectors.

This guide explains how to install & use the test board for EASIROC and how to operate with the associated software.

Orsay MicroElectronics Group Associated

A new test is foreseen at the neutron test facility in Legnaro toward the end of this month. The test is meant to evaluated the SEE rate in the DACs of the EASIROC chip and evaluate the TID dose effects on the analog signal processing units of the ASIC.

We also plan to look for TID effects on the op amps which could be used for the active “pick-up” option mentioned above.

We would stack the ACTEL FPGA board on top of the OMEGA board, in such a way to have correlated measurements failure rate measurements (the FPGA acting as a radiation monitor). In such a way the FPGA would act as some sort of neutron dose monitor, to be checked against the calibration data from the Legnaro facility.