picoTDC board

P. Antonioli

slides essentially based on talk given by D. Falchieri@TWEPP2024

Design, test and performance of a picoTDC based board

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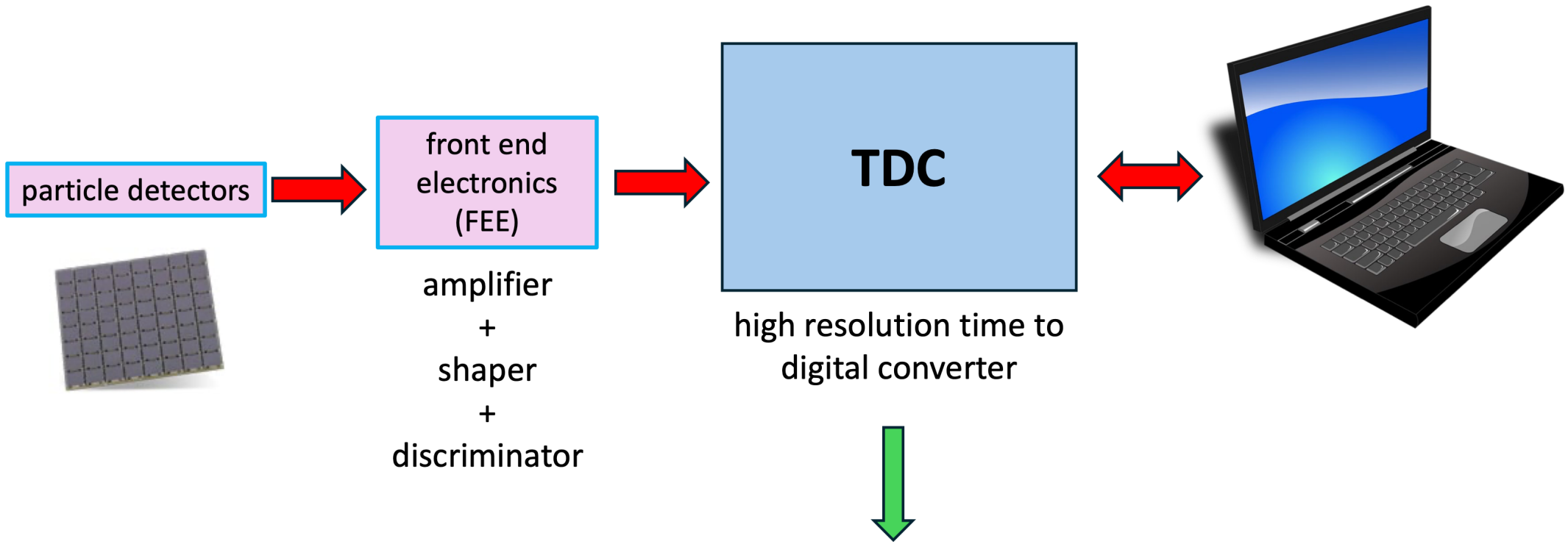
INFN Bologna [a], University of Bologna [b], INFN Lecce [c]

TWEPP 2024, Glasgow, 30 September - 4 October 2024

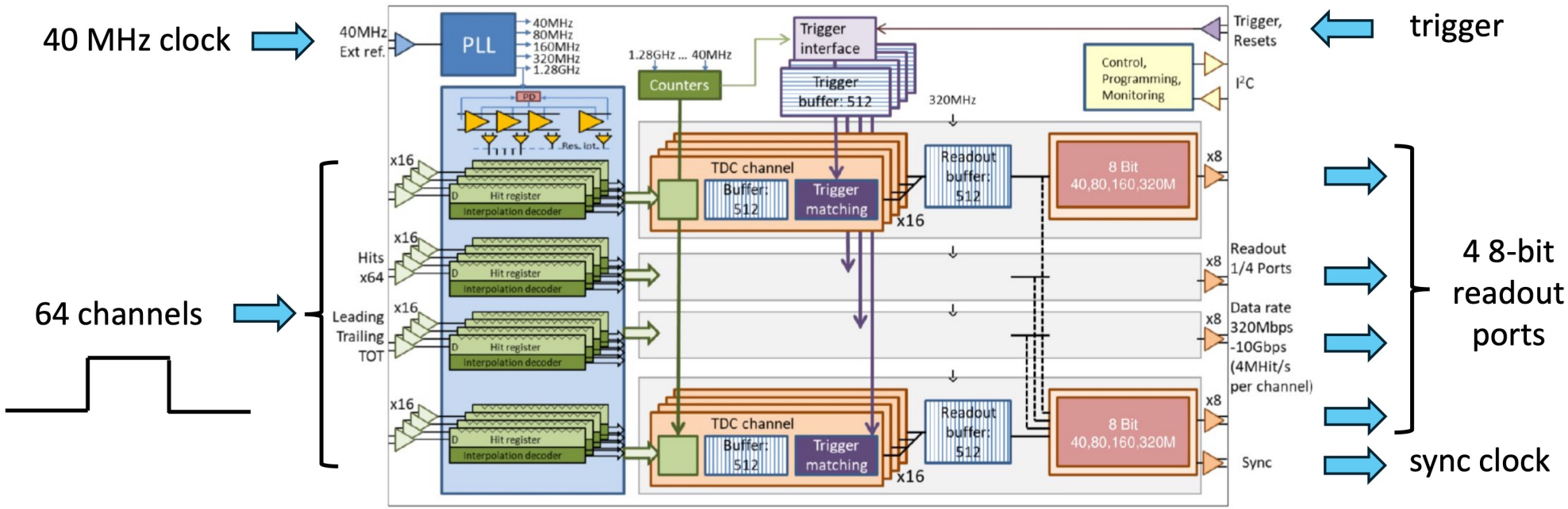
Towards a flexible timing measurement device

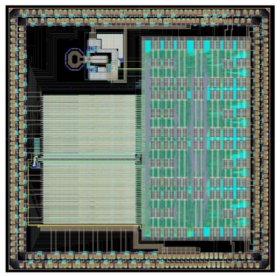


Our goal was to build **a flexible high resolution timing measurement device** able to:

- connect to multiple detector types + FEE with standard connectors
- provide high data bandwidth towards a PC via standard interfaces (Ethernet + USB3)
- provide the best achievable timing resolution on a lot of channels (128)

The picoTDC ASIC from CERN





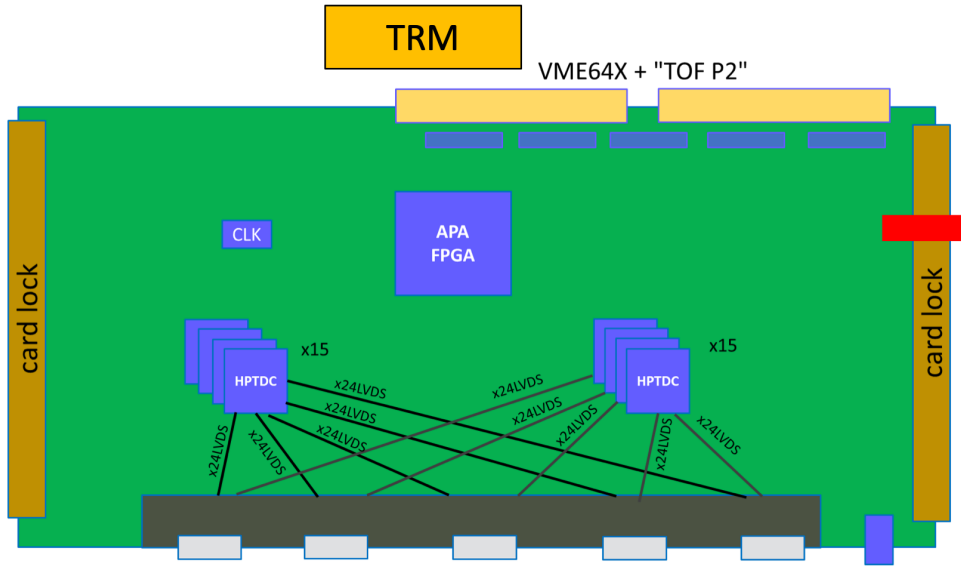
picoTDC main features:

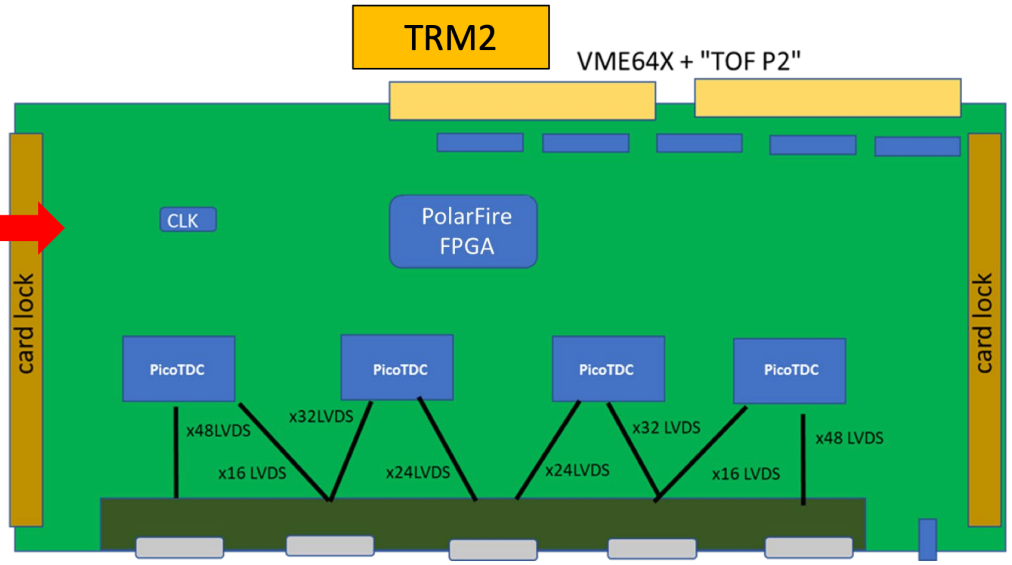
- bin size: 3.05 ps (fine resolution) or 12.2 ps (coarse resolution)
- single shot resolution: <3.3 ps in fine mode or <4.2 ps in coarse mode
- measurement range: 204.8 μs
- measurement scheme: triggered or un-triggered time-tagging

https://iopscience.iop.org/article/10.1088/1748-0221/18/07/P07012/pdf

S. Altruda et al., JINST 18 P07012

From TRM to TRM2 for time measurements in ALICE TOF detector





The **TRM VME** card is the main element of the TOF readout system and it hosts:

- an **Actel ProASIC FPGA** to manage the readout and board operations.
- **30 HPTDC** ASICs (24.4 ps LSB, 8 ch/chip) to provide time measurements.

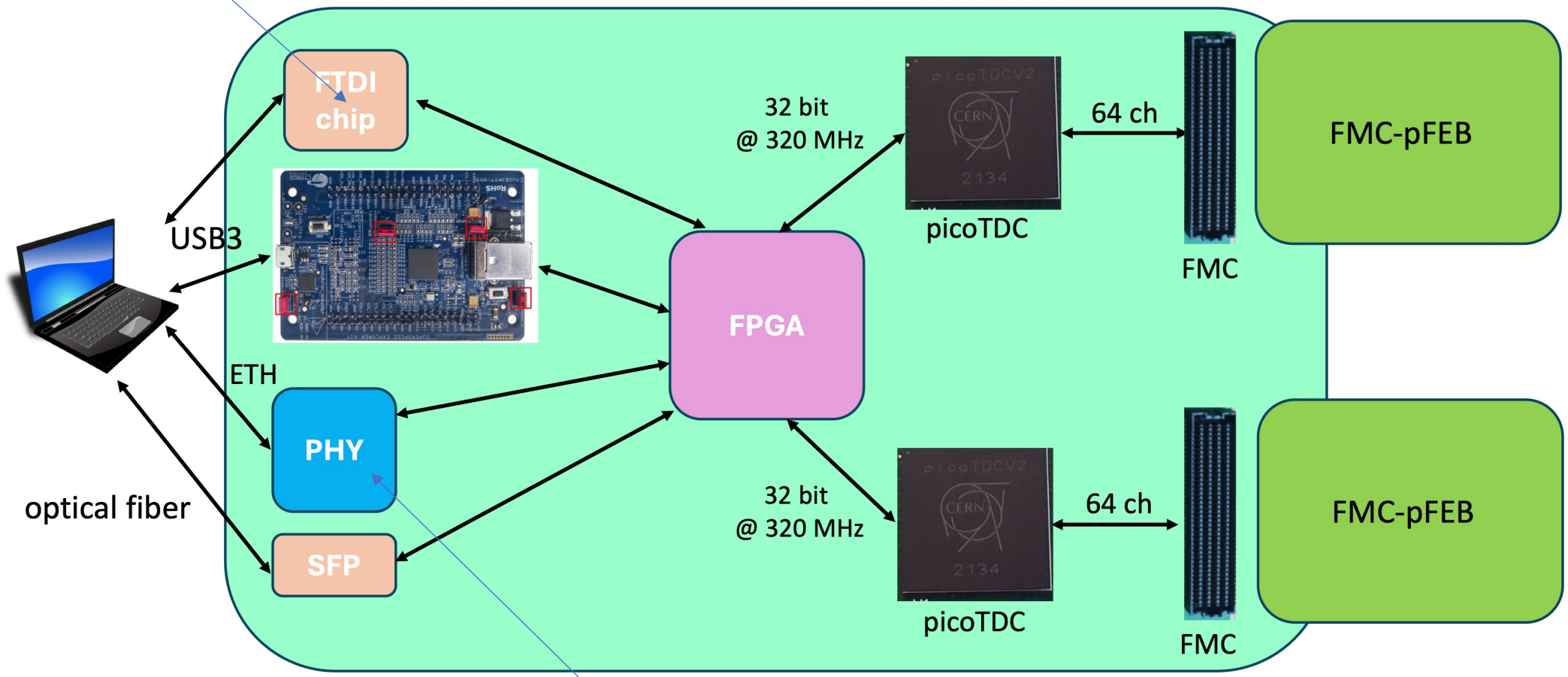
To replace damaged TRMs during LHC Run 4, a new **TRM2** project began, considering:

- **a PolarFire FPGA** to manage the readout and board operations.
- **4 PicoTDC** ASICs (12.2 ps or 3.05 ps LSB, 64 ch/chip) as successors of the HPTDCs.

Context: the choice of FPGA for picoBoard was driven by learning a FPGA suitable for ALICE-TOF (FLASH based)
The whole picoBoard was funded via ALICE as a development card toward TRM2. We are now doing some kind of spin-off…

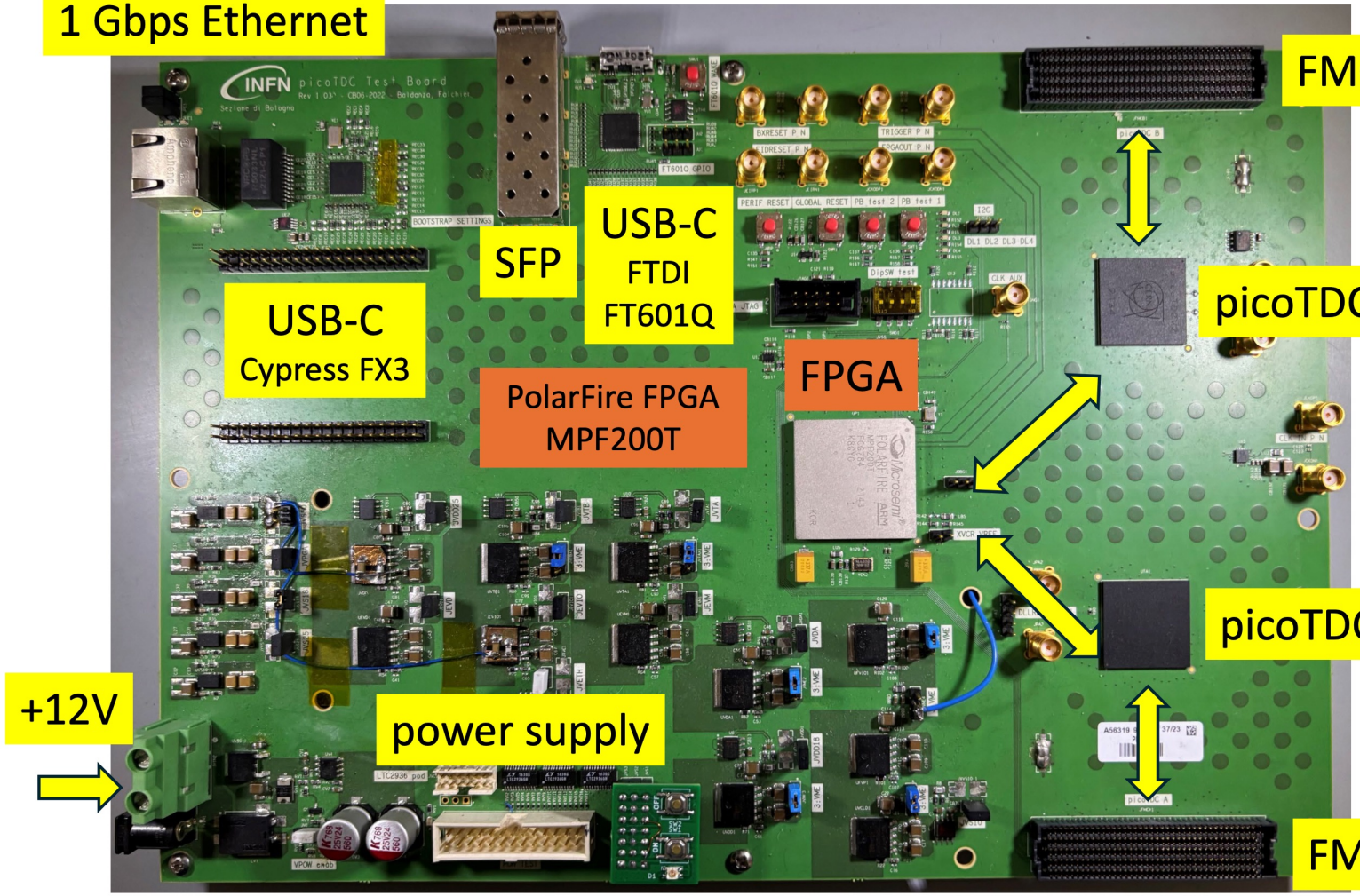
one master thesis (J. Succi): March 2025

Towards the picoTDC board



one master thesis (S. Geminiani): July 2024

The picoTDC board



standard FMC HPC

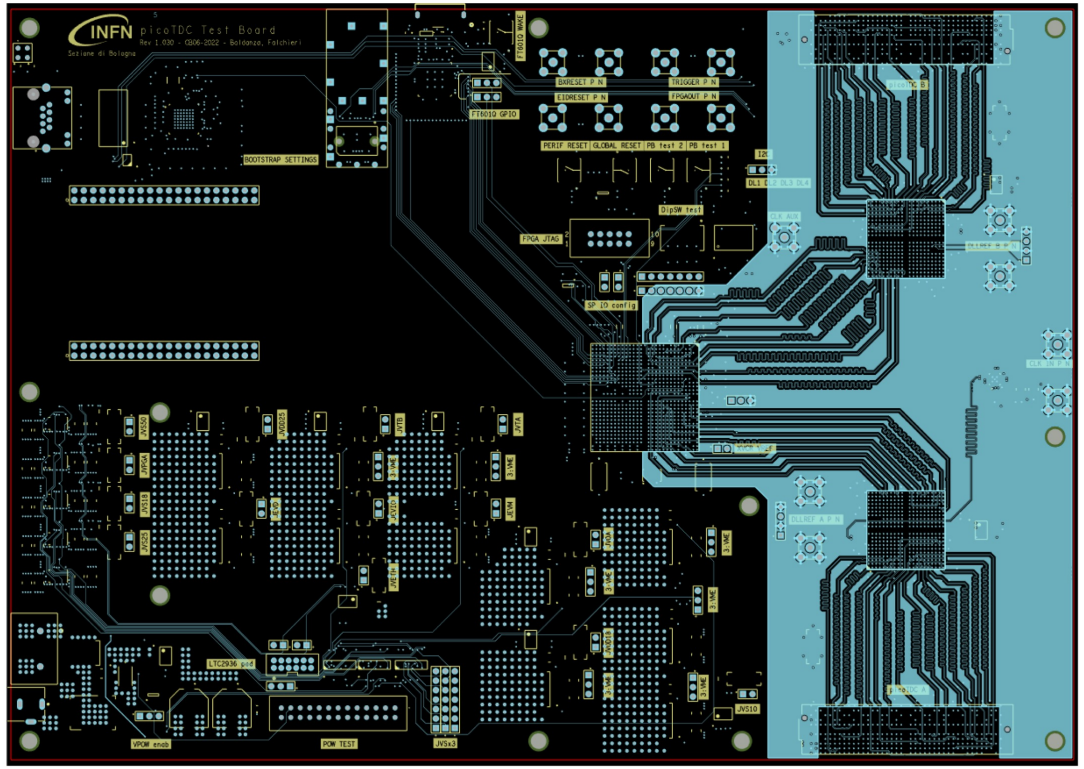
table-top board (20 x 15 cm) to be used in conjunction with pFEBs

15 SMA I/Os, among which an option reference external clock

standard FMC HPC

1. several fixes needed ”by hand”: desirable a second version
2. we have just 2 cards (working), to share it among groups desirable having more

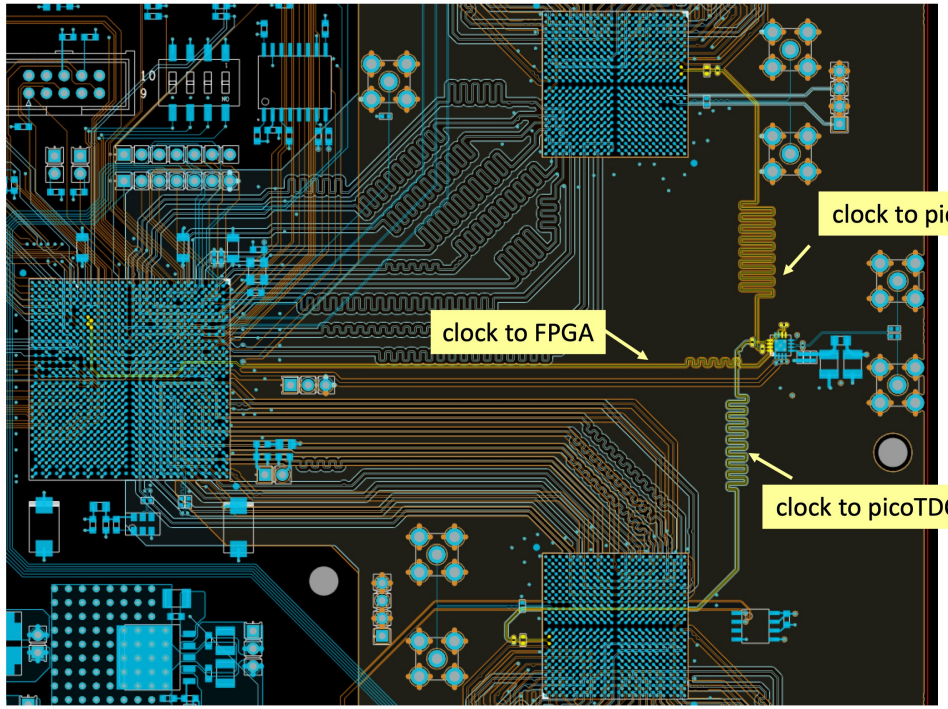
layout



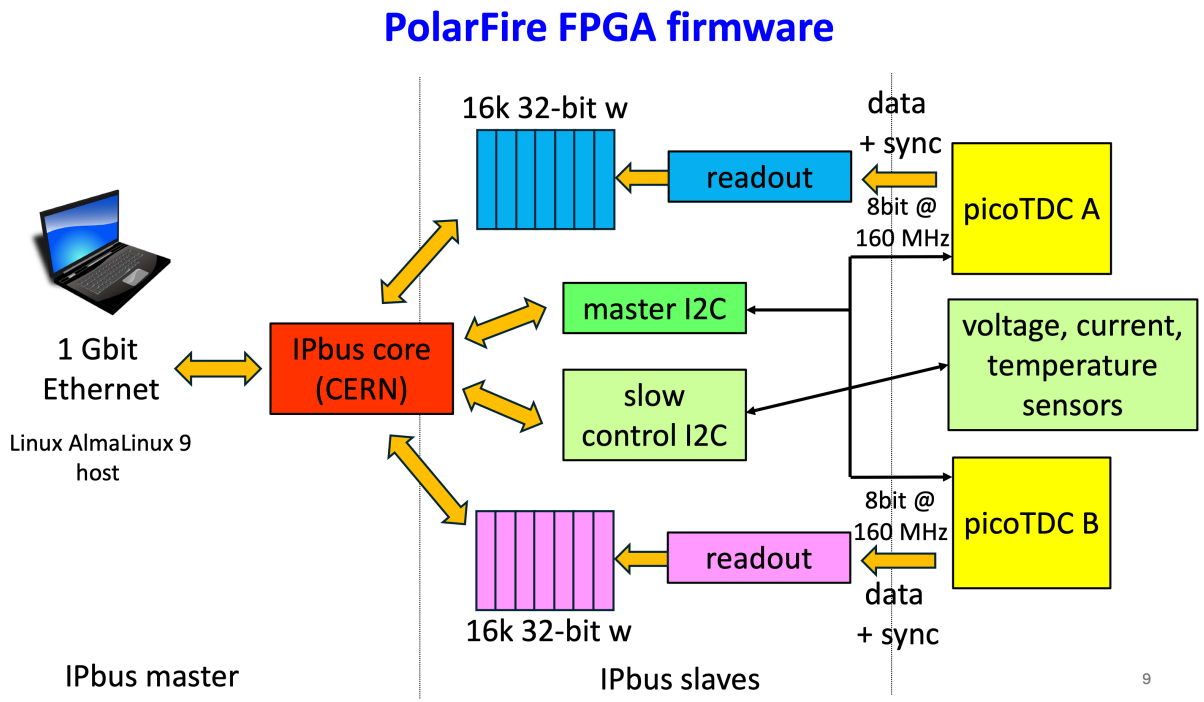
dieletric: FR-408, PREPREG_58
total thickness: 1.6 mm

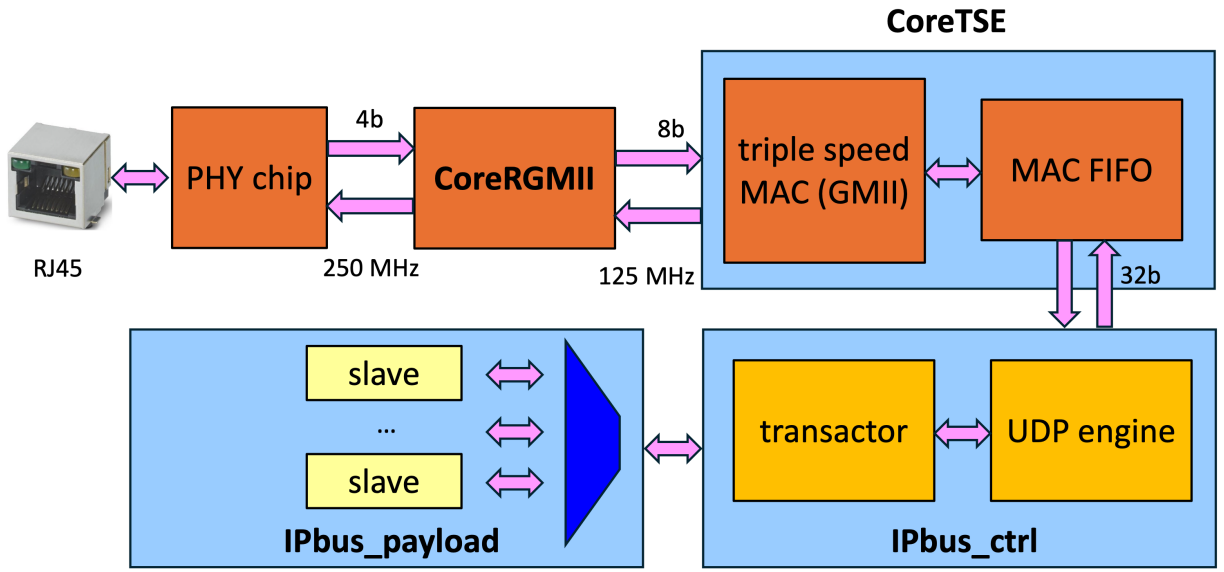
differential lines and equalization
PCB stackup, 14 layers

the 3 clock tracks are equalized



Firmware





We used the Microchip IP cores (CoreRGMII and CoreTSE) towards a first implementation of CERN IPbus core over a Microchip FPGA

Software

picoTDC board software

The **user interface** is designed to hide the system complexity and works through **prompt line commands.** It provides **two main user programs:**

3-layer software structure (C++)

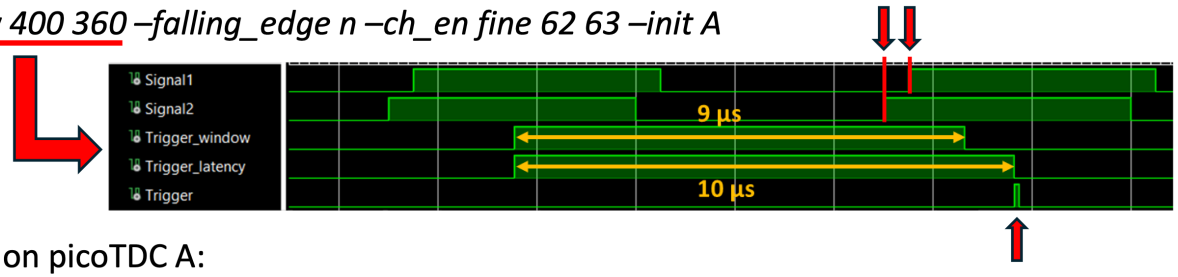
- user main programs
- C++ classes → IPbus slaves
- IPbus API library

PicoTOF — user program to configure both the picoTDCs

PicoRead — user program for reading out data from the picoTDC chips, considering a **trigger-based** readout

Configuration for triggered mode with channels 62-63 on picoTDC A:

*$ ./**PicoTOF** –triggered –lw 400 360 –falling_edge n –ch_en fine 62 63 –init A*



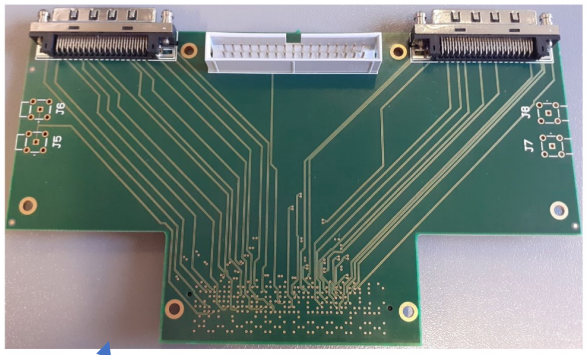
Acquisition of 10M events on picoTDC A:

*$ ./**PicoRead** –chip A –events 10000000 –output file.ptdat*

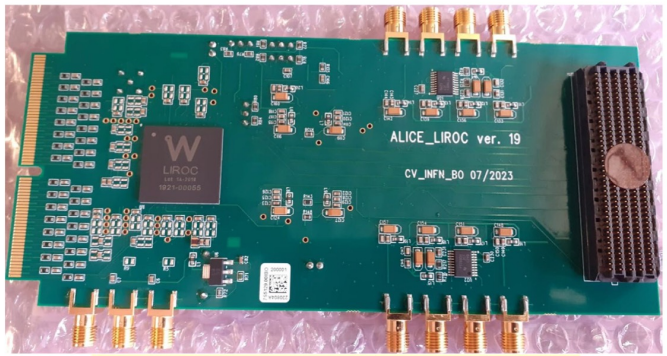
basic “Run Control” suite, for test beam operations
Multi-threaded program taking advantage of PS-spill structure
External signals: “trigger” and “spill”
Suitable also for LAB acquisition (with spill duty cycle tuned at pleasure)

Towards a family of pFEBs

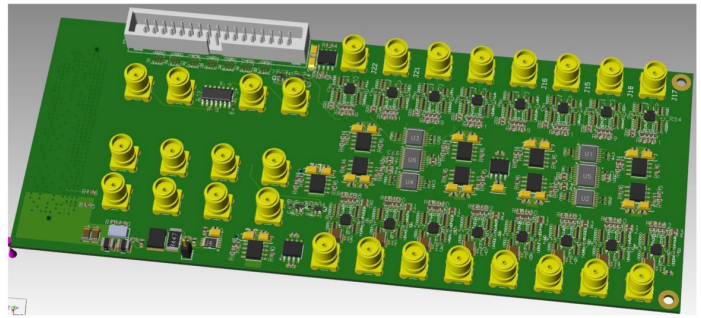
pFEBs



picoTDC breakout board



picoTDC LIROC board

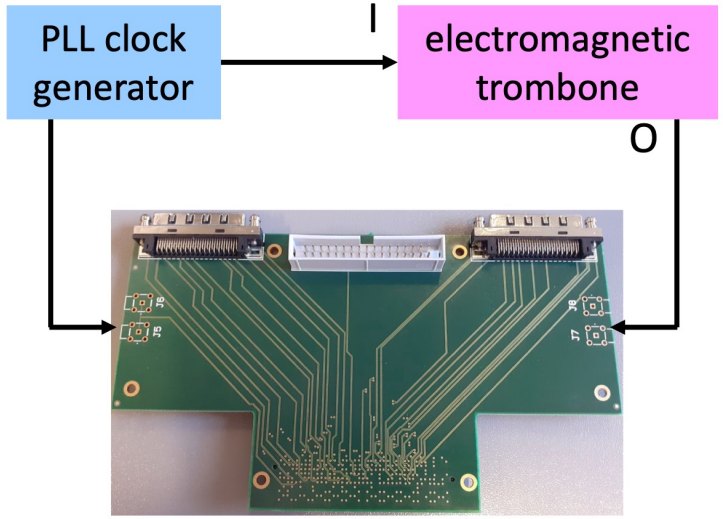


pFEB-D board

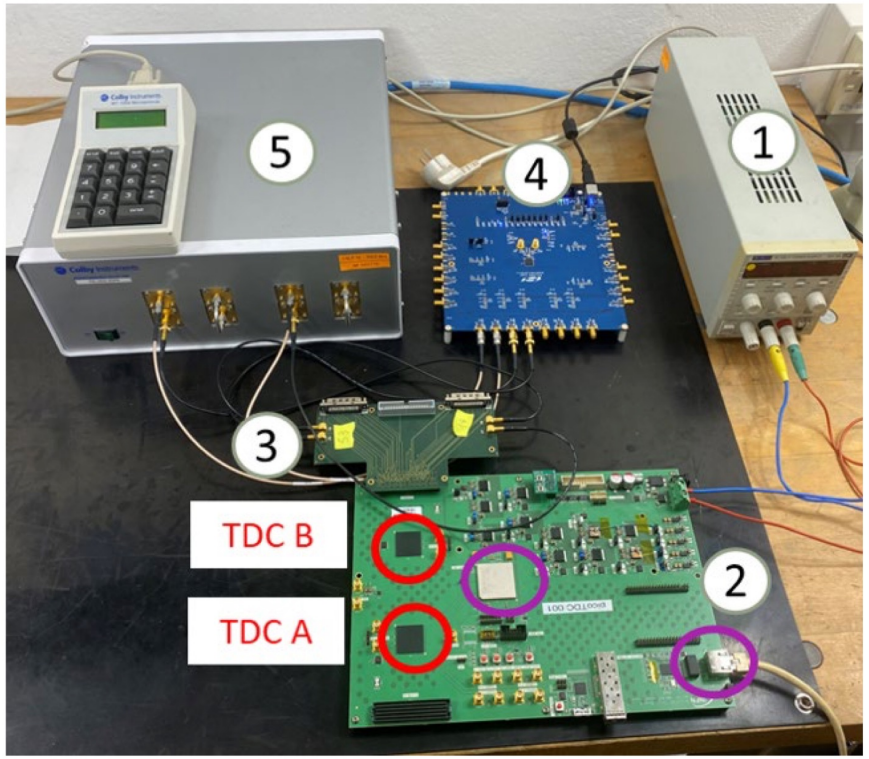
We designed a family of custom picoTDC board – compatible mezzanines to provide connection towards detectors and their front-end electronics

just routing signals no adaptation to CLPS (Cern Low Power Signals) 0.6V Common Mode (with 0.1-0.4 diff. swing) (aka sub-LVDS)

TDC resolution measurements



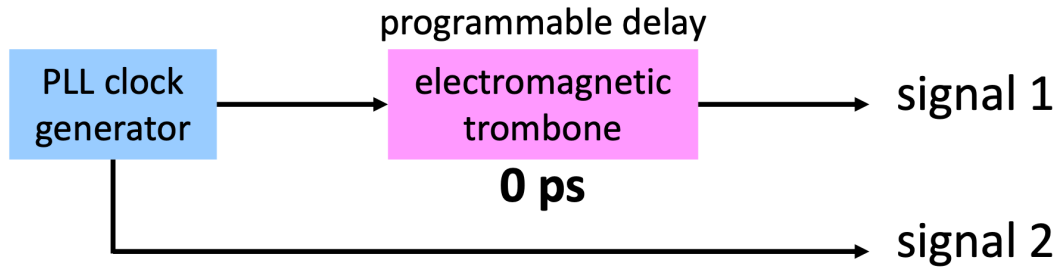
1. power supply
2. picoTDC board
3. pFEB breakout board
4. PLL clock generator (SiLabs Si5341-D)
5. electromagnetic trombone

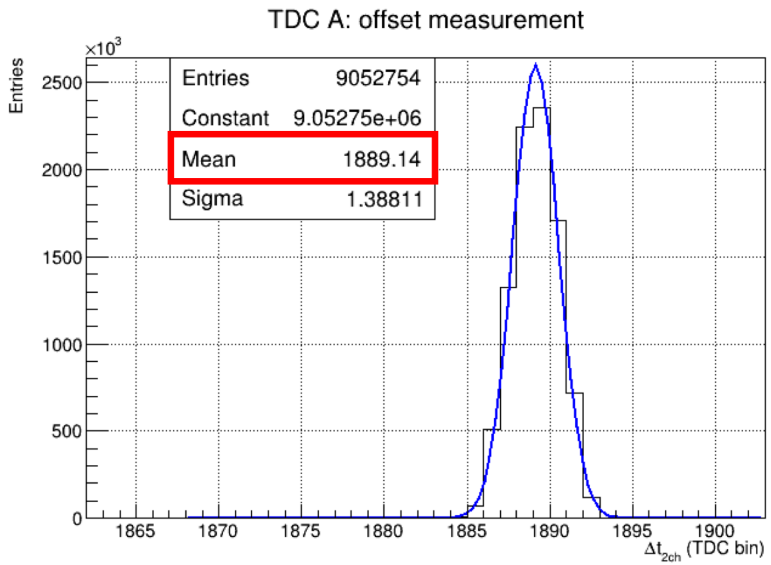


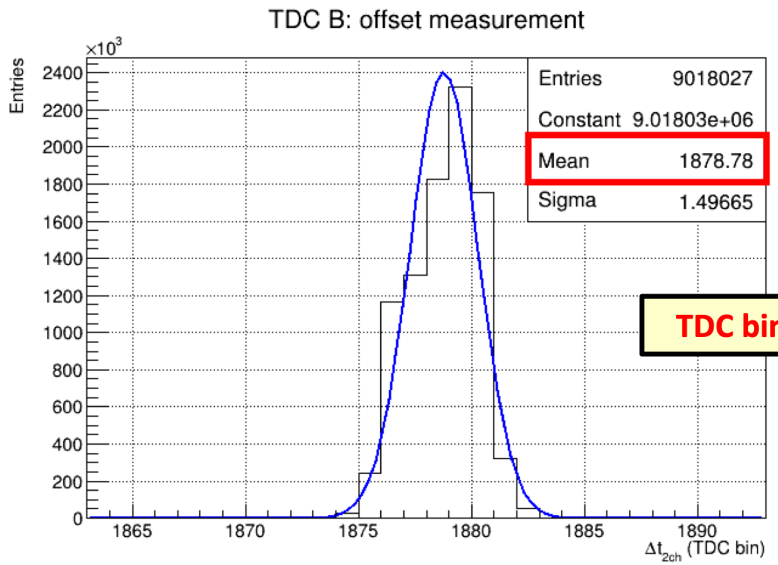
This is the setup used for the **TDC resolution estimation** performing a **two-channel time measurement,** considering **two clock signals** (100 kHz) and employing an **electromagnetic trombone** to shift one of the two signals by a **delay within the 0-600 ps range**

https://amslaurea.unibo.it/32161/

Data analysis and results: offset measurement





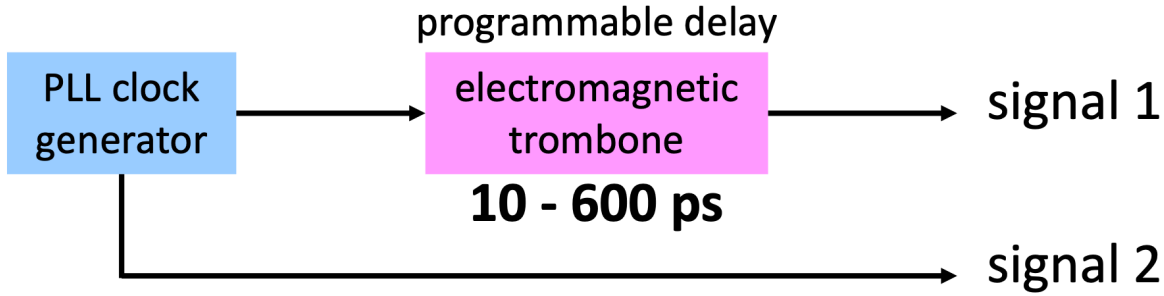


TDC bin = 3.05 ps

offset picoTDC A = 1889.1 · 3.05 ps = **5761.9 ps**

offset picoTDC B = 1878.8 · 3.05 ps = **5730.3 ps**

Data analysis and results (2)



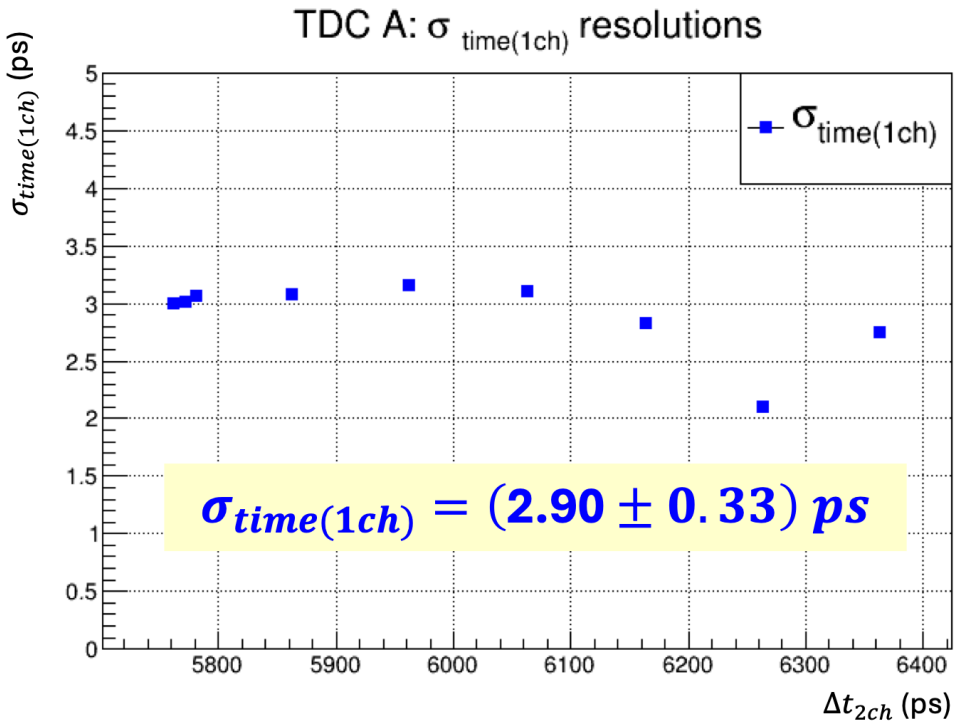
	picoTDC A		picoTDC B	
delay (ps)	$delay_{meas}$ (ps)	$\sigma_{time(2ch)}$ (ps)	$delay_{meas}$ (ps)	$\sigma_{time(2ch)}$ (ps)
10	10.5	4.3	8.7	4.6
20	20.2	4.3	18.7	4.6
100	101.0	4.4	100.7	4.6
200	200.9	4.5	200.5	4.6
300	301.4	4.4	300.8	4.5
400	401.9	4.0	401.0	3.8
500	501.3	3.0	500.4	2.9
600	601.8	3.9	600.8	3.6

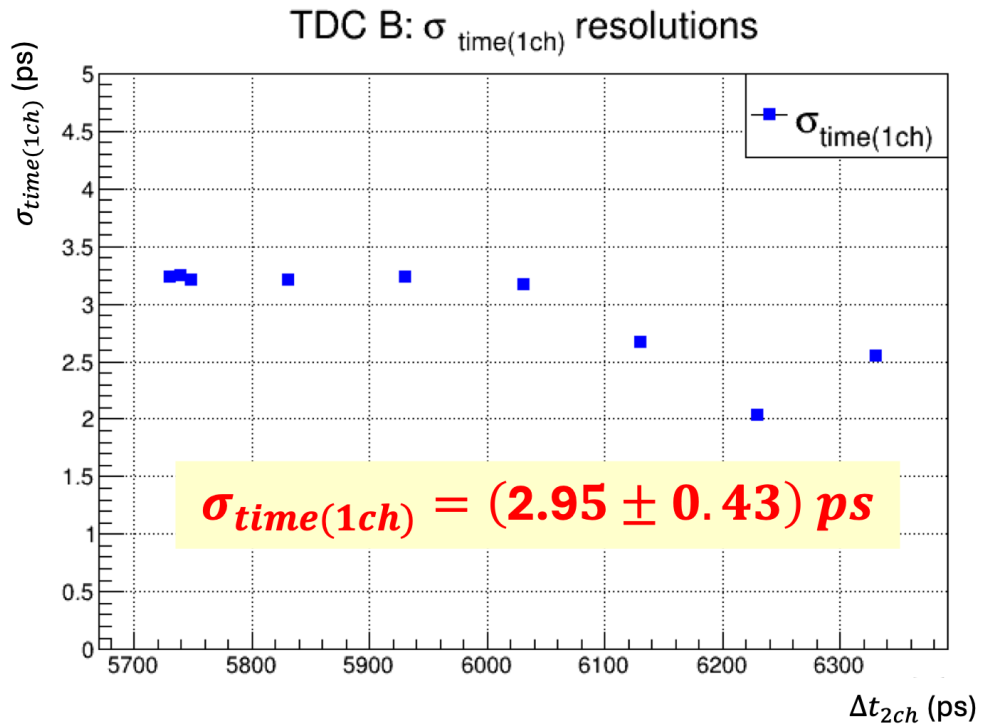
$$\mathbf{delay_{meas} = (mean_{meas} - mean_{offset}) \cdot 3.05\ ps}$$

$$\mathbf{\sigma_{time(2ch)} = sigma_{meas} \cdot 3.05\ ps}$$

The analysis results for the measured delays show an **excellent agreement (within 2 ps)** with the programmed delays

Data analysis and results (3)





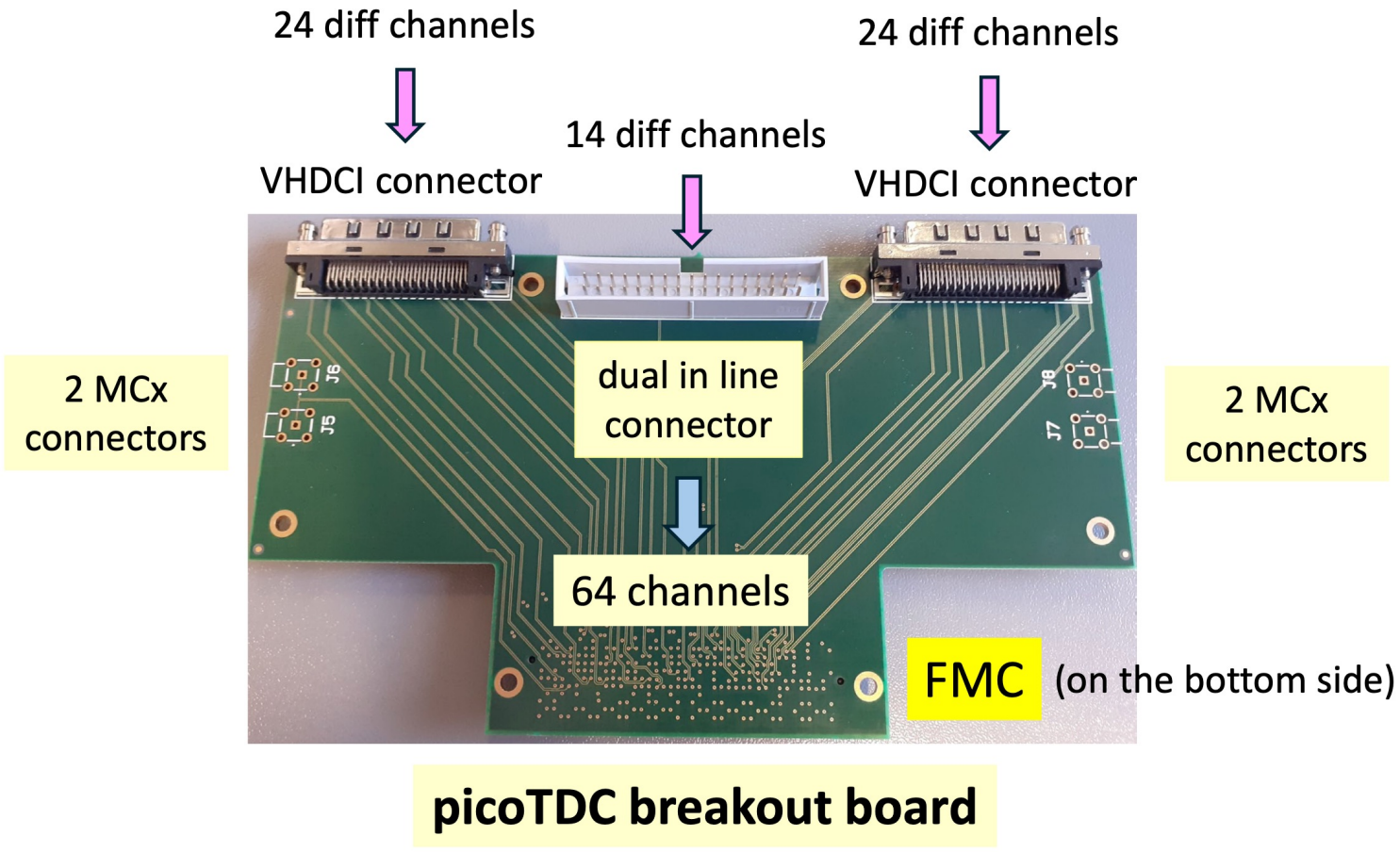
The $\boldsymbol{\sigma_{time(1ch)}}$ **resolution** value for each dataset is estimated, using the following:

$$\boldsymbol{\sigma_{time(1ch)} = \frac{\sigma_{time(2ch)}}{\sqrt{2}}}$$

The **1-channel resolution** measured for both TDCs, **within a time interval of 600 ps**, is found considering the **mean** and the **standard deviation** for all 9 measurements

A family of picoTDC compatible Front-End Boards (1)

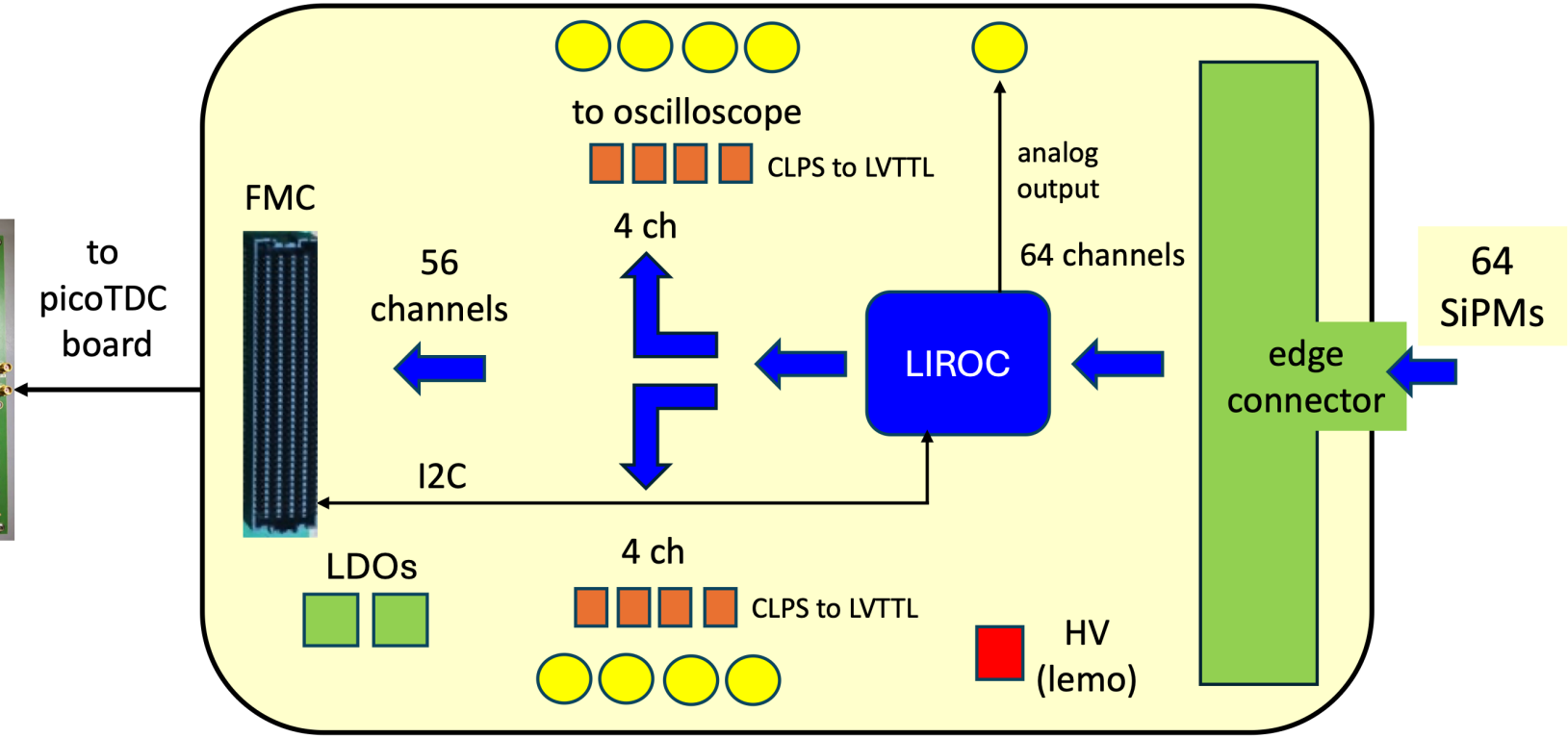
from ALICE TOF MPRCs front -end



picoTDC breakout board

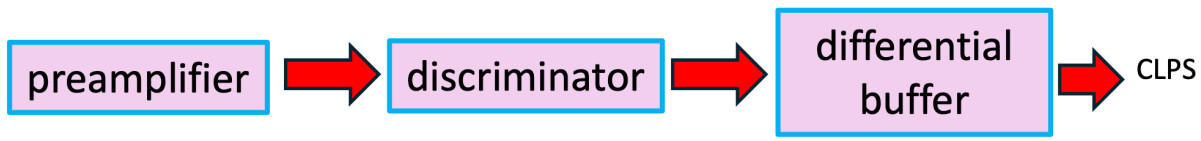
Korean group is preparing a variant of this with signal adaptation (LVDS – CLPS)

A family of picoTDC compatible Front-End Boards (2)



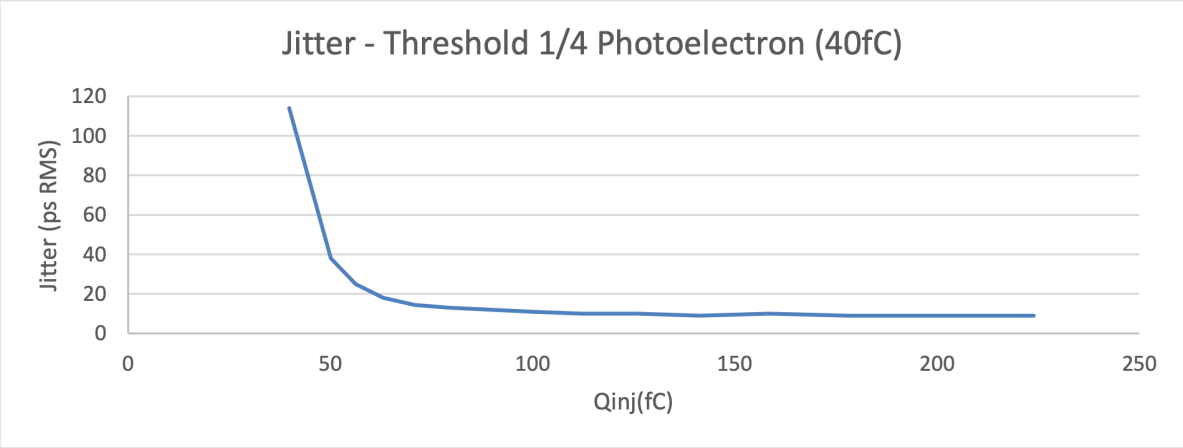
LIROC (from Weeroc) is a 64-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM) for LIDAR application

https://www.weeroc.com/products/sipm-read-out/liroc



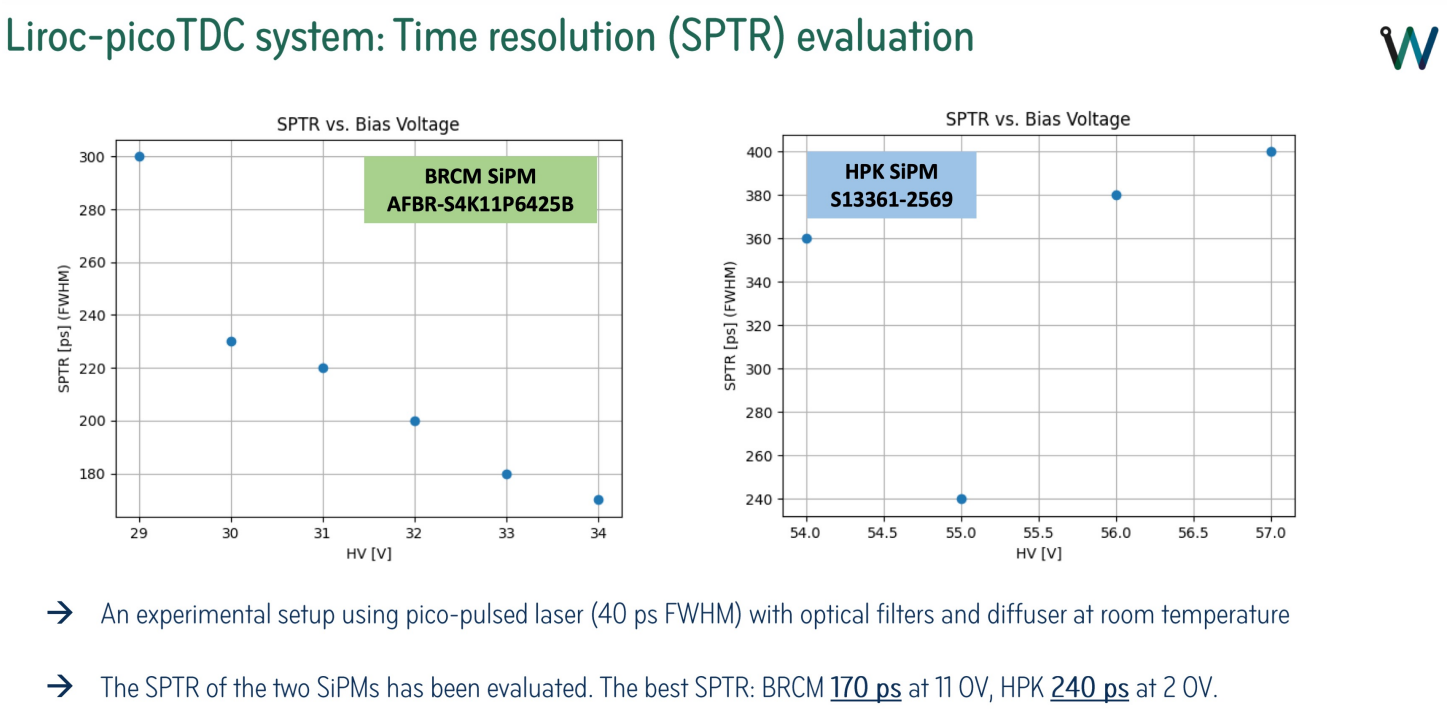
timing resolution (better than 20ps FWHM)

About LIROC time resolution



from WEEROC data sheet

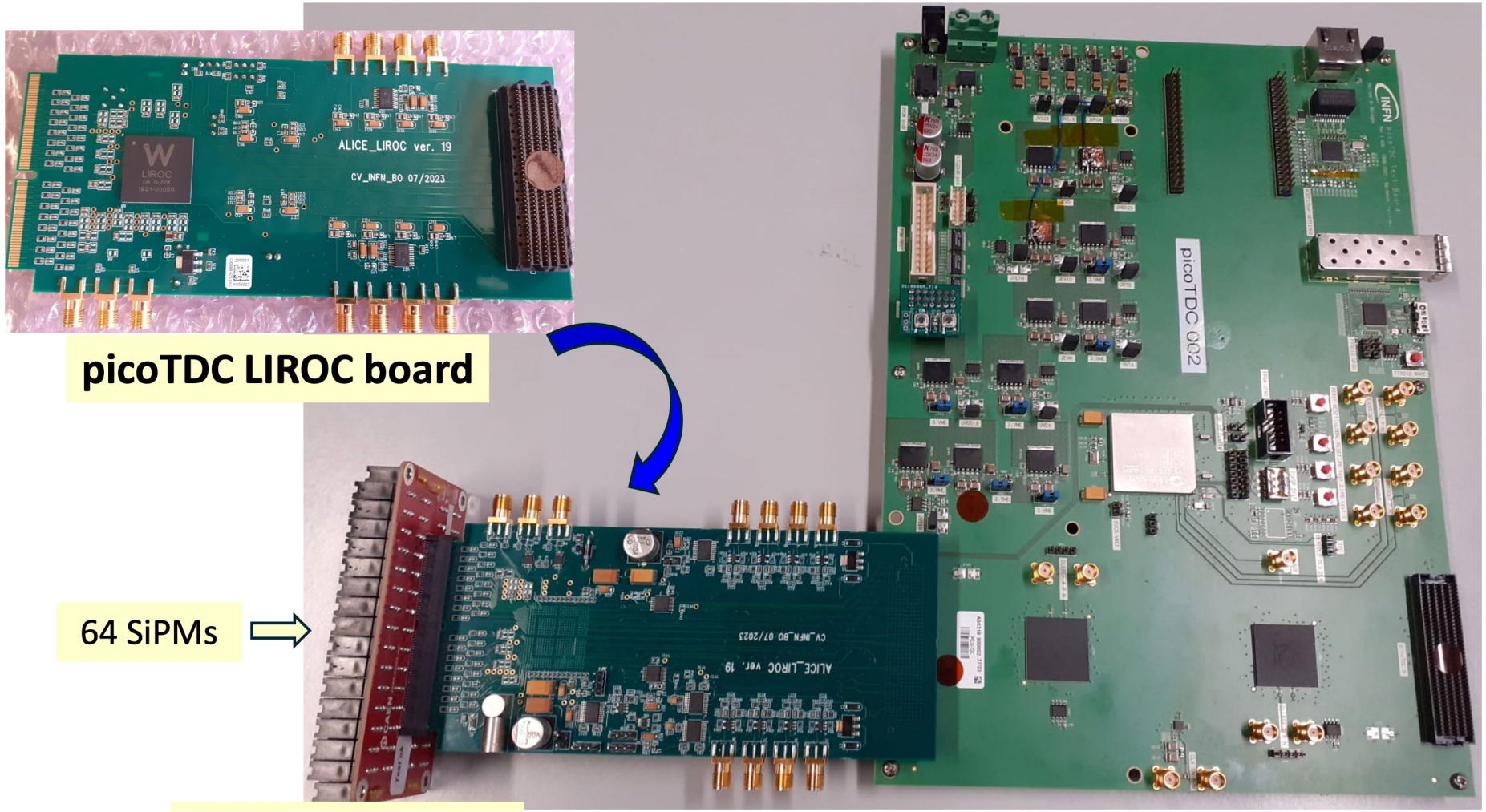
Fleury (Weeroc):
results with two SIPM



My View:

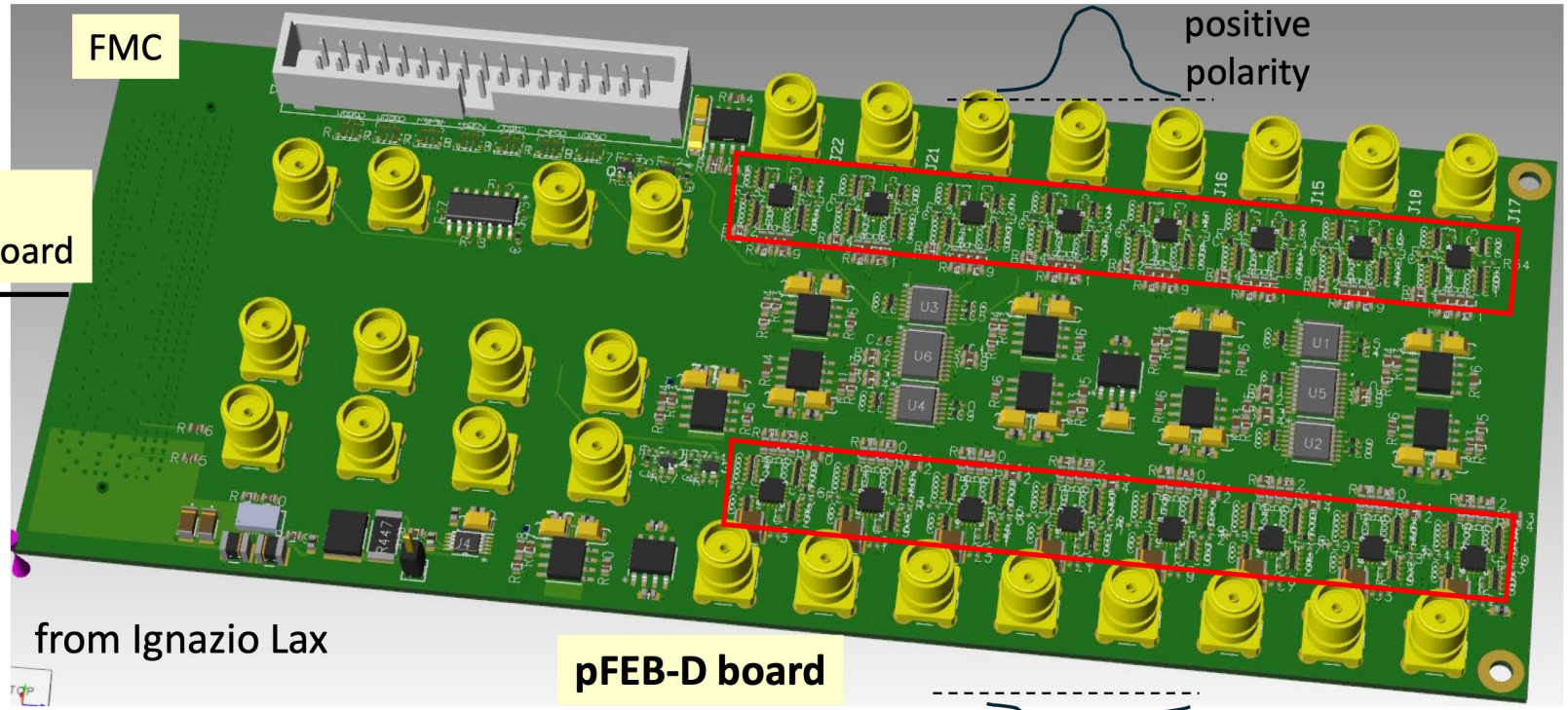
- immediate step should be qualify in the lab LIROC+picoTDC resolutions
- next step should be try FastIC (from LHCb)

A family of picoTDC compatible Front-End Boards (2)

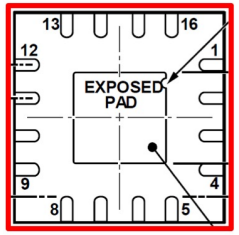


(a custom made FERS with much more flexibility…)

A family of picoTDC compatible Front-End Boards (3)



ADCMP573



ultrafast SiGe
discriminator

propagation delay error < 15 ps

- 8 positive polarity inputs to discriminators
- 8 negative polarity inputs to discriminators
- 4 LVDS inputs (SMAs)
- 16 LVDS inputs (dual in line connector)

→ 36 channels

https://www.analog.com/en/products/adcmp573.html

Plan to use with LGAD signals

Data Sheet **ADCMP572/ADCMP573**

FEATURES

- 3.3 V/5.2 V single-supply operation
- 150 ps propagation delay
- 15 ps overdrive and slew rate dispersion
- 8 GHz equivalent input rise time bandwidth
- 80 ps minimum pulse width
- 35 ps typical output rise/fall
- 10 ps deterministic jitter (DJ)
- 200 fs random jitter (RJ)
- On-chip terminations at both input pins
- Robust inputs with no output phase reversal
- Resistor-programmable hysteresis
- Differential latch control
- Extended industrial −40°C to +125°C temperature range

FUNCTIONAL BLOCK DIAGRAM

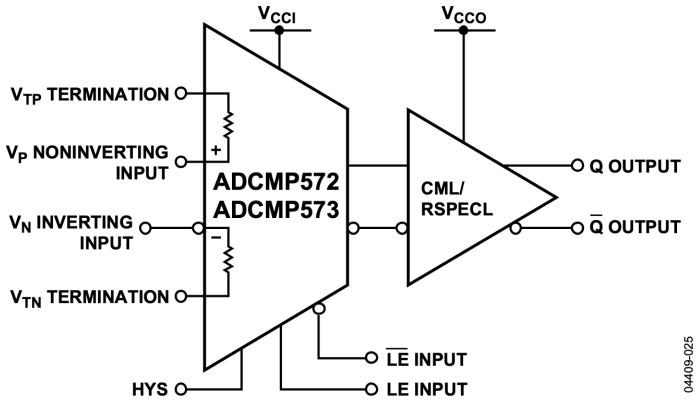


Figure 1.

layout done
→ close to preventivi
but still to be fixed two points below!

drive conditions vary (Figure 17 and Figure 18). For the ADCMP572/ADCMP573, dispersion is typically <15 ps because the overdrive varies from 10 mV to 500 mV, and the input slew rate varies from 2 V/ns to 10 V/ns. This specification

- RSPECL output ---> still studying adaptation to CLPS
- TOFO offset → unclear how to handle the LATCH signal

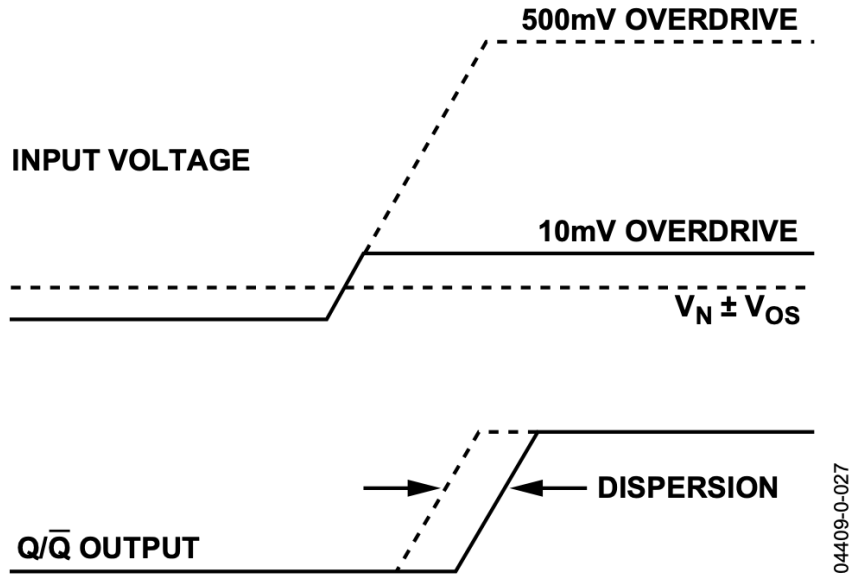
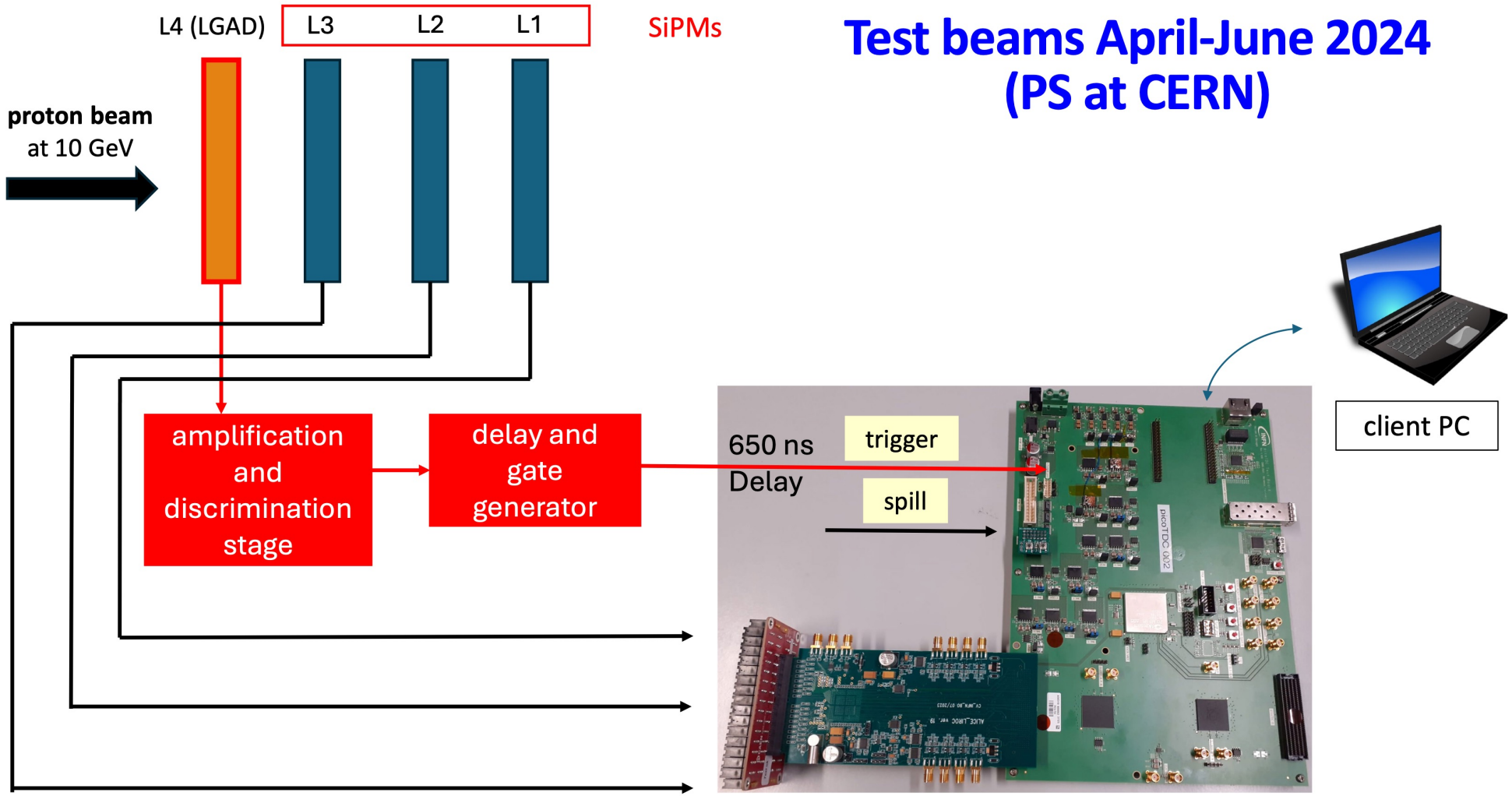
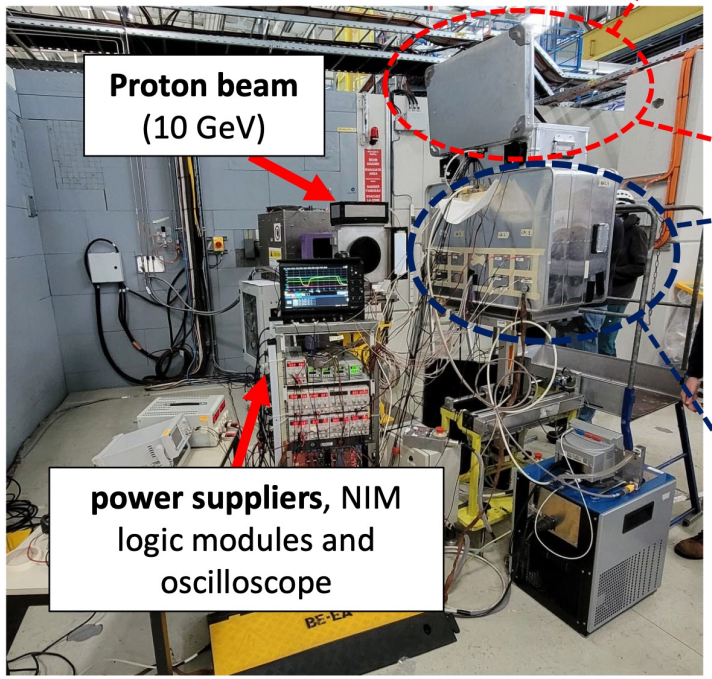


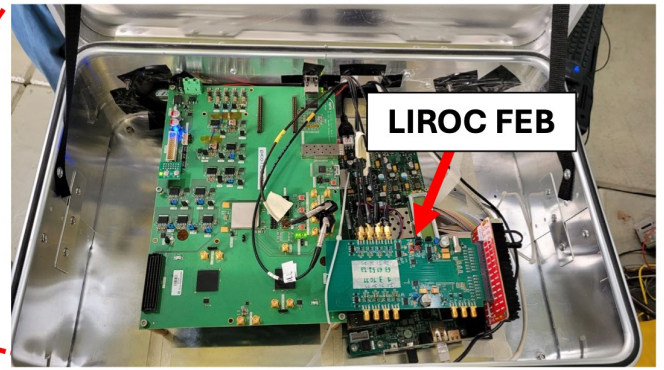
Figure 17. Propagation Delay—Overdrive Dispersion

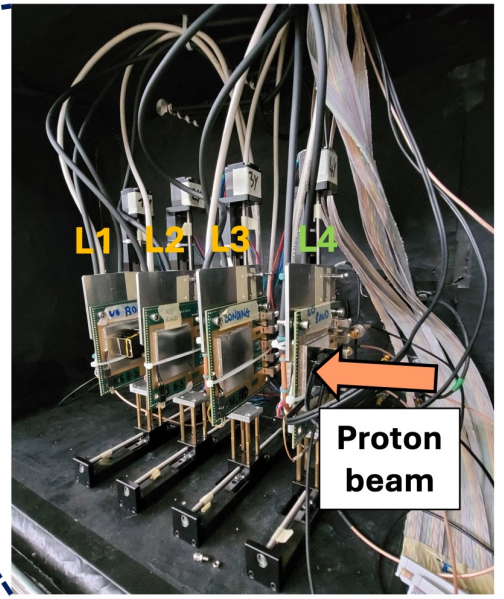
Test beams April-June 2024 (PS at CERN)



Test beams April-June 2024 (PS at CERN)





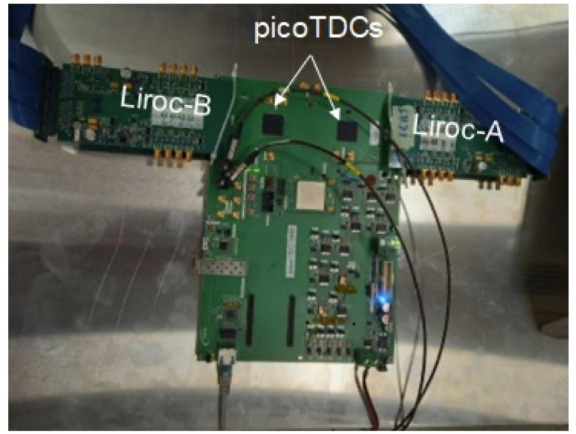


Sensor box including **four layers** (**LGADs** and **SiPMs**):

- **L4:** LGAD signal used as **the trigger signal**
- **L3, L2, L1:** **SiPM** sensors connected to **TDC input channels**

Readout electronics box including:

- **the DAQ chain**: the **PicoTDC board** and the **LIROC FEB**



at TB of June/July 2024, five layers were employed and **both the TDCs on board** were used!

2025 plans

- finalize USB interface
- check in the lab performance of [pFEB-”X” + picoTDC]
- use in Spring test beam pFEB-D (LGAD) + pFEB-Liroc (SiPM)
- [consider fastIC-based pFEB?] (it would mimic LHCb, note they use lpGBTx)
- [consider ALCOR chain ? (extensive experience/use in the group)]

- good gym for undergrad. students