OAK RIDGE National Laboratory

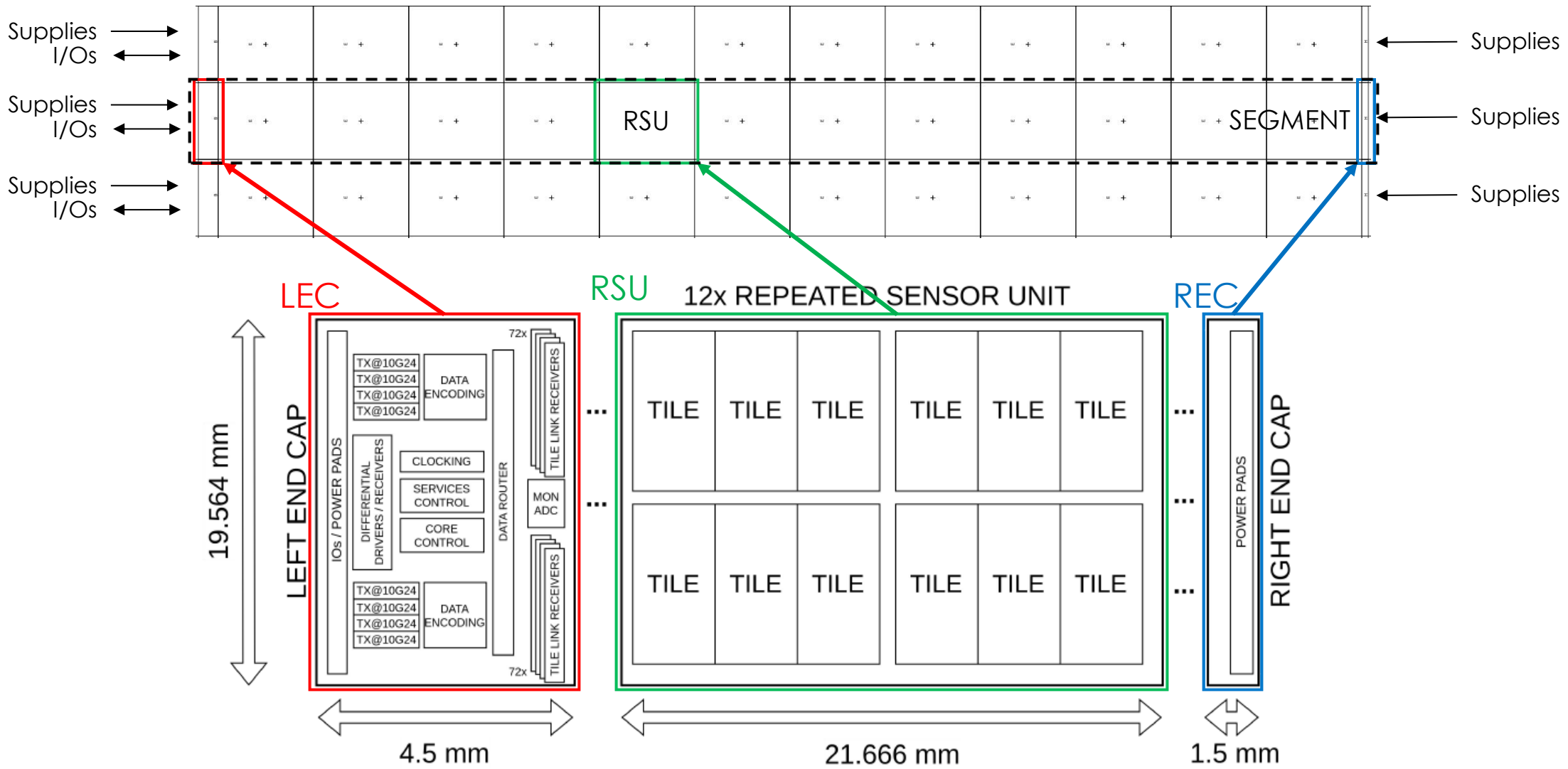
SVT Readout

J. Schambach

ORNL is managed by UT-Battelle LLC for the US Department of Energy

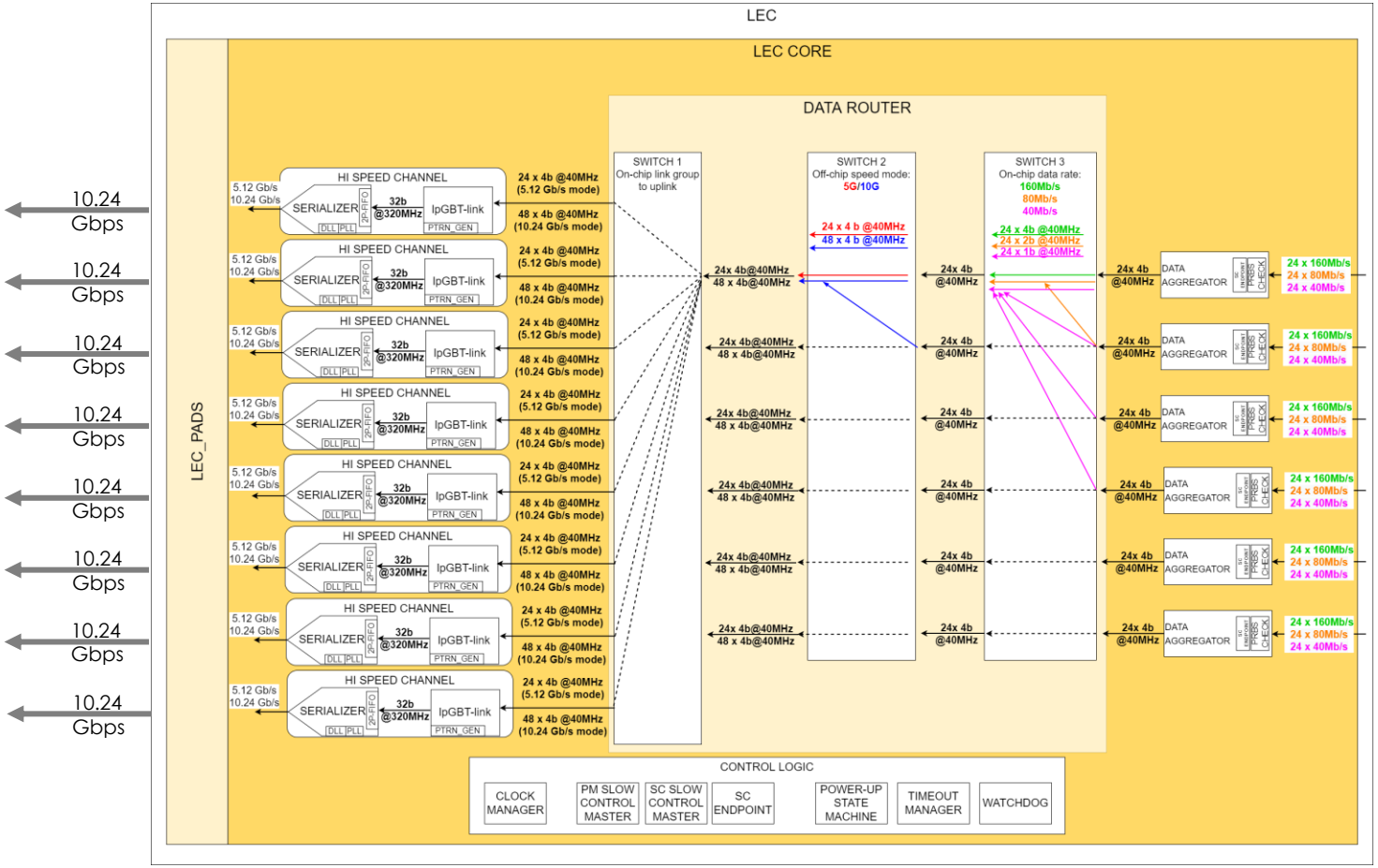
U.S. DEPARTMENT OF ENERGY

MOSAIX Architecture



OAK RIDGE National Laboratory

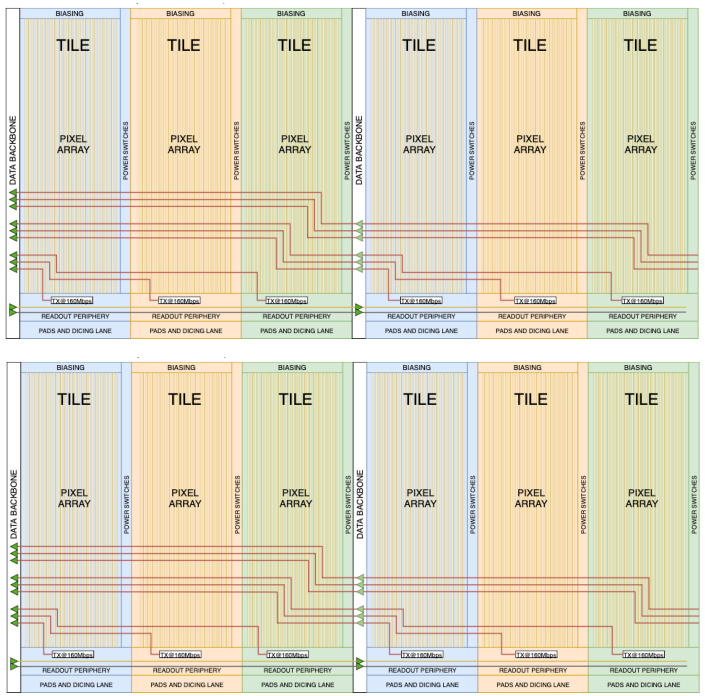
Data Flow – From Tiles to Left Endcap



72 Links

72 Links

x 12 RSU



12-RSU MOSAIX (SVT IB)

The data encoding block is the **lpGBT's TX** core
160 Mbps x 144 = 22.5 Gbps
Full capacity: 8 HS serializers = 80 Gbps (10 Gbps each, only 3 used)
Fallback: 40 Gbps, 5 Gbps each (6 used)
4 serializer data outputs drive one VTRx+

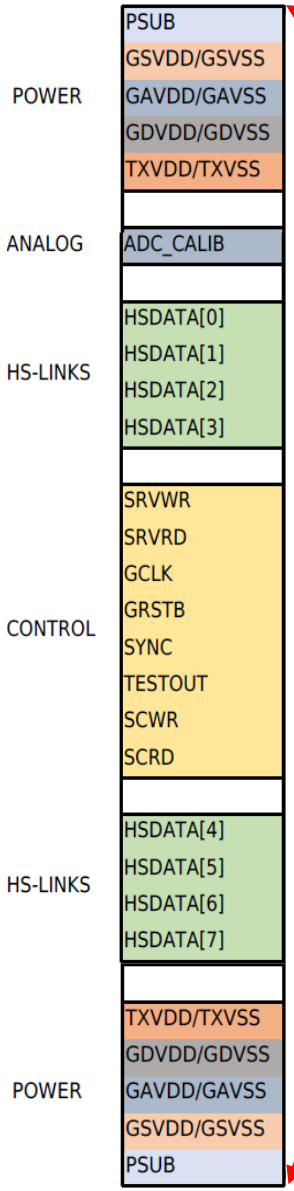
SVT Outer Barrel & Disks

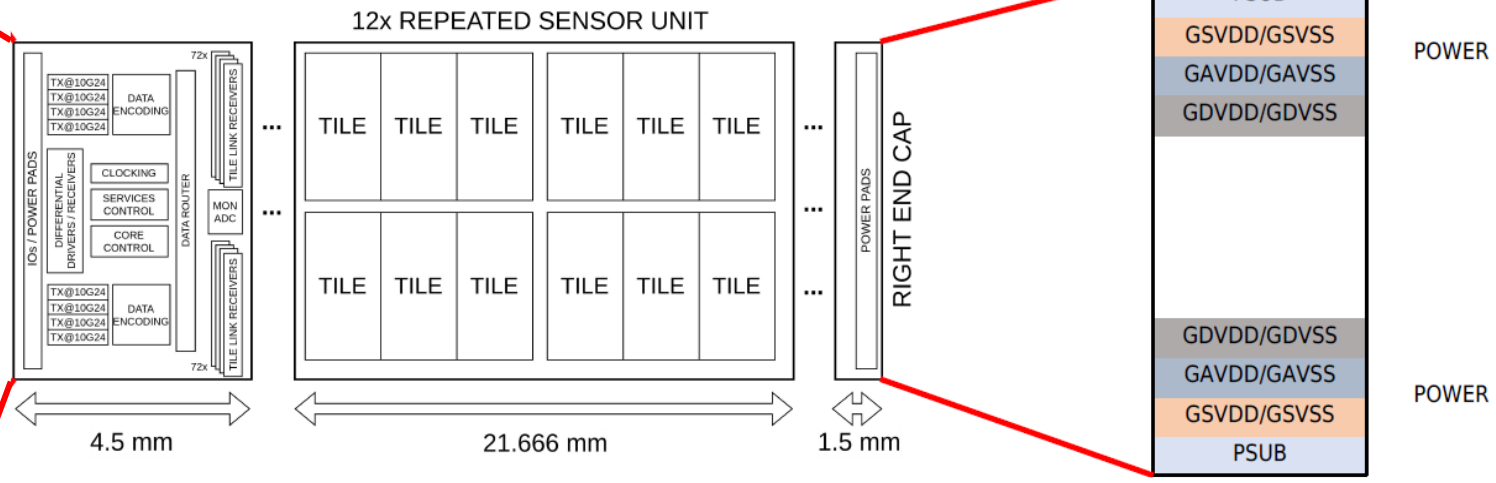
6-RSU LAS
72 Tiles
1 HS serializer = 10 Gbps

5-RSU LAS
60 Tiles
1 HS serializer = 10 Gbps

OAK RIDGE National Laboratory

Supplies and I/Os





All I/Os are differential

8x 10.24 Gb/s data outputs

1x clock at 160 MHz

2x slow control buses at 5 Mbps

2x synchronization signals

(slow controls via lpGBT: 1 clk, 4 elink down, 2 elink up, 1 spare down)

Global analog and digital supplies per *segment*

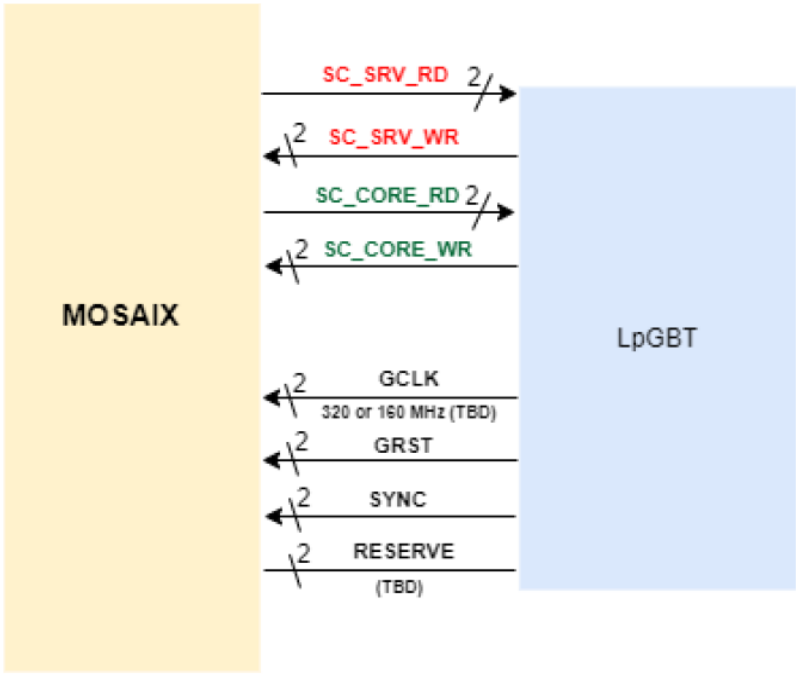
On-chip supply segmentation and control

Reverse biasing of substrate (PSUB)

SVT LAS has power only from the LEC, no REC on LAS

OAK RIDGE National Laboratory

MOSAIX Slow Controls



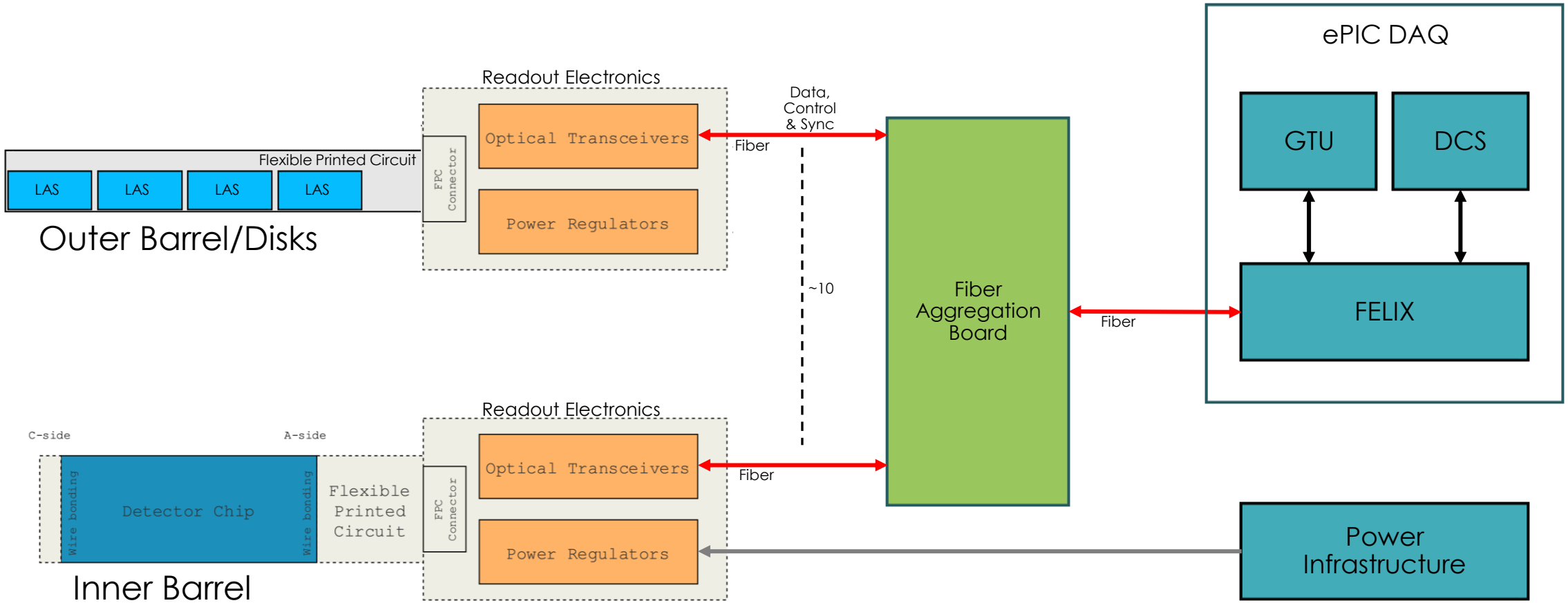
Field ID	Field Name	Width	Description
A	HDR	4	Fixed 4bit (4'hA) value that indicates a start of transaction
B	RW	2	2bit field to indicate transaction type: 0 – WRITE_posted transaction, 1 – WRITE_non-posted transaction, 2 – READ transaction
C	EP_ADDR	8	Endpoint Address
D	REG_ADDR	8	Register Address
E	REG_DATA	16	Register write or read data
F	PARITY	1	Transaction parity bit (bit-wise xor of RW, EP_ADDR, REG_ADDR and REG_DATA fields
G	STOP	1	Stop bit: 1'b0: Fixed 1bit (1'b0) value that indicates end of transaction

Slow Controls Physical Layer:

- CERN Low Power Signaling (CLPS)
- MSB first
- Manchester encoded

Transaction type	Direction	HDR	RW	ADDR	DATA	PARITY	STOP
WRITE_posted	Input to the ASIC	4'b1010	2'b00	Any valid register address	Data to write to the register	xor(HDR, RW,ADDR,DATA)	1'b0
WRITE_non-posted	Input to the ASIC	4'b1010	2'b01	Any valid register address	Data to write to the register	xor(HDR, RW,ADDR,DATA)	1'b0
WRITE-response	Output of the ASIC	4'b1010	2'b01	Register address as specified in the corresponding WRITE_non-posted transaction	Value of the register	xor(HDR, RW,ADDR,DATA)	1'b0
READ	Input to the ASIC	4'b1010	2'b10	Any valid register address	16'd0 (or 8'd0)	xor(HDR, RW,ADDR,DATA)	1'b0
READ-response	Output of the ASIC	4'b1010	2'b10	Register address as specified in the corresponding READ transaction	Value of the register	xor(HDR, RW,ADDR,DATA)	1'n0

SVT Electronics – Simplified Overview



OAK RIDGE National Laboratory

Backend: ATLAS FELIX Development for Phase-2

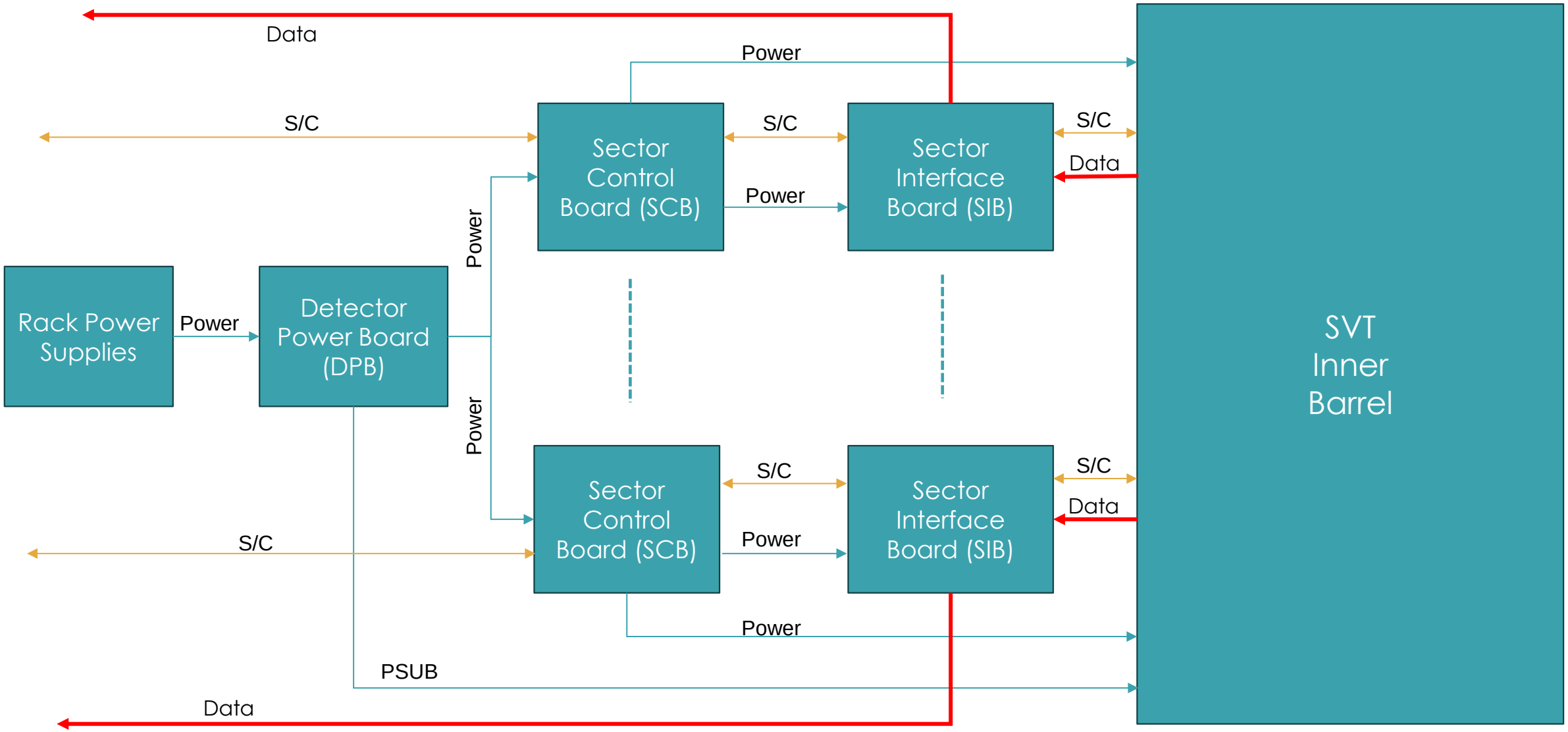
FELIX - 182

- FPGA: AMD Versal Prime VM1802
- PCIe Gen4x16 interface (240 Gb/s)
- 4 FireFly transceivers with 3 possible configurations
  - 24 links up to 25 Gb/s
  - 24 links up to 10 Gb/s (CERN-B FireFly)
  - One duplex FireFly transceiver with 2 possible configurations with 14 or 25 Gb/s

FELIX - 155

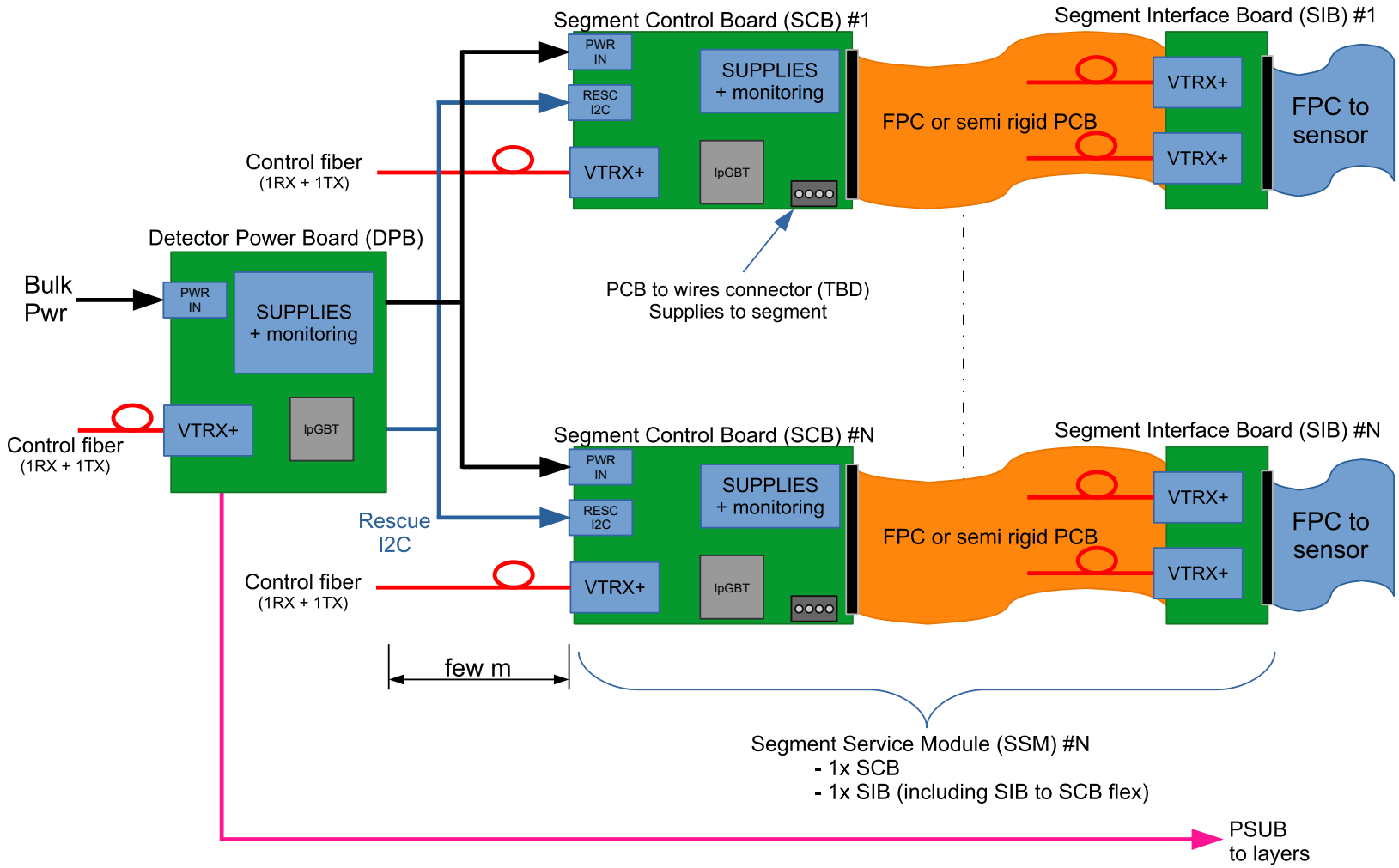
- FPGA: AMD Versal Premium VP1552 FPGA,
- PCIe Gen5x16 interface (482 Gb/s) ,
- up to 48 bidirectional links

IB Readout Scheme

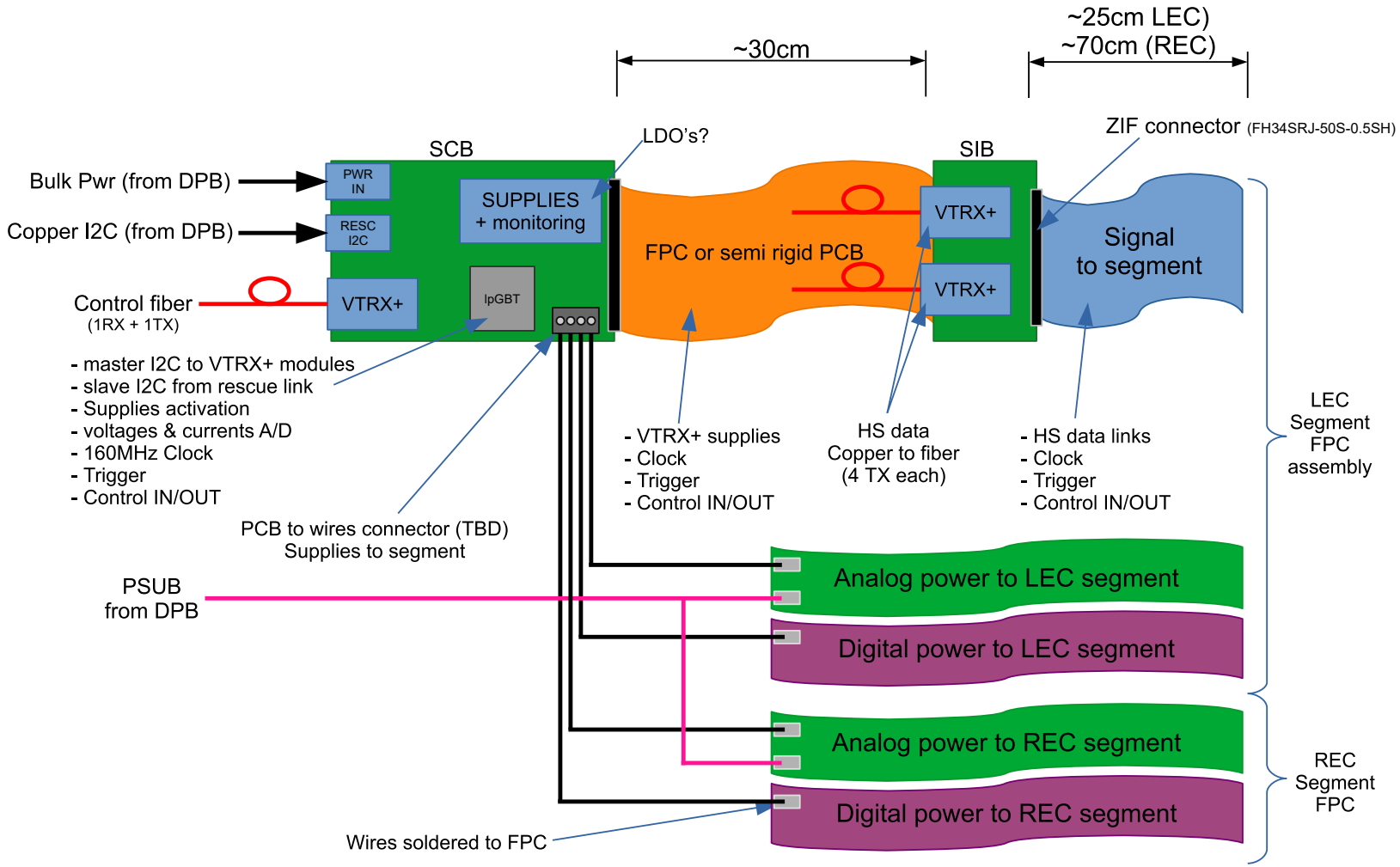


OAK RIDGE National Laboratory

IB Readout Architecture



Readout Segment Architecture

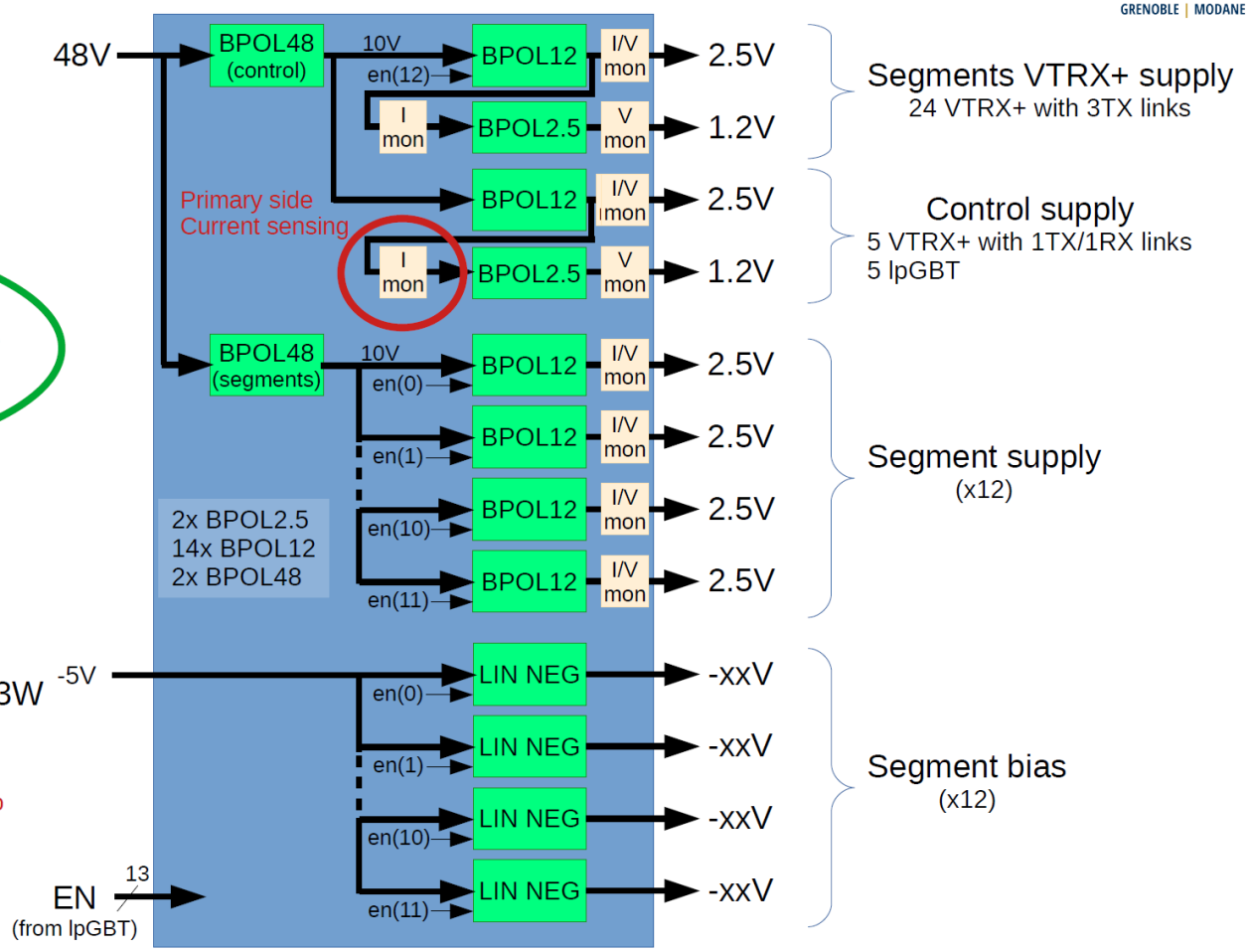


Detector Electronics – Power Tree ITS3 Half Barrel

Starting hypothesis :

- Segment VTRX+ supply
  - @1.2V : 24 x (3 x 10 + 5) = 840mA
  - @2.5V : 24 x 3 x 15 = 1080mA
    - 2 VTRX+ for 1 segment
- Control supply
  - @1.2V : 5 x 15 + 5 x 416 = **2155mA**
  - @2.5V : 5 x 55 = 275mA max
    - LpGBT (5GBPS) < 500mW
- ASIC (segment) supply & bias
  - @2.5V : 1700mA ?
  - @bias V : -1mA ?
- TOTAL Power : **97W** (~2A@48V)
  - BPOL48 control output power : 15W
  - BPOL48 segments output power : 73W
    - assuming BPOL48 efficiency = 90%
    - assuming BPOL12 efficiency = 70%
    - assuming BPOL2.5 efficiency = 80%

Power Tree (updated)



D. Tourres - LPSC/IN2P3/CNRS

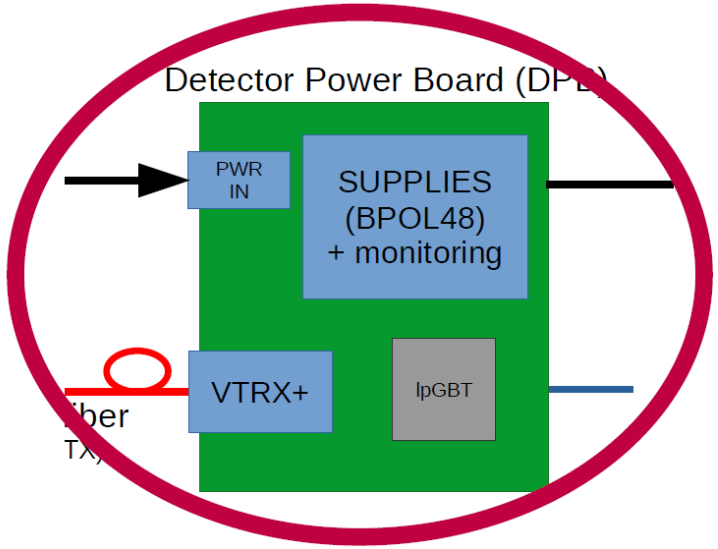
OAK RIDGE National Laboratory

J. Schambach

DPB Power & Thermal Estimation

- 1.2V supply (lpGBT & VTRX+) : 431mA / 518mW
  - BPOL12 consumption @10V : 740mW
  - BPOL12 onboard dissipation : **~222mW**
- 2.5V supply (VTRX+) : 55mA / 138mW
  - linPOL12 consumption @10V : 550mW
  - linPOL12 onboard dissipation : **~0.42W**
- 10V supply : 0.74W + 0.55W + 12x 6.1W = ~74.5W / 7.5A
  - BPOL48 consumption @48V : 83W
  - BPOL48 onboard dissipation : **~8.5W**

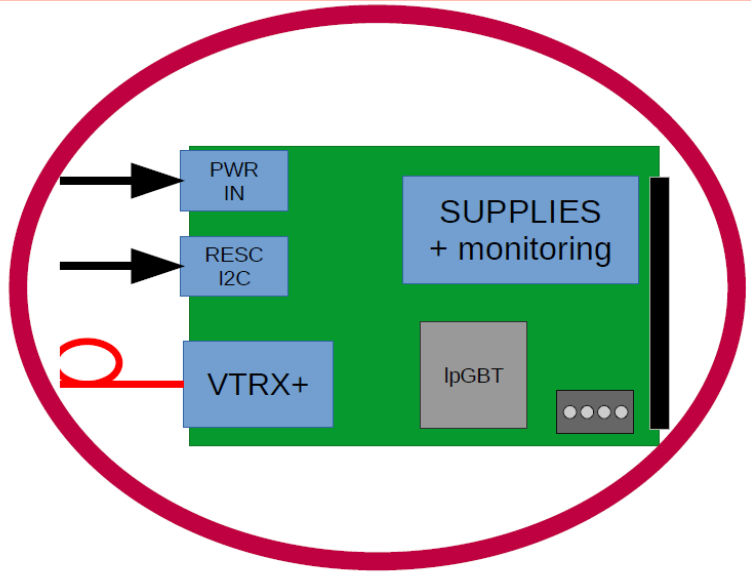
DPB onboard
thermal dissipation
8.5W



Assuming:
- BPOL12 efficiency **70%**
- BPOL48 efficiency **90%**

SCB Power & Thermal Estimation

- 1.2V Control supply (lpGBT & VTRX+) : 501mA / 602mW
  - BPOL12 consumption @10V : 860mW
  - BPOL12 onboard dissipation : **~0.26W**
- 2.5V Control supply (VTRX+) : 145mA / 363mW
  - BPOL12 consumption @10V : 519mW
  - BPOL12 onboard dissipation : **~0.16W**
- GSVDD Segment supply : 50mA@1.32V → 66mW
  - linPOL12 consumption @10V : 500mW
  - linPOL12 onboard dissipation : **~0.44W**
- GDVDD Segment supply : 1.43A@1.3V → 1.86W
  - BPOL12 consumption @10V : 2.66W
  - BPOL12 onboard dissipation : **~0.8W**
- GAVDD Segment supply : 0.54A@1.3V → 0.7W
  - BPOL12 consumption @10V : 1W
  - BPOL12 onboard dissipation **: ~0.3W**
- TXVDD Segment supply : 0.2A@1.8V → 0.36W
  - BPOL12 consumption @10V : 0.52W
  - BPOL12 onboard dissipation **: ~0.16W**



→ Assuming BPOL12 efficiency **70%** ←

SCB onboard thermal dissipation:
- One SCB: **~2.12W**
- Half-barrel (12x SCB): **~25.5W**

SCB power consumption:
- One SCB: **~6.1W**
- Half-barrel (12x SCB): **~73.2W**

6/8

SIB Power & Thermal Estimation

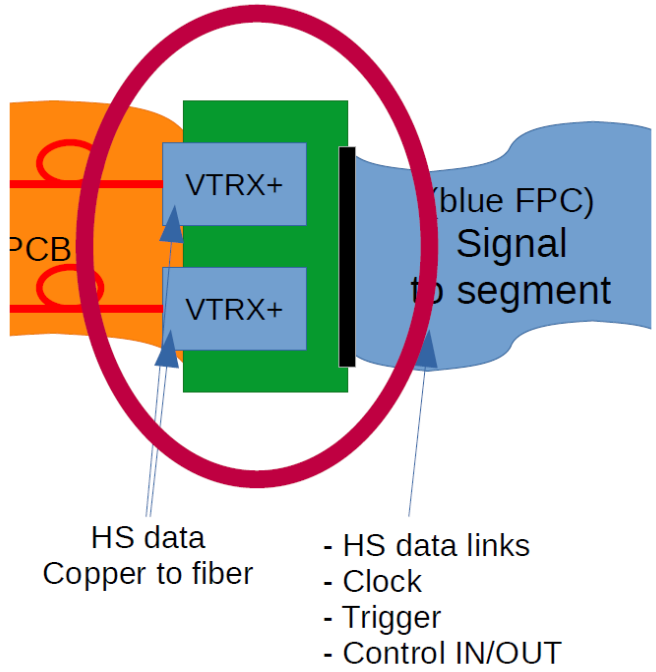
one VTRX+ supplies (3 TX links enabled)

- 1.2V : 3x 10mA + 5mA = 35mA / 42mW
- 2.5V : 3x 15mA = 45mA / 113mW

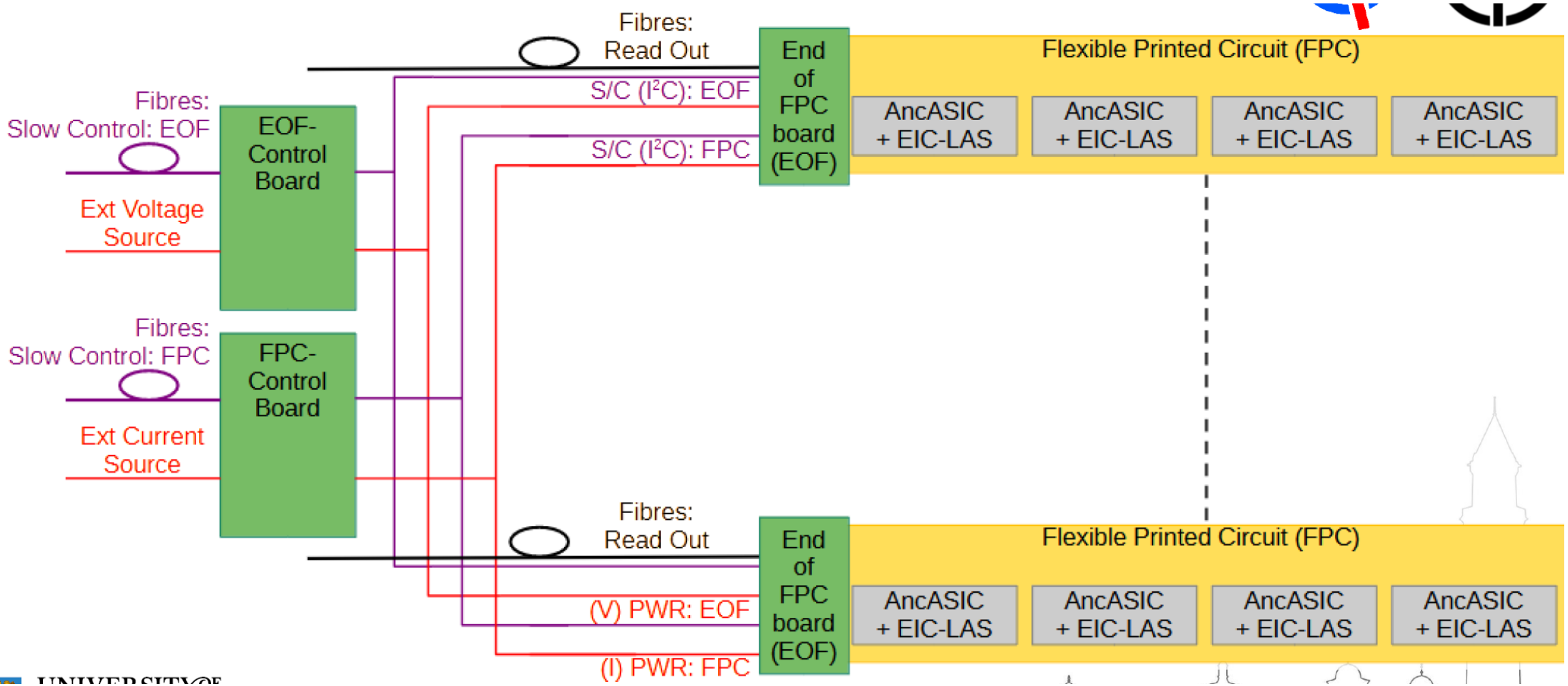
one SIB supplies & dissipation

- 1.2V : 70mA
- 2.5V : 90mA
- Power : **310mW**

Half-barrel (12x SIB)
thermal dissipation
3.72W



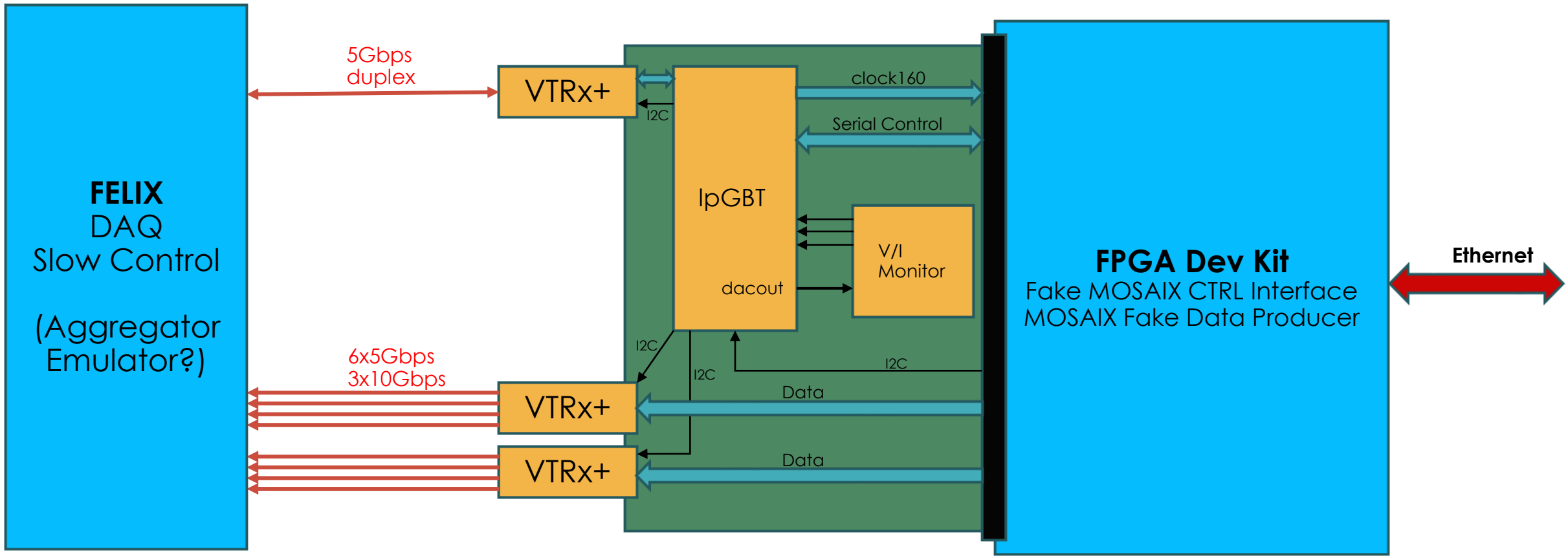
OB/Disc Readout Architecture (from James)



OAK RIDGE National Laboratory

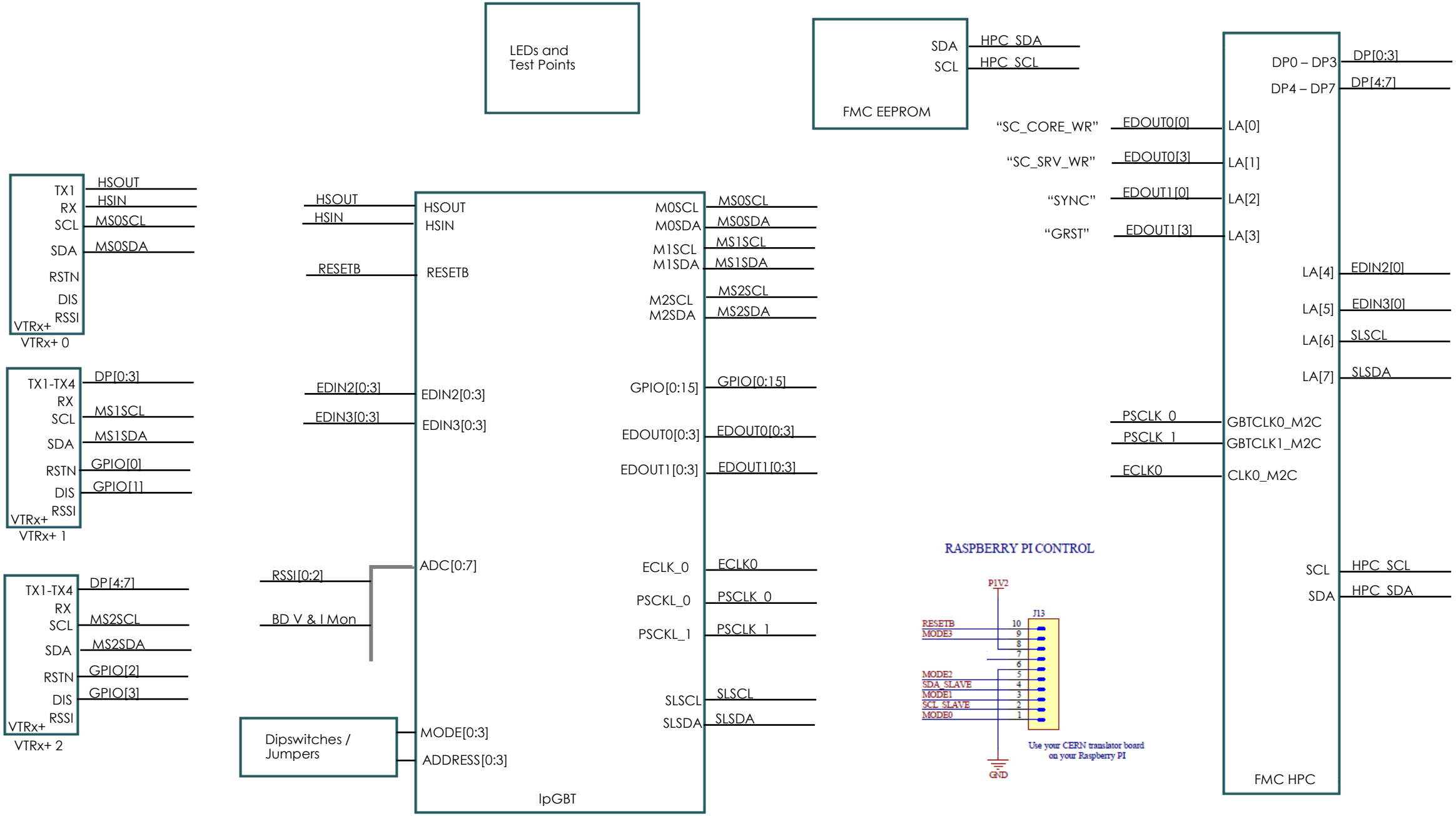
Prototyping Efforts

MOSAIX Hardware Mockup

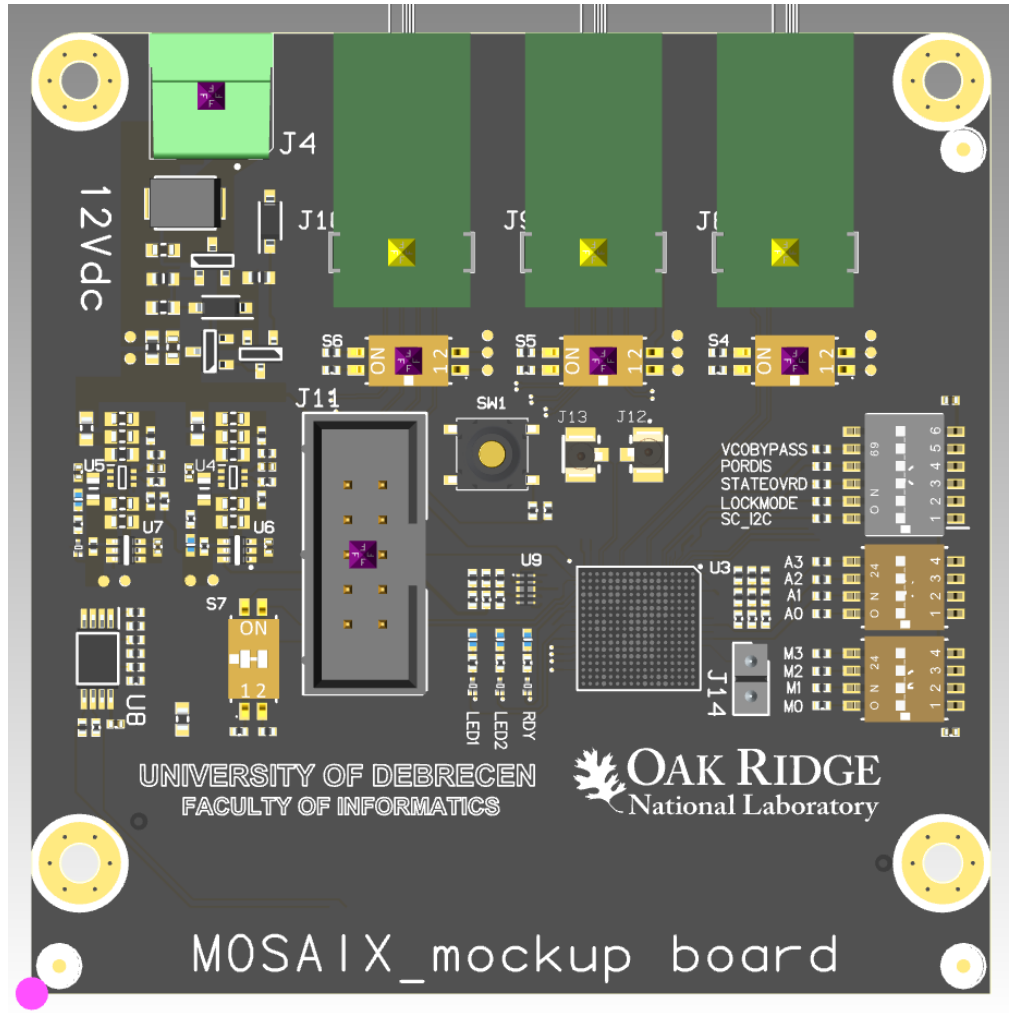


VTRx+ connected to FMC HPC (8 MGT available), emulate typical packets

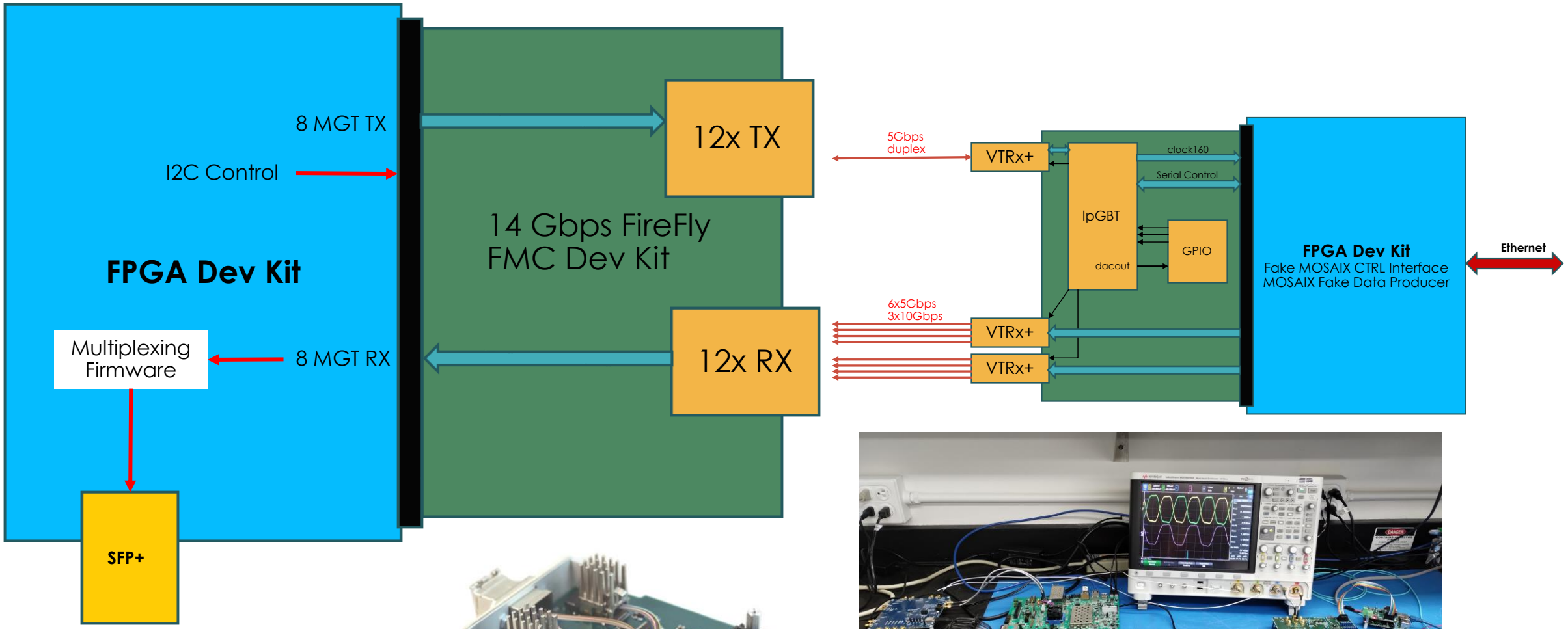
OAK RIDGE National Laboratory

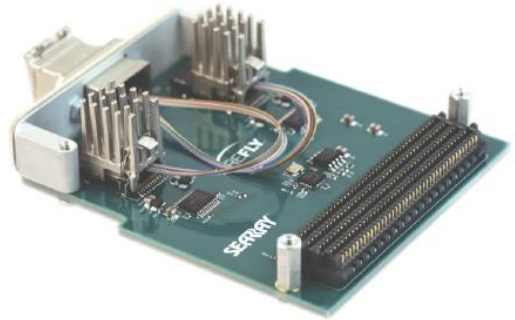


OAK RIDGE National Laboratory


J4
12Vdc
S6
S5
S4
J11
SW1
J13
J12
U5
U4
U7
U6
U9
U3
S7
ON
U8
J14
VCOBYPASS
PORDIS
STATEOVRD
LOCKMODE
SC_I2C
A3
A2
A1
A0
M3
M2
M1
M0
LED1
LED2
RDY
UNIVERSITY OF DEBRECEN
FACULTY OF INFORMATICS
OAK RIDGE
National Laboratory
MOSAIX_mockup board

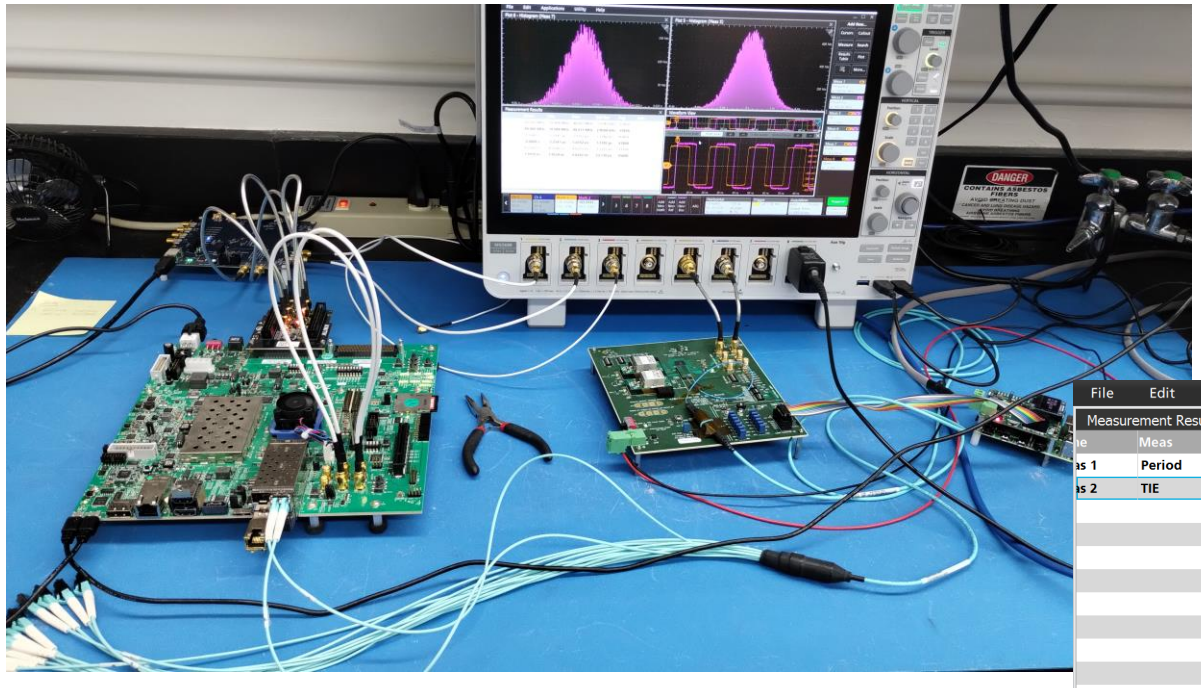
Aggregator Board Prototyping





OAK RIDGE National Laboratory

TIE Measurement with ZCU102 and Tektronix Scope



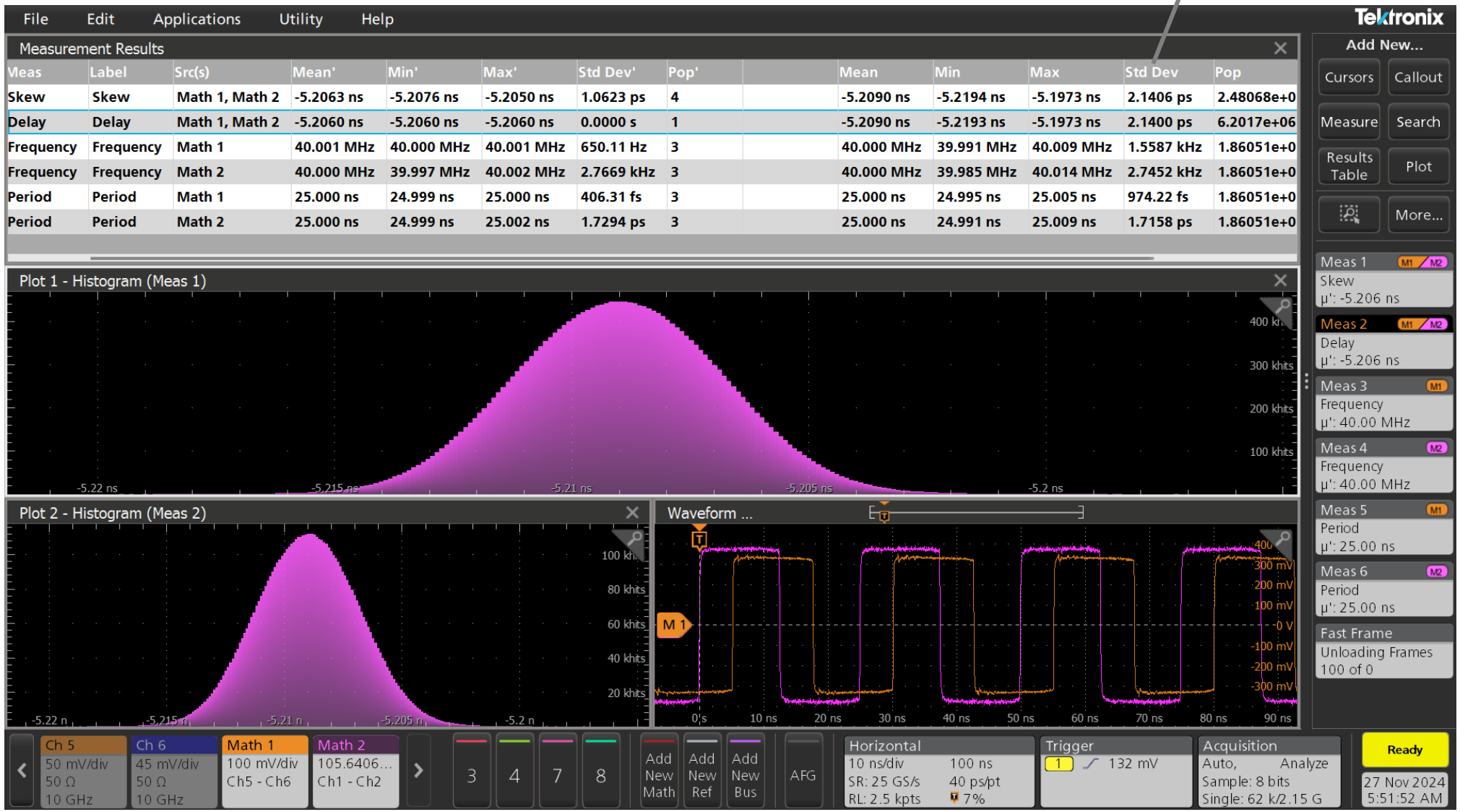
TIE Std Dev ~800ps

OAK RIDGE National Laboratory

J. Schambach

Skew and Delay Measurements

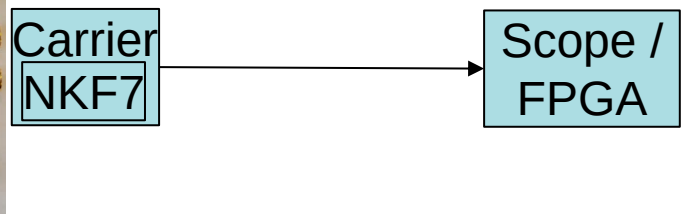
Phase Std Dev ~2.2ps

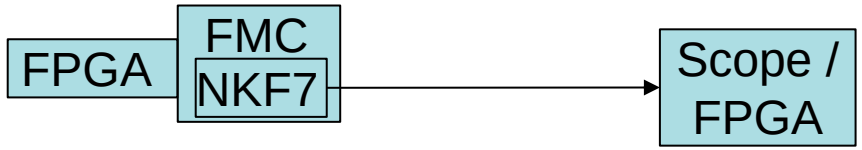


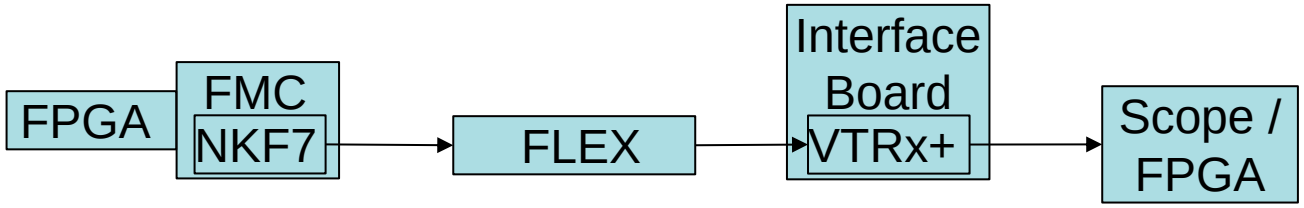
OAK RIDGE National Laboratory

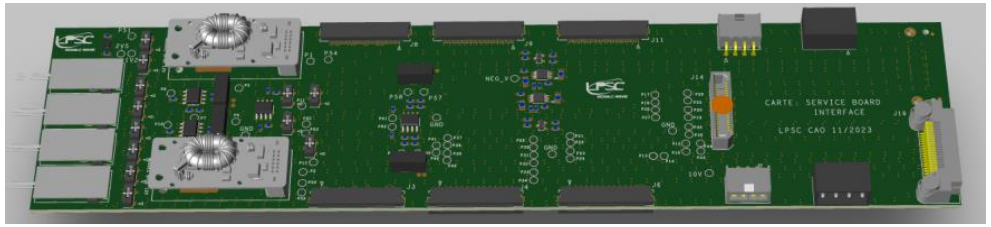
NKF7 Serializer Test Steps

- Characterize NKF7 with fixed 16-bit pattern
  - Scope eye-pattern
  - FPGA BER test
  - Radiation test with Prague 32 MeV protons Done
- Characterize NKF7 with variable pattern
- Characterize NKF7 + Flex (design by Antoine)
  - Scope eye-pattern
  - FPGA BER test & statistical eye
- Characterize NKF7 + Flex + VTRx+ Transceiver
  - Scope eye-pattern (optical probe or after minipods on CRU)
  - Receiver (minipod / FPGA / CRU) BER test



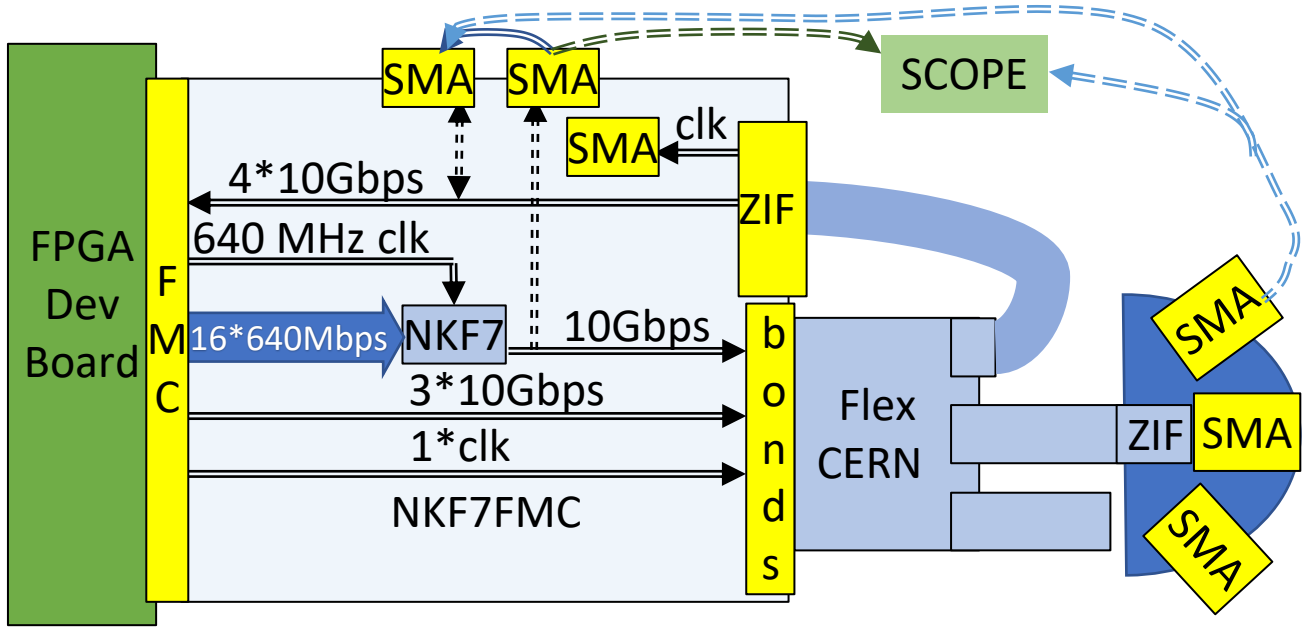






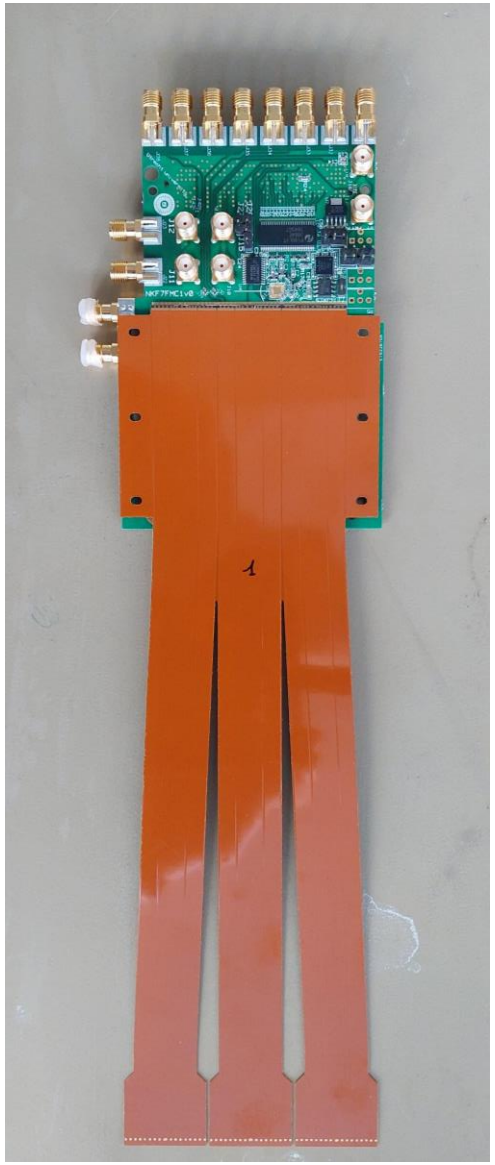
NKF7FMC Concept

- NKF7 16bit data controlled by FPGA
  - Allows for PRBS or (8b/10b encoded) data
- Data input rate 640Mbps
  - Are NKF7 inputs fast enough?
  - Use fast interface (e.g. FMC)
  - No switches, jumpers & capacitors on data lines
  - Measurements showed CMOS 1.2V not feasible
    => Use differential signals.

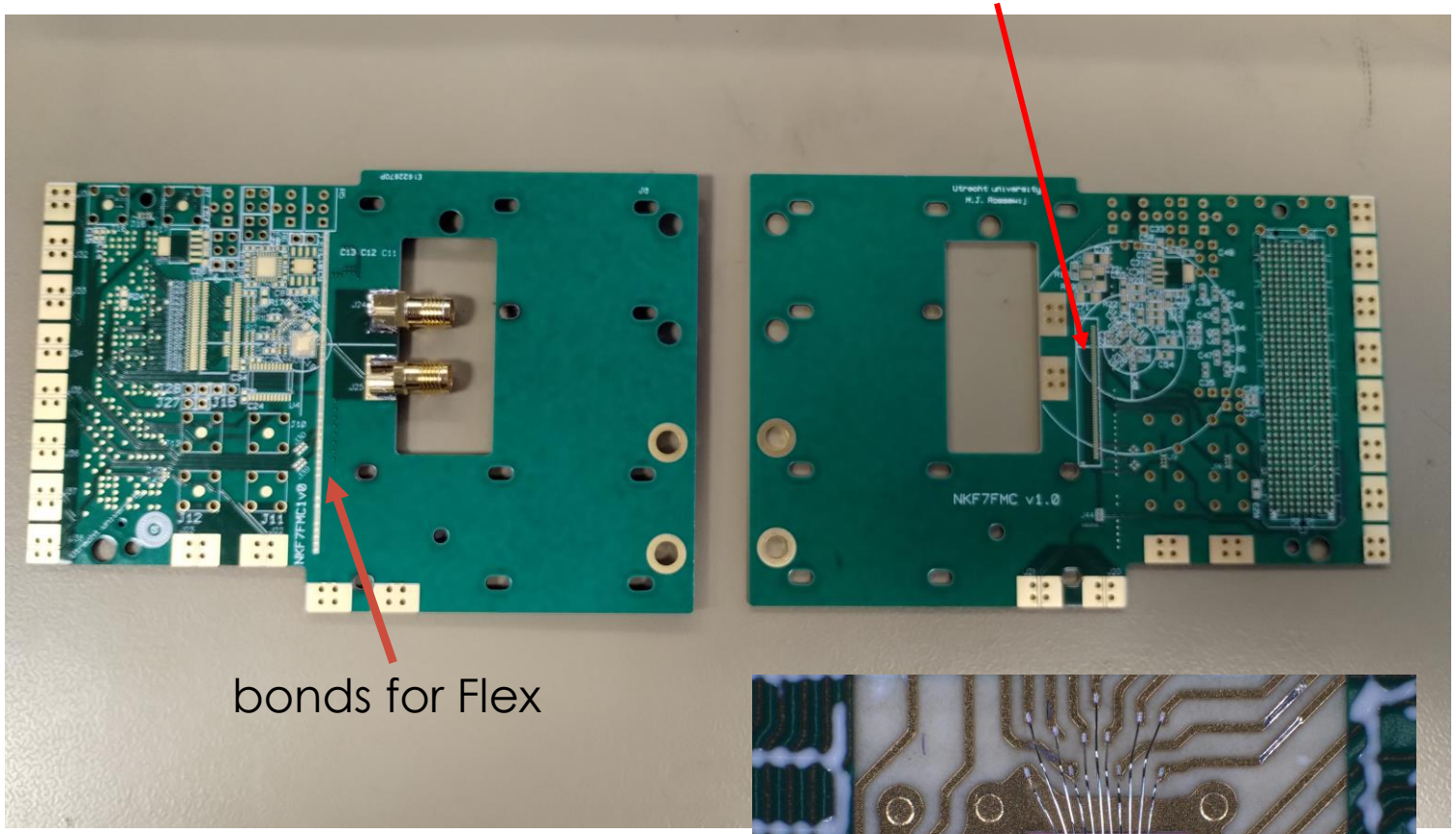


- NKF7 10 Gbps data output:
  - to SMA connectors (scope or loopback to FPGA transceiver input)
  - CERN ITS3 designed Flex cable
- 3 adjacent high-speed lines (+ clock line) connected to FPGA transceivers
  - Allows for transmission & xtalk tests
- CERN flex cable either goes to
  - SMA breakout board (to scope)
  - Loop back to the NKF7FMC ZIF connector
- Minimize bond wire length & power decoupling capacitors closer to NKF7 to reduce PS network inductance

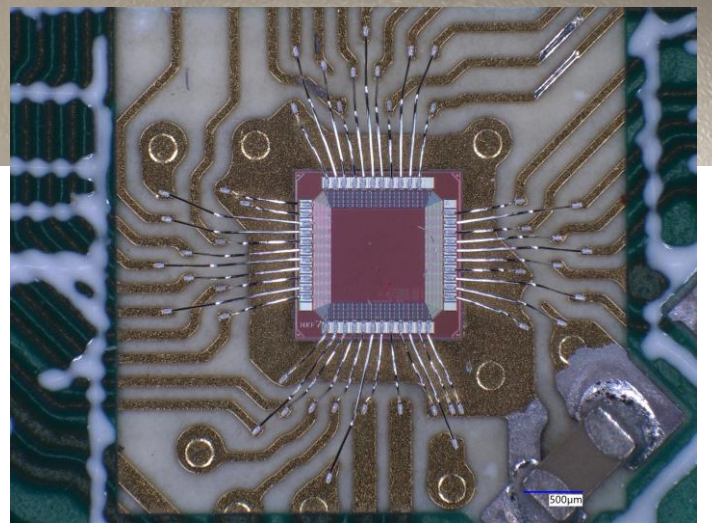
NKF7FMC Pictures



ZIF connector for
Flex loop back



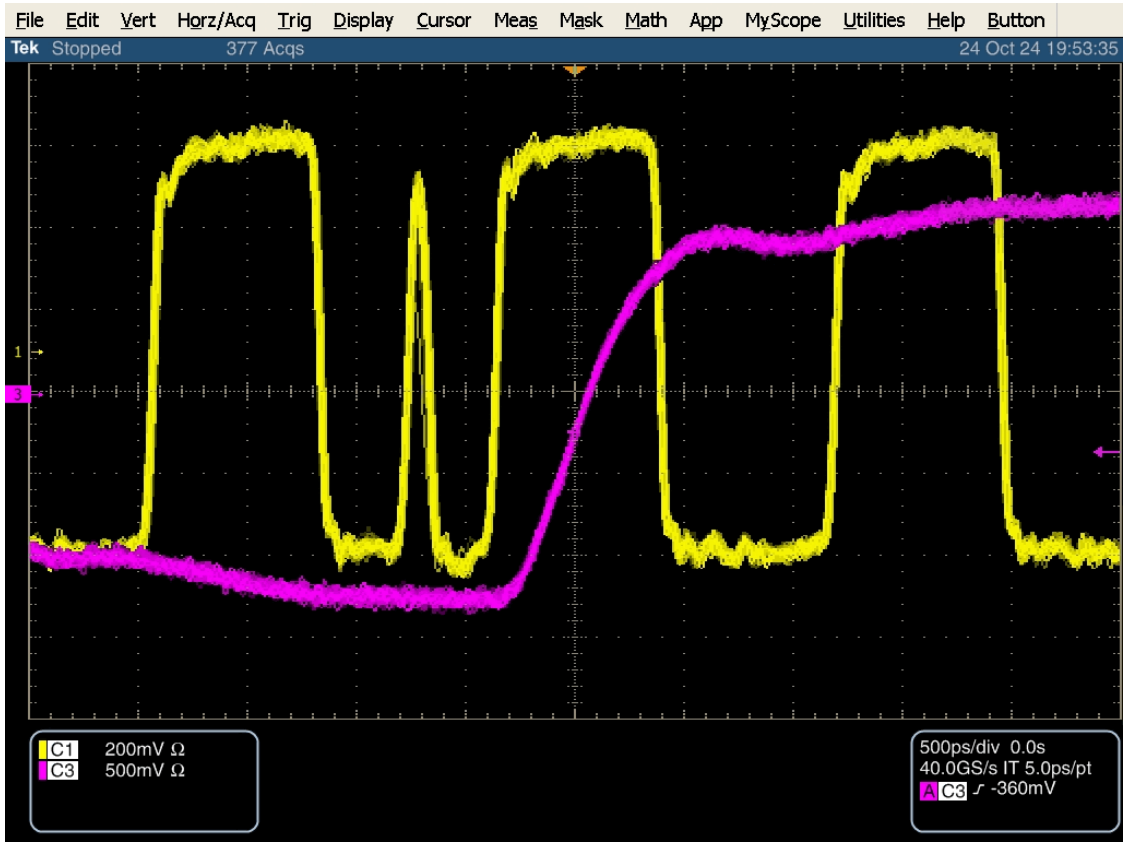
bonds for Flex



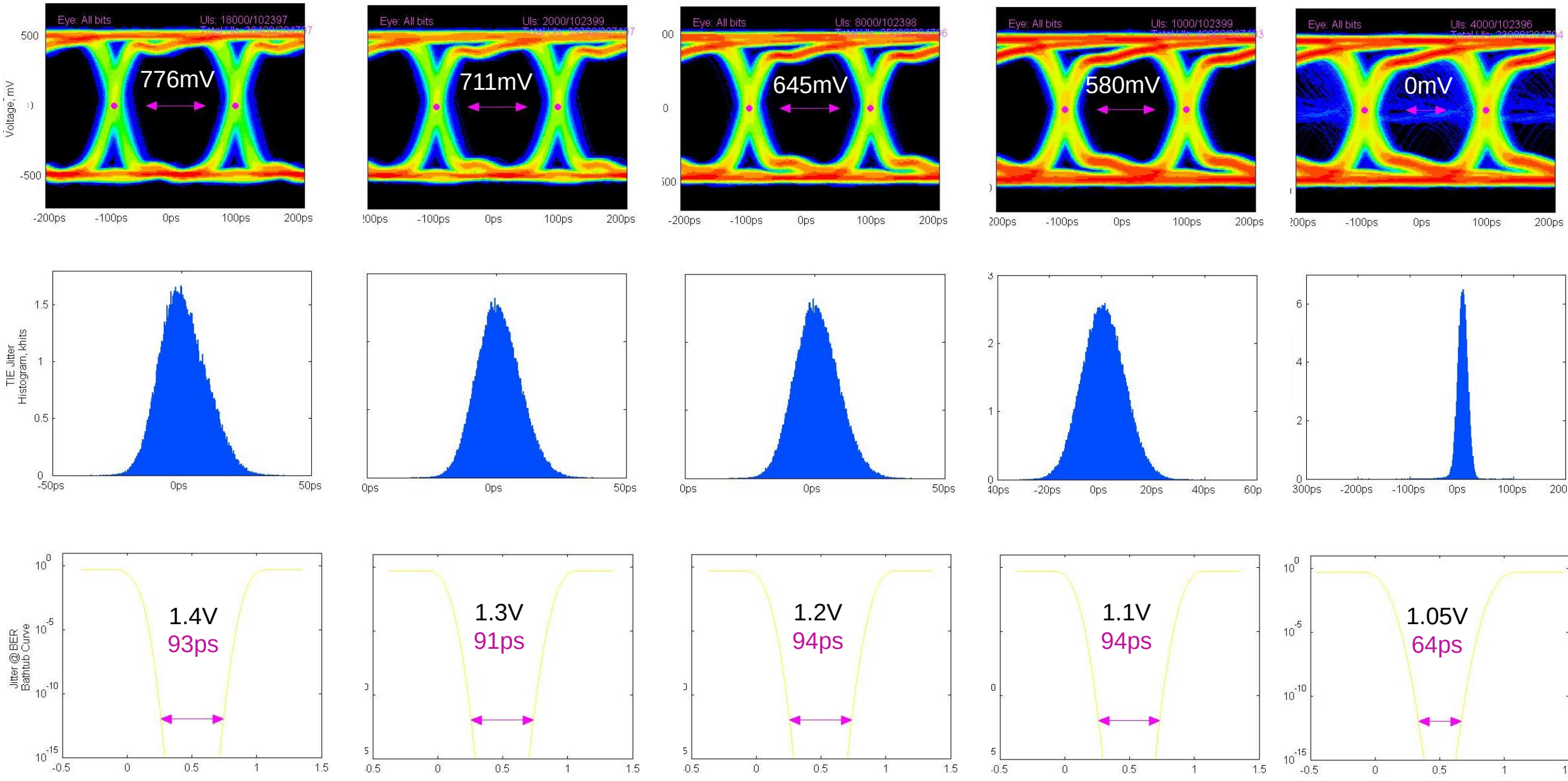
OAK RIDGE National Laboratory

ZCU Firmware with variable (parallel data) bit delays

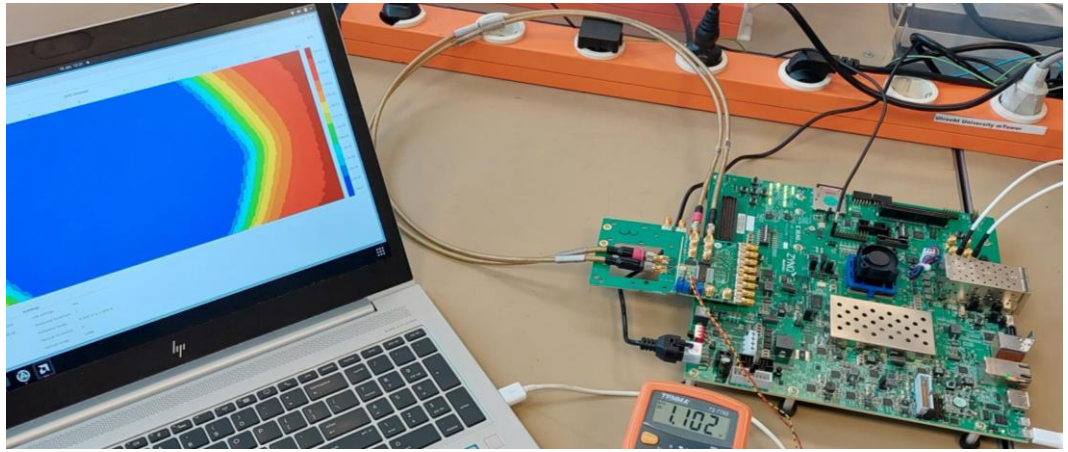
- Firmware can send either fixed patterns or PRBS patterns at 640 MHz via HSSIO
- Enabled the firmware to set a variable bit sequence for fixed patterns in time.
  - Created 4 time slots (640 MHz fits 4 times into 160 MHz)
  - One can set a sequence for each time slot.
- For example one can set the sequences as:
  - F00F: 1111 0000 000 1111
  - F00F: 1111 0000 000 1111
  - F00F: 1111 0000 000 1111
  - F10F: 1111 0001 000 1111
- Adjust bit delays until all bits appear in same frame



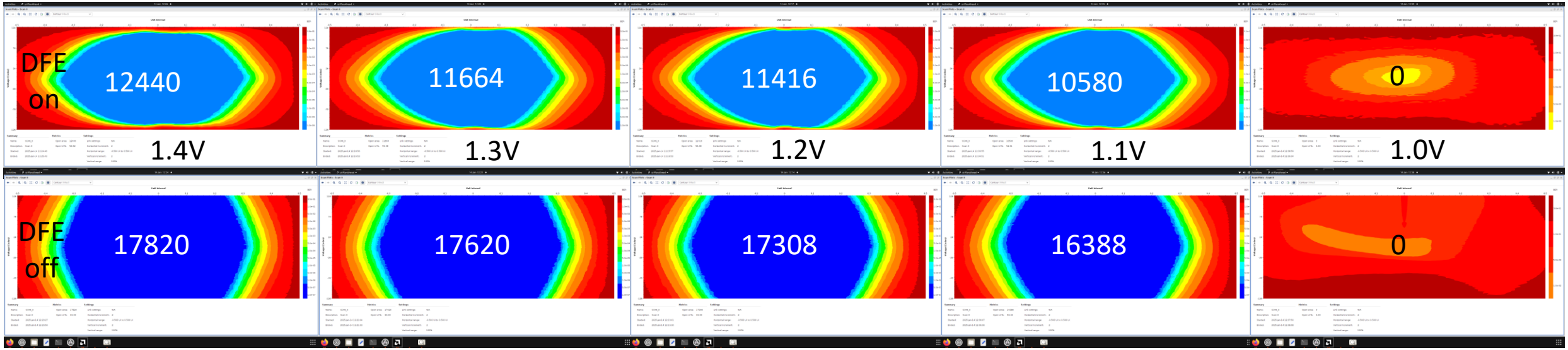
Oscilloscope Eyes with PRBS @ 5Gbps



FPGA Transceiver Statistical Eyes



Conclusion:
At 5.12 Gbps NKF7 operation seems stable
(within certain parameters)

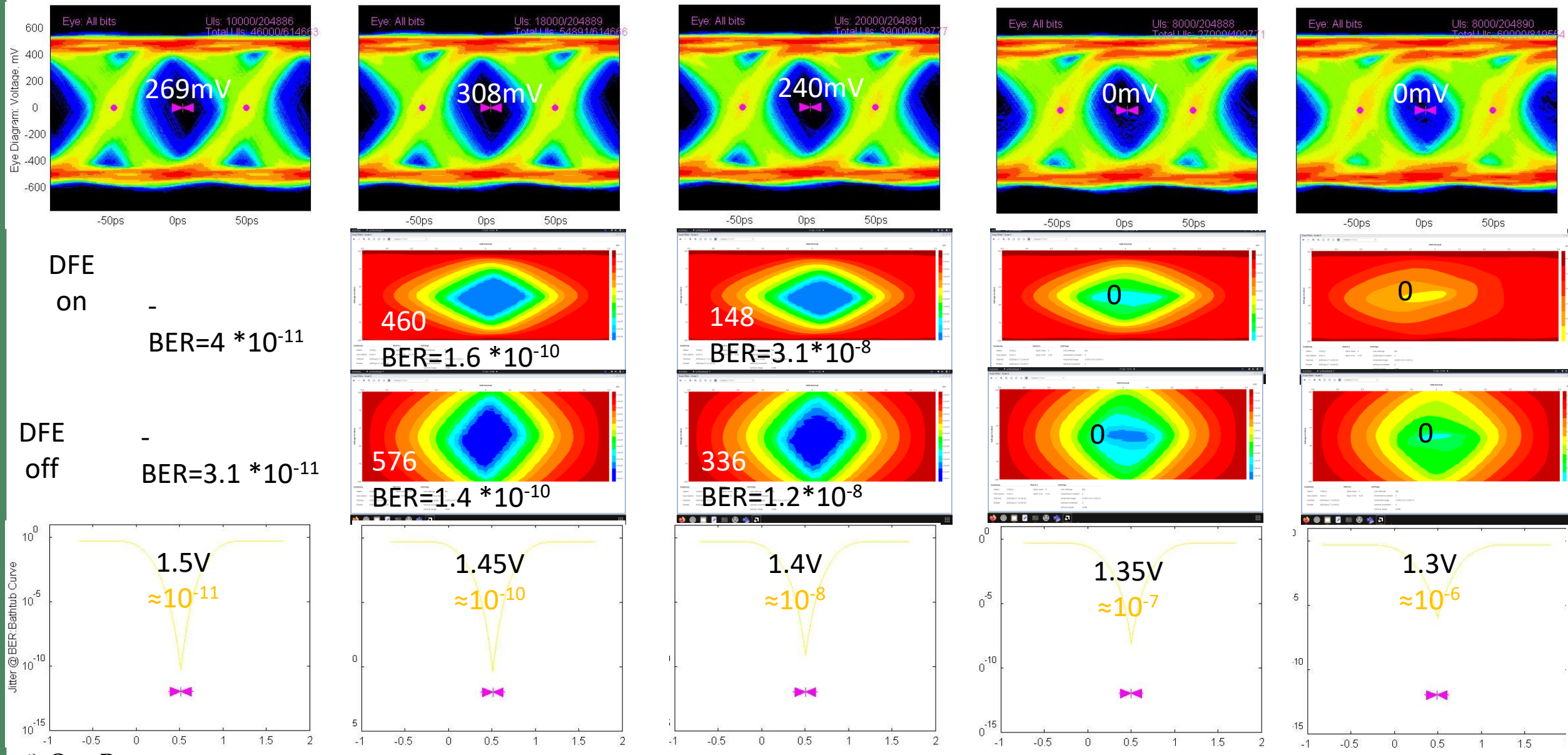


PRBS7, DFE off: 1.35V, 0 error in 20 hrs => BER< $3*10^{-15}$

1.1V, 0 err 20 hrs => $3*10^{-15}$ <1.06V BER explodes

OAK RIDGE National Laboratory

PRBS7 Pattern @ 10.24 Gbps



DFE on - BER=4 *10^{-11}

DFE off - BER=3.1 *10^{-11}

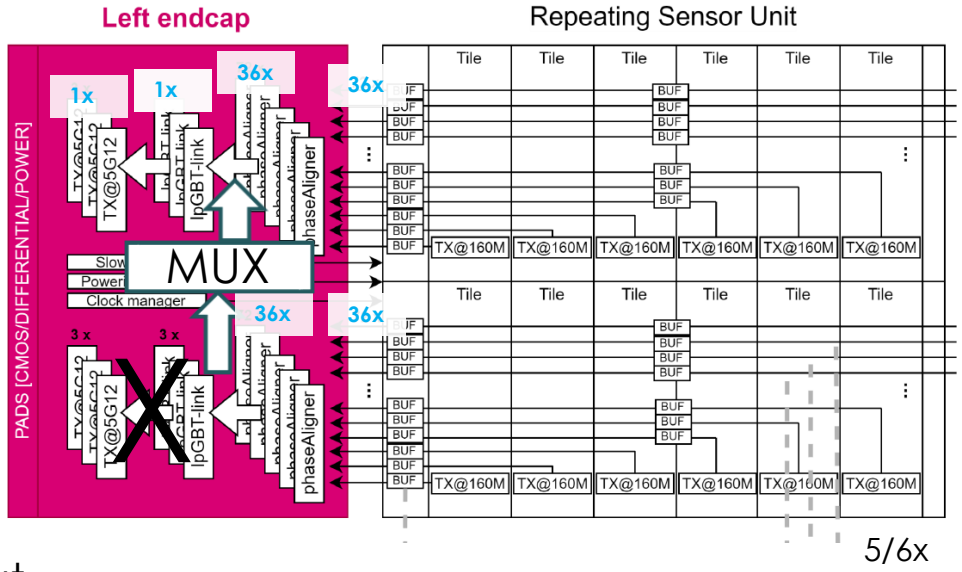
OAK RIDGE National Laboratory

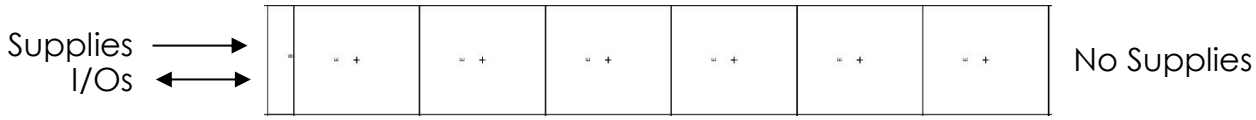
Backup

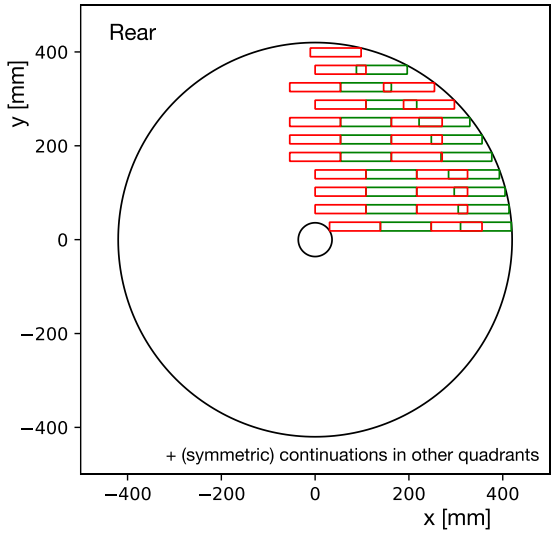
ePIC SVT: "Large Area Sensor" (LAS)

- **Inner Barrel** (Layers 0,1,2) will reuse ITS3-like sensors as is
  - **Layer 0:** 4 sensors in r-phi, 3 segments of 12 RSU
  - **Layer 1:** 4 sensors in r-phi, 4 segments of 12 RSU
  - **Layer 2:** 8 sensors in r-phi, 5 segments of 12 RSU
- EIC **variant** for the **Outer Barrel** (Layers 3,4) and **Endcap Disks**
  - "Large Area Sensor" (LAS)
  - Will be stitched, but not to wafer scale
  - Likely 1 Segment of 5 or 6 RSU (no need for right endcap)
  - The intention is to multiplex Tile data lines to **1** High-Speed output
  - More conventional carbon composite mechanical support with integrated cooling

6-RSU LAS



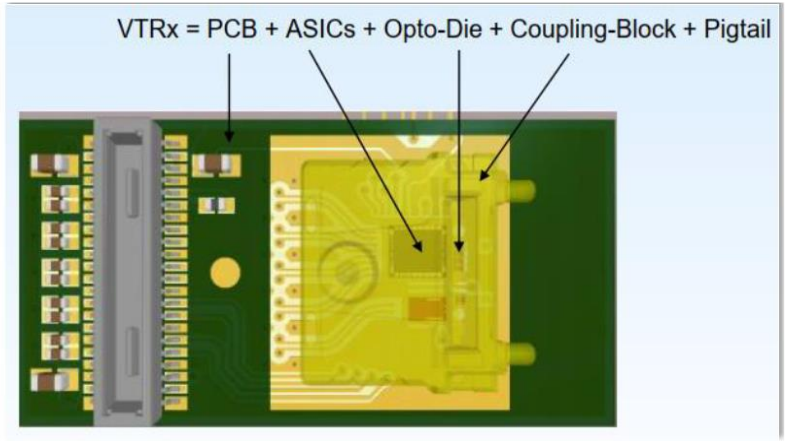


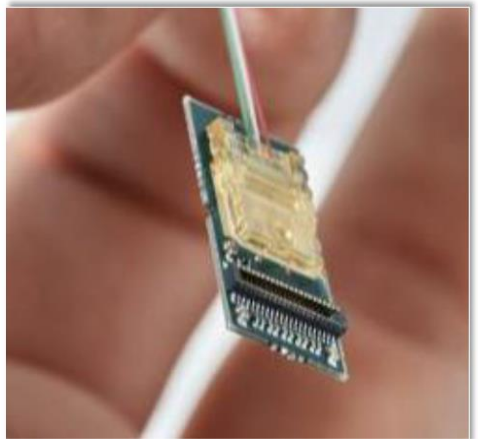


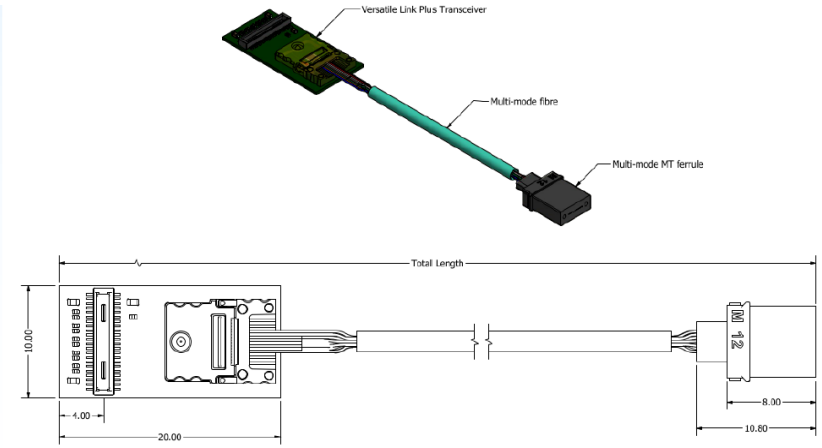
OAK RIDGE National Laboratory

VTRx+ Front-end Module

- **Versatile**
  - Up to 4 Tx + 1 Rx, configurable by masking channels
- **Miniaturised**
  - 20 x 10 x 2.5 mm
- **Pluggable**
  - Electrical connector
- **Data-rate**
  - Tx: up to 4×10 Gb/s, Rx: 2.5 Gb/s
- **Environment**
  - Temperature: -35 to + 60 °C
  - Total Dose: 100 Mrad
  - Total Fluence: $1x10^{15}$ n/cm^2 and $1x10^{15}$ hadrons/cm^2
- **Status**
  - Pre-production ongoing
  - Solving problems with module assembly
    - Alignment of optical components
  - Ramping up to 2k modules/month in 2023







OAK RIDGE National Laboratory

Remark on timing

Projections for timing resolution

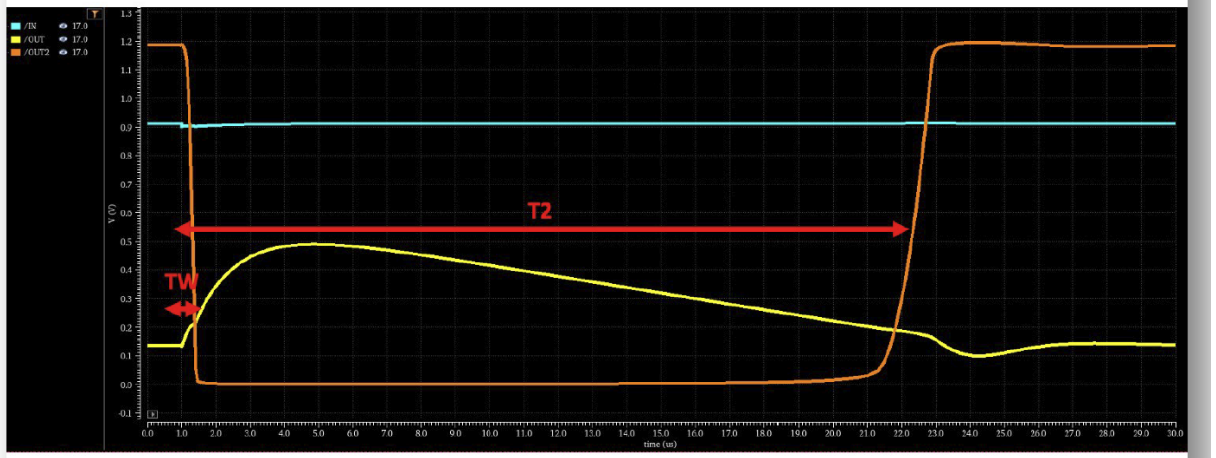
Targeting figures similar to ALPIDE

- Continuous mode readout
- Integration period: 5 / 10 / 20 us
- Frame rate: 200 / 100 / 50 kHz

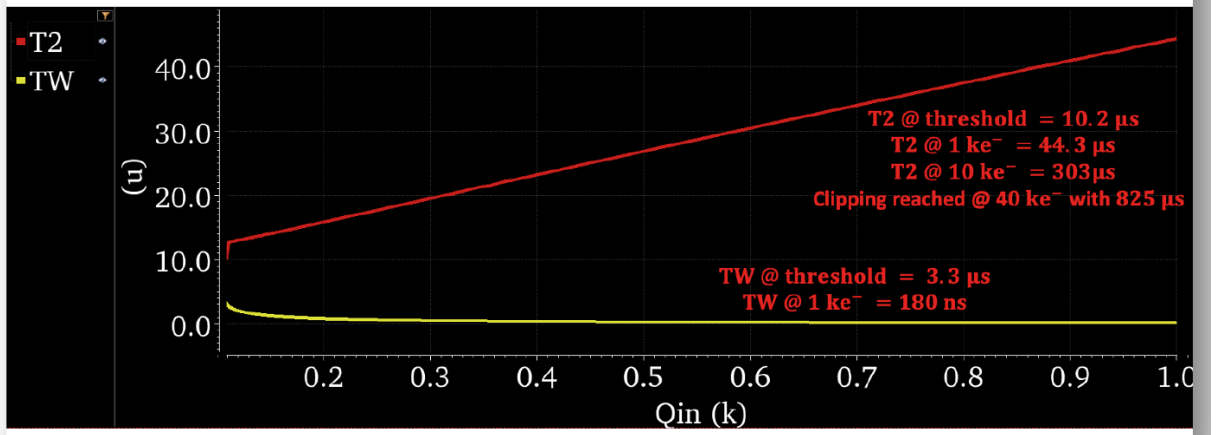
Low power constrains response speed

- MOSS pulse duration 40 us @ 1 ke
- MOSS time walk ~3.3 us
- Reviewing timing specs for next design

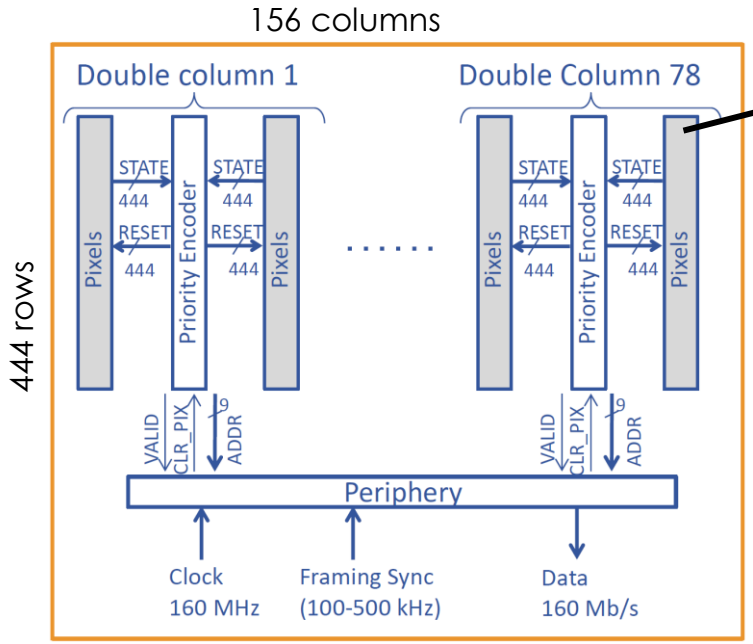
Discriminator time window (MOSS, nominal bias for low power)

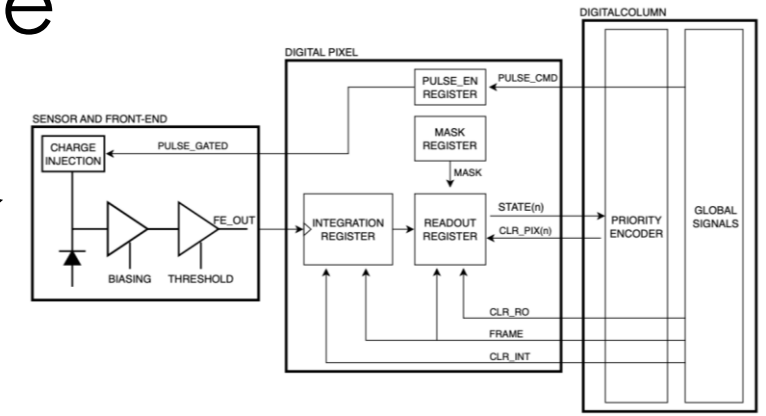


Discriminator time window



Domain (Tile) Architecture





444 x 156 pixels / domain
831168 pixels per RSU
144 domains / segment
9.974 Mpixels / segment

20.8 µm x 22.8 µm pixel pitch(*)
Continuously active front-end (40 nW typ.)
Global shutter
Zero-suppressed matrix readout
Continuous readout mode
Integration time: 2µs to 2^{16}*25ns = 1.6384ms

(*) **Baseline: 20.8 µm * 22.8 µm**
Abs. Max: 22.5 µm * 25 µm

In pixel:

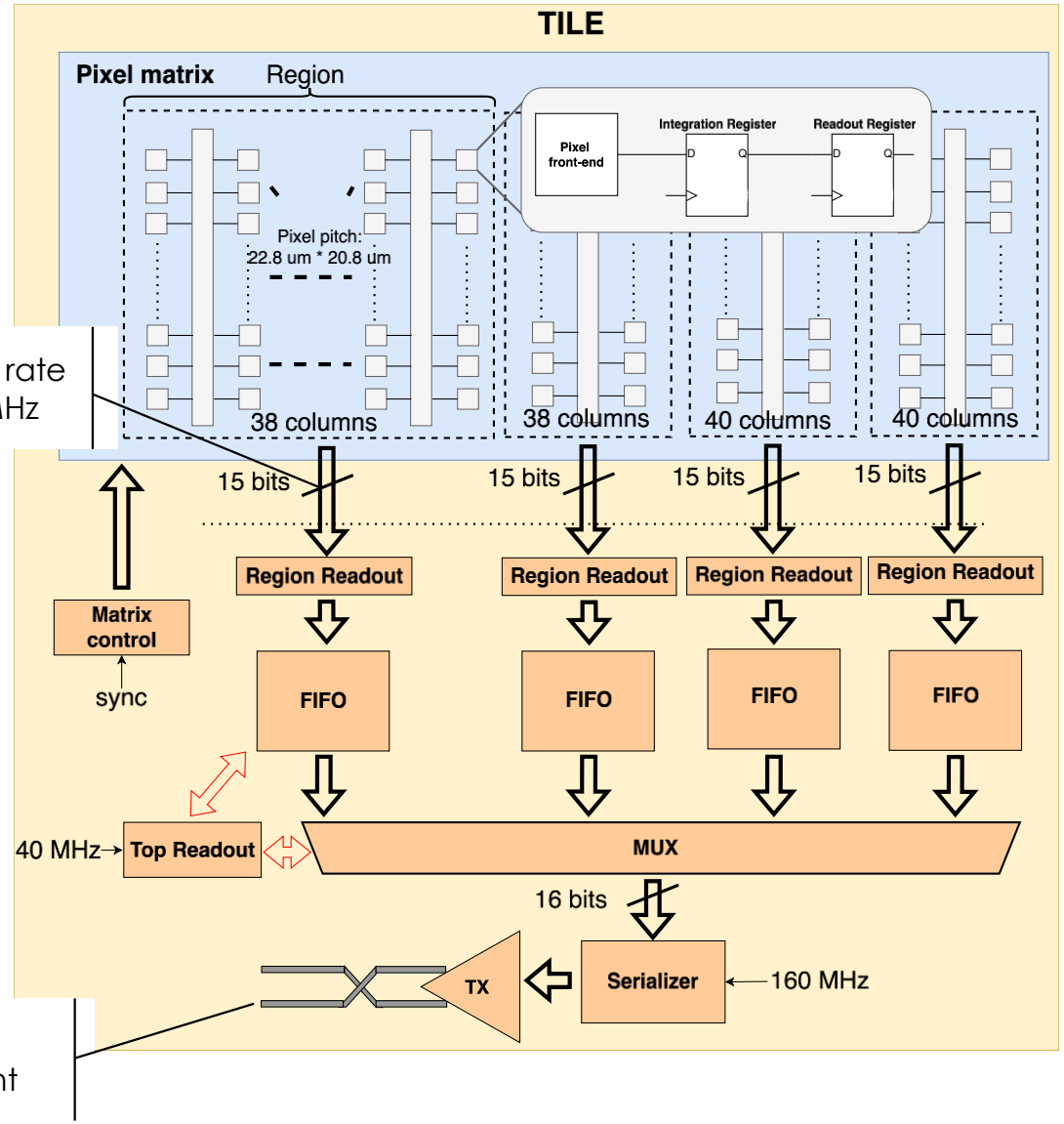
- Amplification
- Discrimination
- Hit integration register and readout register
- Test charge injection
- Digital pulsing
- Masking

Digital pixel designed with low-leakage, high reliability std cells

OAK RIDGE National Laboratory

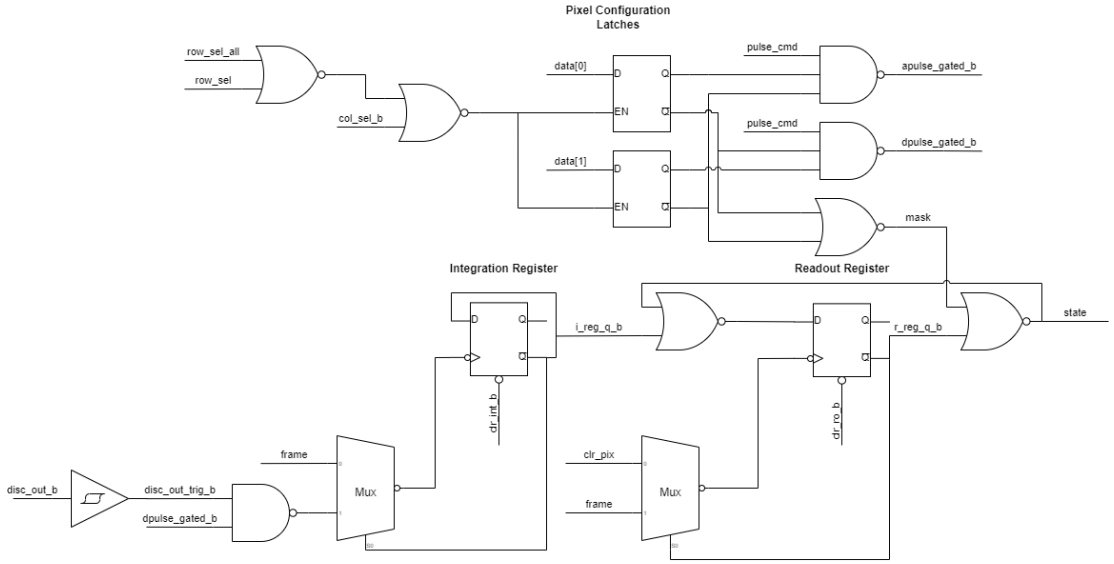
On-chip Readout Scheme in the Periphery

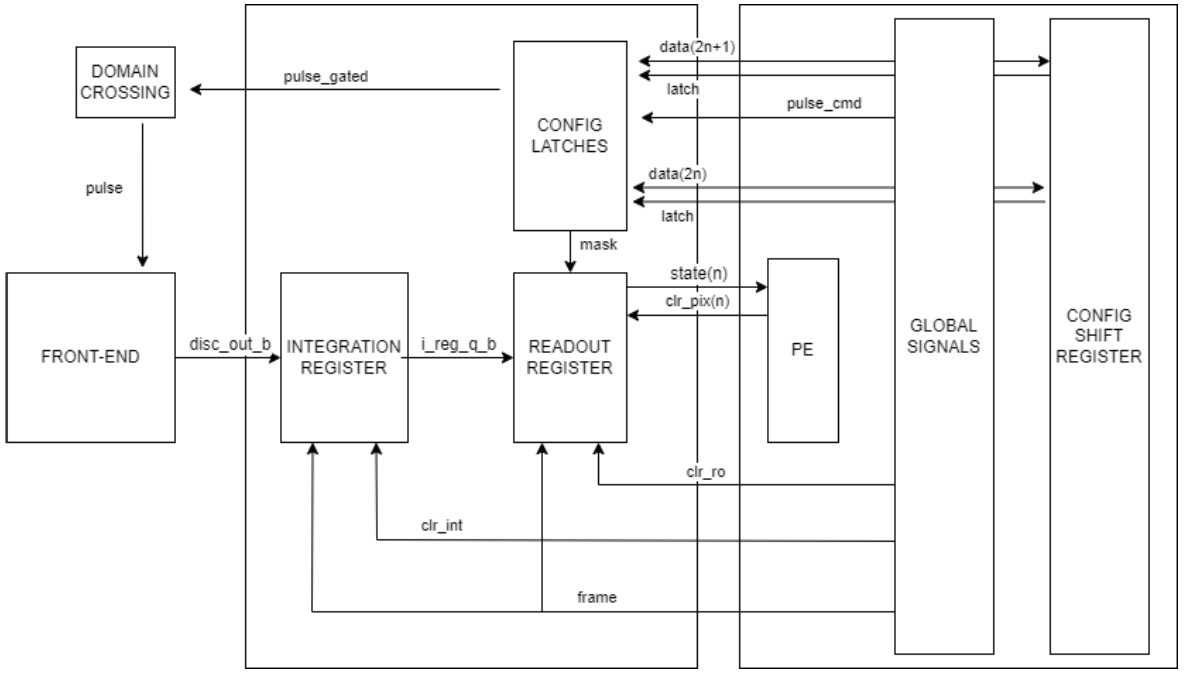
- Framing time base re-generated in each TILE periphery
  - FRAME local signal synchronizes pixels, Region Readout and Top Readout
  - Global SYNC input signal *aligns in time* the integration intervals across tiles
- Four parallel readout processes in each tile
  - Regions have 38 or 40 columns
  - Double columns in one region are sequentially read out
  - Region data packet is stored in FIFOs
  - Double columns and full regions can be masked
- Serial transmission of tile packet to LEC
  - Top readout aggregates region data packets for the same frame interval
  - Tile transmits one data packet for each frame interval, in order

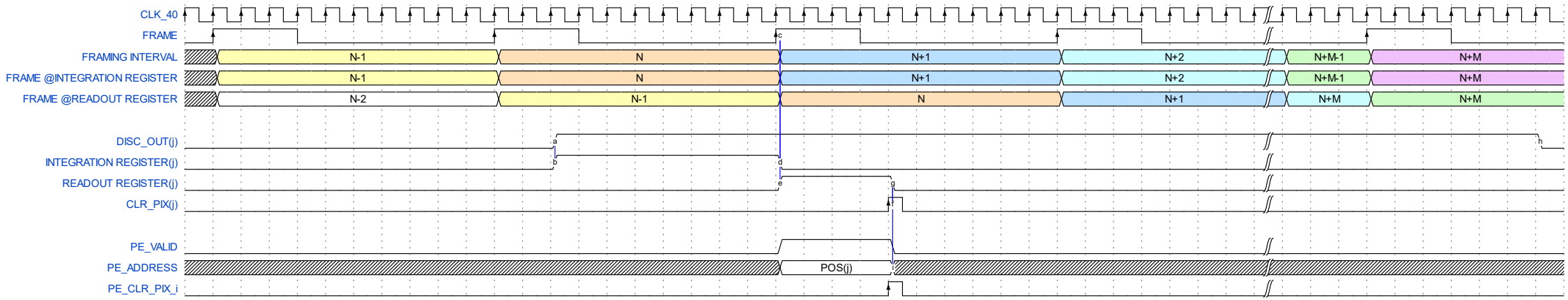


OAK RIDGE National Laboratory

Tile Data Output



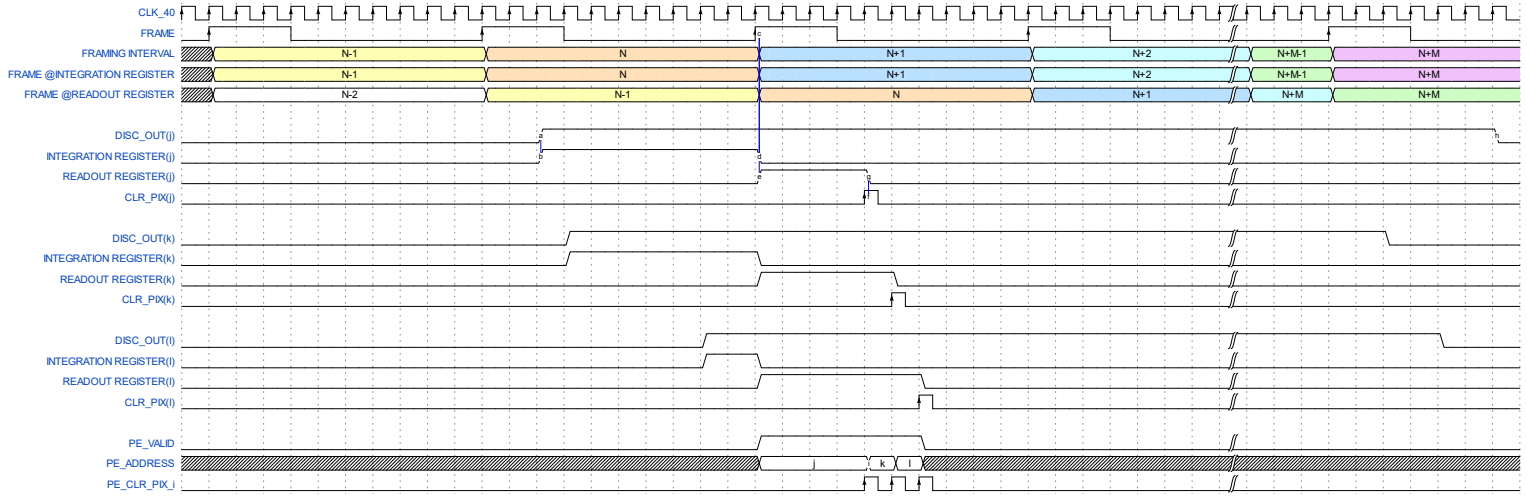




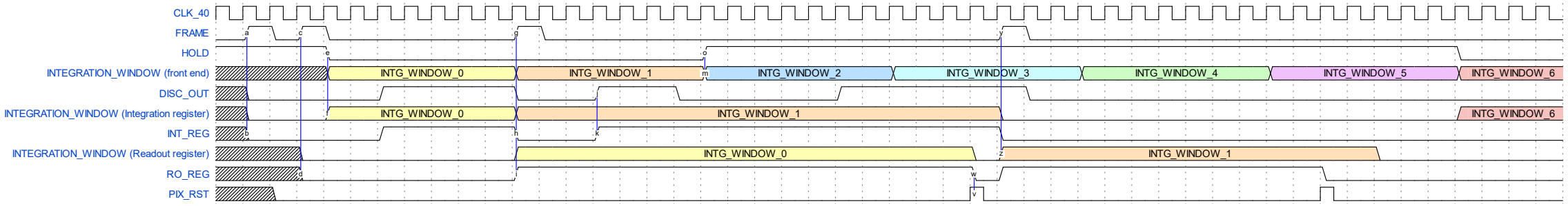
OAK RIDGE National Laboratory

Pixel Array Readout Waveforms

Hits from one collision can be recorded in consecutive frame packets (time walk and spread of FRAME signals)



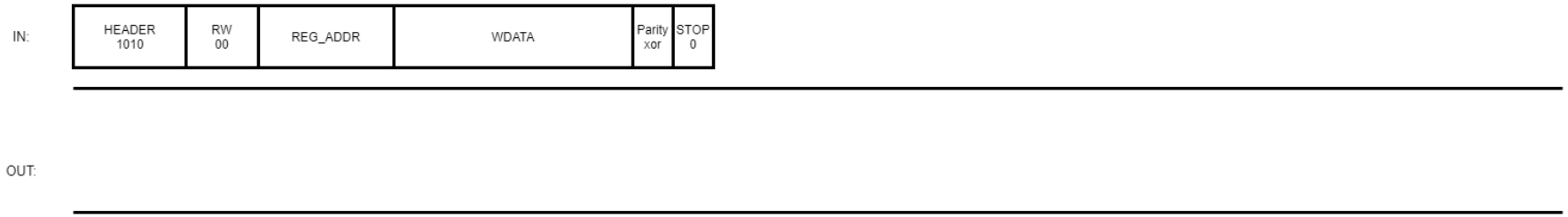
Region frame readout time can exceed the framing interval (from drop mode with priority to earliest frames)



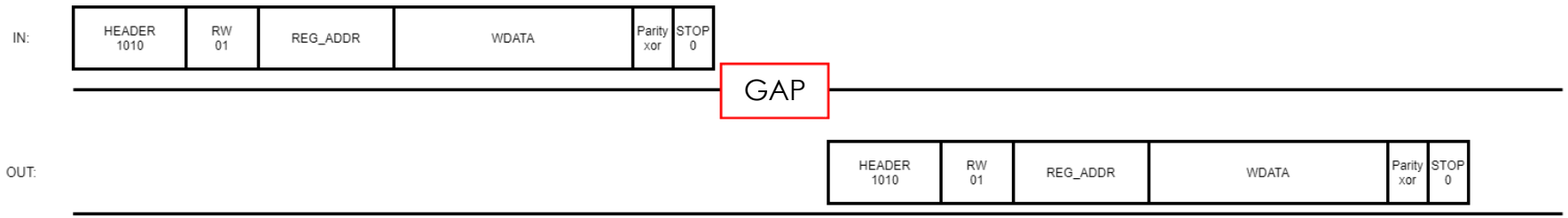
OAK RIDGE National Laboratory

Slow Control Transactions

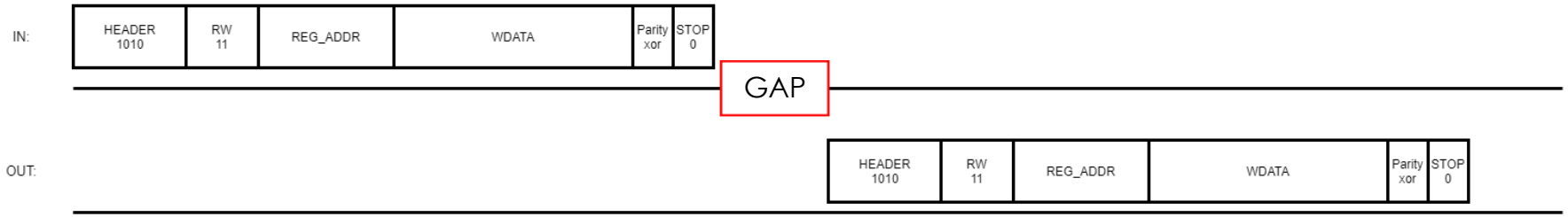
Posted Write Operation



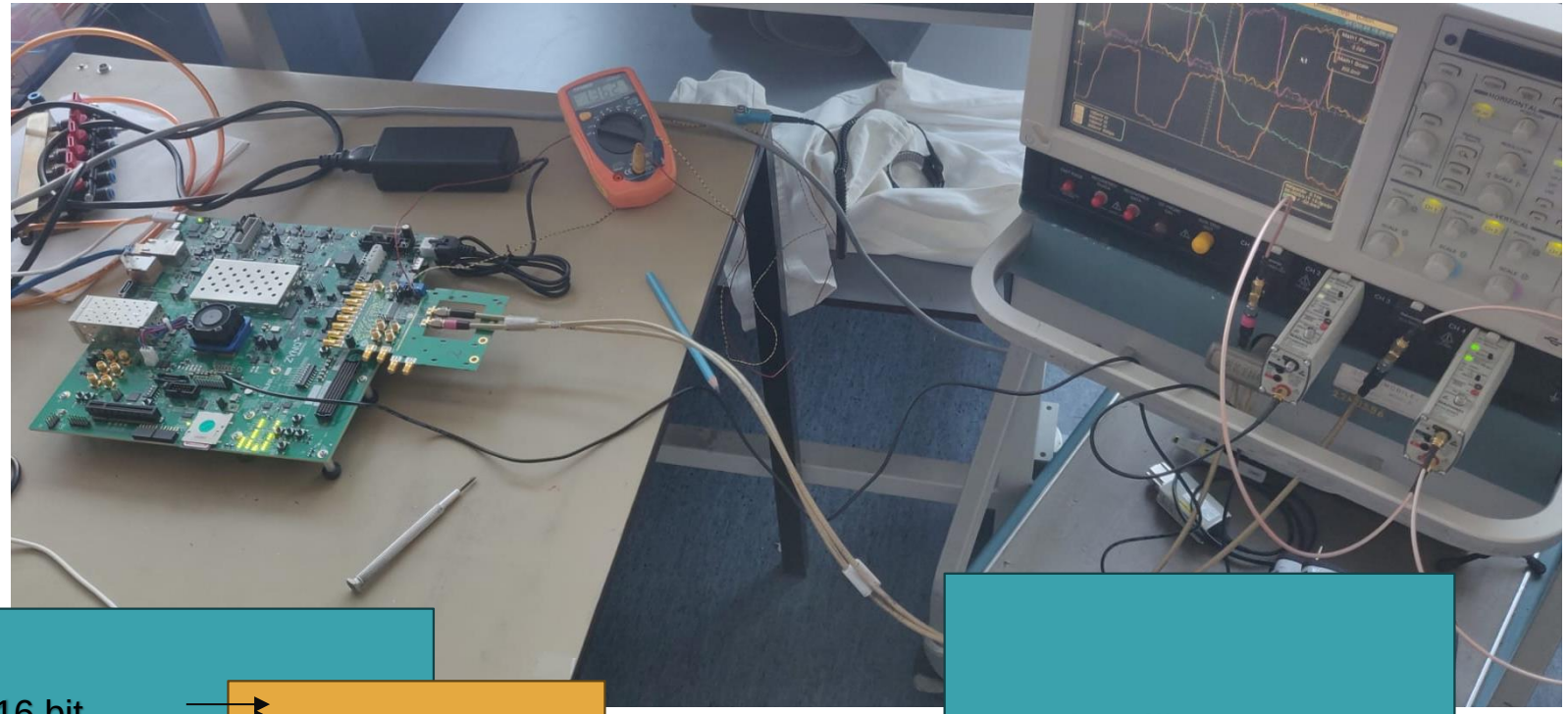
Non-Posted Write Operation

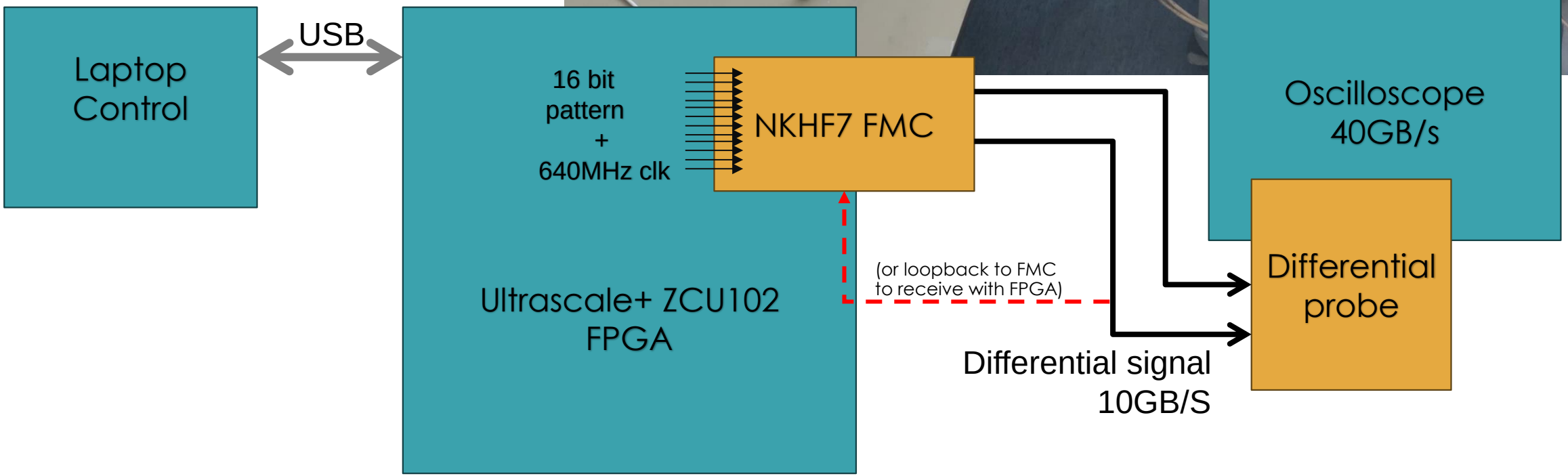


Read Operation



NKF7FMC Test Setup

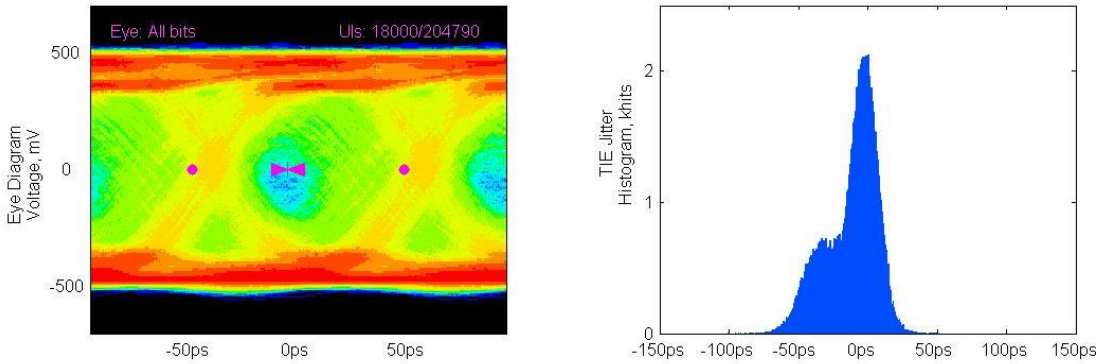




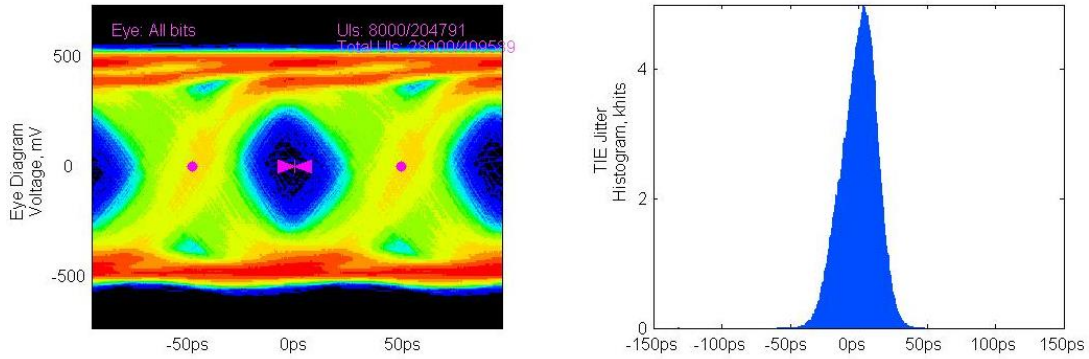
OAK RIDGE National Laboratory

Oscilloscope Eyes with PRBS @ 10 Gbps

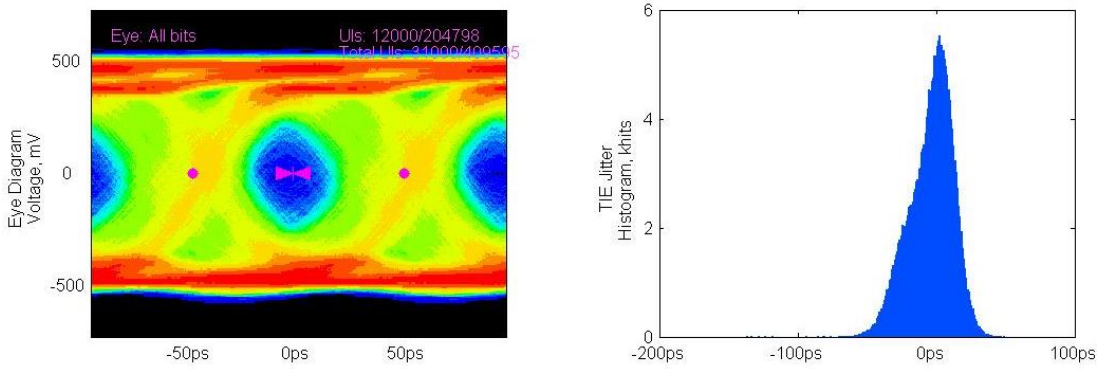
1.20 V



1.30 V



1.25 V



1.40 V