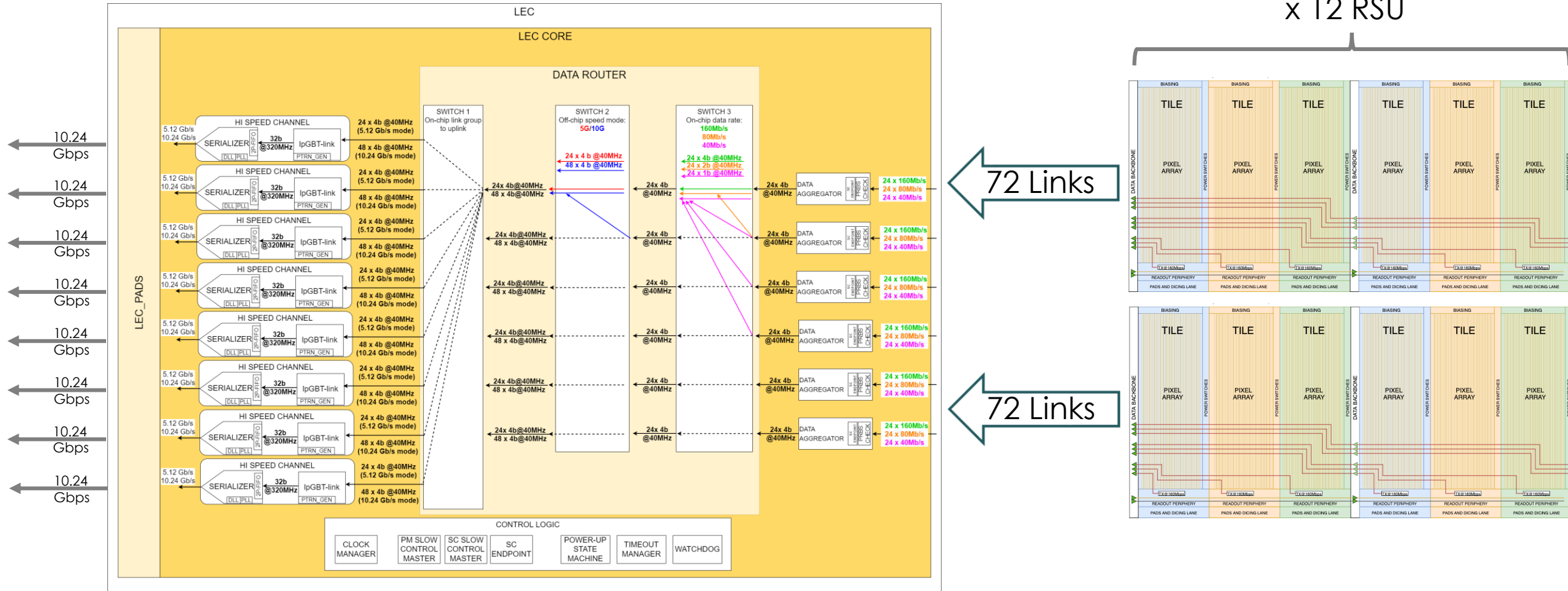


SVT Readout

J. Schambach

ORNL is managed by UT-Battelle LLC for the US Department of Energy

Data Flow – From Tiles to Left Endcap



12-RSU MOSAIX (SVT IB)

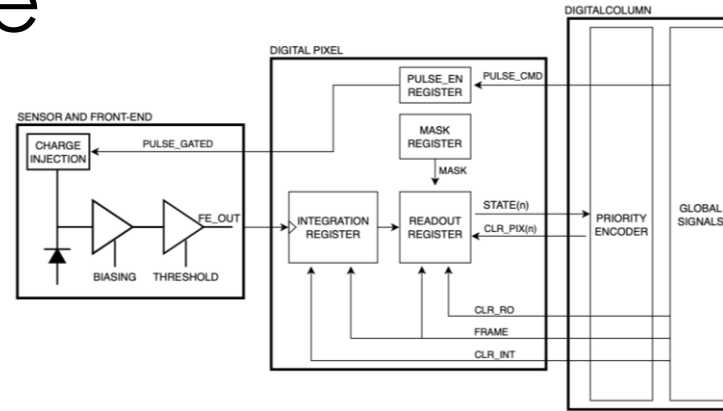
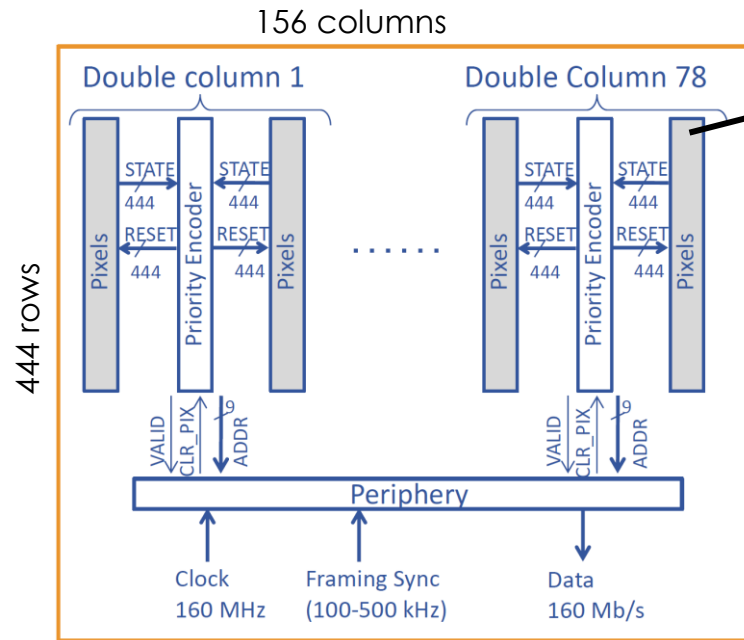
The data encoding block is the **IpGBT's TX core**
 160 Mbps x 144 = 22.5 Gbps
 Full capacity: 8 HS serializers = 80 Gbps (10 Gbps each, only 3 used)
 Fallback: 40 Gbps, 5 Gbps each (6 used)
 4 serializer data outputs drive one VTRx+

SVT Outer Barrel & Disks

6-RSU LAS
 72 Tiles
 1 HS serializer = 10 Gbps

5-RSU LAS
 60 Tiles
 1 HS serializer = 10 Gbps

Domain (Tile) Architecture



444 x 156 pixels / domain
 831 168 pixels per RSU
 144 domains / segment
 9.974 Mpixels / segment

In pixel:

- Amplification
- Discrimination
- Hit integration register and readout register
- Test charge injection
- Digital pulsing
- Masking

Digital pixel designed with low-leakage, high reliability std cells

- 20.8 μm x 22.8 μm** pixel pitch(*)
- Continuously active front-end (40 nW typ.)
- Global shutter
- Zero-suppressed matrix readout
- Continuous readout mode
- Integration time: 2 μs to 2¹⁶*25ns = 1.6384ms

(*) **Baseline: 20.8 μm * 22.8 μm**
 Abs. Max: 22.5 μm * 25 μm

On-chip Readout Scheme in the Periphery

Framing time base re-generated in each TILE periphery

FRAME local signal synchronizes pixels, Region Readout and Top Readout

Global SYNC input signal *aligns in time* the integration intervals across tiles

Four parallel readout processes in each tile

Regions have 38 or 40 columns

Double columns in one region are sequentially read out

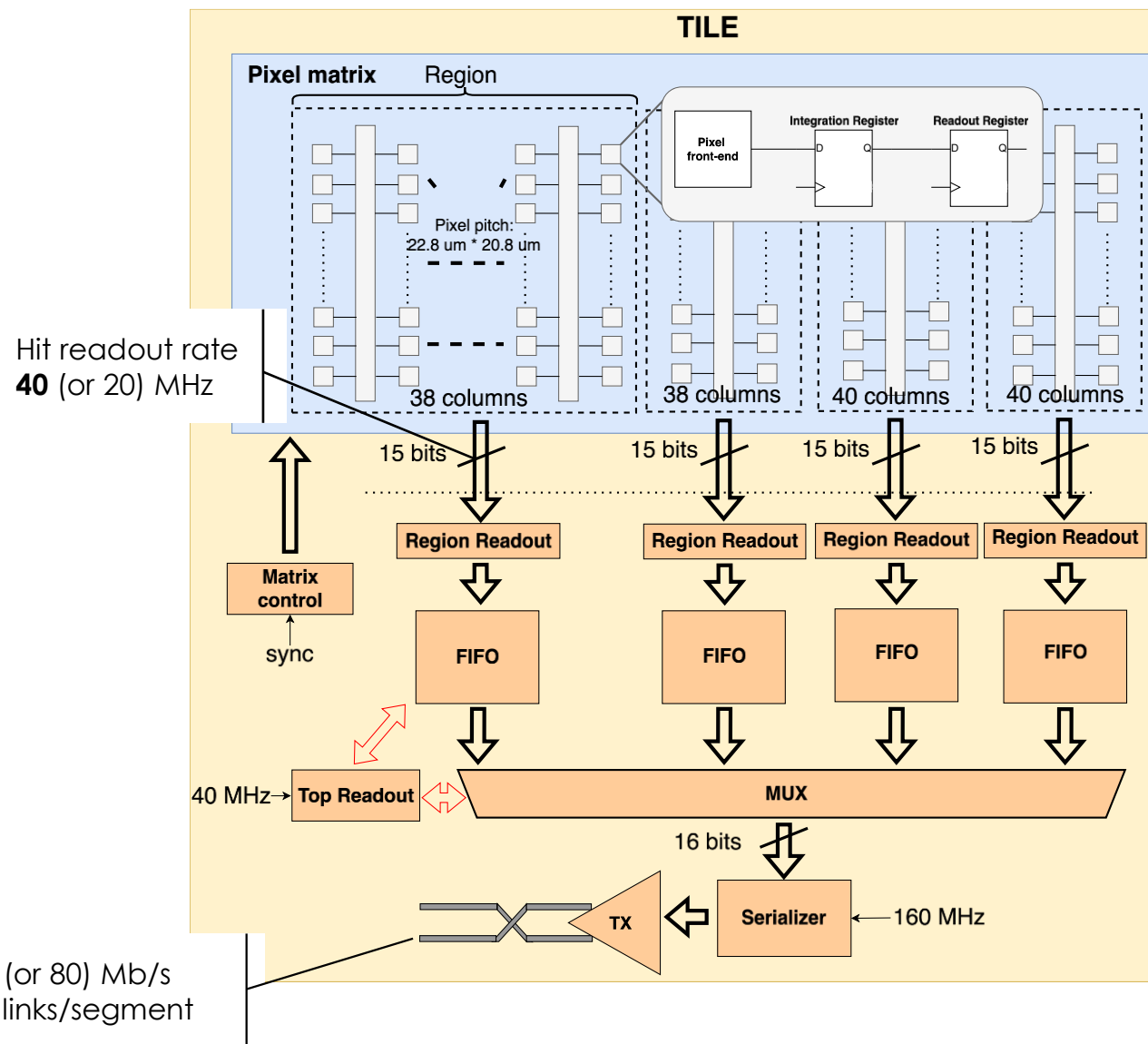
Region data packet is stored in FIFOs

Double columns and full regions can be masked

Serial transmission of tile packet to LEC

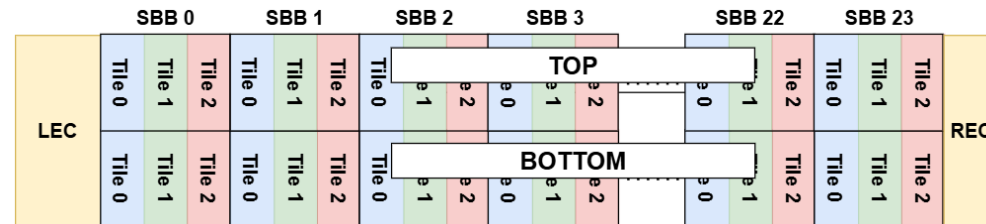
Top readout aggregates region data packets for the same frame interval

Tile transmits one data packet for each frame interval, in order

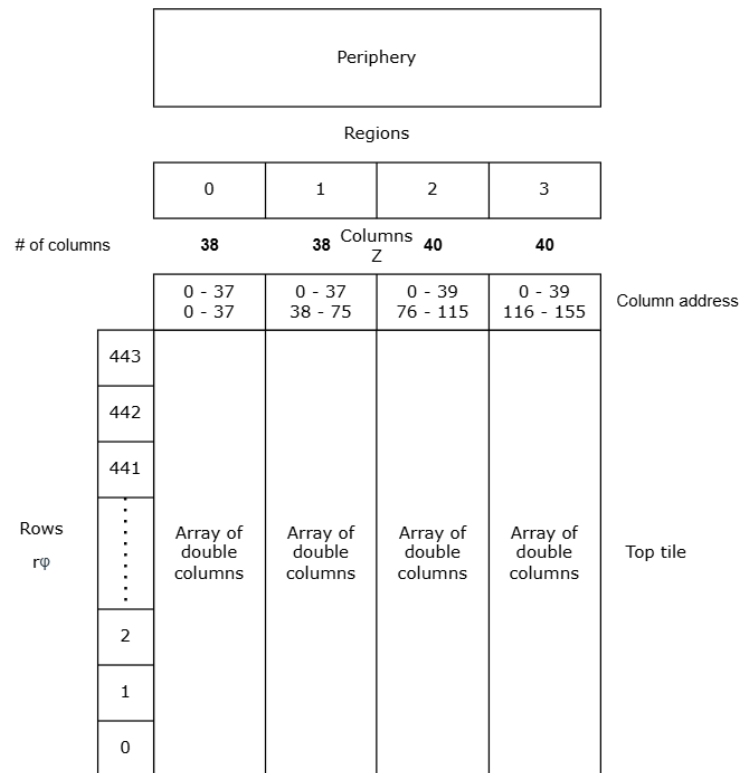


Addressing

- Stitched Back Bone (SBB) -> 5 bits for SBB, 2 bits for tile in SBB, 1 bit for Top/Bottom

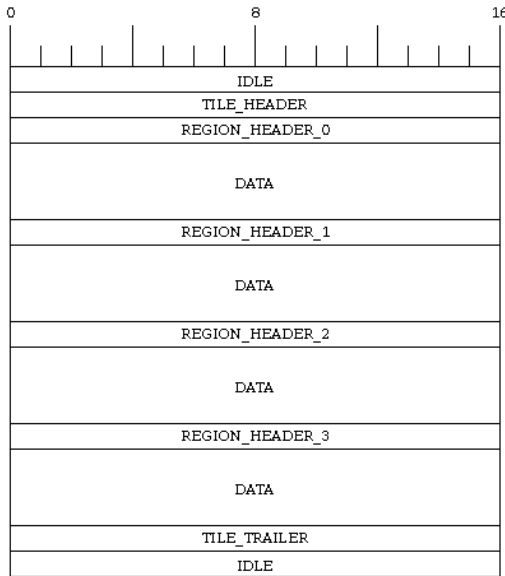


- Pixel row: 0 -443 -> 9 bits
- Pixel columns per region 38 or 40 ->6 bits
- 4 regions -> 2 bits

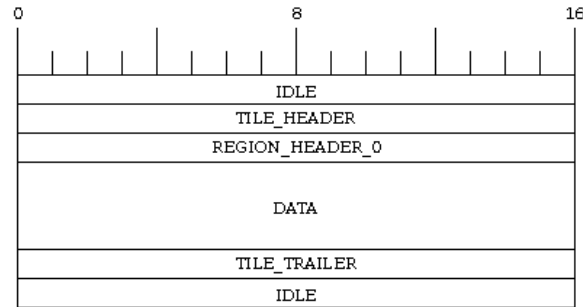


Tile Readout Protocol

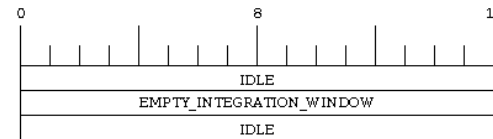
Hits in all 4 regions



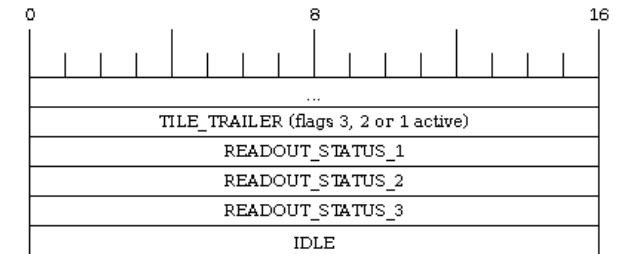
Hits in 1 region



No hits

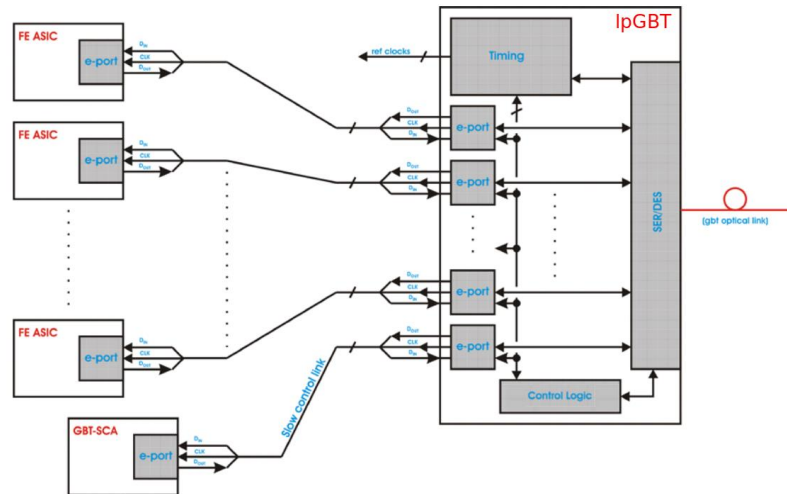


Status

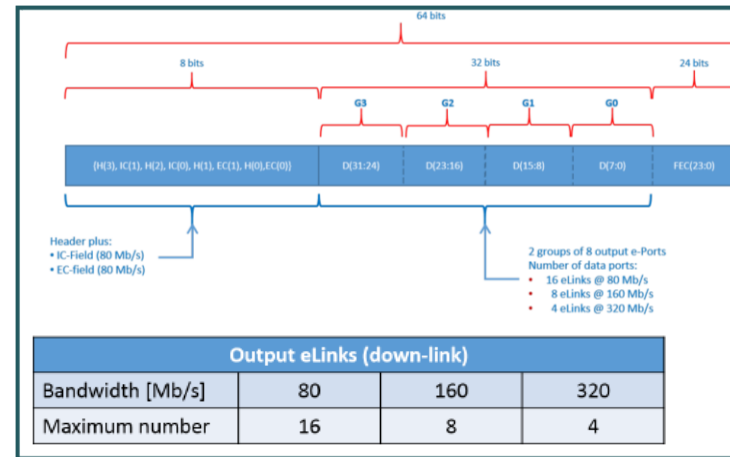


READOUT PROTOCOL																
Word type	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDLE	1	1	0	0	0	1	0	1	IDLE config [7:0]							
LOCK	1	1	0	0	1	0	1	0	IDLE config [7:0]							
READOUT_STATUS_1	1	0	0	1	1	1	0	0	Integration Window Counter [15:8]							
READOUT_STATUS_2	1	1	1	1	IWC Checksum [3:0]			Integration Window Counter [7:0]								
TILE_HEADER	1	0	1	0	0	0	0	0	Unit Slice [4:0]			Tile [1:0]		T/B		
REGION_HEADER	1	0	1	0	1	1	Region Address.		Integration Window Counter [7:0]							
DATA	0	Pixel Address Row [8:0]							Pixel Address Column [5:0]							
TILE_TRAILER	1	0	1	1	TRU Status Flags [3:0]			Packet Checksum [7:0]								
EMPTY_INTEGRATION_WINDOW	1	1	1	0	TRU Status Flags [3:0]			Integration Window Counter [7:0]								
DROPPED_INTEGRATION_WINDOW	1	1	0	1	TRU Status Flags [3:0]			Integration Window Counter [7:0]								
RECOVERY	1	0	0	1	0	0	1	1	'0							
RESERVED	1	0	0	0	RESERVED											

IpGBT Protocol



- Front Ends connect to “e-links”
- The fiber protocol includes “Forward Error Correction”
- Downlink runs at 2.56 Gbps
 - Downlink frame is 64bit wide, of which 32 bits are payload
 - 1.28 Gbps payload
 - Up to 16 e-links @ 80 Mbps
- Uplink runs at either 10.24 Gbps or 5.12 Gbps
 - Uplink frame is either 128bit or 256bit
 - 256bit frame contains 192bits of payload (7.68 Gbps)
 - Up to 24 e-links at either 160 Mbps or 320 Gbps



Downlink
 Line Rate: **2.56 Gbps**
 32 out of 64 bits are data:
 Payload = **1.280 Gbps**

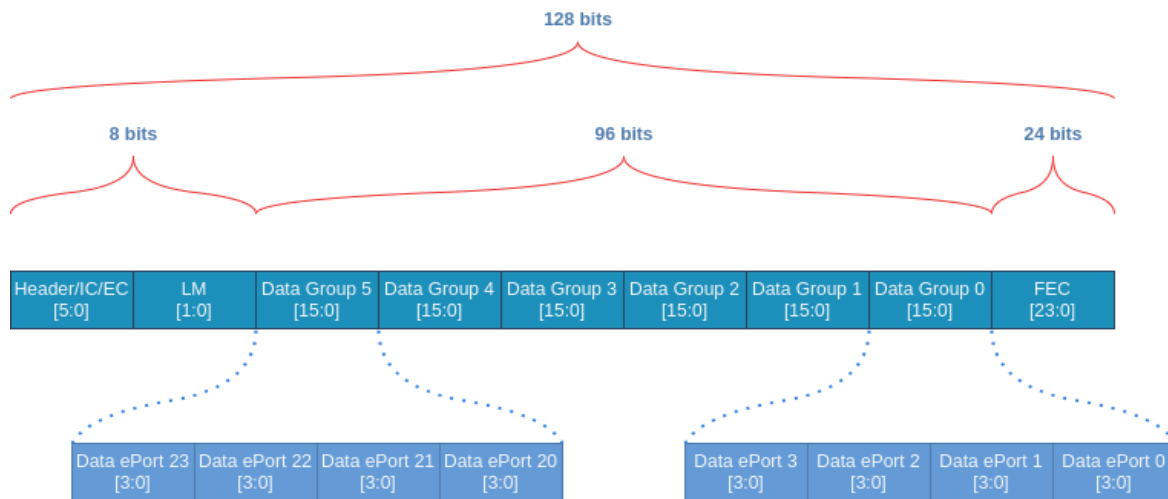
Data Uplink
 192 out of 256 bits are data:
 Payload = **7.680 Gbps**

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

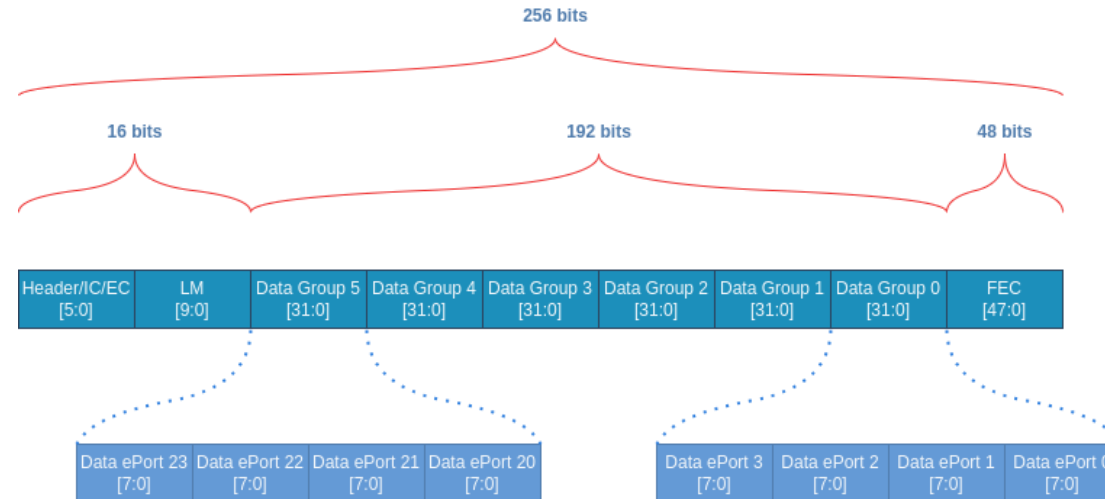
Field	5.12 Gbps		10.24 Gbps	
	FEC5	FEC12	FEC5	FEC12
Frame [bits]		128		256
Header [bits]		2		2
IC [bits]		2		2
EC [bits]		2		2
D [bits]	112	96	224	192
FEC [bits]	10	24	20	48
LM [bits]	0	2	6	10
Correction [bits]	5	12	10	24
# of eLink groups	7	6	7	6

IpGBT ePort Routing

5.12Gbps



10.24Gbps



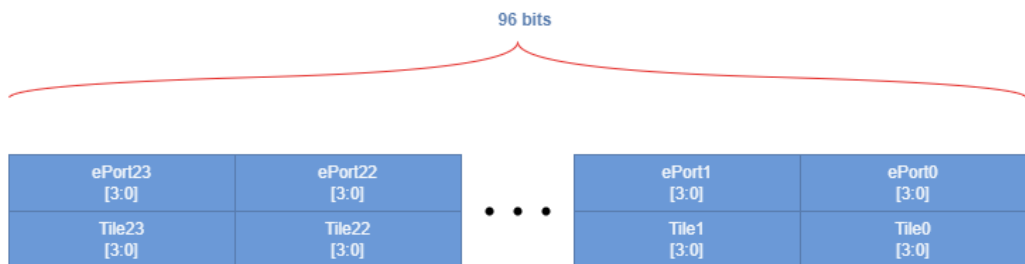
MOSAIX uplink						
Uplink bandwidth (Gbps)	5.12			10.24		
FEC Coding	FEC12			FEC12		
Tile bandwidth (Mbps)	40	80	160	40	80	160
Tiles per uplink ¹	48	48	24	48	48	48
Bits per tile	1	2	4	1	2	4
Tiles per ePort	2	2	1	2	2	2
Bits per ePort	4	4	4	8	8	8
Used bits per ePort	2	4	4	2	4	8
Bandwidth efficiency	50%	100%	100%	25%	50%	100%

1. To simplify routing scheme, 48 tiles are connected in instances where there are bandwidth enough to support a higher number of tiles.

LEC Data Routing

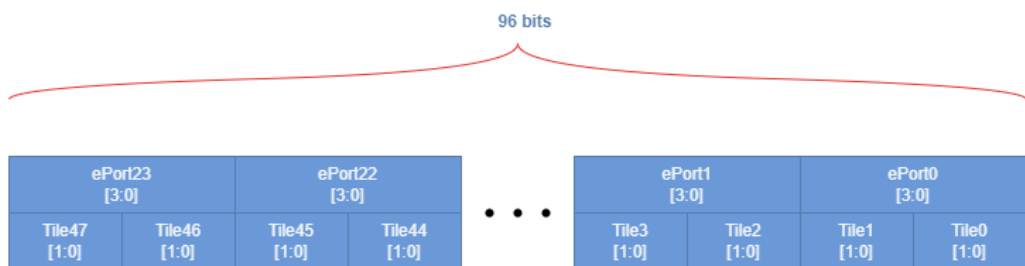
5 Gbps / 160 MHz

(6 links)



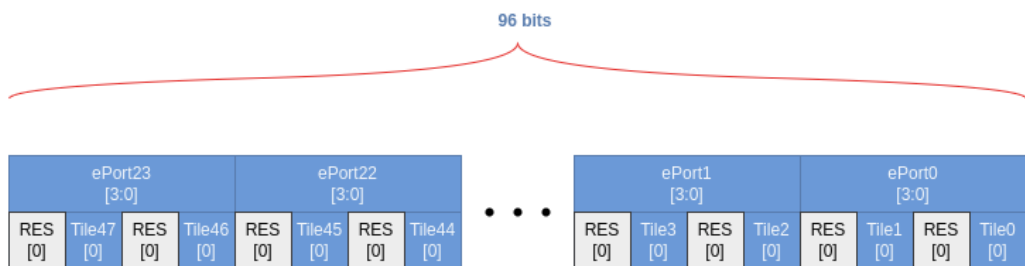
5 Gbps / 80 MHz

4 frames to reconstruct file word



5 Gbps / 40 MHz

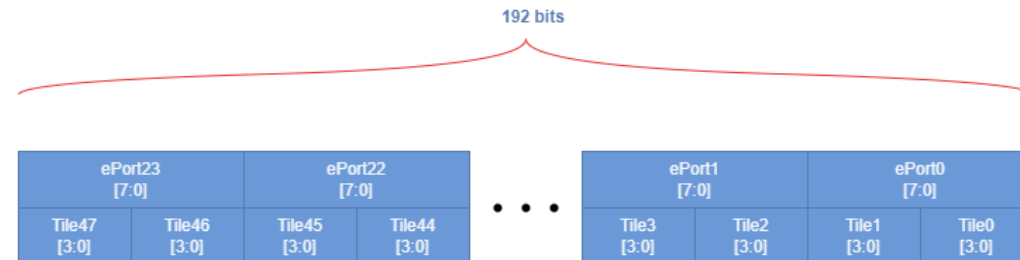
8 frames to reconstruct file word



16 frames to reconstruct file word

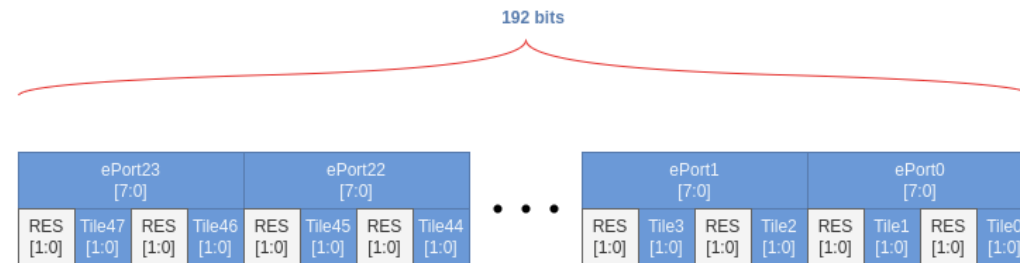
10 Gbps / 160 MHz

(3 links)



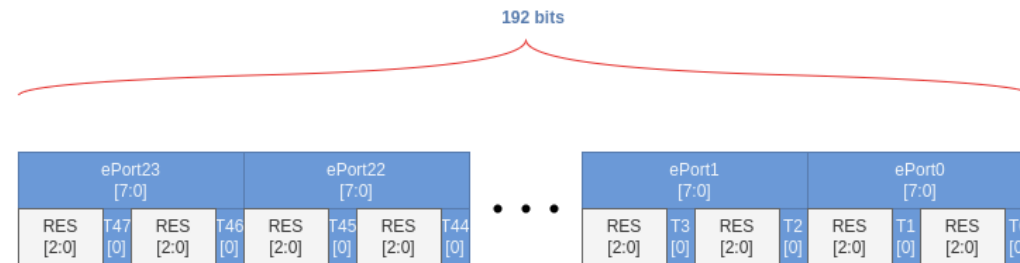
10 Gbps / 80 MHz

4 frames to reconstruct file word



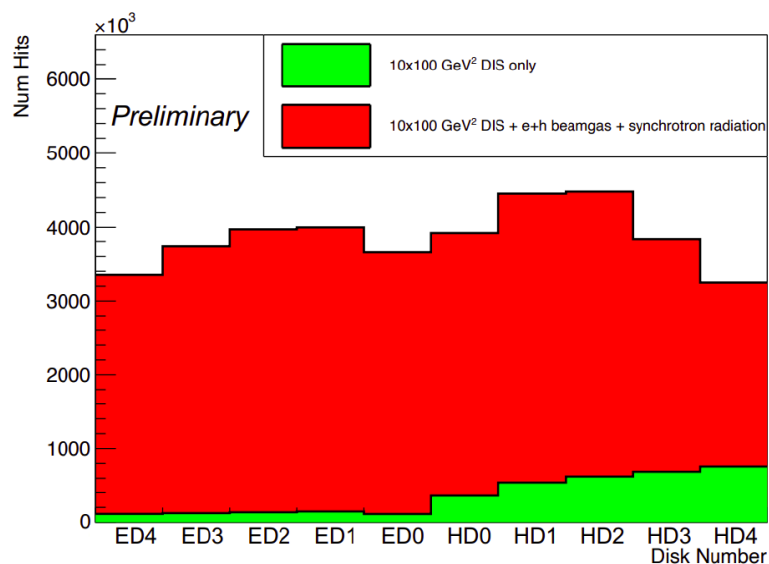
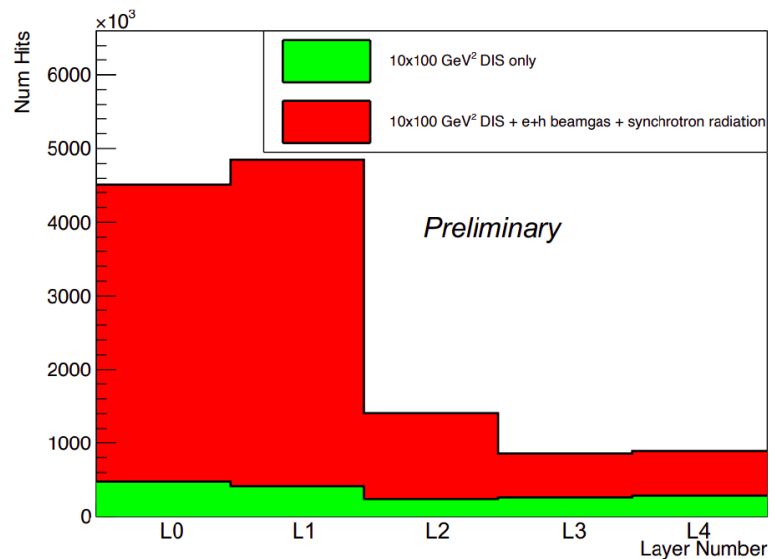
10 Gbps / 40 MHz

8 frames to reconstruct file word



16 frames to reconstruct file word

S. Maple's Presentation: SVT Hit Rates



- 10x100 GeV ep, $4.48 \times 10^{33} \text{ cm}^{-2}\text{s}^{-1}$, 184 kHz DIS event rate
- 10 GeV SR
- 10 GeV e beam gas, 10000 Ahr
- 100 GeV proton beam gas, 100 Ahr

10x275 GeV:
 (Factor 2 in luminosity?)
 Factor 3 in e-p rate

	Hit Rate (Hz)	Area (cm ²)	Hits/s/cm ²
L0	4.50E+06	610.73	7.37E+03
L1	4.85E+06	814.30	5.96E+03
L2	1.41E+06	2035.75	6.93E+02
L3	8.55E+05	9160.88	9.33E+01
L4	8.89E+05	22167.08	4.01E+01

	Hit Rate (Hz)	Area (cm ²)	Hits/s/cm ²
ED0	3.66E+06	1767.11	2.07E+02
ED1	4.00E+06	5368.16	7.45E+02
ED2	3.97E+06	5536.32	7.17E+02
ED3	3.74E+06	5532.26	6.76E+02
ED4	3.35E+06	5524.62	6.06E+02

	Hit Rate (Hz)	Area (cm ²)	Hits/s/cm ²
HD0	3.92E+06	1767.11	2.22E+03
HD1	4.45E+06	5368.16	8.29E+02
HD2	4.48E+06	5533.75	8.10E+02
HD3	3.83E+06	5513.51	6.95E+02
HD4	3.25E+06	5486.76	5.92E+02

Operational environment



- EIC bunch crossing frequency 98.5 MHz
 - Interaction frequency orders of magnitude lower

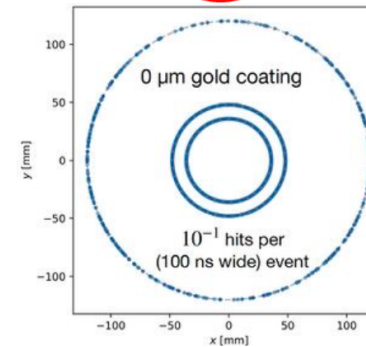
- Rates for DIS ep events up to 500 kHz

Beam energy [GeV]	5 x 41	5 x 100	10 x 100	10 x 275	18 x 275
L [$10^{33}\text{cm}^{-2}\text{s}^{-1}$]	0.44	3.68	4.48	10	1.54
DIS ep rate [kHz]	12.5	129	184	500	83

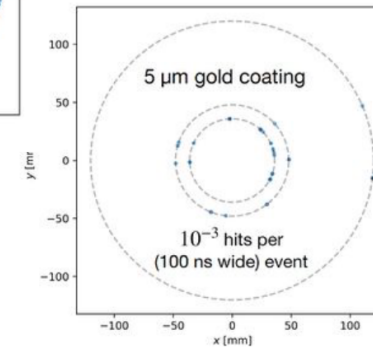
[EIC Conceptual Design Report, Table 3.3](#)

- Up to O(MHz) rate for background events
 - Hadron and electron beam gas event rate lowers with improving vacuum condition
 - Synchrotron radiation reduced of two orders of magnitude with $5\ \mu\text{m}$ gold coating of the beam pipe

- Manageable readout frame rate



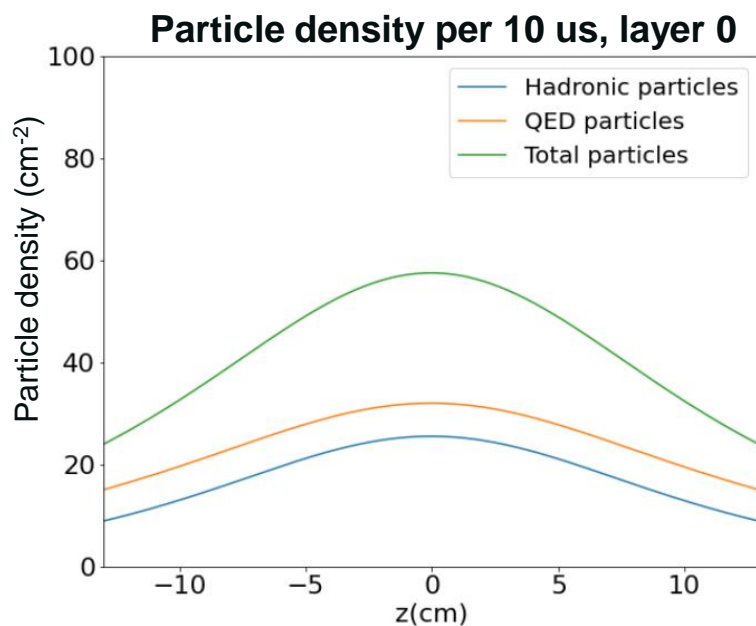
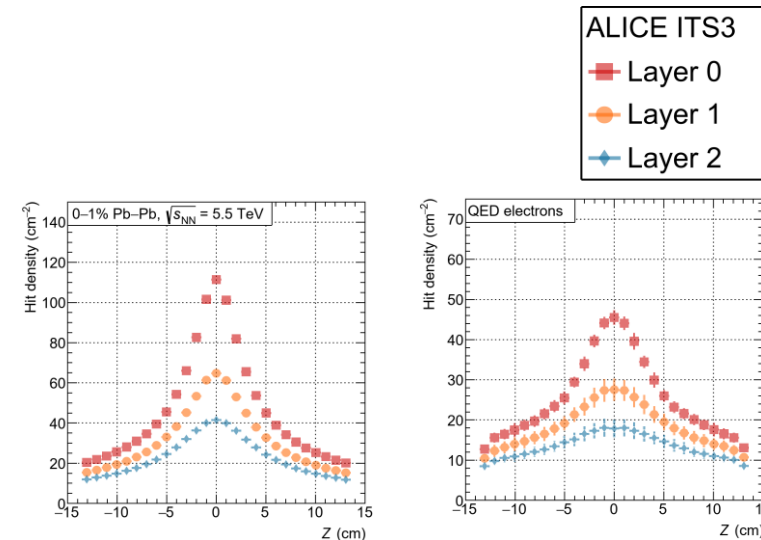
Scatter plot of SR hits in the innermost silicon tracker layers



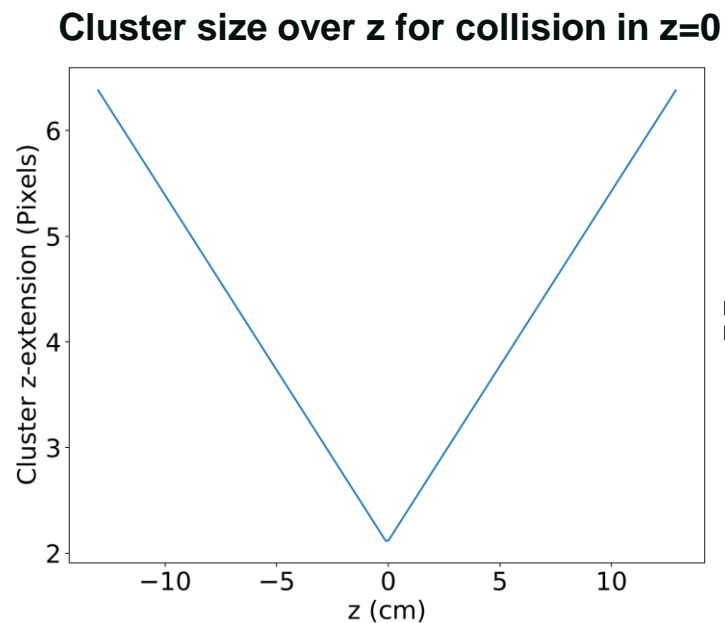
ITS3 simulation for central PbPb

- Collisions and QED distributed along vertex (z) by gaussian of RMS = 6cm.
- Particle flux from collisions in z=0, layer 0 of **2.95 MHz/cm²**
- Particle flux from QED in z=0, layer 0 of **3.55 MHz/cm²**
- Occupancy in 2 μ s period of **2 \times 10⁻⁴**

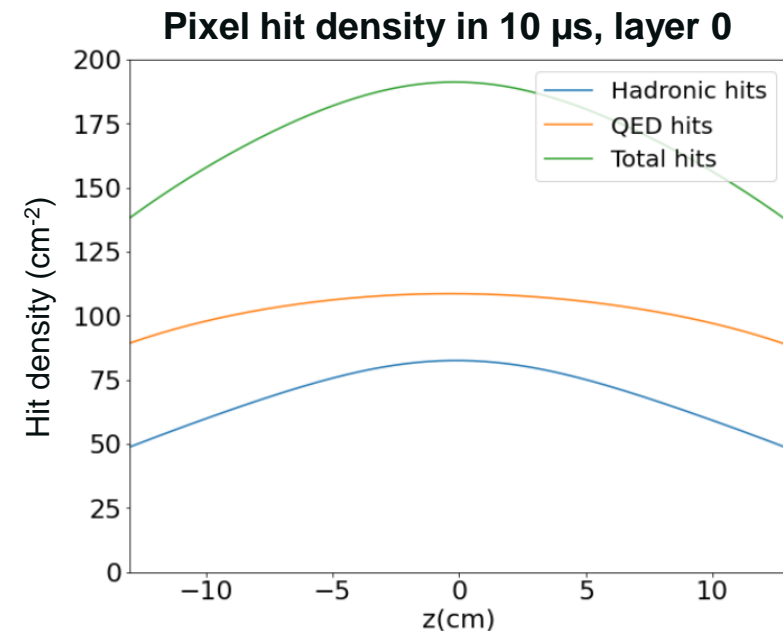
2 – 6 pixels per hit (“cluster”)



X



=



Bit Counts

1 tile noise pixel:

- 1 tile header
- 1 region header
- 1 data
- 1 tile trailer

4 words

-> **64 bits per pixel**

1 tile hit (4 pixels):

- 1 tile header
- 1 region header
- 4 data
- 1 tile trailer

7 words

-> **112 bits**

-> **28 bits per pixel**

1 hit (4 pixels) per region:

- 1 tile header
- 1 region header
- 4 data
- 1 region header
- 4 data
- 1 region header
- 4 data
- 1 region header
- 4 data
- 1 tile trailer

22 words

-> **352 bits**

-> **22 bits per pixel**

2 hits (4 pixels) in 1 region:

- 1 tile header
- 1 region header
- 8 data
- 1 tile trailer

11 words

-> **176 bits**

-> **22 bits per pixel**

4 hits (4 pixels) in 1 region:

- 1 tile header
- 1 region header
- 16 data
- 1 tile trailer

19 words

-> **304 bits**

-> **19 bits per pixel**

