

FTOF Module assembly procedure and requirements

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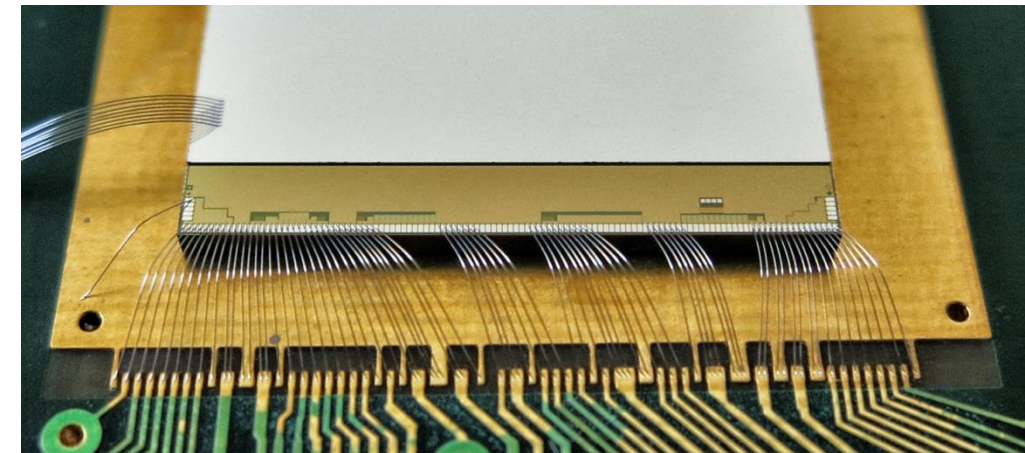
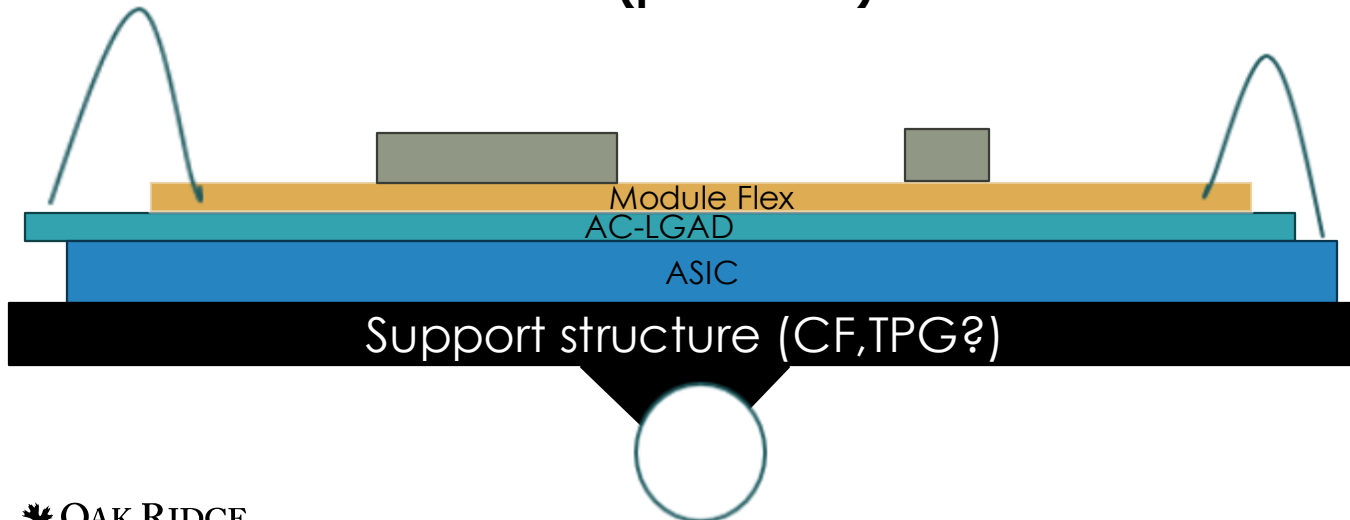
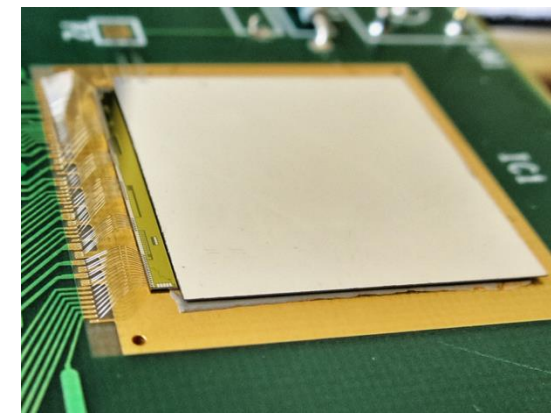
Outline

- Module design and consideration
- Bump-Bonding
- Module assembly procedure
 - Gantry-based assembly scheme
 - Jig-based assembly scheme
- Towards first Thermo-mechanical prototypes
- Module QA/QC

Module design and consideration

Module consist of :

- Thin AC-LGAD (20-50 μm) + support material bonded to thick ASIC (200-300 μm preferable)
 - Thick ASIC, if allowed by material budget, allow for more rigidity
- Module flex hybrid populated with HV decoupling, connectors and other needed components
 - HV-Capacitor should be potted to avoid sparks
 - Flexible circuit is preferred for material budget but also for the flexibility limiting possible stress on the thin sensor
 - ASIC and sensor backside are wire-bonded to flex circuit (encapsulated)
 - **Sensor DC Node (pixel side) should be connected to ASIC (?)**



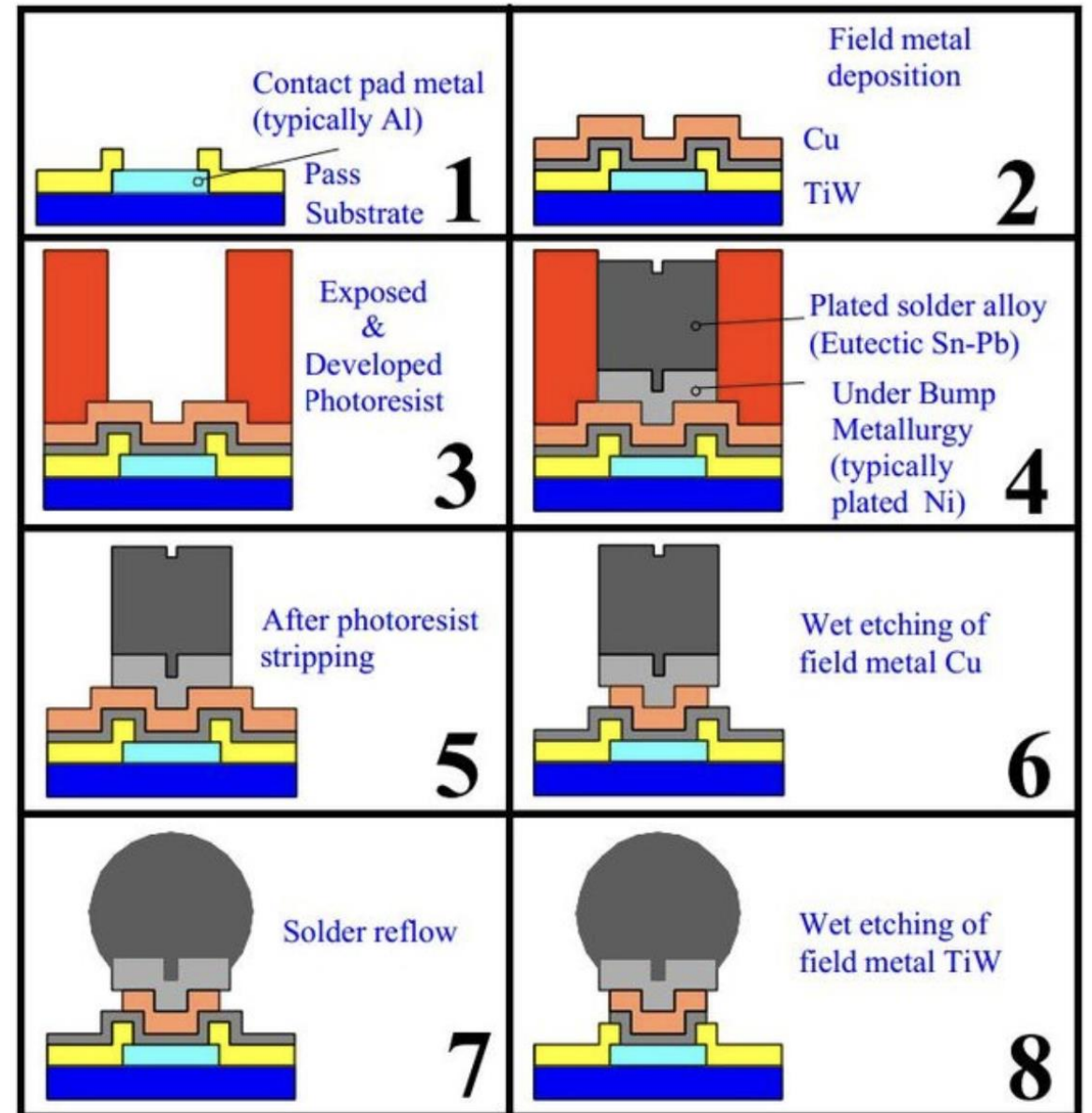
Module assembly procedure

- Module assembly consist of:
 - Alignment of Assembly to glue dispenser coordinates
 - Dispensing of glue pattern (stamping, motorized dispenser)
 - Alignment of Flex circuit to Assembly
 - Mating of Flex to Assembly
 - Curing (UV/heat/time)
 - Wire-bonding of signals
 - QA/QC testing of module
 - Mounting to mechanical/thermal support
- Produced modules in **design and pre-production phase should be tested for failure modes under stress**
 - Delamination, fracture of thin sensor, chipping, wire-bond integrity
 - Thermal cycling (accelerated aging) and thermal shock should be carried to ensure reliability of the assembly method

Bonding of sensor and ASIC



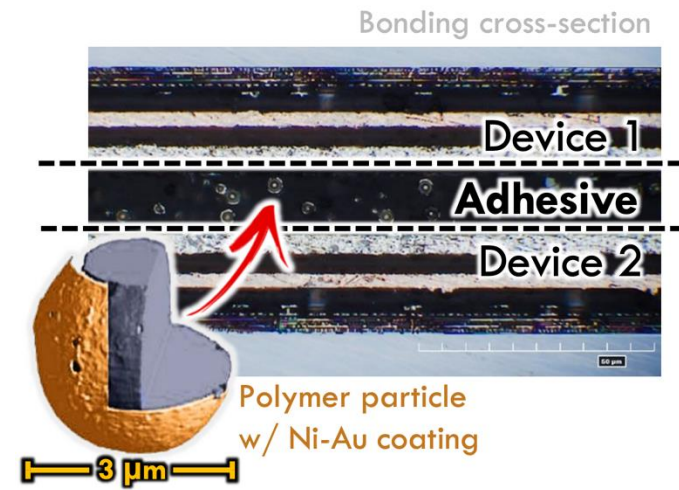
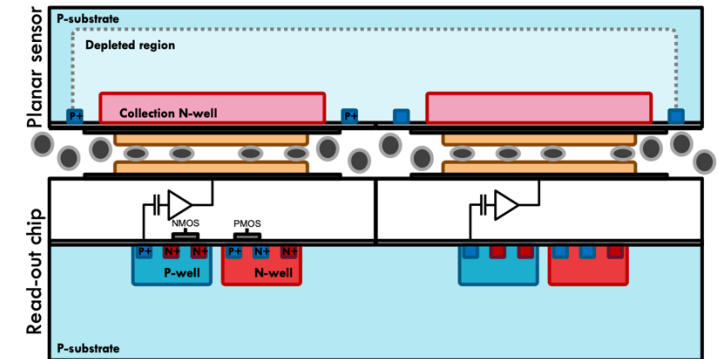
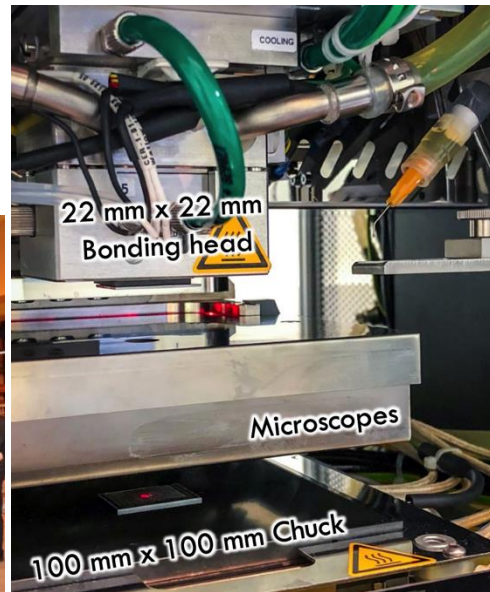
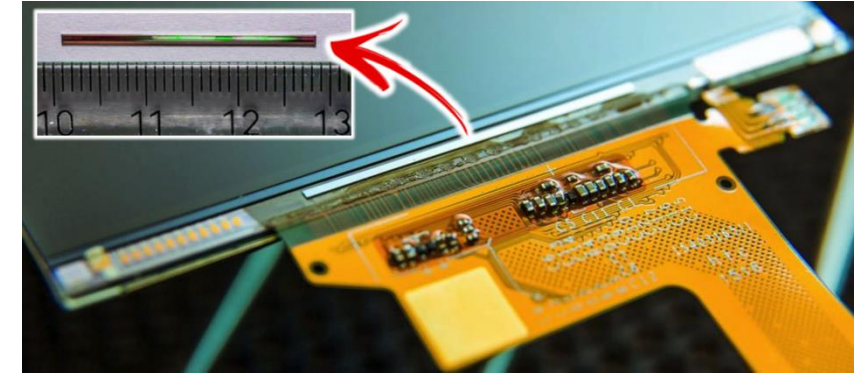
Bump-bonding (Solder Reflow)



Anisotropic Conductive Films (ACF)

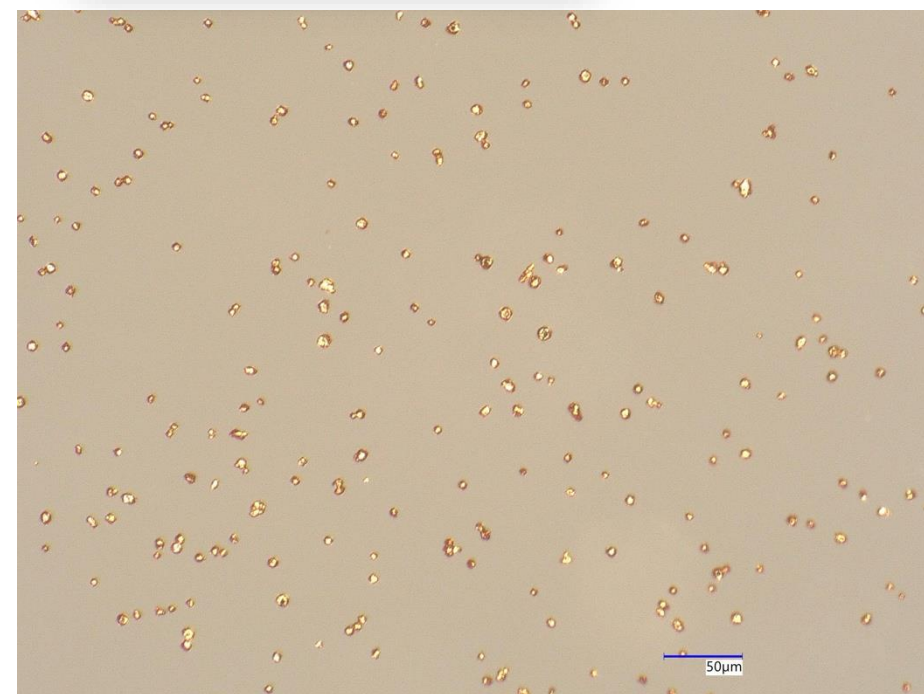
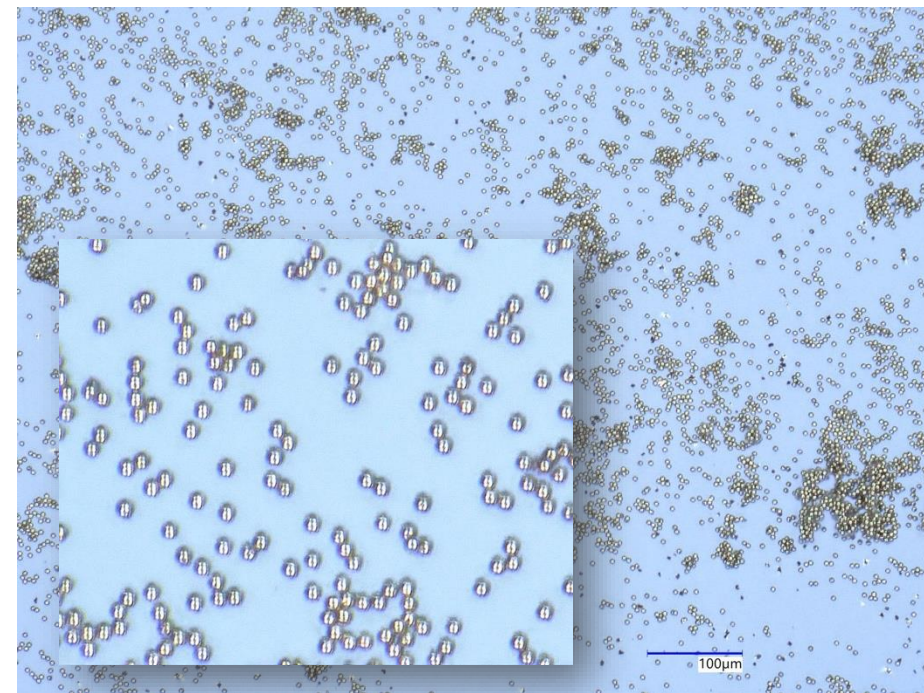
ACF is a technology developed for the LCD Display industry to connect drivers to each pixel row. Next step in the industry is μ LED, which are driven individually and can measure as little as $15 \times 15 \mu\text{m}^2$. Medipix and CLIC have been working with industry partners to adapt this process to pixel sensors

- Low cost, no lithography involved
- Wafer processing for pillar (ENIG) can be done in house with modest equipment



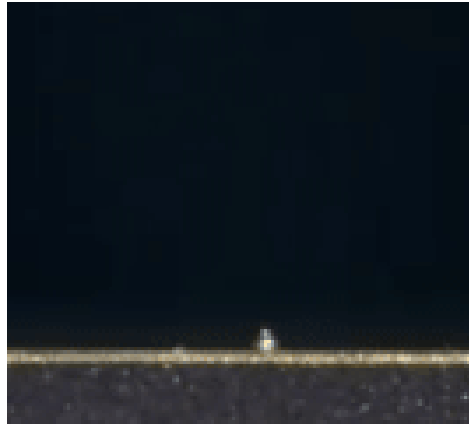
ACP Fabrication at ORNL

- We have started using ACP from various manufacturer to evaluate achievable pitch and reliability, handling, throughput etc.
- A much cheaper and efficient solution is to mix and fabricate our own ACP from particles from various vendors
- We can select the most appropriate matrix glue for our application, for example for radiation hardness
- Give access to more glues that have short lifetime for example



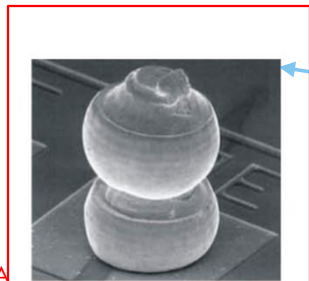
Gold-stud hybridisation of ALTIROC3/A and LGAD sensors

- Using ALTIROC3/A ASICs and LGAD sensors from ATLAS High-Granularity Timing Detector (HGTD) to develop new in-house bonding process for sensor and ASIC qualification
- Single and stacked double gold studs used for the connections between the chips, epoxy underfill for bonding
- Used for radiation-hardness qualification of LGAD sensors
- Low temperature process (60°C) to avoid uncontrolled annealing

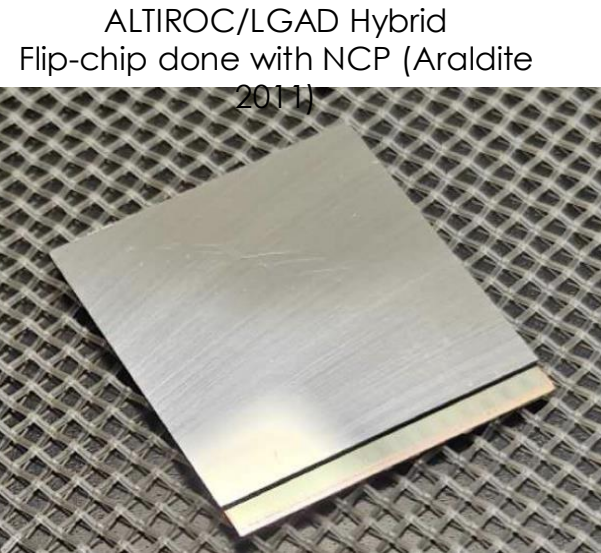


Gold studs are deposited one by one

https://www.youtube.com/watch?v=C8D8jmeo&t=42s&ab_channel=IPT-Wirebonder
 Stacked Gold studs
 Gold stud

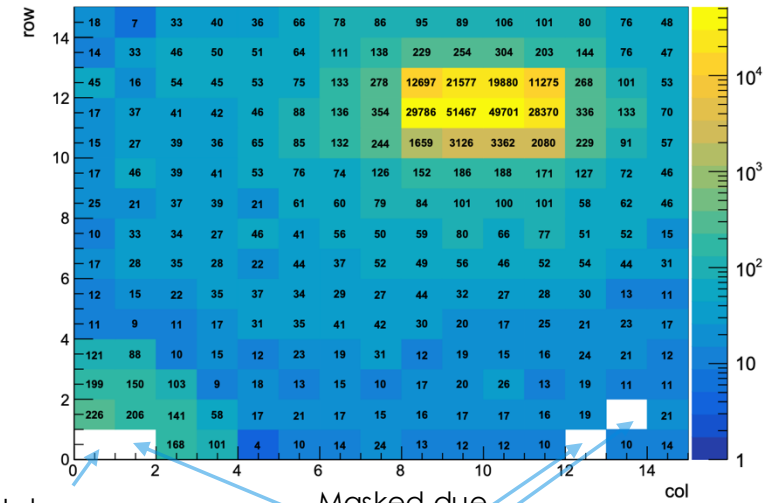


Preferred this solution to increase the gap between ASIC and sensor from 20 μm to 35 μm and thereby decrease coupling between them



ALTIROC/LGAD Hybrid Flip-chip done with NCP (Araldite 2011)

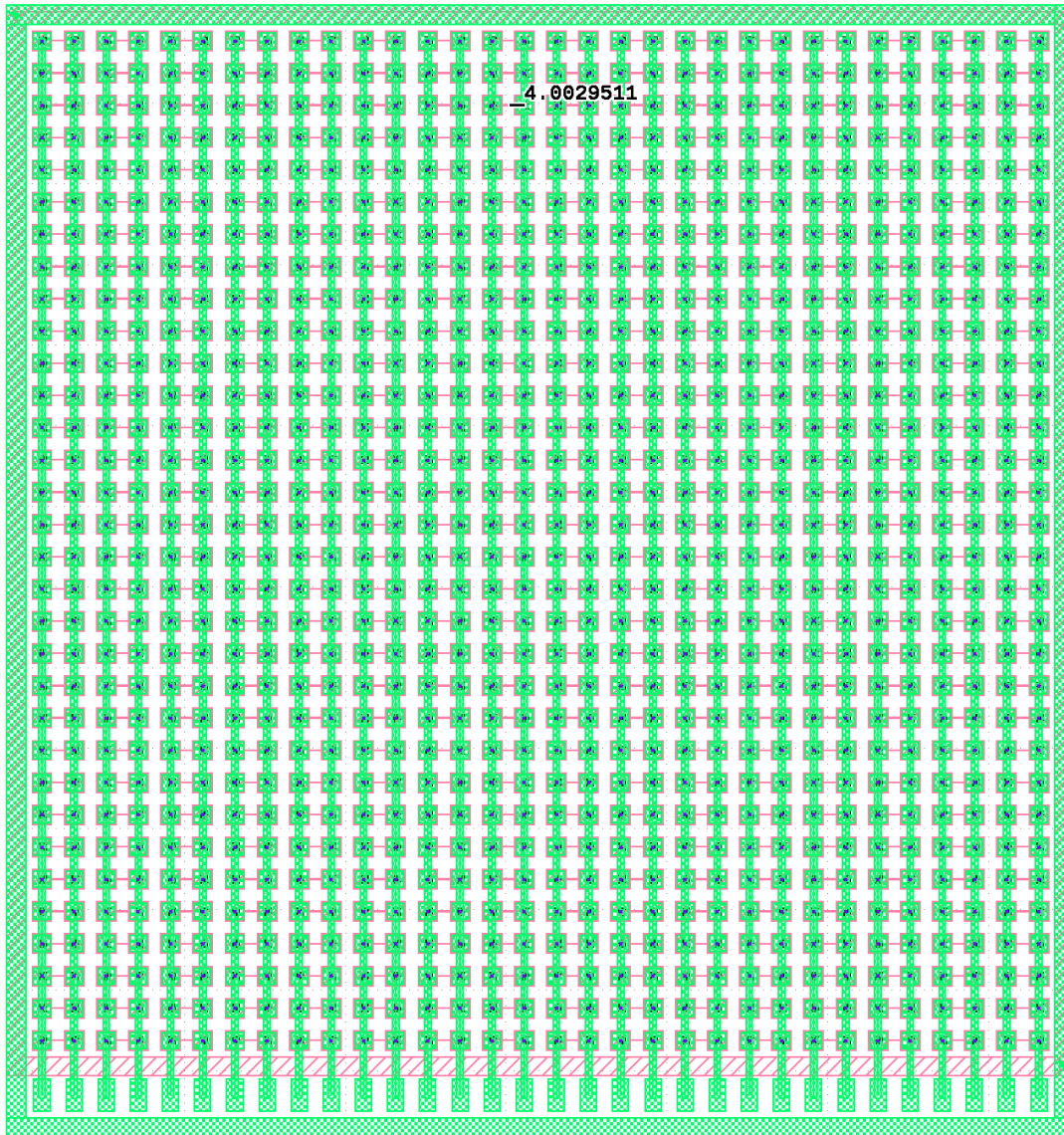
Test-beam occupancy map of ALTIROC with double gold studs + irradiated LGAD sensor



Not connected by design
 Masked due to high noise
 Confirmation of good inter-connection with occupancy map (≈ 100%)

- High connection yield, reproducibility, low temperature process
- Only for large pitch (>100μm), large pads (>80μm) chips

Daisy Chain for bonding testing

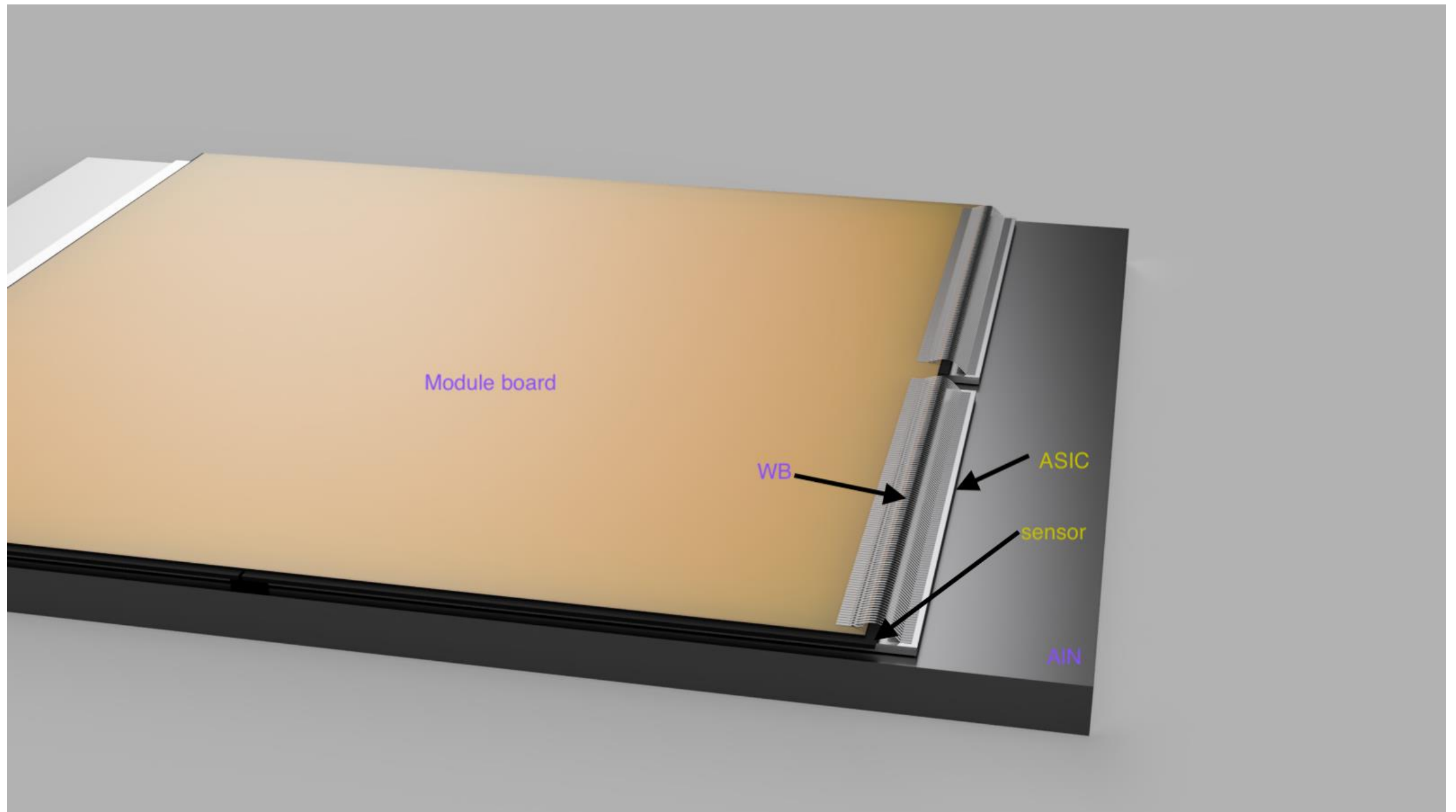


We are planning on testing the production of Daisy-Chain test structure on Silicon at CNMS Clean room

- Testable connection via interconnect on the top layer with thin metal resistors
- Realistic dimensions
- Resulting structure can be used for mechanical integration

Module assembly

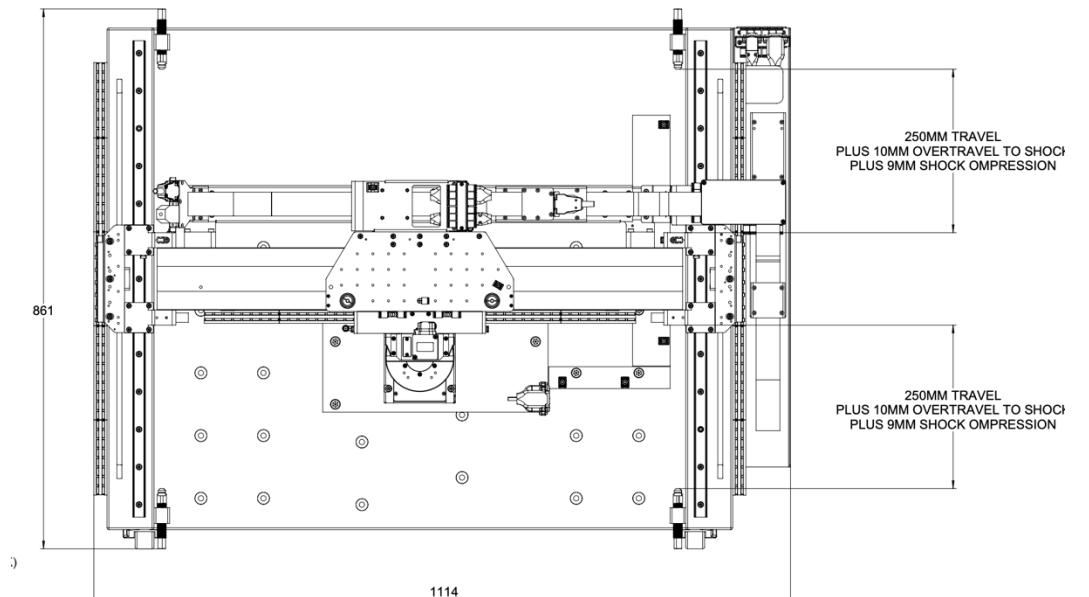
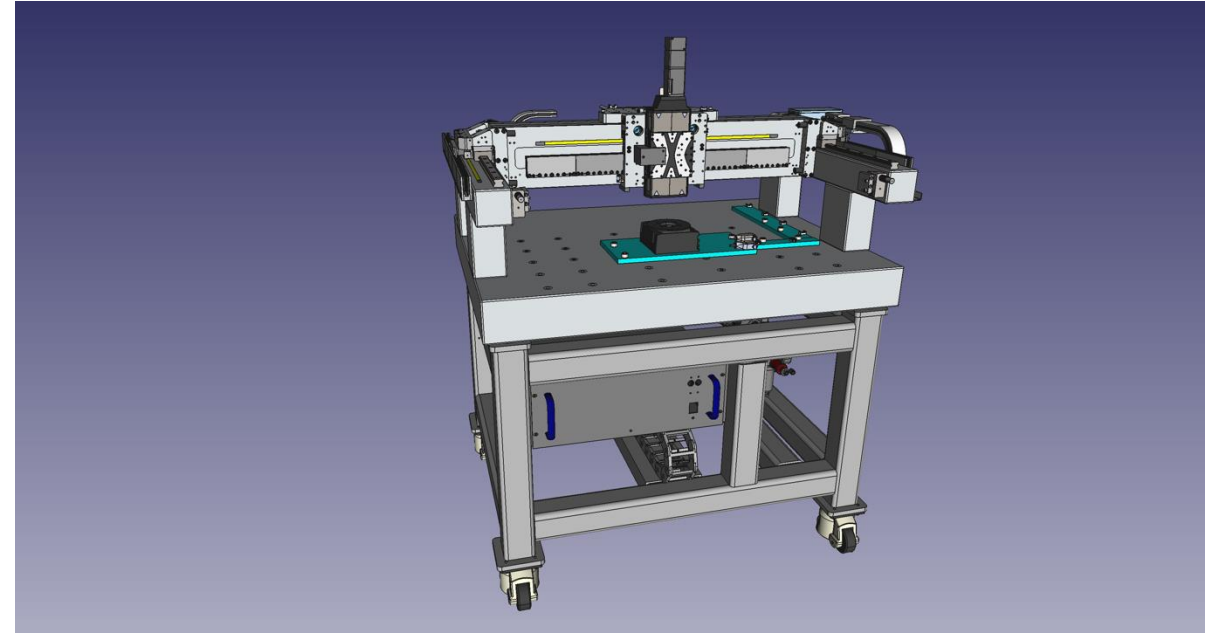




Gantry/Flip Chip assembly

Automated gantry is often used for serial assembly in microelectronics factories

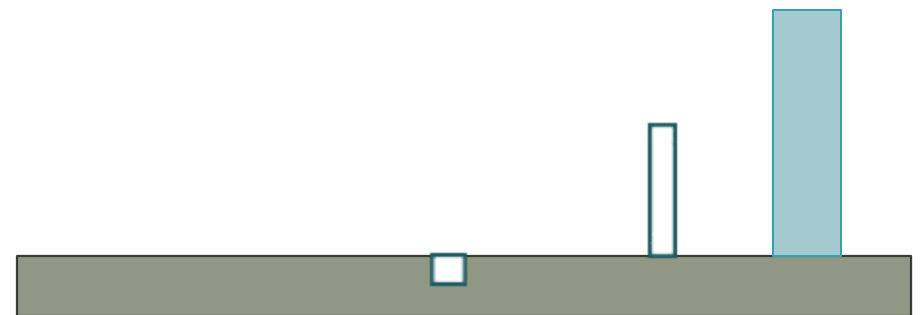
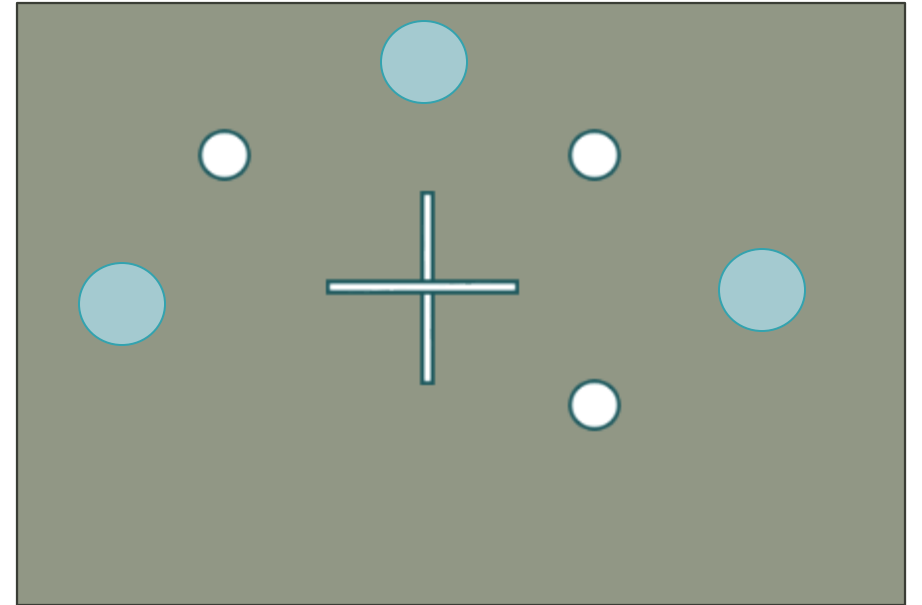
- High precision movement over large volume
- Tool handling and switch capabilities
 - Vision for alignment
 - Suction handling tools
 - Dispenser head
 - Weight handling and curing tool
- Delivery to ORNL cancelled due to delay in production, seeking alternate solution
- Possible alternate solution is using the FC150 dispenser and bonding head to add Flex circuitry to assembly after bonding, in one go
 - Sensor+ASIC already aligned after bonding
 - Need to develop precise pickup tool adapted to Flex circuit



Jig-based assembly procedure

A precisely machined jig can be used to manually perform module assembly.

- vacuum site
- alignment pins
- Insertion pins

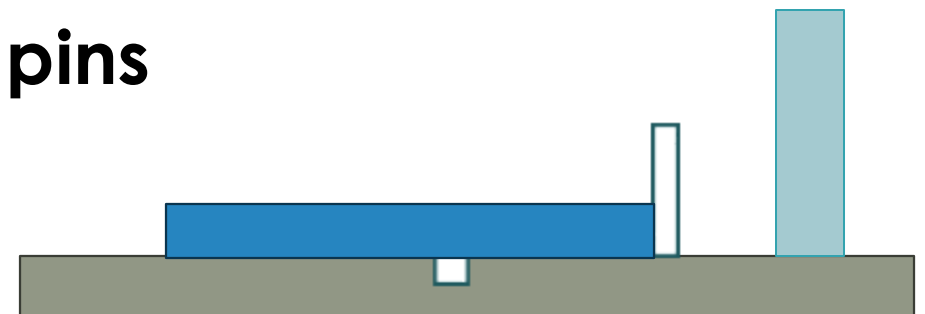
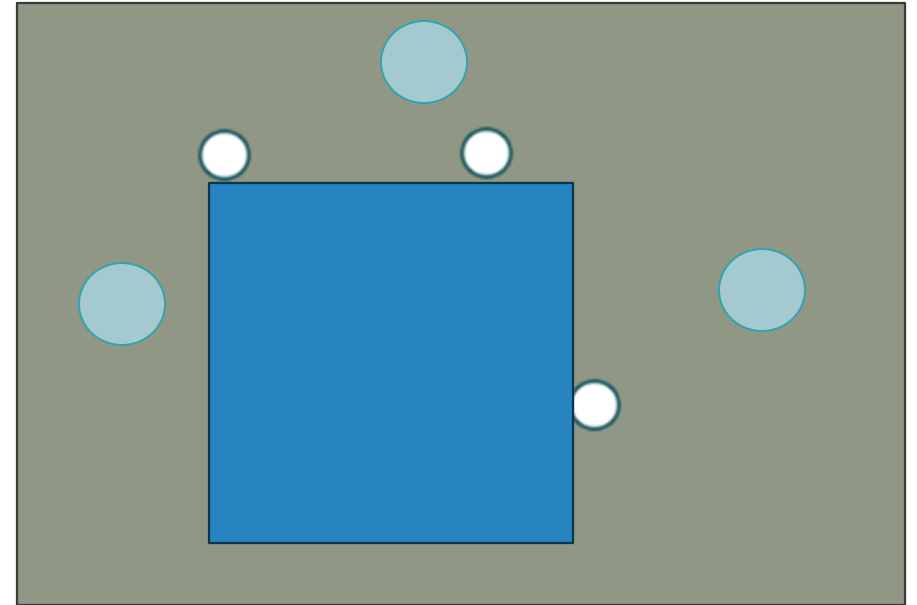


Jig-based assembly procedure

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- alignment pins
- Insertion pins

Sensor is aligned to jig using alignment pins

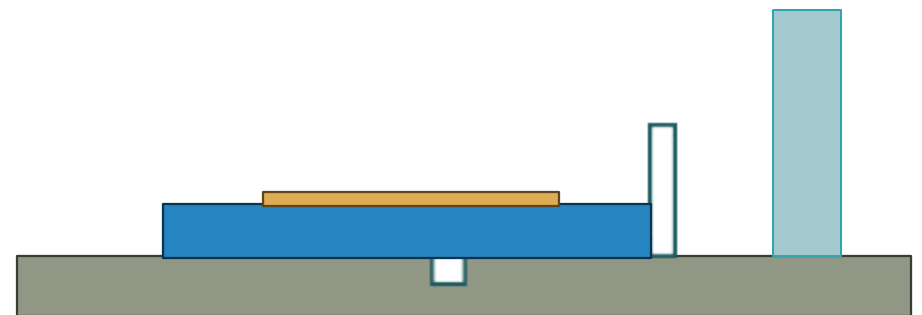
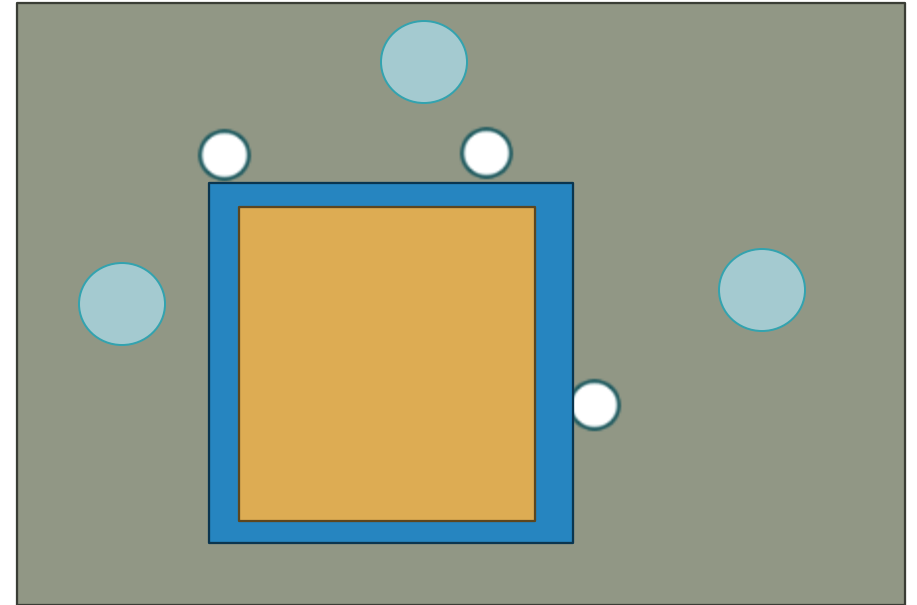


Jig-based assembly procedure

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- vacuum site
- alignment pins
- Insertion pins

Glue is dispensed

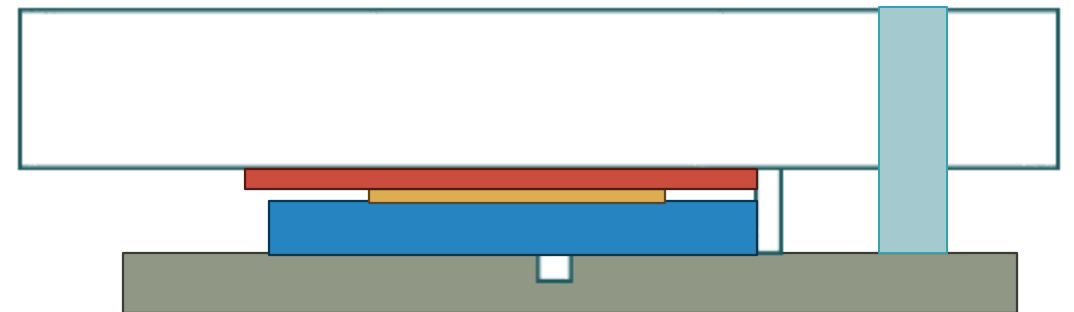
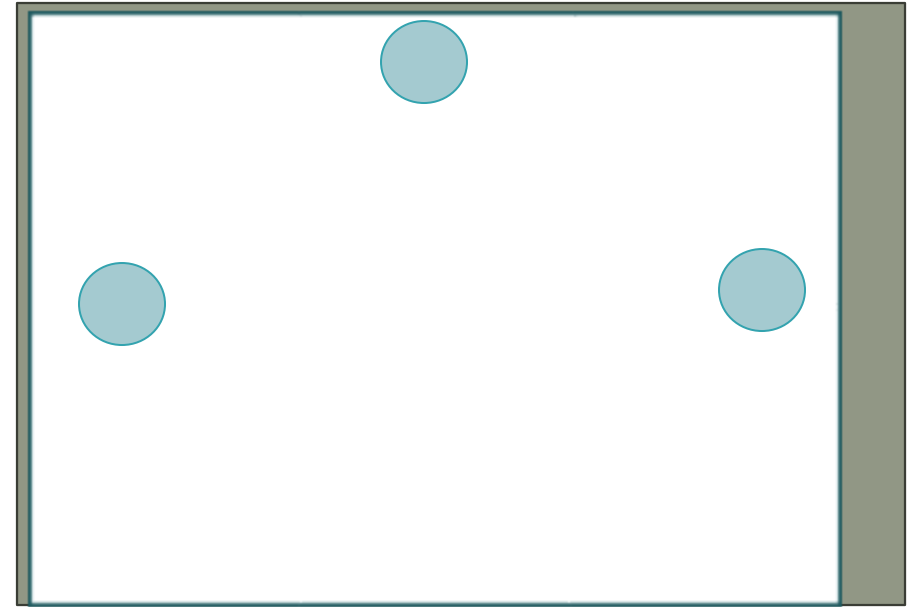


Jig-based assembly procedure

A precisely machined jig can be used to manually perform module assembly.

- vacuum site
- alignment pins
- Insertion pins

Flex is aligned in a similar way to a top jig and applied to assembly

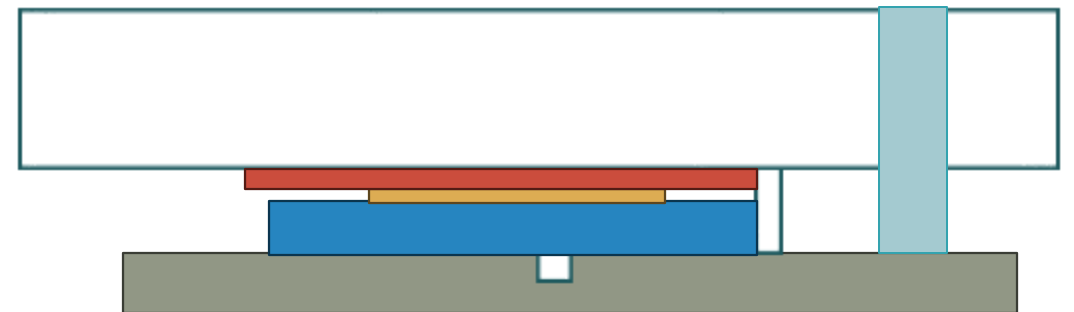
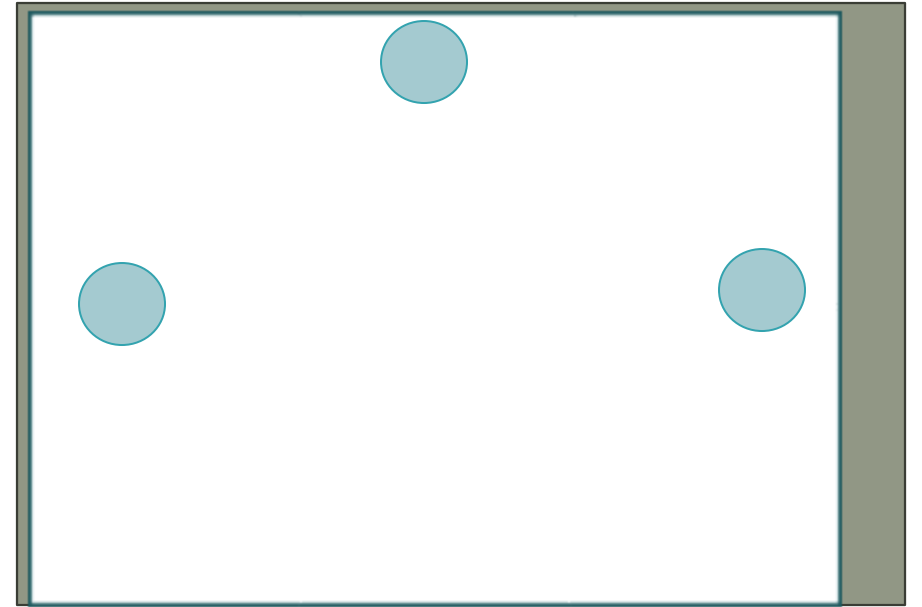


Jig-based assembly procedure

A precisely machined jig can be used to manually perform module assembly.

- vacuum site
- alignment pins
- Insertion pins

Glue is cured in place , then alignment pins are removed and module ready for wire-bonding





QA/QC procedure for module testing

- The main deliverable for the module part of the scope is **known good modules** , tested to meet a set of requirements at the assembly site
- The testing of production modules done covers
 - **Visual inspection** of the module after assembly
 - **Functional testing** : Power-up, tuning, stress test, thermal cycling
 - **Source testing** : Functional testing with source, test beam with subset of modules for QA
 - Repeat test after **irradiation** to verify compliance with requirements

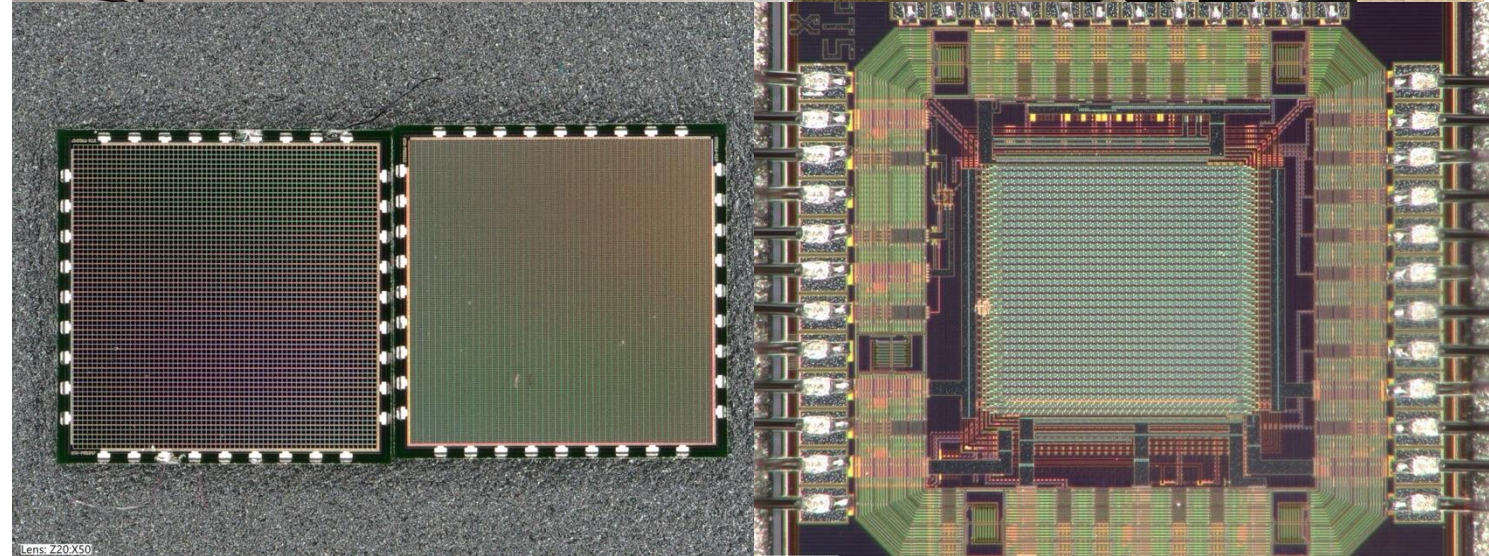
Visual inspection QA Test setup

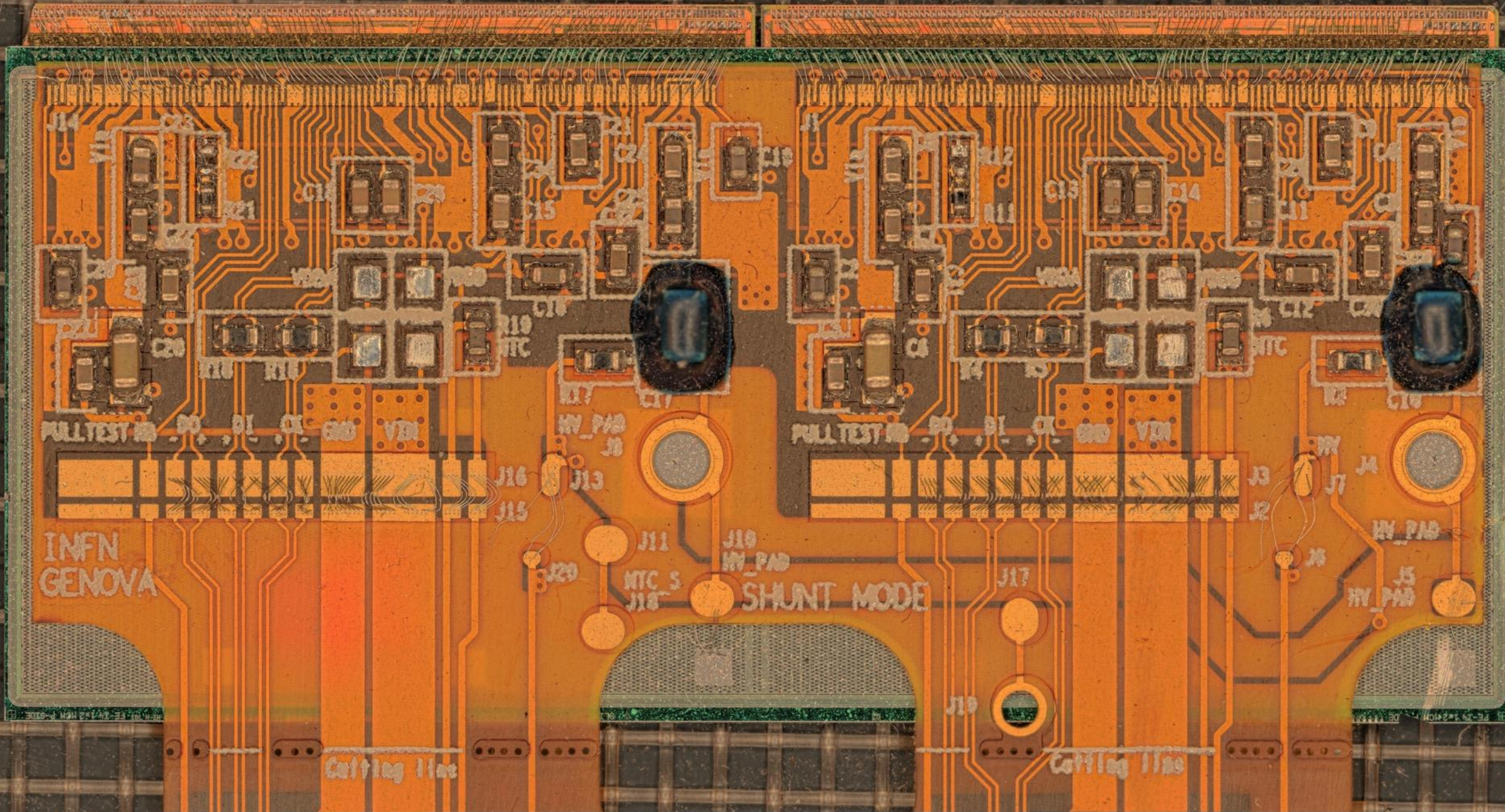
We have a Keyence VHX-650 digital microscope with :

- 100X zoom , 100x100mm platen
- +/- 75deg observation angle
- Motorized XY staged
- Stching, 3D scanning capabilities
- Automated metrology

Visual inspection and logging into the database is an important step of QA, to spot damage during transport and keep track of possible defects that could have consequences down the line after bonding.

We are exploring the possibility to use machine learning in the production phase to accelerate inspection





INFN
GENOVA

Cutting line

SHUNT MODE

Cutting line

PULL TEST NO. DO, DI, CL, GND, VDI

PULL TEST NO. DO, DI, CL, GND, VDI

J14
C21
C20
R18
R19
R10
MTC

J12
C13
C14
R11
R12
R13
MTC

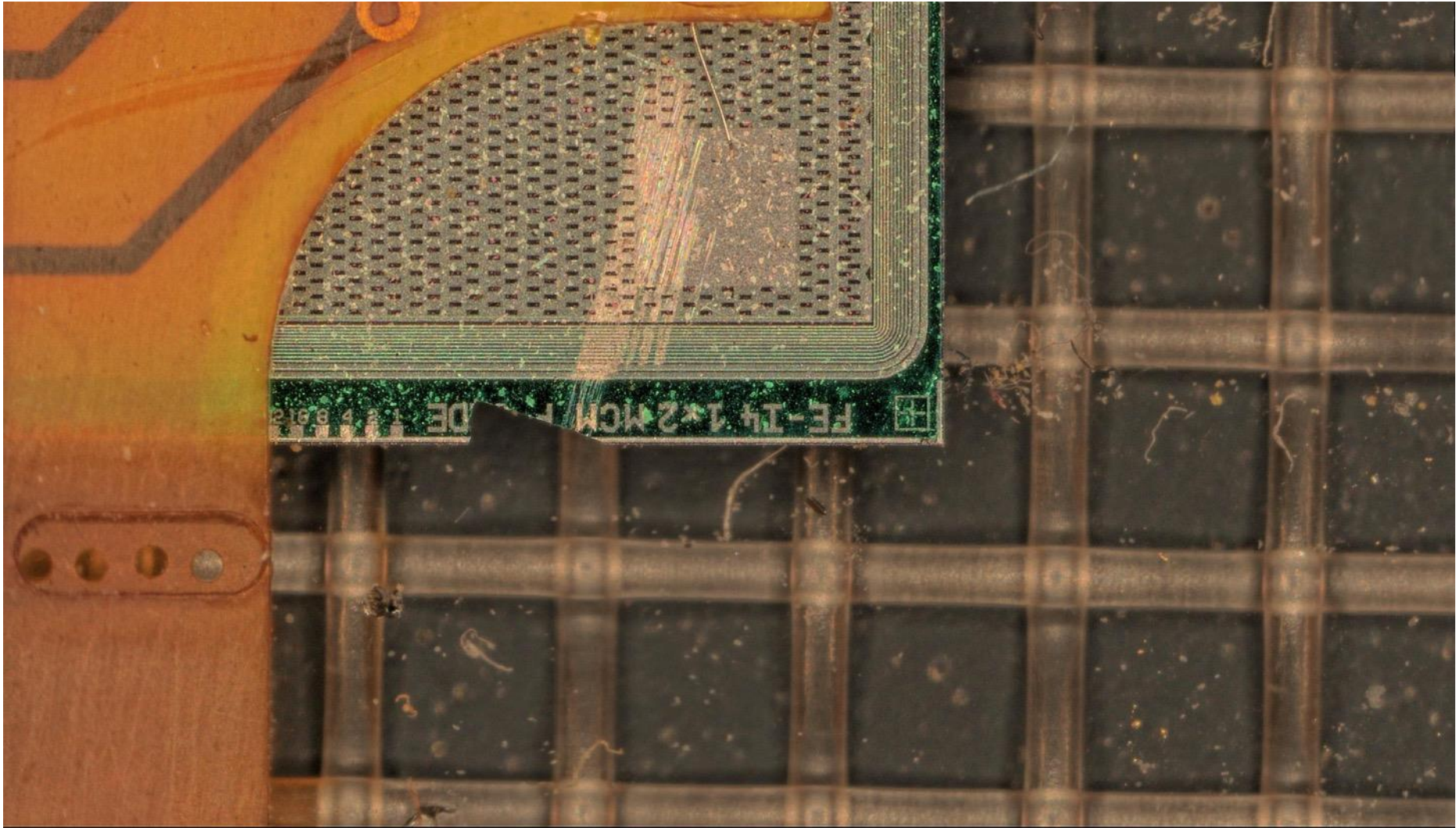
J16
J15
J13
J11
J10
MTC 5
J18

J3
J2
J7
J4
J5
MTC

REV. 1.00 24/07/15

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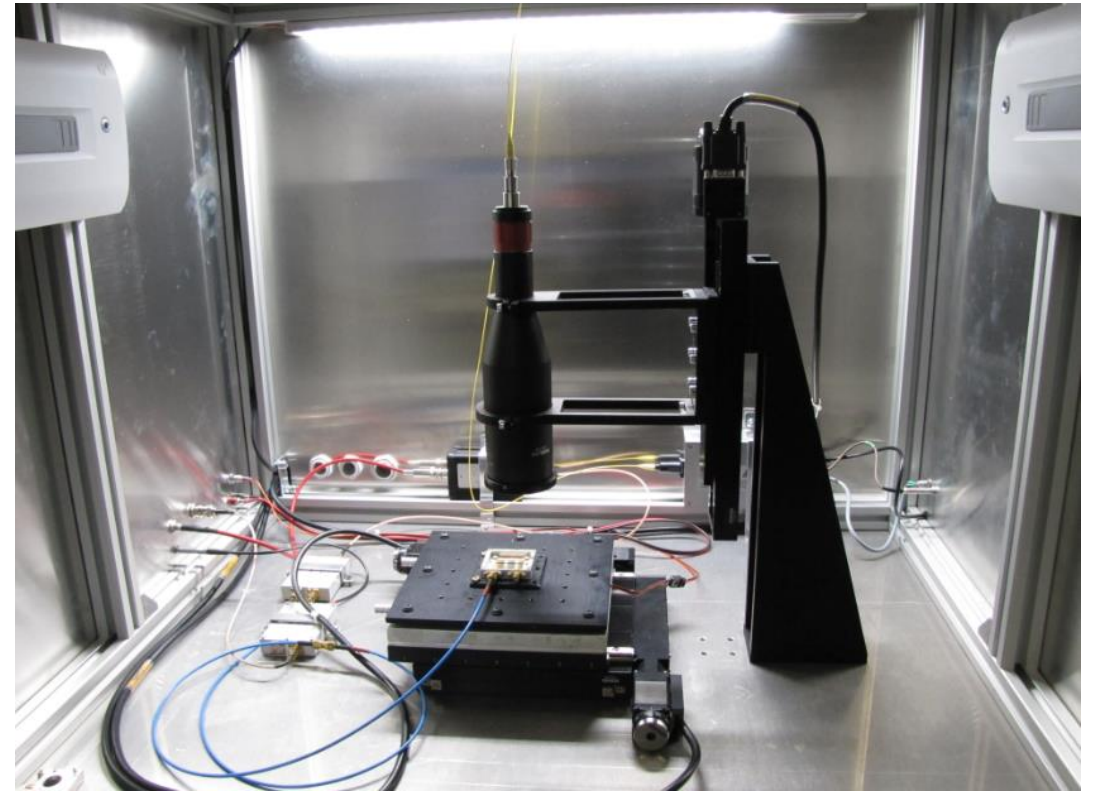
Visual inspection QA Test setup



Source/Laser characterization QA Test setup

Samples selected to be taken out of production for testing will be assembled on PCB for testing with a scanning laser setup

- 100X100mm scanning area
- 1064nm and 550 nm pulsed laser, 350-4000 ps pulse
- Focus to $\sim 10 \mu\text{m}$ spot
- Scanning axis to map response over sensor surface
- The setup will be equipped with Peltier and chiller for operation at -20C after irradiation
- Laser system from Particulars
- Chiller, amplifiers, power supplies and table for the test setup after irradiation



Next steps

- Thermo-mechanical dummies need to be produced to advance the interconnect for fTOF
 - Key building block for thermo-mechanical prototype (FY24-25)
 - Allow testing of assembly procedure, cooling, stress testing etc.

- EICROC1 will be the first available ASIC for functional module assembly
 - Targeting first module prototypes in FY25
 - Subsequent iteration with EICROC2-3 in FY25-26