Toward BTOF FPC design

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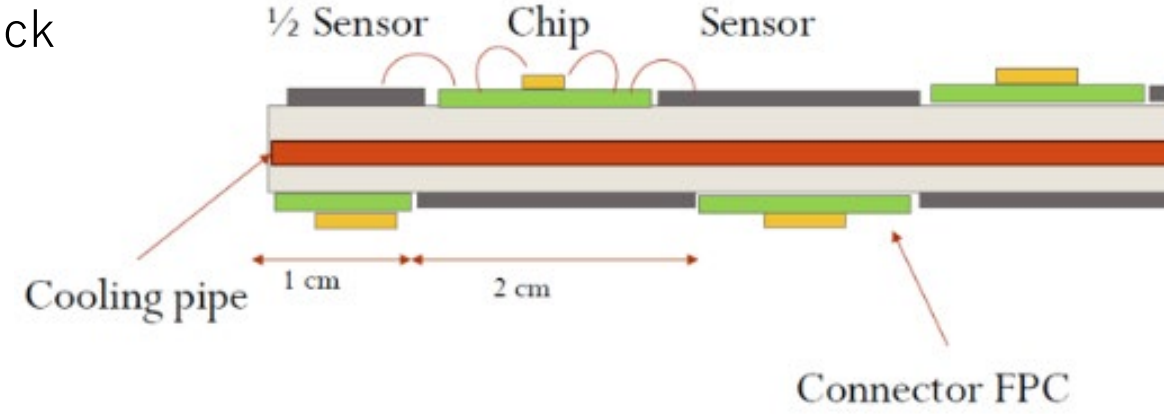
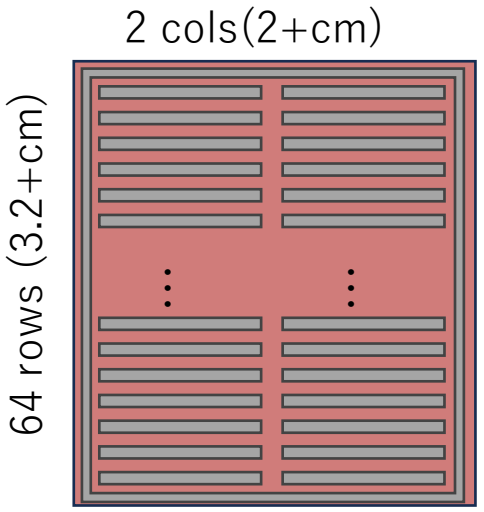
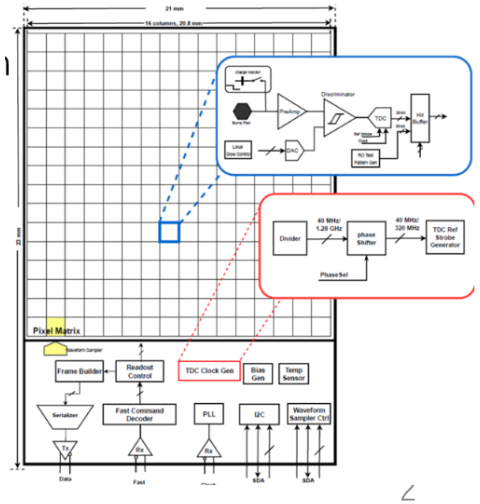
Basic information and requirements

- BTOF Ladder structure (Half)
  - Sensor/ASIC on FPC are put at both front and back sides
    - 2 FPCs are necessary
- Sensor dimension
  - 64x2 strips as unit = 3.2 x 2 cm^2
    - Strip size : 0.5mm x 1cm
- ASIC: ETROC2 as 1st candidate
- Requirements for FPC
  - 135cm length x 5cm width
  - 1% X_0 thickness (in total)
  - Digital signal transmission (lpGBT)
  - Power and GND supply
- More practical Info is needed for FPC design



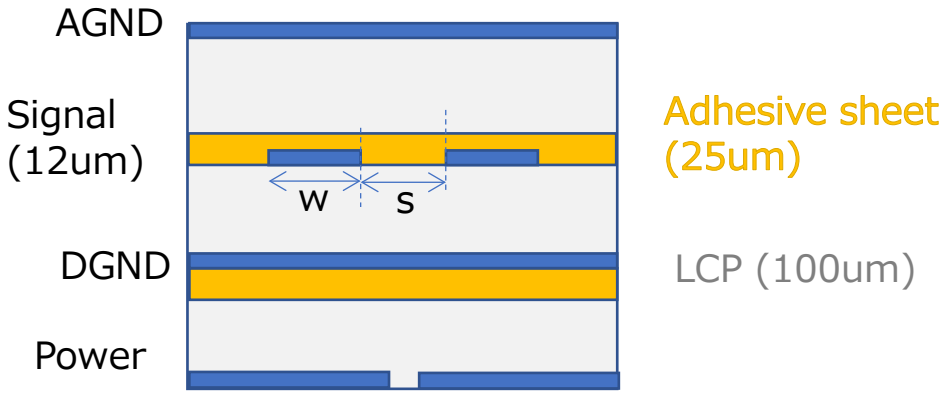


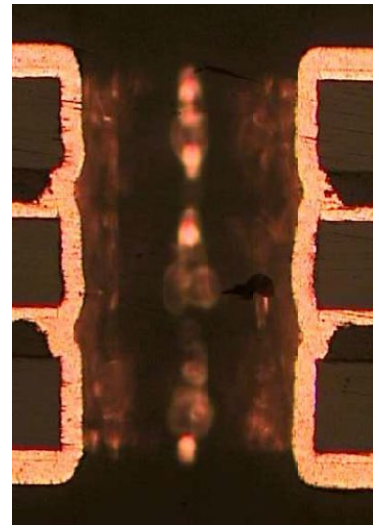


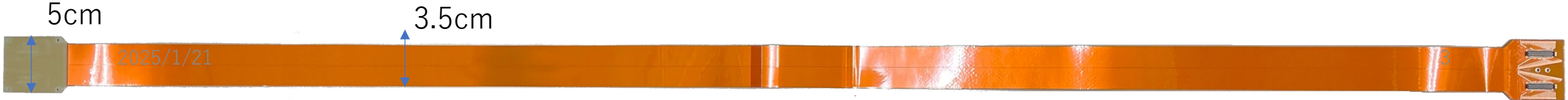
Long FPC from sPHENIX INTT

- Cable design (prototype)
  - Dimension (L x W): 130 x 5 cm^2
  - 4 layers (signal , 2xGND, PWR): X = 0.8% X_0
    - Cu : 12um thick per layer + 30 um Cu plating on surface
  - Lines : 124 lines (Line and space : 130 & 130 um)
  - Z_{diff} : 100Ω by strip line structure
    - Signal layer is sandwiched by GND layers
  - Liquid Crystal Polymer (LCP) as substrate
    - Less signal loss due to low di-electric constant & tan(δ)
    - Thick LCP available for Z_{diff} : 100um

4 layers laminated by the adhesive sheet



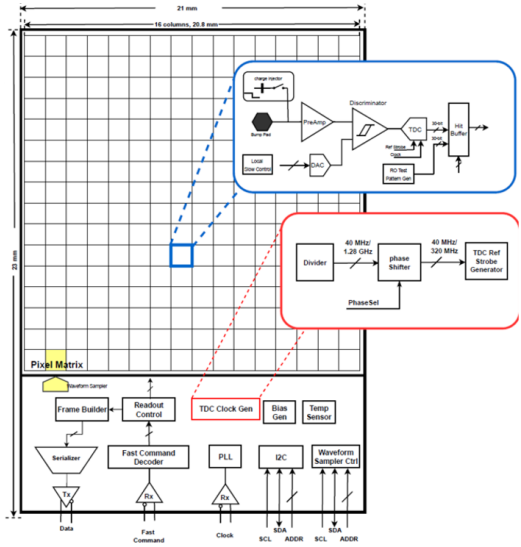




Signal lines based on ETROC2

- Size : 21x23mm^2 (Box shape) since 2D for the pixels
  - Bump bonding for pixel (CMS)
- Npads : 124 w/ wire bond
  - CMS Digital lines: 13 lines
    - Tx: 2x DataOut (DS)
    - Rx: *CLK40 (DS)*
    - Rx: *FastCom (DS)*
    - Rx: **I2C (2 lines, SCK, SDA)**
    - Rx: **RSTn (1 line)**
    - Rx: I2C addr (5bits)
  - Analog : 1 line (Vtemp)

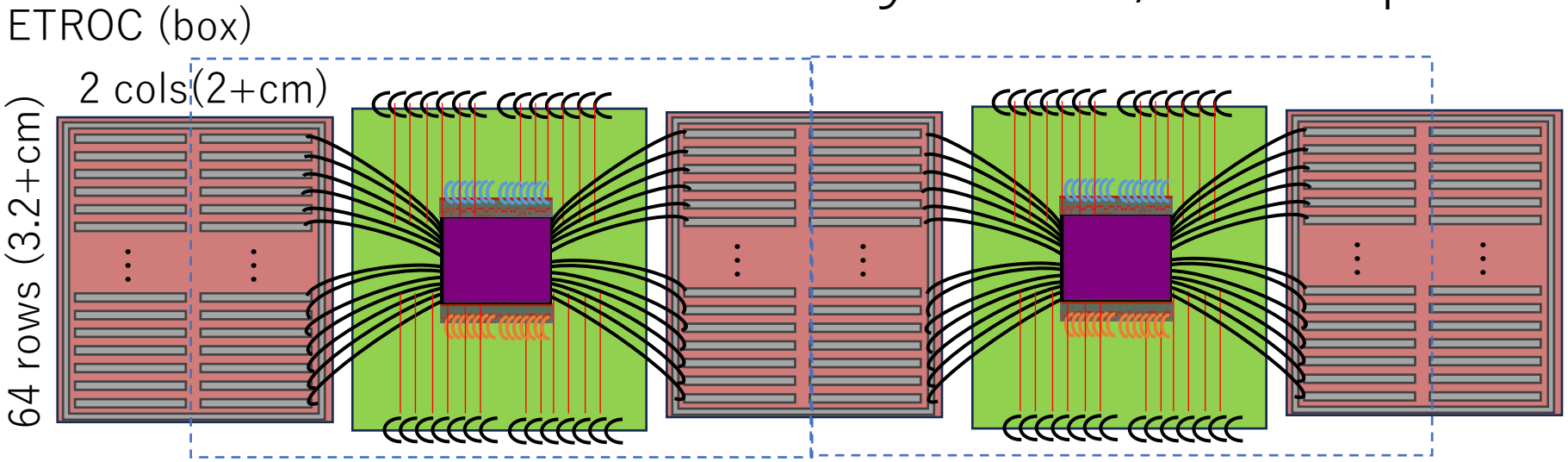
ETROC for BTOF FPC
→ BTOF FPC ~5 or 6 lines
→ 1x DataOut (DS) = 2 lines
→ *p2p = 2 lines*
→ *bus w/ 4 chips (not p2p) = 2 /4 lines*
→ *bus w/ 17 chips = 2/17 lines*
→ **bus for all chips = 1 / 34**
→ 5 or 6 bits (depending on FPC conf.)
→ *1 line*



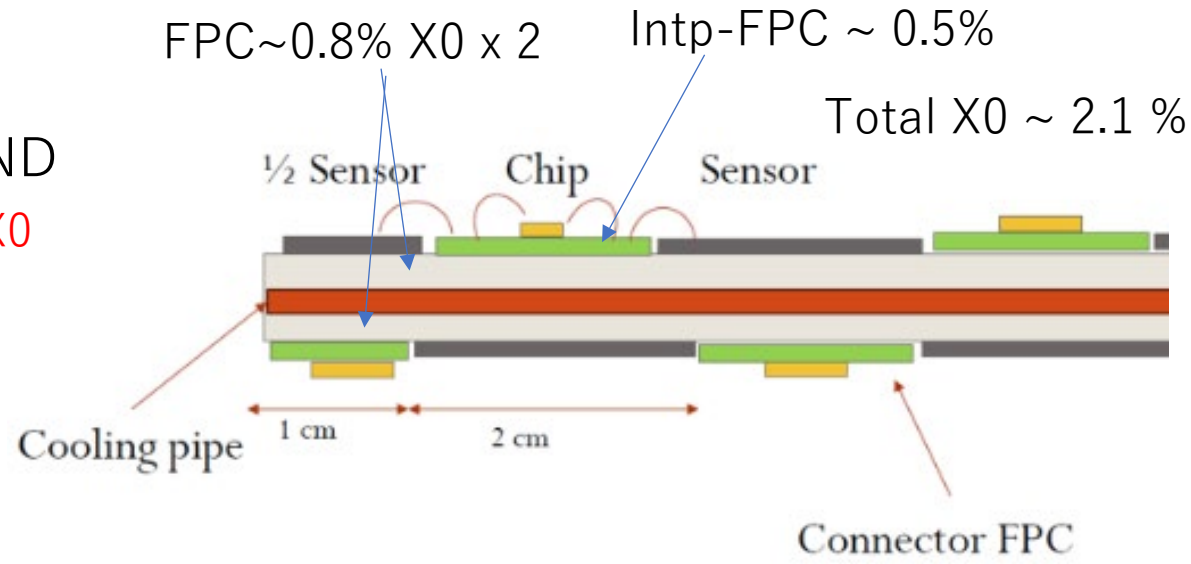
https://etl-rb.docs.cern.ch/Specifications/etroc-test-card/#Specifications

- 135 cm FPC = 33 or 34 ASICs/FPC (x2 FPC x 2cm/sens)
  - **33 or 34** sensors are necessary
- If 34 ASIC's are in a FPC, 34 x {4 + 2/4+ 2/17 + 1/34+1} = 194 lines in total
  - INTT: 124 lines w/ 3.5cm width (1.5 times more than INTT,)
  - If use INTT technology, Thickness is ~0.8 % X0 / FPC We use 2 FPC for a ladder ~ 1.6%X0

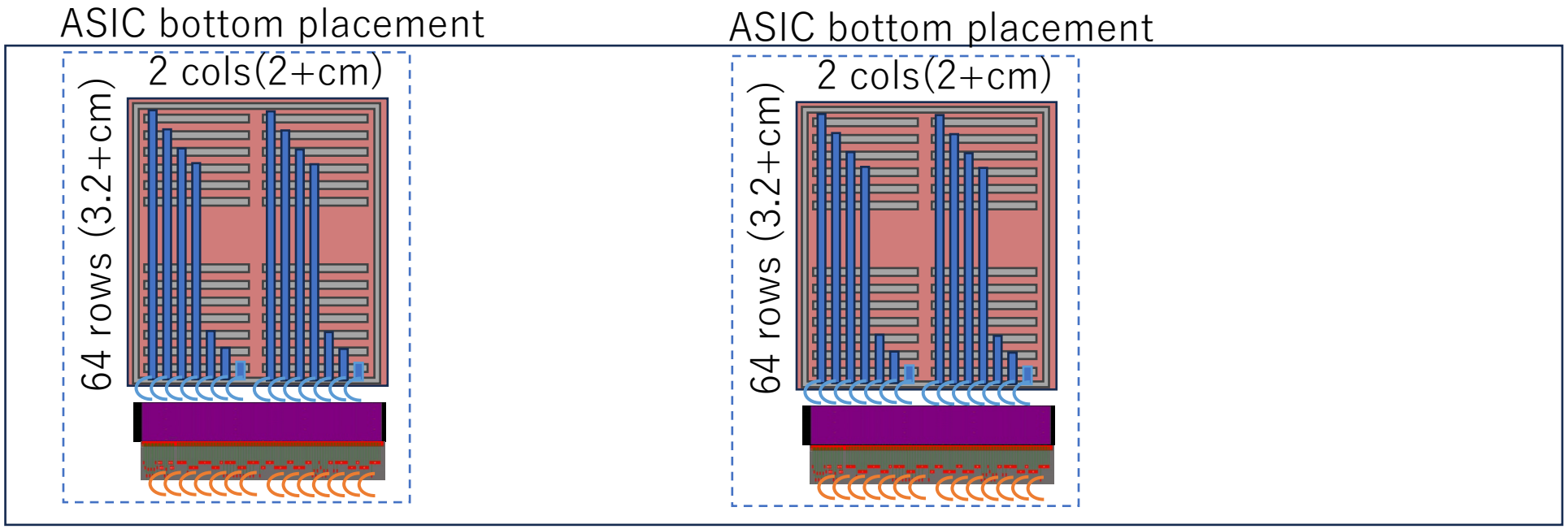
Sensor and ASIC Layout w/ interposer



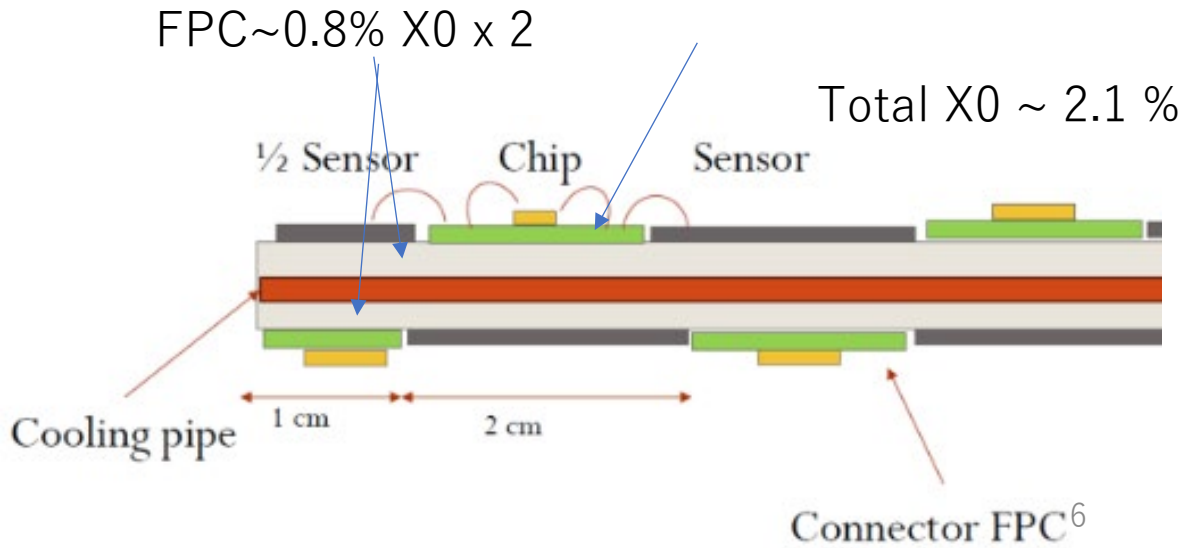
- Interposer FPC (green)
  - Routing signal lines from ASIC to FPC
  - Multiple (3) layers needed for DIO, power, GND
    - Additional thickness >0.5 % X0 -> Total~ 2.1% X0
  - Length of lines could be different
    - may get the time resolution worse
- Sensors & ASICs are connected
  - Difficult to make a (simple) module structure



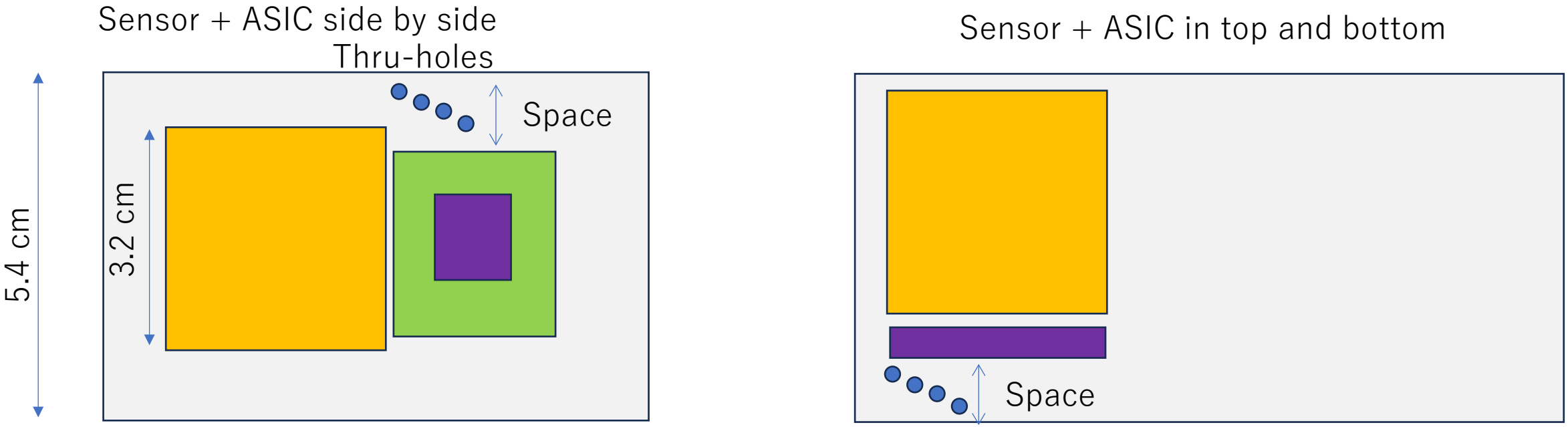
Option : Bottom layout of Sensor and ASIC



- ASIC at Bottom
  - Easy to make a module
  - Different lengths of double metal
    - Signal might be distorted
  - Simpler wire bonding
- If interposer, routing the lines get easier

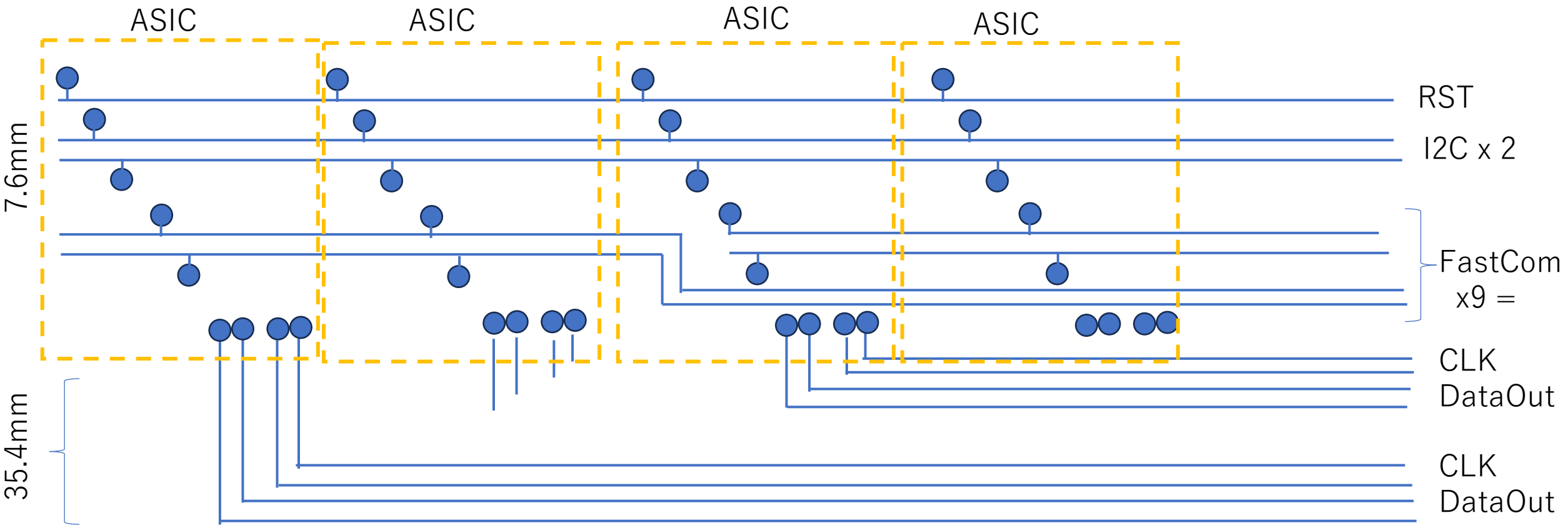


Space btw FPC and ASIC needed for wire bonding



- How much space is necessary to come out the signal lines from inner signal layer

Strawman ideas of routing the signal lines in FPC

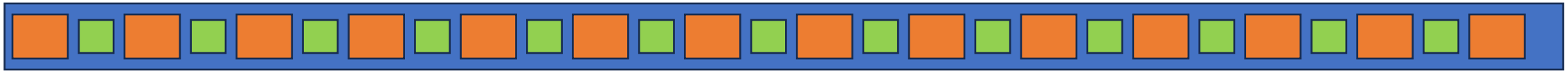


- Line arrangement in signal layer : No cross-over of lines arrowed
  - Line (130um) + space (130um) + Land (for thru hole) = ϕ300um ~ 600 um
- Thru hole width : ~ 8.8mm (0.6mm*7+ 0.52mm*8 + 0.6mm = 4.2+4+0.6)
- Line area width: 34 * 4 * 260um = 35.4mm
- Land for powers and GND are also necessary

~44.2mm :
signal lines occupy < 5cm width

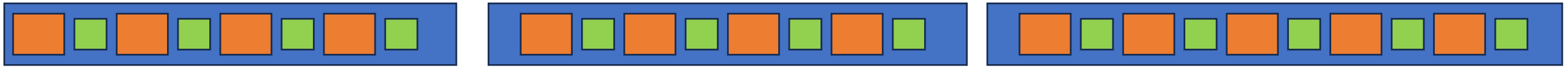
Module structure option

- Ladder : 135cm long with 34 sensors and 34 ASICs



  - Minimize the additional connection
  - Assembling this very long module is difficult
    - Yield rate will be issue during the production

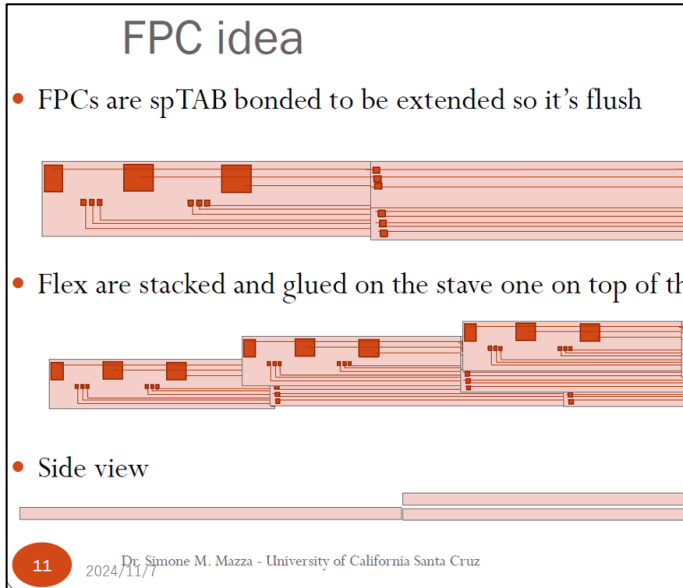
- If split by 3 pieces, each FPC is 50cm long



  - 50cm FPC can be made with minimum risk in production
    - Finer line & space available (60um x 60um)
  - Multiple connection needed
    - Reduce active area by connecting these FPCs

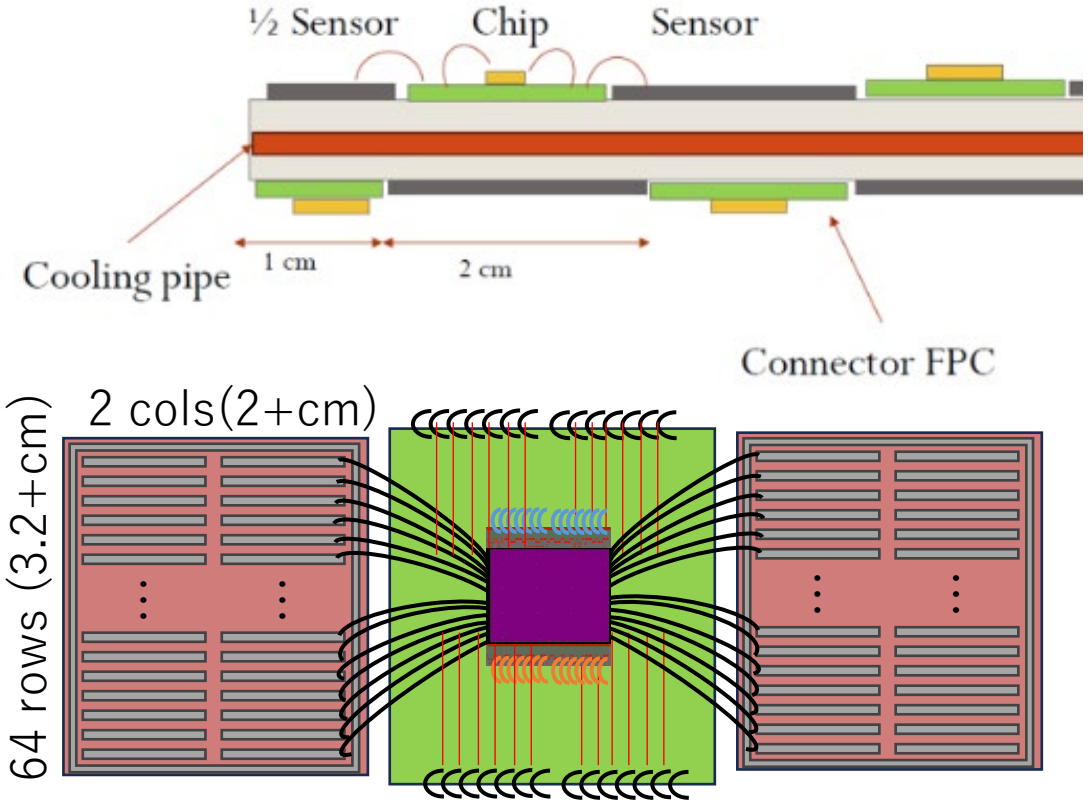
- How connect each other ~ 200 lines + power + GND
  - spTAB bonding
  - Connector (micro pitch)
    - Fragile, (not so reliable?)

Simone's slide in Nov. 2024



Summary

- FPC design started
  - 135 long FPC with 34 sensors and ASIC's
- There are some challenge
  - Material budget ~ 2.1%
- More discussion necessary
  - How does ASIC is placed?
  - What ASIC size (dimension) good for us?
  - How signal lines are placed in FPC ?
    - Complicated routing of the signal lines are not good for the long FPC.
  - Module option
    - Connecting some short FPC to make long FPC is possible option
- I would like to make a reasonable FPC proposal soon

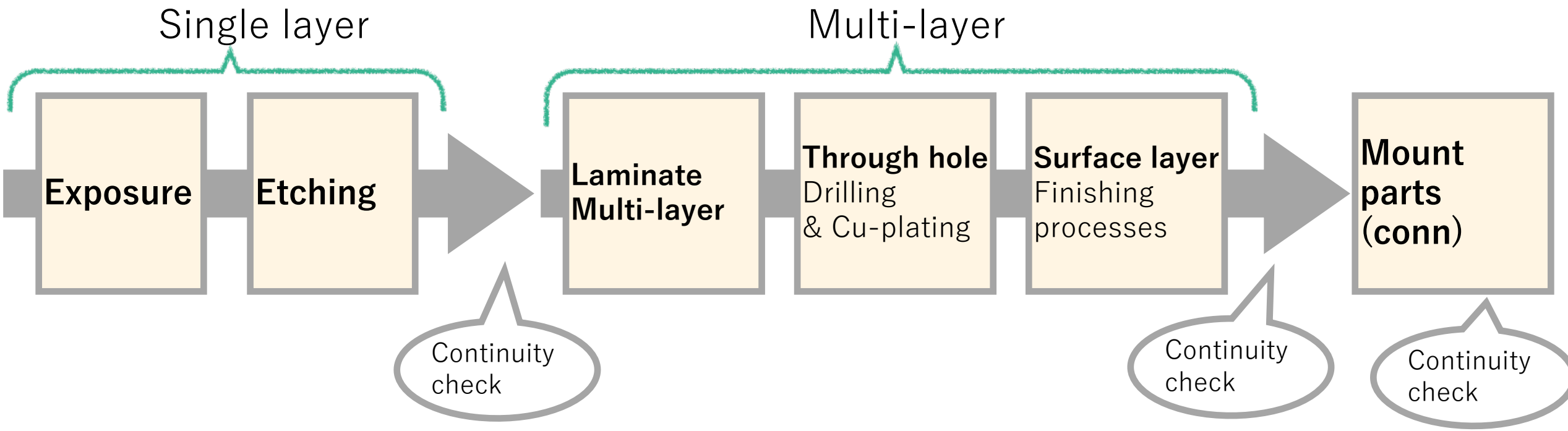


ETROC2 io, pwr, gnd connections

- Digital
  - Tx: DataOut (LVDS) x 2
  - Rx: CLK40 (LVDS)
  - Rx: FastCom (LVDS)
  - Rx: I2C (2 lines, SCK, SDA)
  - Rx: I2C addr (5bits)
  - Rx: RSTn (1line)
  - Rx: CLK1280 (LVDS) : debug
- Analog
  - Rx: Temp(1line, analog)
- Power:
  - VDD_A, VDD_D, VSS_D, VSS_A,

5	VDD_A	22-26	27	**I2CAddr0**	83
6	VSS_A	27-28	28	**I2CAddr1**	84
7	**CLK40p**	**29**	29	**I2CAddr2**	85
8	VSS_D	30,32,34,36	30	**RSTn**	86
9	**CLK40n**	31	31	VSS_D	87
10	~~**CLK1280p**~~	33	32	VDD_D	88
11	~~**CLK1280n**~~	35	33	**SCL**	89
12	**FCp**	37	34	**SDA**	90
13	VDD_D	38,40,42	35	**I2CAddr3**	91
14	**FCn**	39	36	**I2CAddr4**	92
15	**DOLp**	41	37	VSS_D	93-95
16	**DOLn**	43	38	VDD_EFUSE	96
17	VSS_D	44,46,48-50	39	VSS_A	97, 99-104
18	**DORp**	45	40	VSS_AO	98
19	**DORn**	47	41	VDD_A	105-109
20	**VP**	51	42	VSS_A	110-111
21	VDD_D	52-54	43	VDD_A	112-117
22	VSS_D	55-59	44	VSS_A	118,120-124
			45	**VTemp**	119

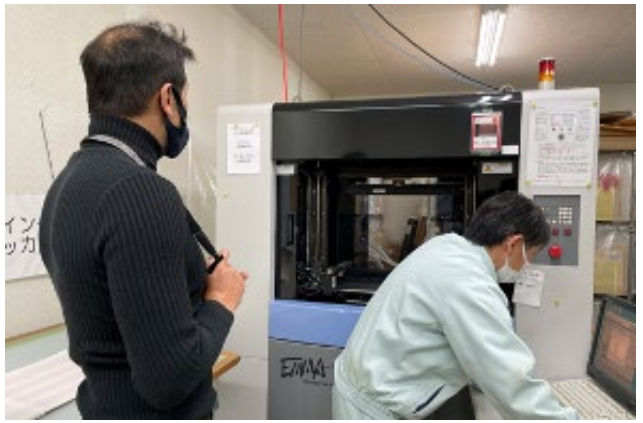
Continuity checks for the production



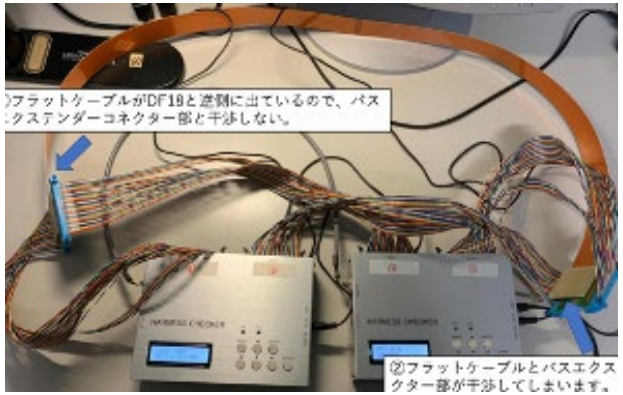
Three times of the continuity checks during the production

- Twice at manufacture.
- One as receiving inspection

Yield rate improved much

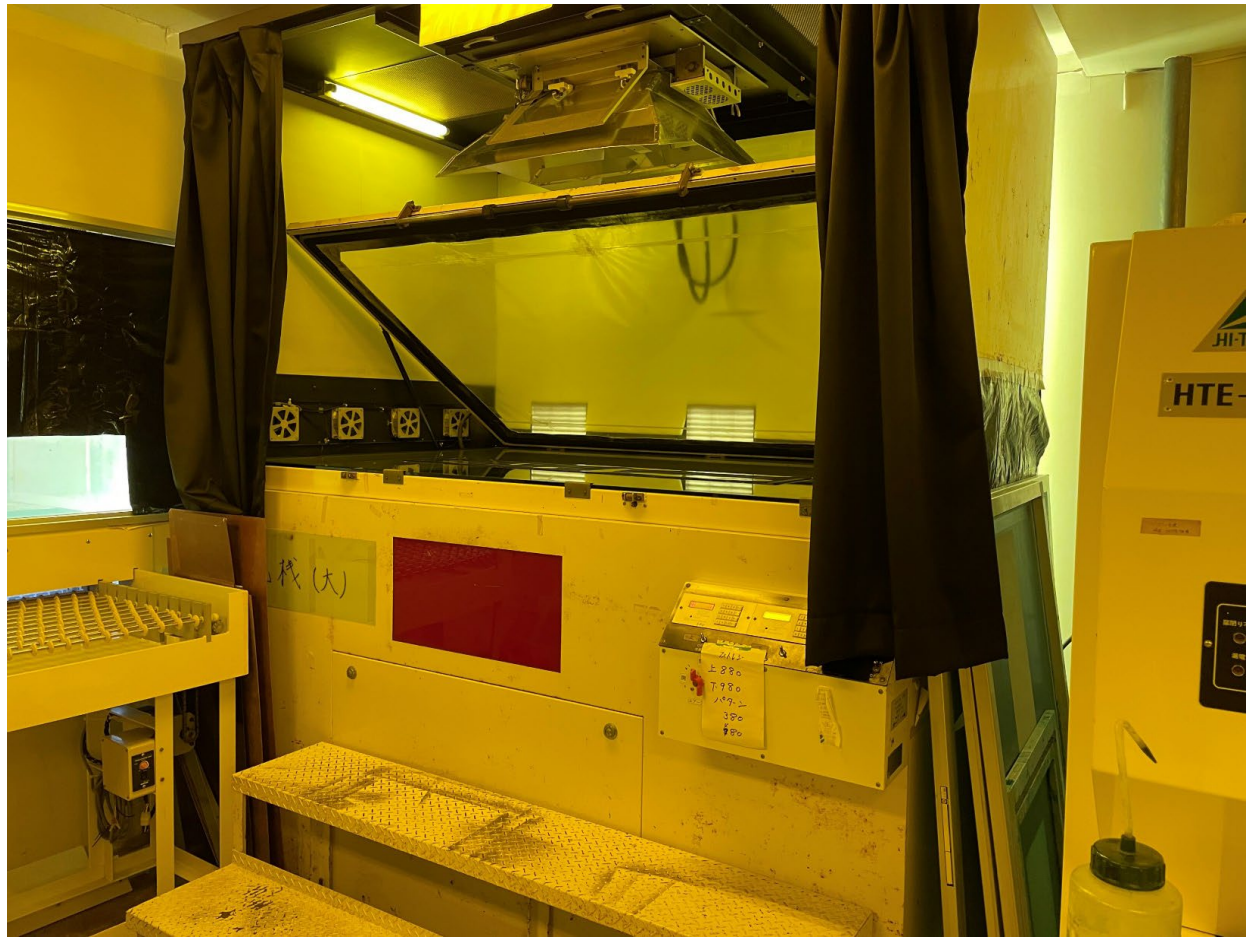


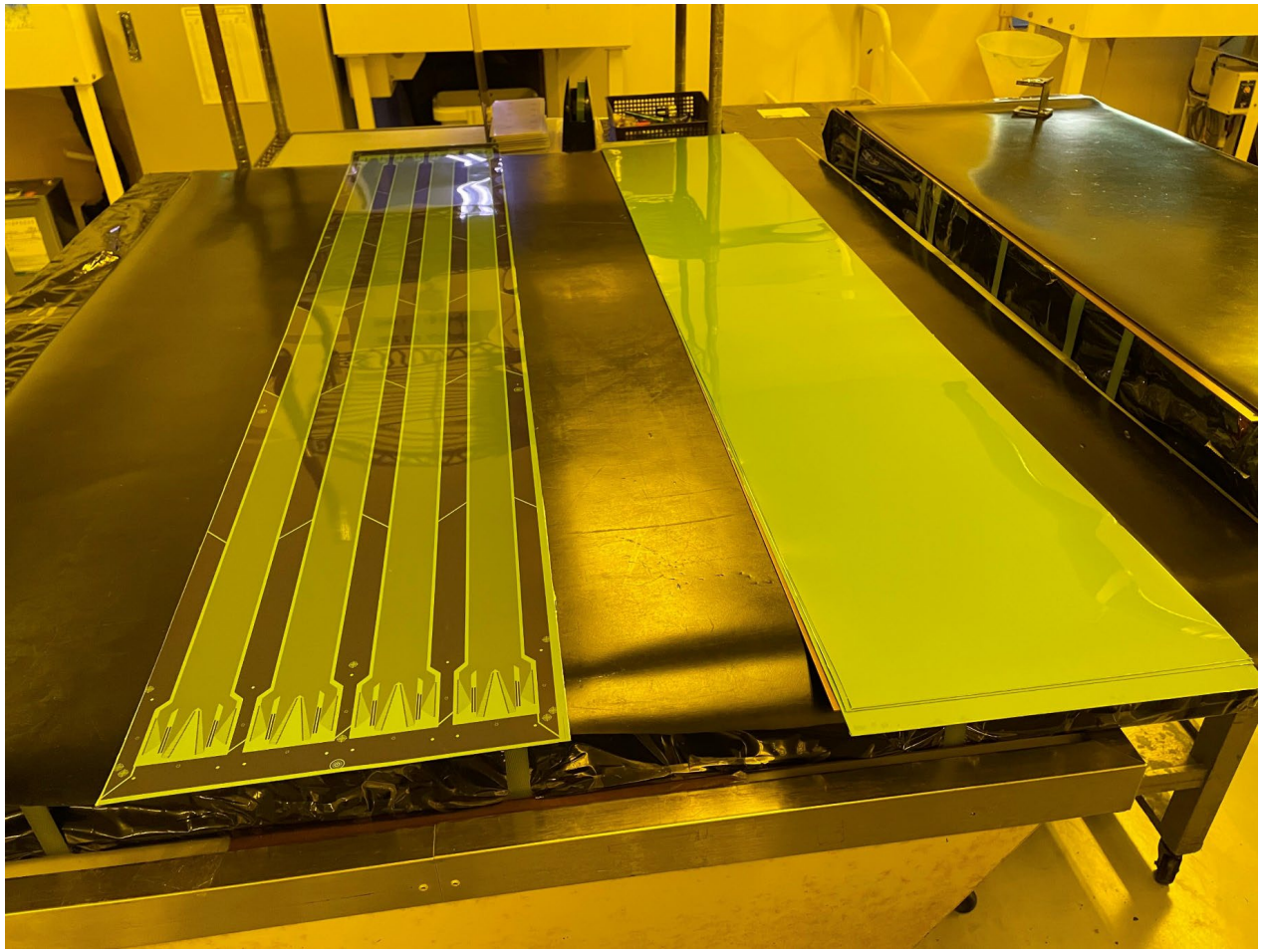
Flying probe tester



The special cable checker

Big light exposure machine needed for long FPC

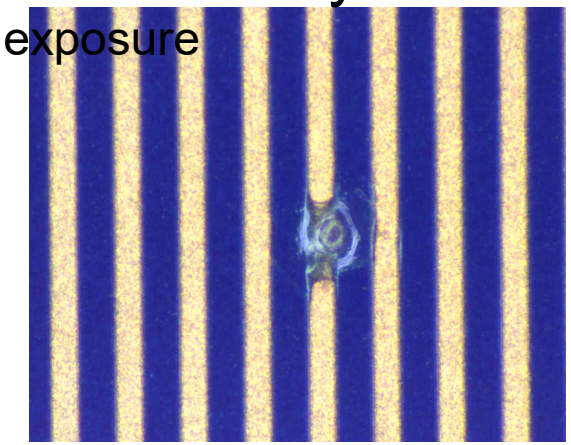




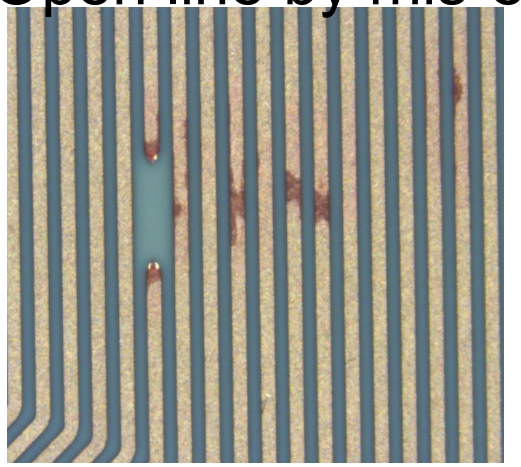
Toward Mass production

- Improving the yield rate is necessary
  - Current good yield rate was ~20~30%
  - Production parameters are best tuned
    - Pressure to make multi-layer & make thru-hole
- Inspected/discussed the production procedure with manufacturers
  - Contamination of small dusts is major cause when producing the FPC
- New procedures to remove the dust as much as possible
  - UV lights to look for remaining dust
  - Silicon roller to remove dust
- Check the continuity before laminating multiple layers
- Expect to be improved to good yield rate ~80%

Short line by mis-exposure



Open line by mis-et



Test machine for Visual inspection

Visual inspection machine developed

- Hardware：
  - Take photo by Camera
- Software
  - Look for the broken (not good) line
- Yield rate improved to 97%