TOF Electronics

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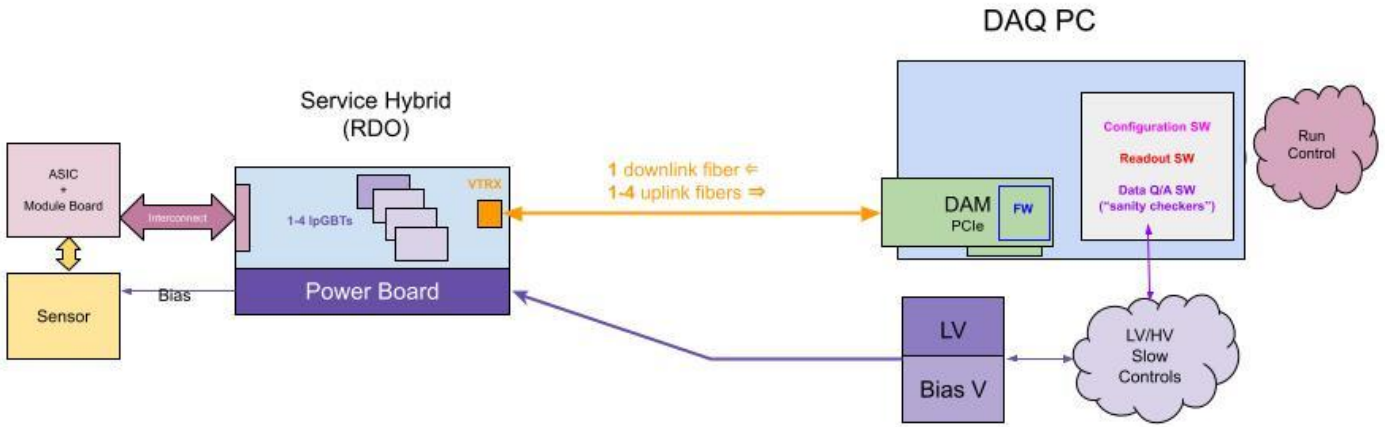
- TOF Readout Chain
  - as well as Roman Pots and friends
- ppRDO (“pre-prototype RDO”)
  - FPGA-based first version from FY24
- New lpGBT-based Service Hybrid (FY25)
  - Readout Board RB1
  - Power Board PB1
- Module Board

Readout Chain



ppRDO Completed

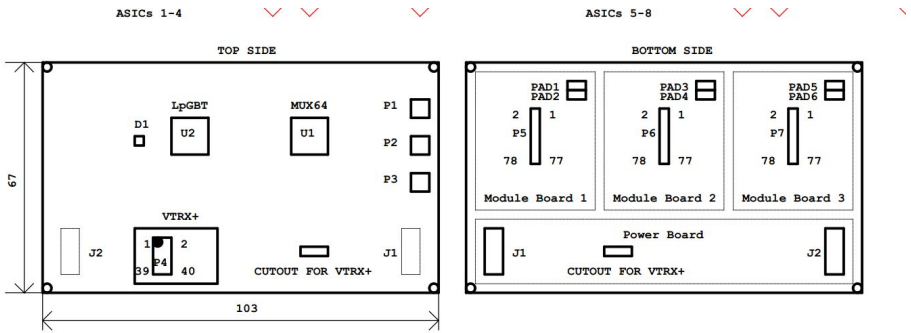
- FPGA-based Readout Board pre-Prototype
  - FPGA readout (Xilinx Artix+)
  - high-precision clock handling and routing
- 1 year project funded through FY24 eRD109
- 6 boards arrived and fully tested
  - checked with ETROC ASIC
- Excellent low jitter measured (Tim Camarda)
  - < 5ps
- Since TOF won't use FPGAs, ppRDO is not going to be continued but the boards we produced will be used for ASIC testing
  - FPGA; FMC connector; high-precision, low jitter, versatile clocking scheme; SFP fiber interface
- EICROC1 ASIC expected mid-2025!

lpGBT-based readout

- TOF decided to use lpGBT for its readout
  - together with VTRX+ fiber transceivers
- We need a newly designed Readout Board based on lpGBT & VTRX+
- We also need a sophisticated power distribution board which supplies power to the ASICs as well as the RDO
- Submitted a funding request for FY25 but got bumped to FY26 which is very late for us → this might cause the entire TOF Project to be delayed
- Discussed the situation with Fernando and decided to re-submit as a PED request, under his guidance
  - a preliminary PED request sent recently to Fernando
    - *"AC-LGAD Frontend Readout Chain Development Proposal"*
  - waiting for his comments…

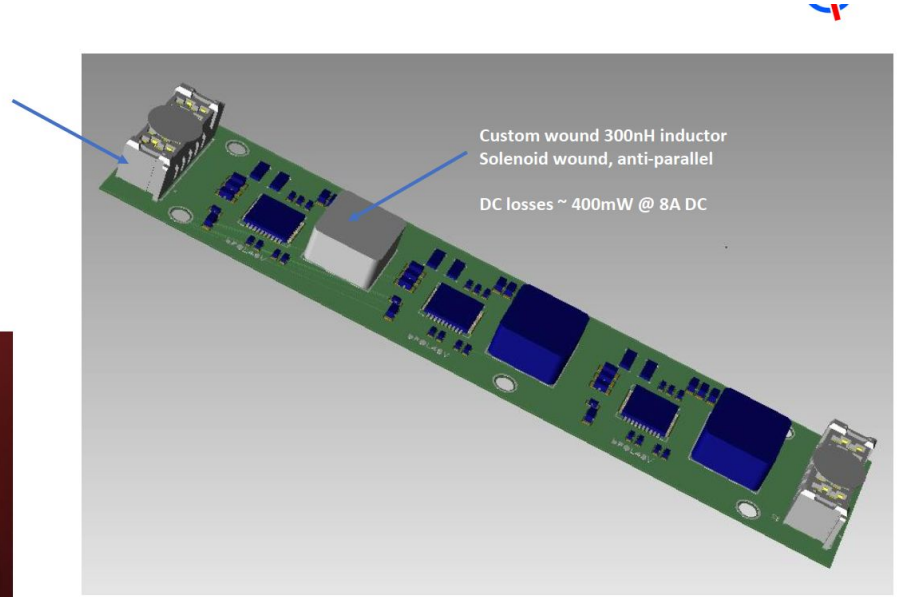
Readout Board RBv1 Prototype

- started schematics and layout of the RBv1 board
  - first version suited for FTOF: power & small dimensions
  - possibly also suited for Roman Pots
- main components
  - lpGBT, VTRX+, MUX64
  - connectors to ASIC module boards
- designed to readout 12 ASICs



Power Board Prototype (PBv1)

- requirements well understood, board design in progress (Tim Camarda)
- based on CERN bPOL48 DC/DC converters
- and commercial (but radiation tested and approved) LT3033
- PB1 will support 12 EICROC ASICs and 1 RB1 RDO



103mm x 22mm service hybrid power board

Module Board

- we are discussing the development of the ASIC+sensor package (“Module Board”)
- FTOF assumes a 2x2 ASIC “package”
  - each ASIC is the EICROC2 with 32x32 channels (1024 chs total)
- module board is 3.2 X 3.2 cm
- other detectors (BTOF, Roman Pots, etc) will be different
- we need more help from the TOF Group to address the technical details
  - and we need the ASIC layout… TBD

Conclusion

- FY25 prototyping plans well understood (and needed!)
- Waiting for the FY25 PED funding decision
  - currently stalled without funds
- Poised for EICROC1 ASIC testing using either ppRDO or commercial FPGA kits