OAK RIDGE National Laboratory

FTOF Overview

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U.S. DEPARTMENT OF ENERGY

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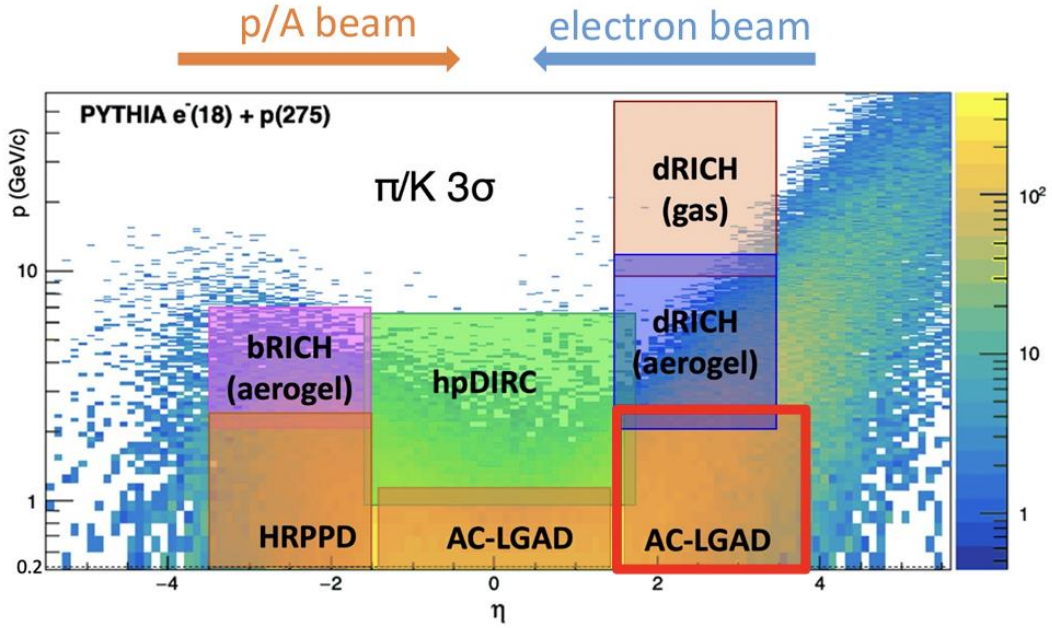
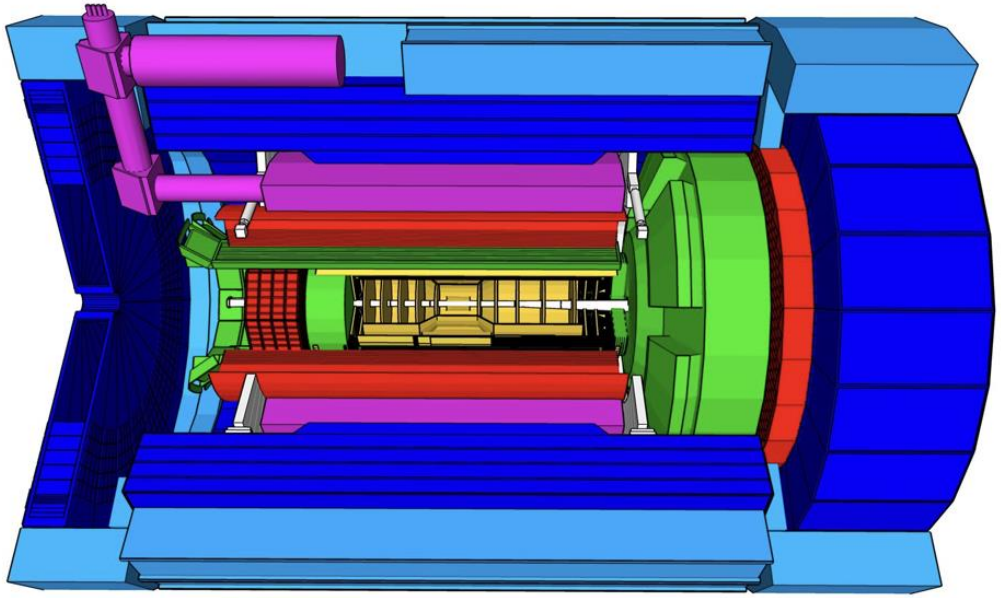
AC-LGADs TOF system for PID





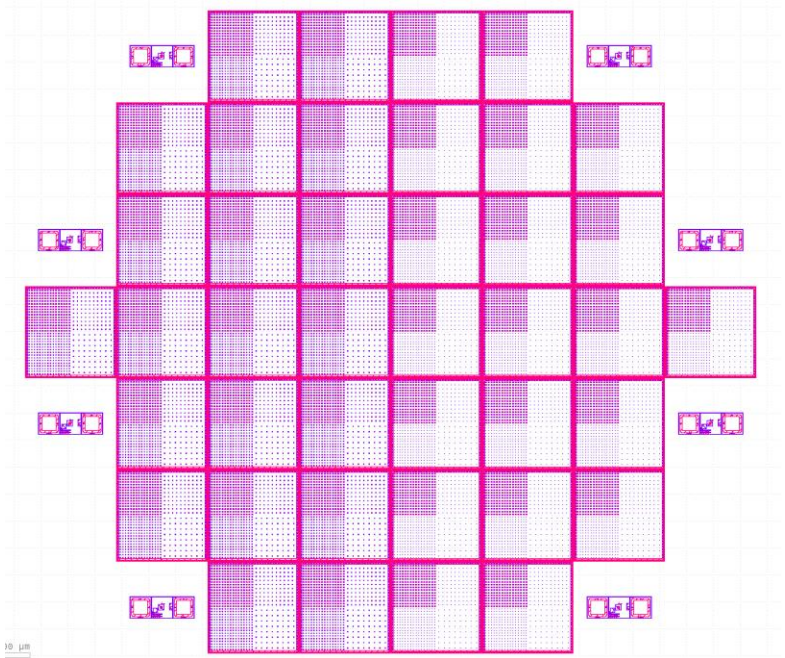
Latest envelope (link)

Detector	r (cm)	z (cm)	Momentum range for 3σ π/K separation
Barrel TOF	62<r<69.5	-117.5<z<171.5	0.2 < p_T < ~1.2 GeV
Forward TOF	10.5<r<60	168<z<175cm	0.2 < p < ~2.3 GeV

FTOF requirements and R&D progress

Current requirements (presented at FY23 EIC Project R&D - DAC Meeting)

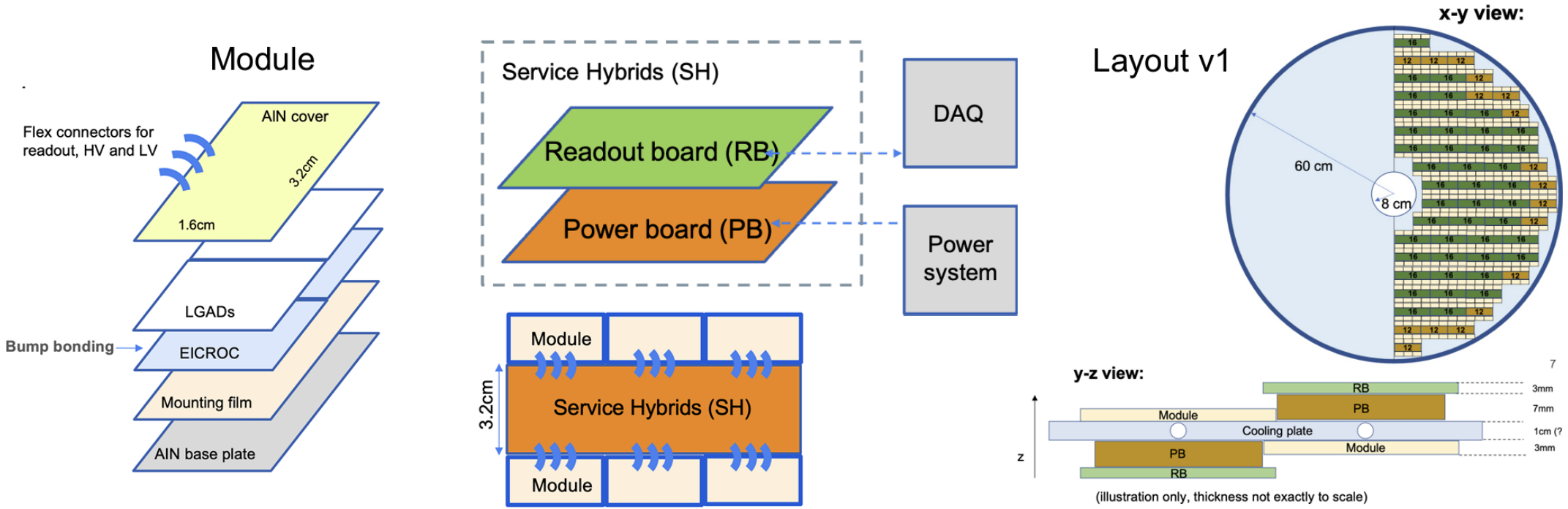
	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10	0.5*10	2.4M	30 → 35 ps	30 μm in $r \cdot \varphi$	0.01 X_0
Forward TOF	1.4	0.5*0.5	5.6M	25 ps	30 μm in x and y	0.08 → 0.025 X_0
B0 tracker	0.07	0.5*0.5	0.28M	30 ps	20 μm in x and y	0.01 → 0.05 X_0
RPs/OMD	0.14/0.08	0.5*0.5	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.



We are expecting soon the HPK sensor production with full size sensors allowing first test of bump-bonding, yield extraction and cost estimation

FTOF Building blocks

Initial FTOF layout design from the Jan. collaboration meeting



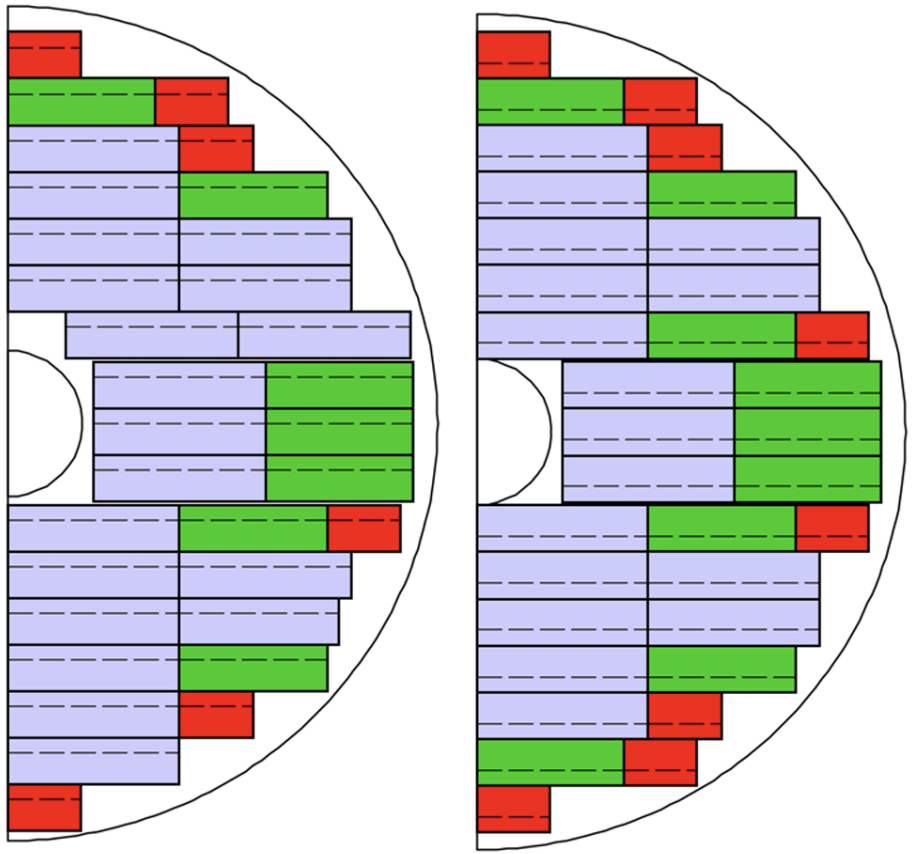
Continue refining the design in light of ongoing SH and module prototyping efforts

- Each SH servicing up to 32 ASICs (previously 16)
- Reduced envelope in z requires us to be more cautious with the layout design

Updated layout

FTOF Layout (x-y view): **v09272024**

Row	modules	RB3	RB6	RB7	All RBs
1	3	1	0	0	1
2	9	1	1	0	2
3	10	1	0	1	2
4	13	0	1	1	2
5	14	0	0	2	2
6	14	0	0	2	2
7	14	0	1	1	2
8	13	0	1	1	2
9	13	0	1	1	2
10	13	0	1	1	2
11	16	1	1	1	3
12	14	0	0	2	2
13	14	0	0	2	2
14	13	0	1	1	2
15	10	1	0	1	2
16	7	0	0	1	1
17	3	1	0	0	1
Sum	**193**	6	8	18	**32**



Row	modules	RB3	RB6	RB7	All RBs
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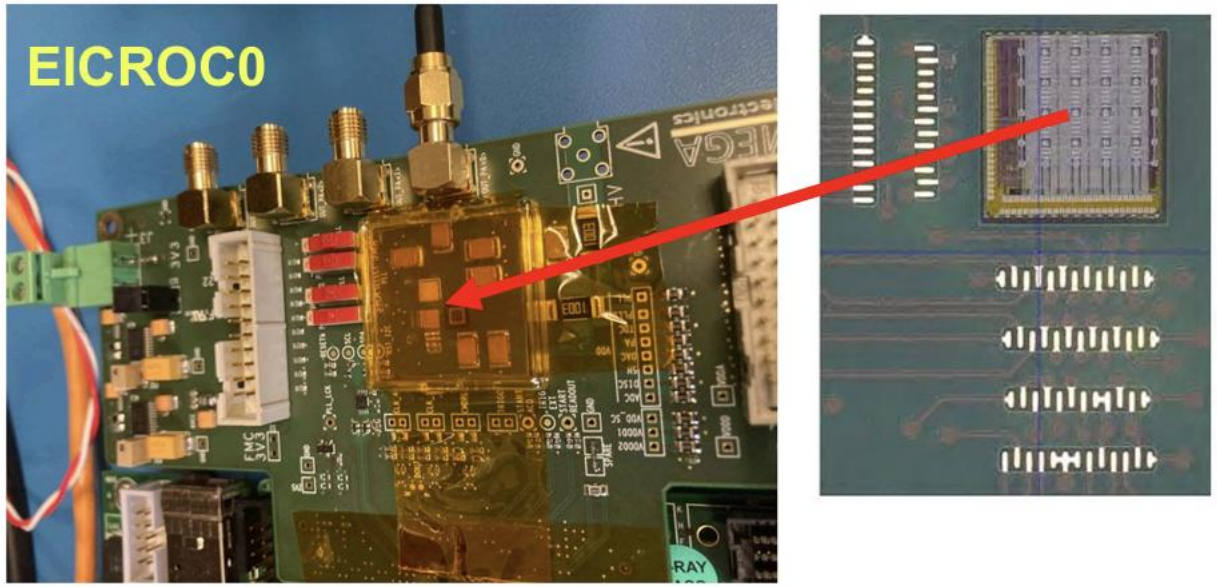
5	14	0	0	2	2
6	14	0	0	2	2
7	16	1	1	1	3
8	13	0	1	1	2
9	13	0	1	1	2
10	13	0	1	1	2
11	16	1	1	1	3
12	14	0	0	2	2
13	14	0	0	2	2
14	13	0	1	1	2
15	10	1	0	1	2
16	9	1	1	0	2
17	3	1	0	0	1
Sum	**197**	8	9	17	**34**

Total number of modules: (193+197)*2 = **780**
Total number of service hybrids: (32+34)*2 = **132**

FTOF ASICs - EICROC

ASIC requirements:

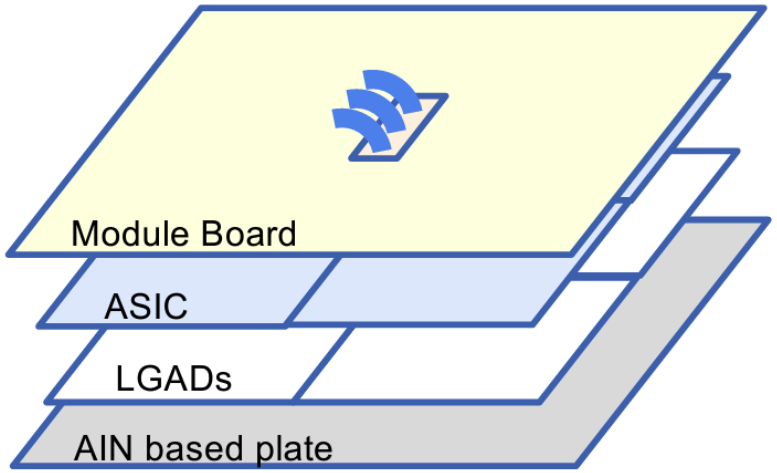
- **Pixel size: 0.5x0.5 mm2**
- **Low jitter: <20ps**
- **Low power consumption: 1mW/channel**

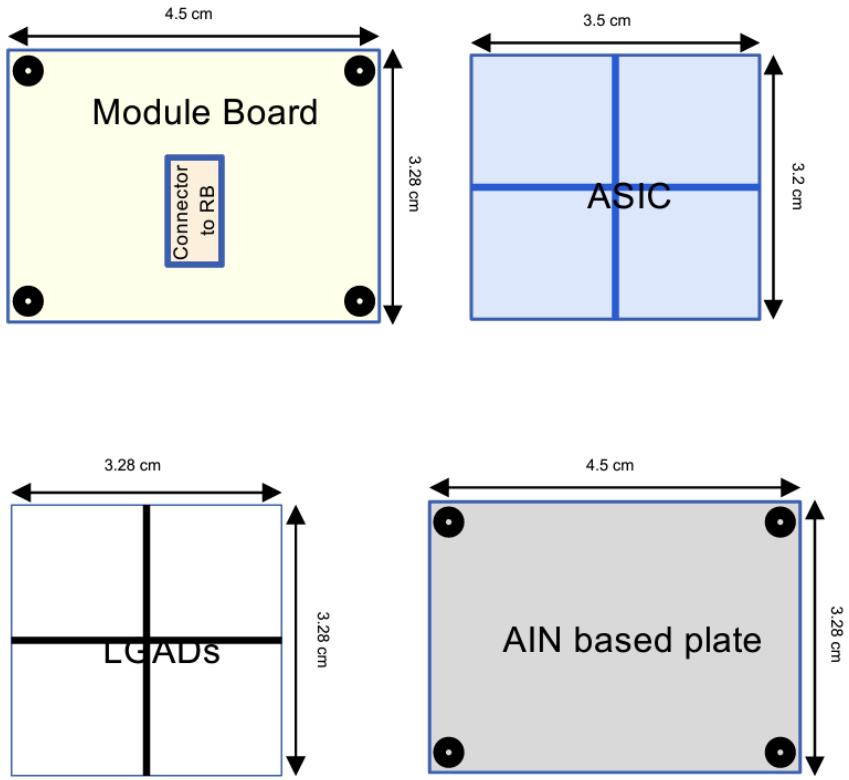


Chip	date	Techno	size	Analog	Digital	goal
EICROC0	Jun 2023	130n	4x4	Conservative	Simple	Study sensor
EICROC0A/B	beg 2025	130n	4x4	Low power	same	Study analog
EICROC1	beg 2025	130n	32x32	Conservative	Same	Study power distribution
EICROC0_65n	end 2025	65n	4x4	final	Simple	Study analog in 65n
EICROC2	End 2026	?	32x32	Low power	Final	First final prototype

FTOF Modules

- 4 AC-LGADs sensor per module
- Each sensor: 32x32 pixels and 1.6x1.6 cm^2



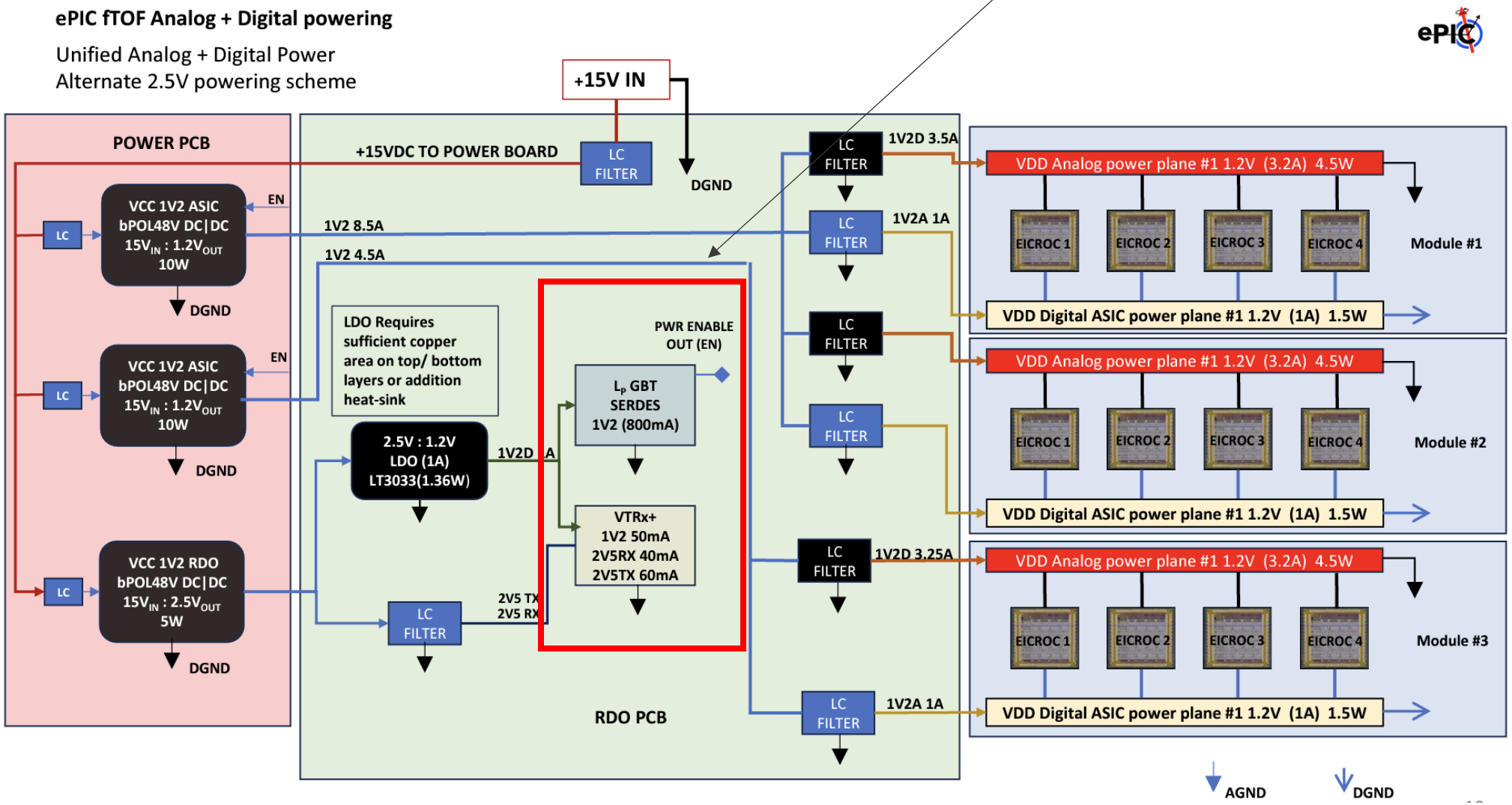


More realistic dimensions considering guard rings, mounting holes etc.

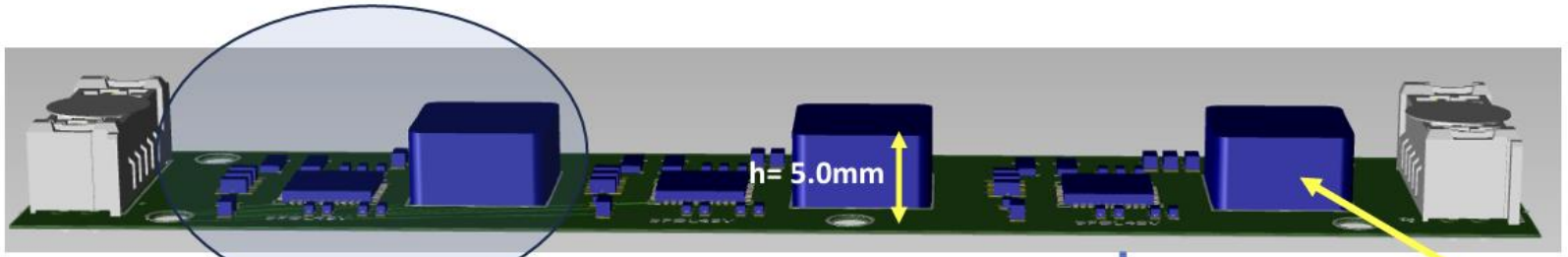
LGAD Cooling by direct contact with stave!!!!

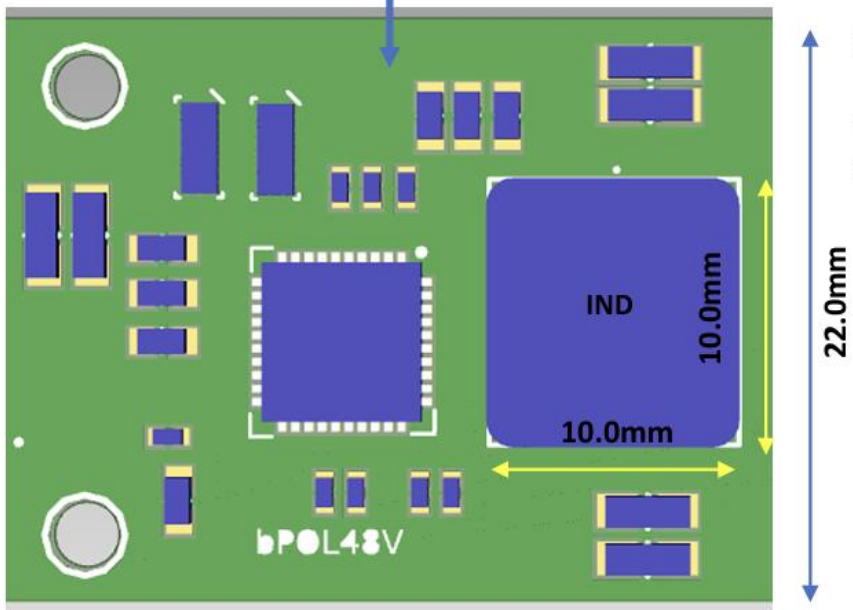
RDO and Powering board

lpGBT and VTRx+ based due to envelope



bPOL48V power regulator board: 30W total (10W/ ch)
1.2V_{OUT} @ 8A





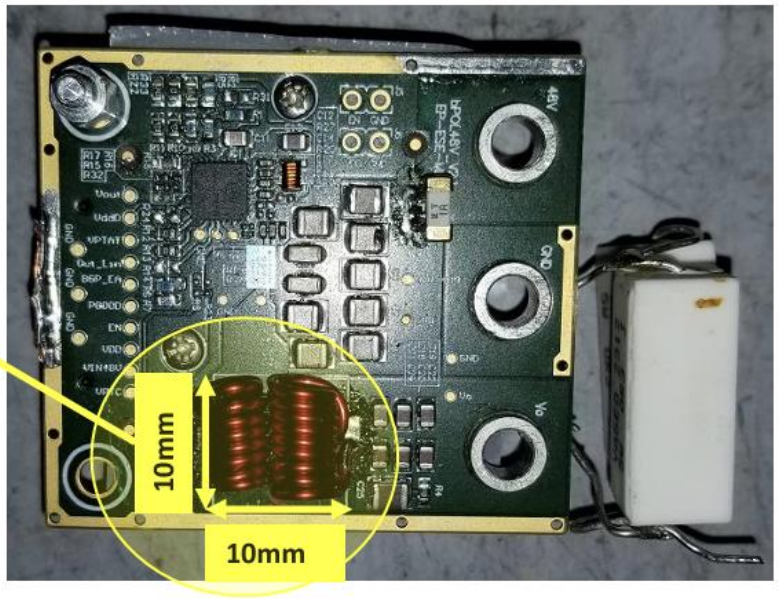
22.0mm

31.0mm

6.82cm^2 circuit footprint size

Proposed fTOF Power Board shown as example

Bottom of PCB will have thermal copper plane attached to liquid cooling plate



CERN bPOL48V evaluation board
Modified for 1.2V_{OUT} 8A, ~10W
Heat-sink attached w/ thermal pad at bottom

- Custom switching inductor: 300nH, 8A air-core, solenoid wound in anti-parallel
- Inductor dimensions (mm) lxWxH => 10 x 10 x 5 => allow ~ 8mm clearance height
- PCB board height: 2.0mm to 2.4mm
- 2.0oZ outer copper

Tim Camarda for ePIC project, OCT 2024

Channel counts and power budget

	Counts
Modules	736
Sensors/ASICs	2944
Data fiber pairs	128
LV cable pairs	128
HV cable pairs	128

	Power
Sensors	0.3kW
EICROC	2.9kW
DC-DC	2kW
FPGAs	0.5kW
Total	5.7kW

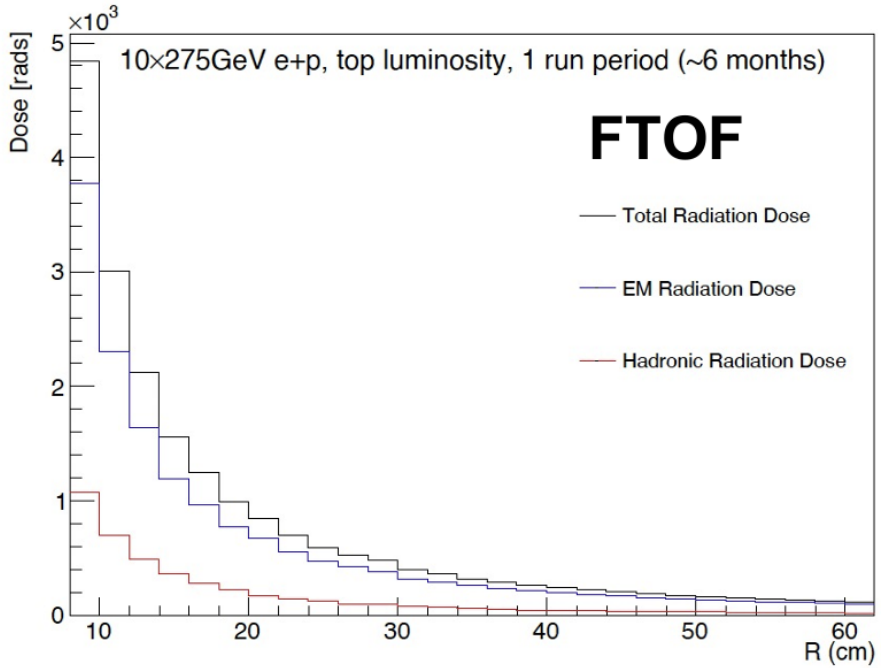
Assuming a single value of HV for each SH

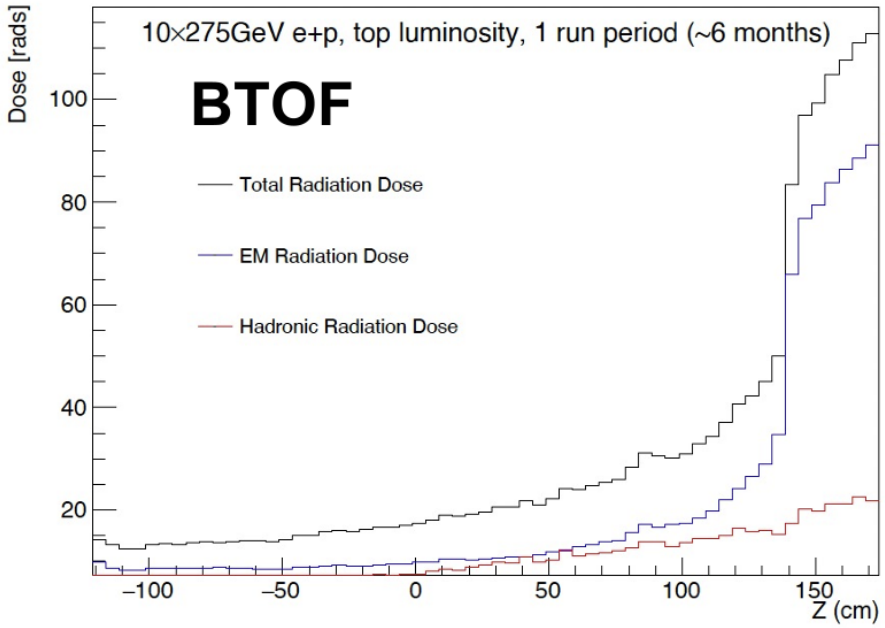
Channels and power budget reduced from v1 by ~30% mainly because of the reduced envelope and # of SHs

FTOF radiation dose

Signal+beam gas (updated)

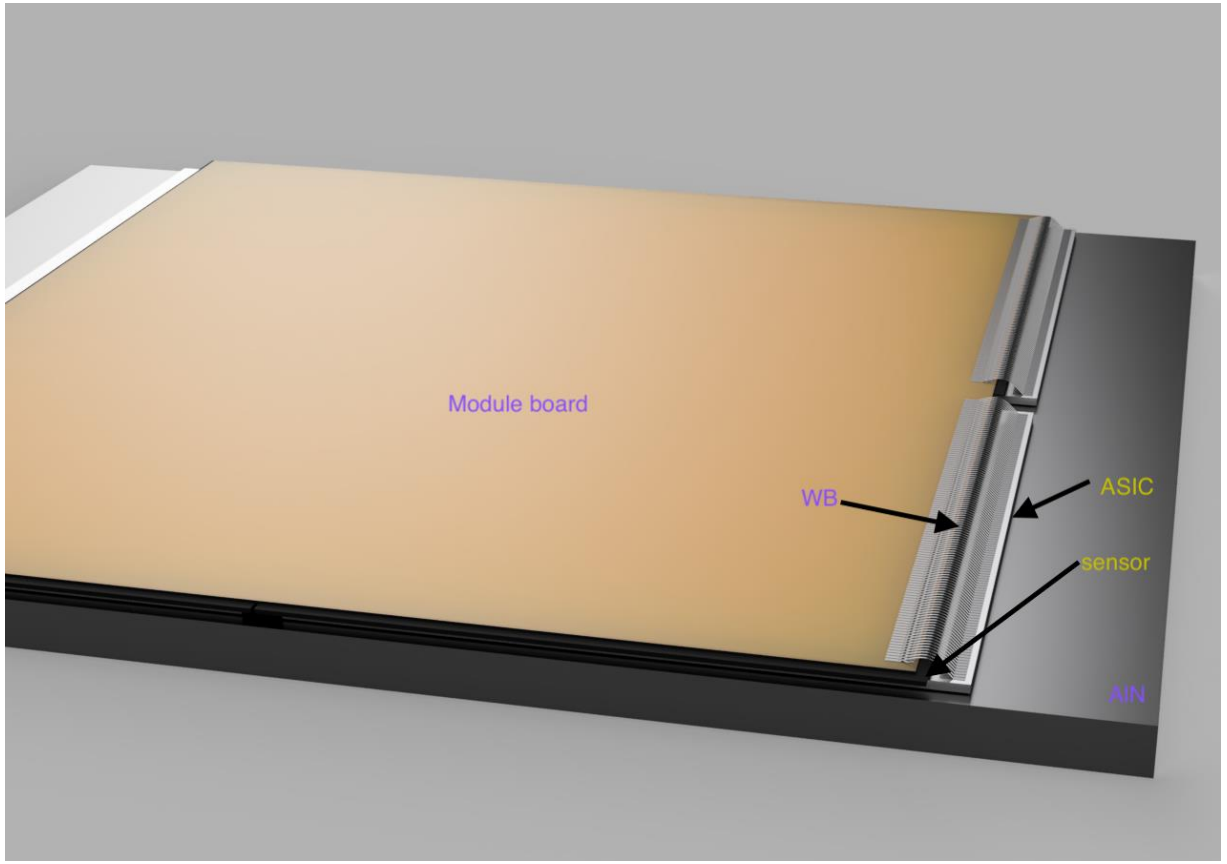
Xiao Huang

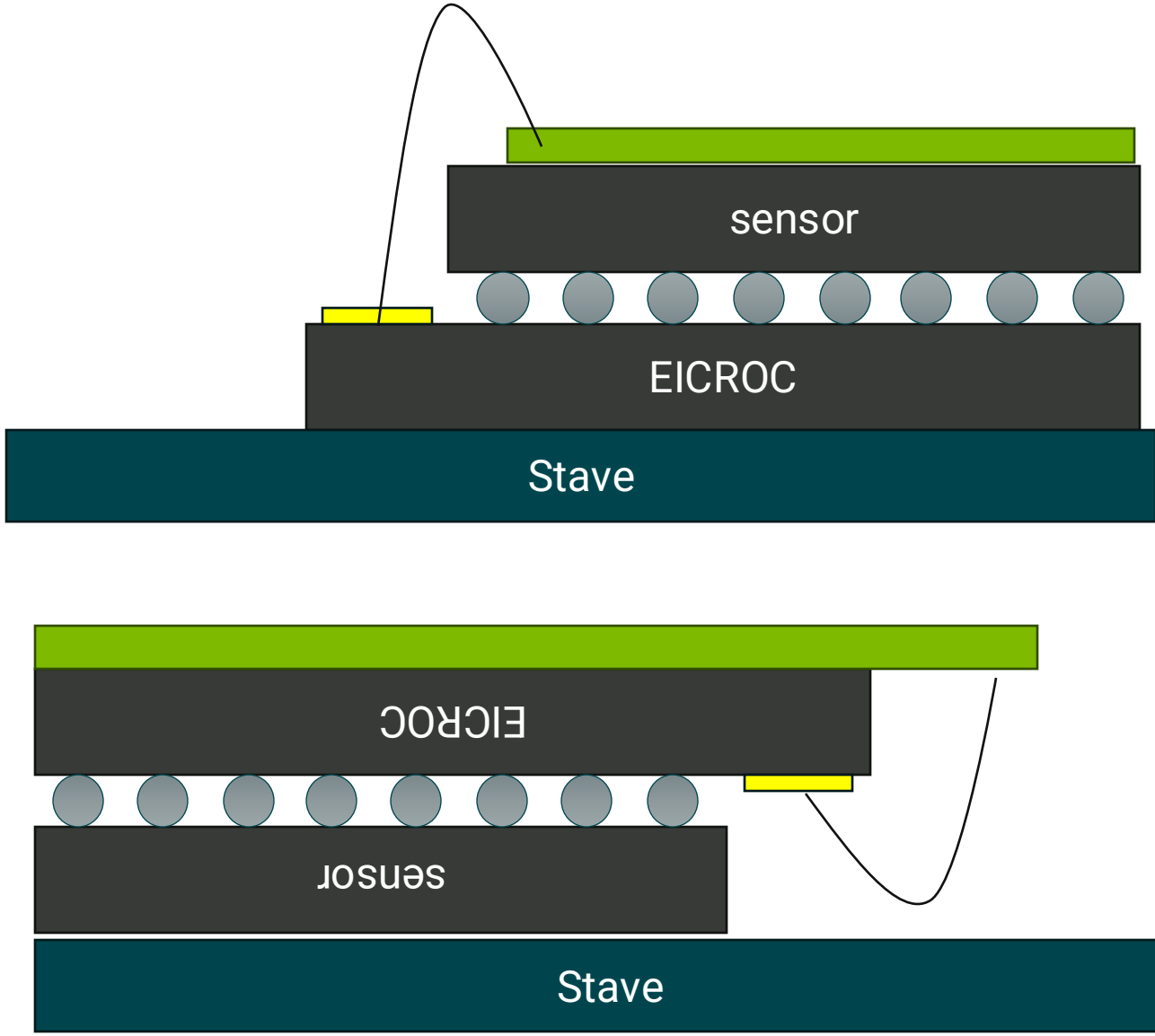




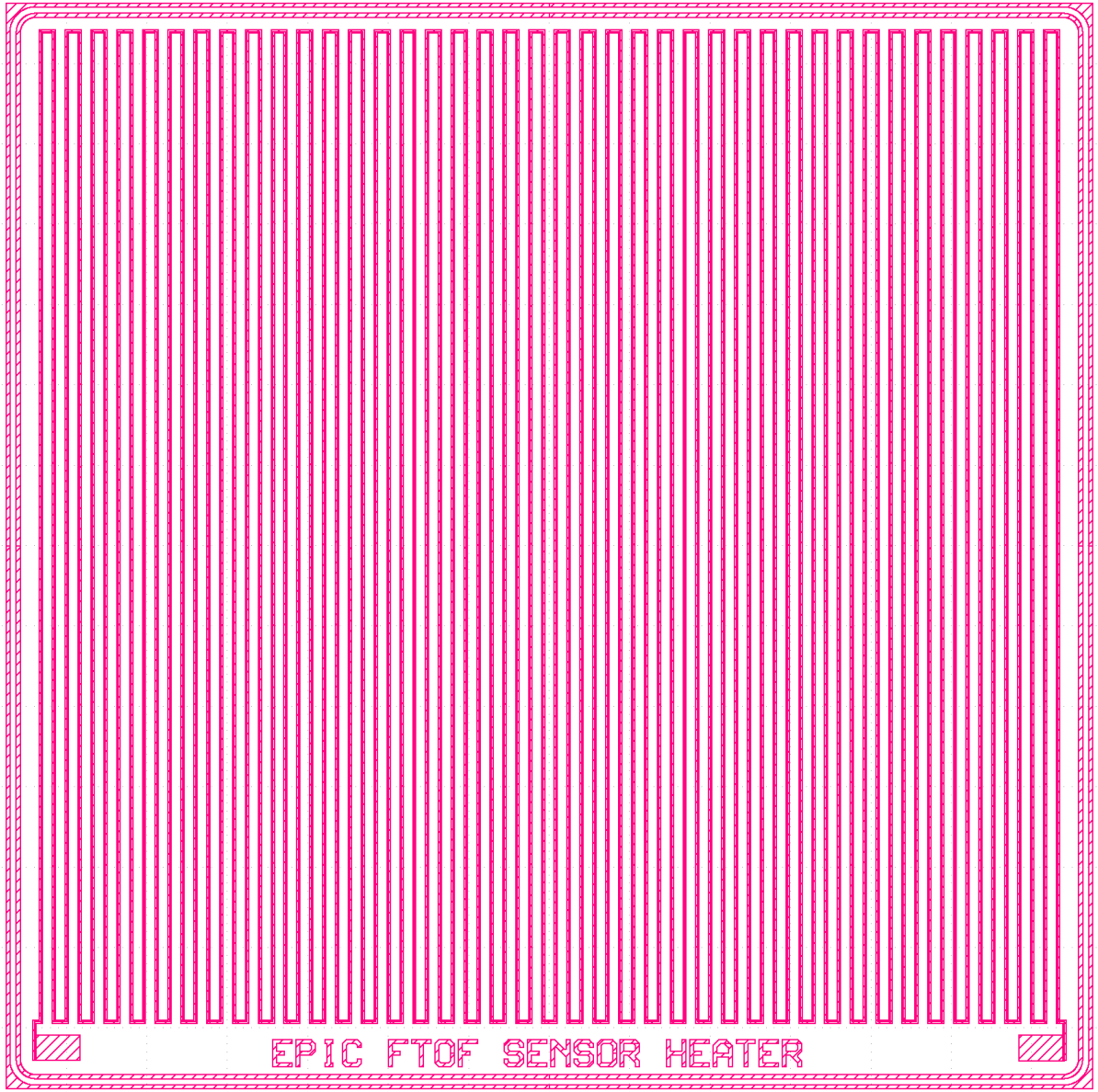
Assuming 10 years of operation and a safety factor of 2, the most inner part of FTOF expects **~ 100 kRad**

The Module stack problem





Thermal mock up for integration tests



We have designed a heater structure than can be used for flip-chipping and thermo-mechanical test on stave while waiting for ASIC and sensors to come to maturity

Conclusion and outlook

Forward TOF design has gain maturity in the last year

- Module layout, RDO and power board design progressing
- EICROC1 design mature and soon will provide full size ASIC for bonding and integration tests
- Integrating VTRx+ and lpGBT allow to fit in reduced envelope at our disposition

Very important discussion on integration , thermal management, Module design need to be addressed to reach good design maturity and achieve demonstration of the system on a slice.