WP3
Electrical Interfaces

20250124

M.Borri

on behalf of WP3

Science and Technology Facilities Council

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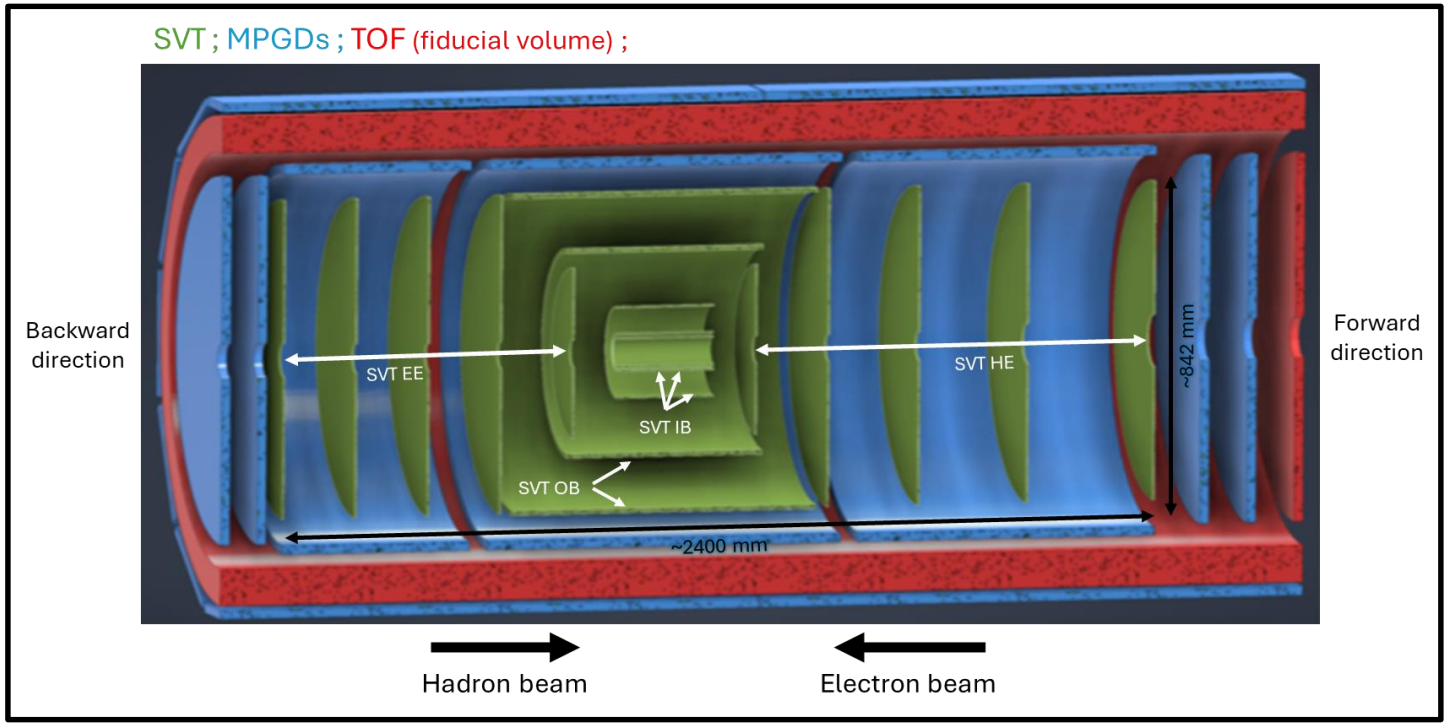
Outline



- WP3 general updates
- Update on Inner barrel
- Update on Outer Barrel
- Update on Disks
- Conclusion

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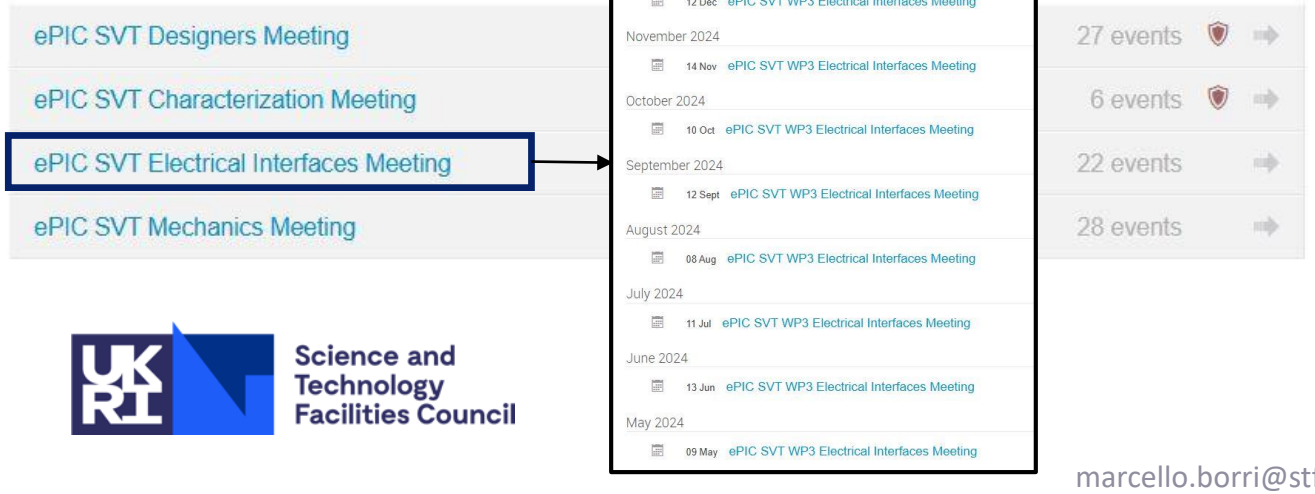
General updates 1

- Zhenyu Ye appointed as co-coordinator

- Monthly meetings since 05/2024
  - IT: Trieste
  - US: BNL, LANL, LBNL
  - UK: DL, Oxford
  - UA: LTU



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WP3: Electrical Interfaces
Coordinators: Marcello Borri, TBC ← Zhenyu Ye (LBNL)

V1.7

WP3: Electrical Interfaces		
3.1	Electrical interfaces IB (L0—2)	
3.1.1		Definition of specifications for FPCs & electrical interconnection
3.1.2		Design & supplier evaluation
3.1.3		Prototyping & testing of module, FPCs & electrical interconnection
3.1.4		Iterative improvements of FPC design & electrical interconnection
3.1.5		FPC design complete & electrical interconnection validated
3.1.6		Pre-production of FPCs for system test, including QC
3.1.7		Production of FPCs for production detector, including QC
3.2	OB HIC (L3--4)	
3.2.1		Definition of specifications for module, FPCs & electrical interconnection
3.2.2		Design & supplier evaluation
3.2.3		Prototyping & testing of module, FPCs & electrical interconnection
3.2.4		Iterative improvements of module design, FPC & electrical interconnection
3.2.5		OB module design complete
3.2.6		Pre-production of FPC for system test, including QC
3.2.7		Production of FPCs for detector grade modules, including QC
3.3	Disks HIC (ED0-4, HD0-4)	
3.3.1		Definition of specifications for module, FPCs & electrical interconnection & back plate
3.3.2		Design & supplier evaluation
3.3.3		Prototyping & testing of module, FPC, electrical interconnection & back plate
3.3.4		Iterative improvements of module design, FPC, electrical interconnection & back plate
3.3.5		Disk module design complete
3.3.6		Pre-production of FPCs for system test, including QC
3.3.7		Production of detector grade FPCs, including QC

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General updates 2

- WP3 contribution to PDR:
  - Part of Chap.8, Experimental Systems:
    - Complete
  - Appendix:
    - in progress

Electron Ion Collider DRAFT
EIC PDR
Preliminary Design Report December 9, 2024

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Inner barrel

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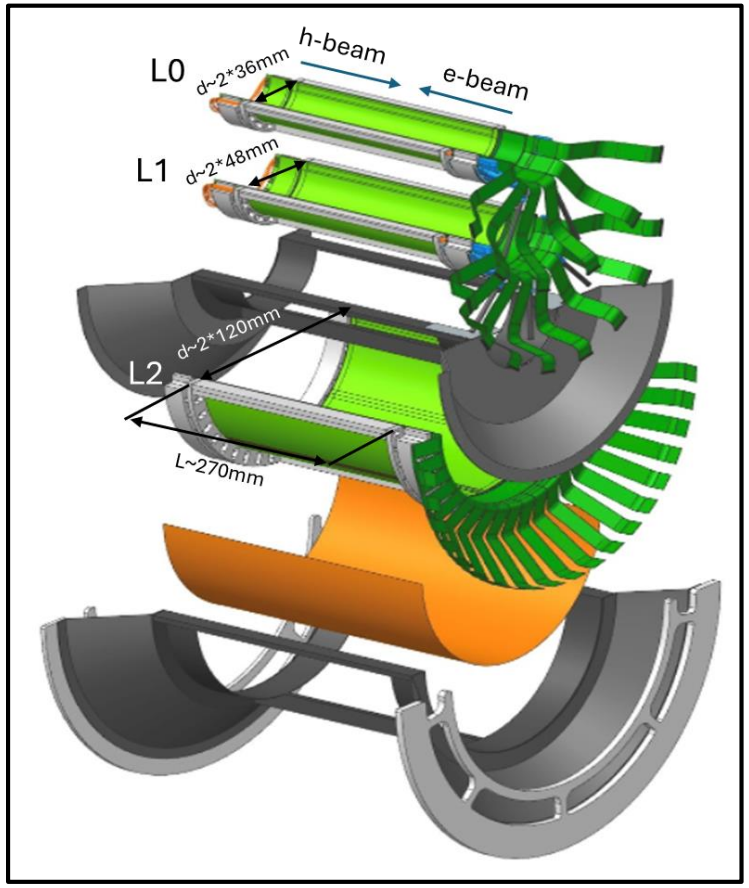
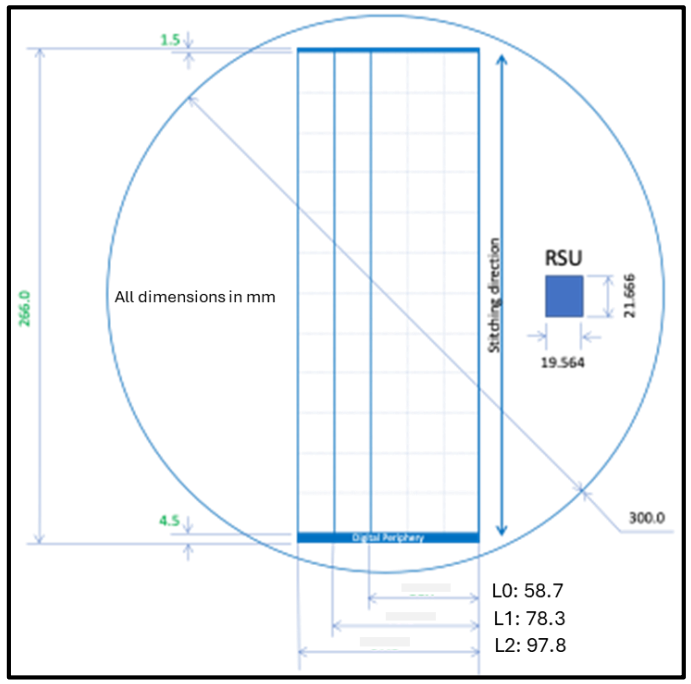
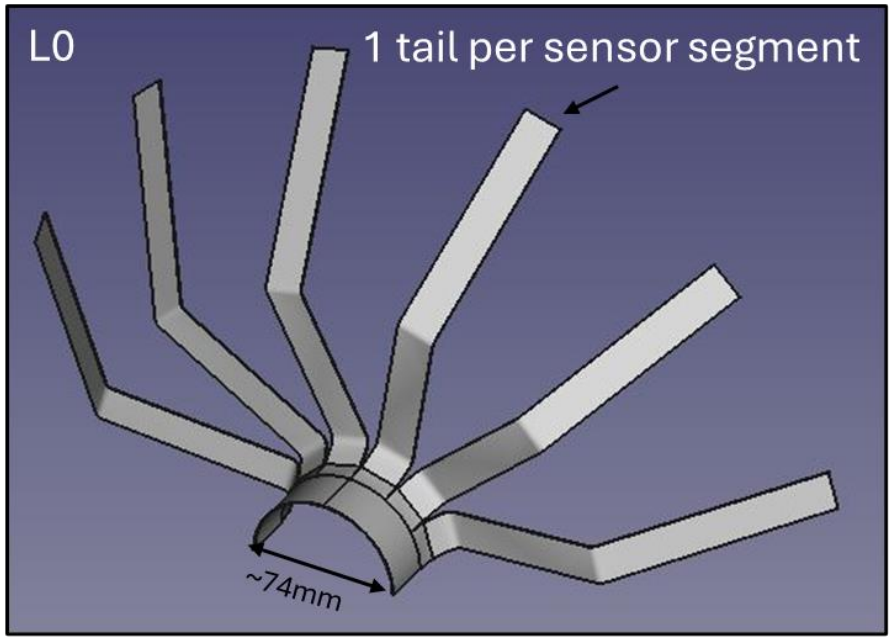
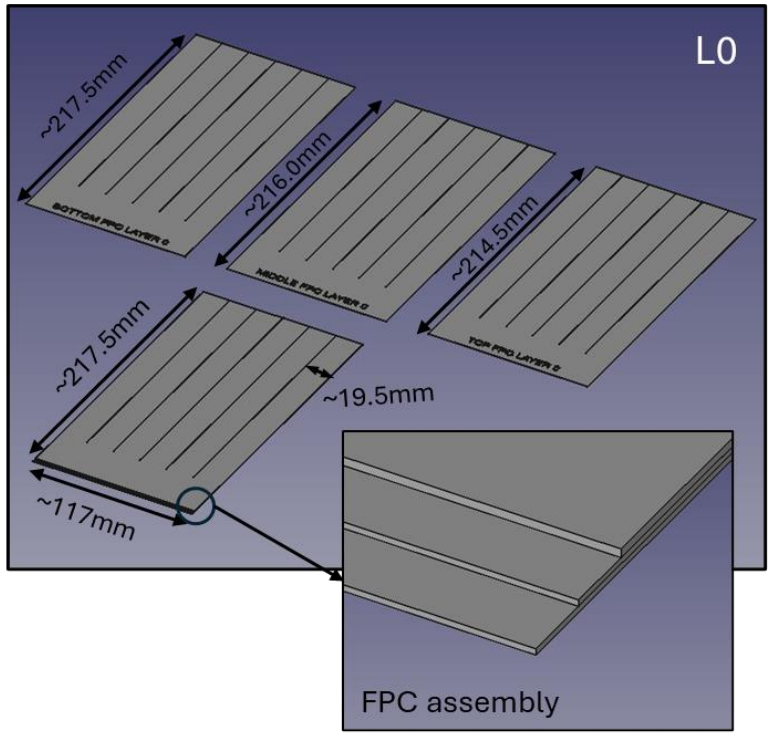
Overview





- Initial activity on the Forward-side FPCs:
  - Mainly L0&L1;
- IB FPCs (forward-side):
  - Assembly of 3 FPCs (2 layers each);
  - FPC length ~ 22cm;
  - 1 tail per sensor segment;
- Design of mechanical mock-ups the L0&L1 FPC;
  - STP files provided by INFN Padova;
  - Ported into Allegro;
  - Reviewed, and now waiting for final approval from INFN Padova.
  - Then procure in Cu technology (cheaper faster)





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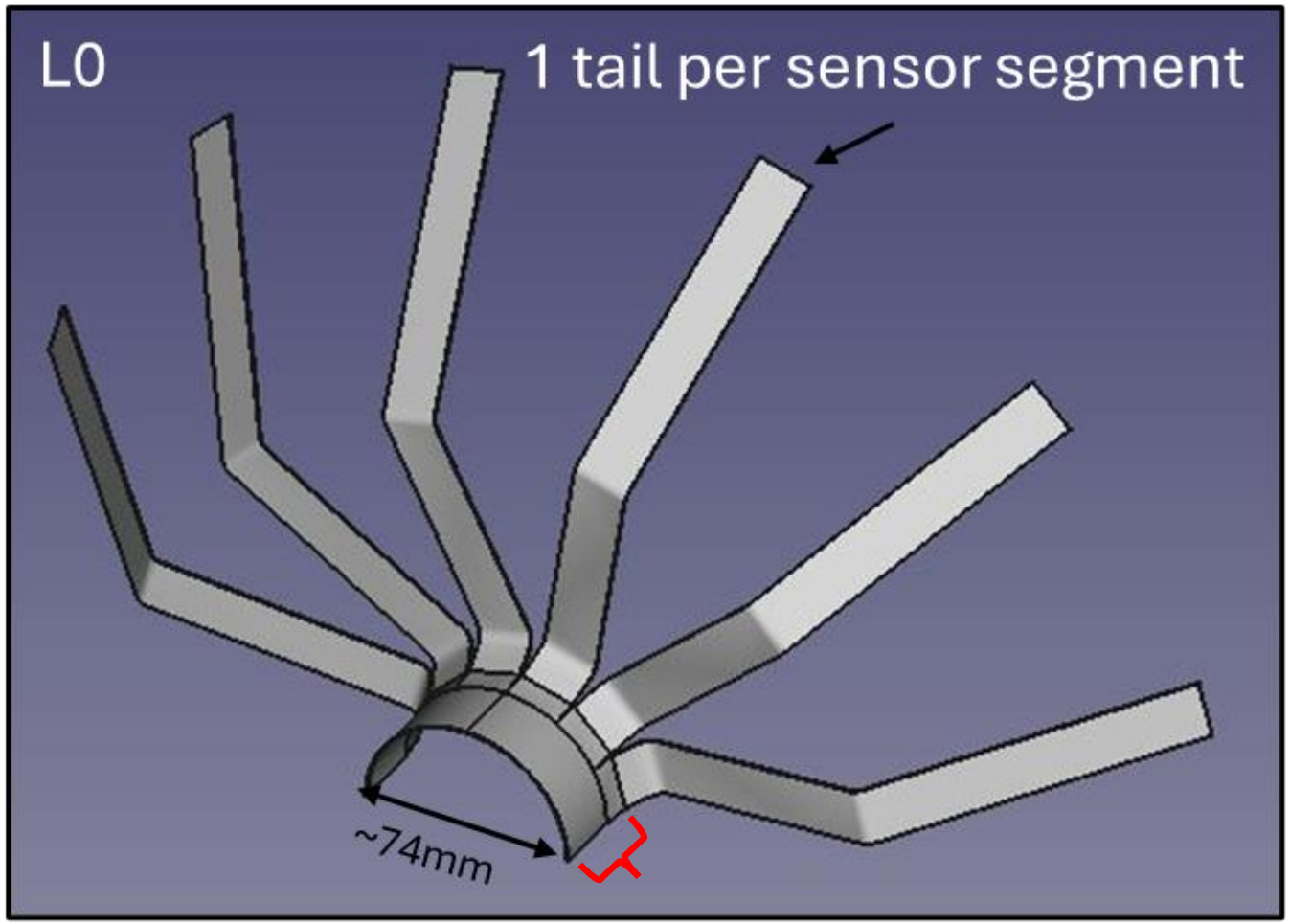
Forward side: detail



Inactive region for SVT, but **active region** for EPIC.
To keep material budget low.

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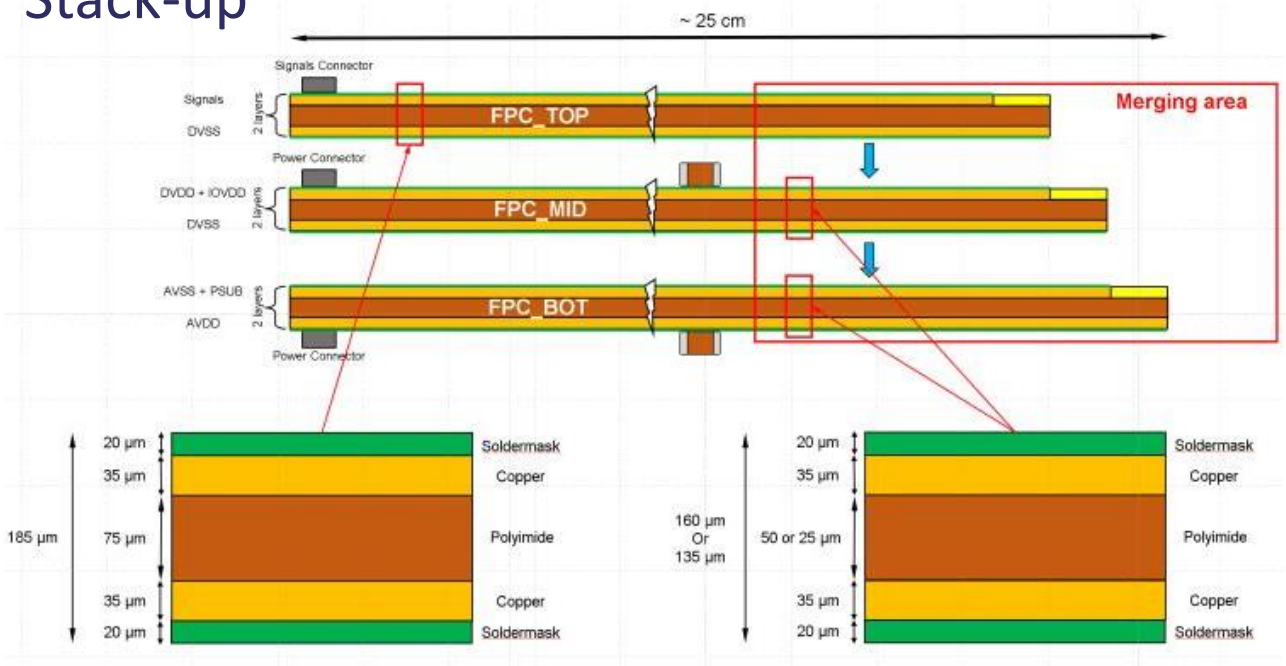
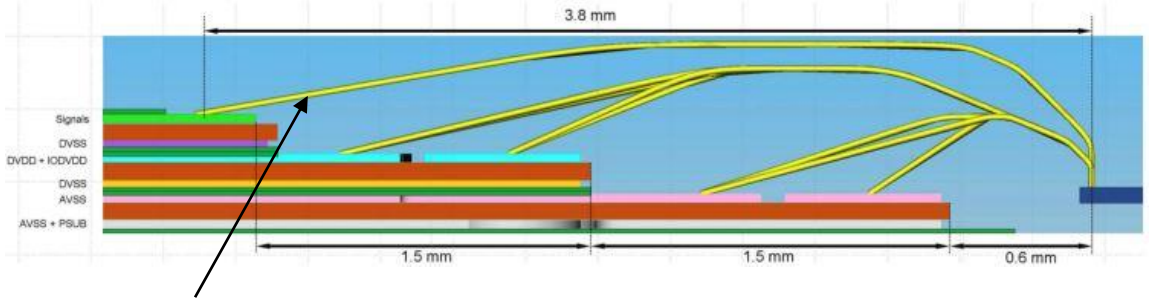
Furter details from ITS3 TDR

Stack-up



Wire-bonds profile



The longest wire bonds include high speed data (up to 10Gb/s)

Note:
ALICE ITS3 originally planned to manufacture this FPCs in Cu technology, now planning to do it Al technology?

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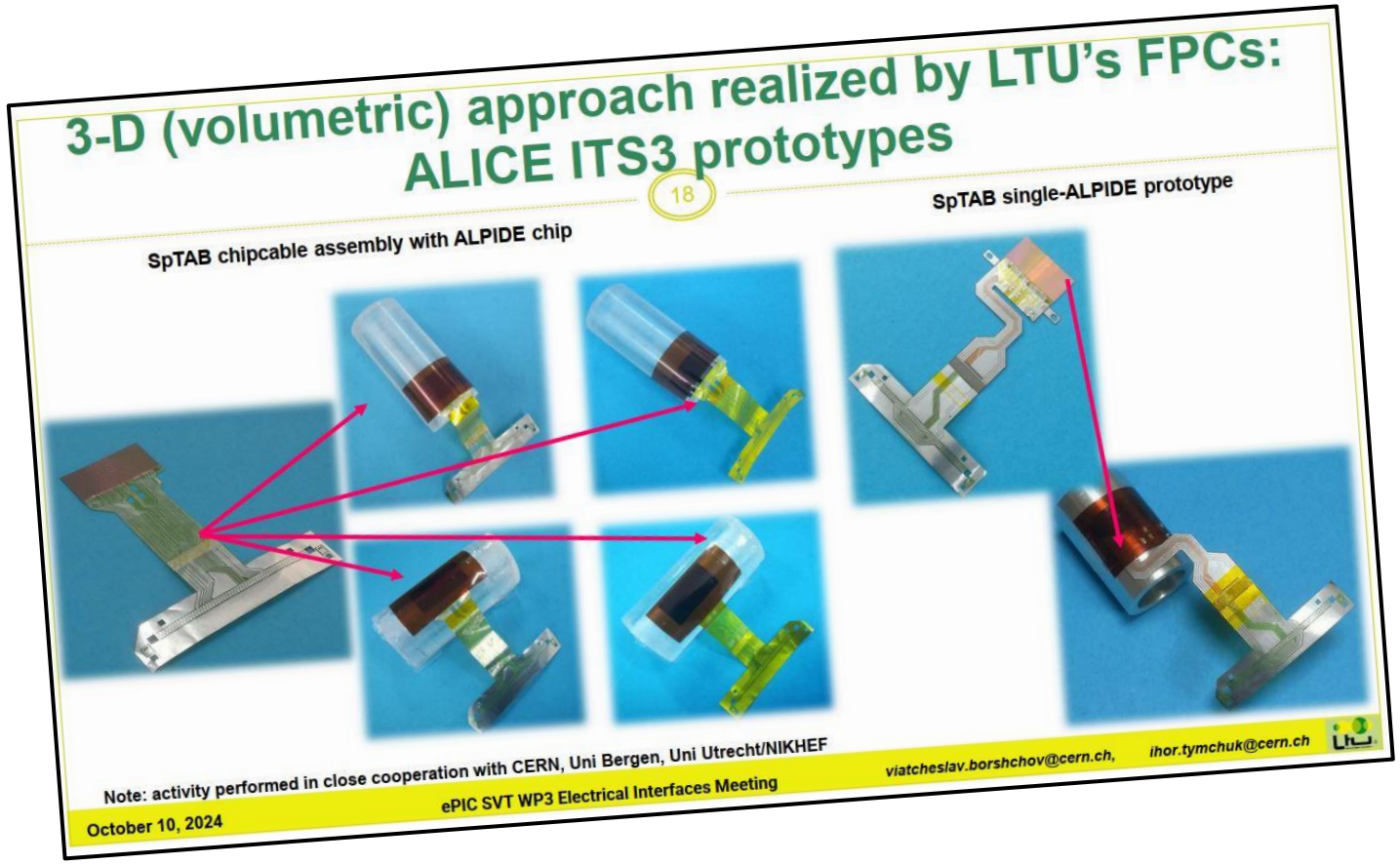
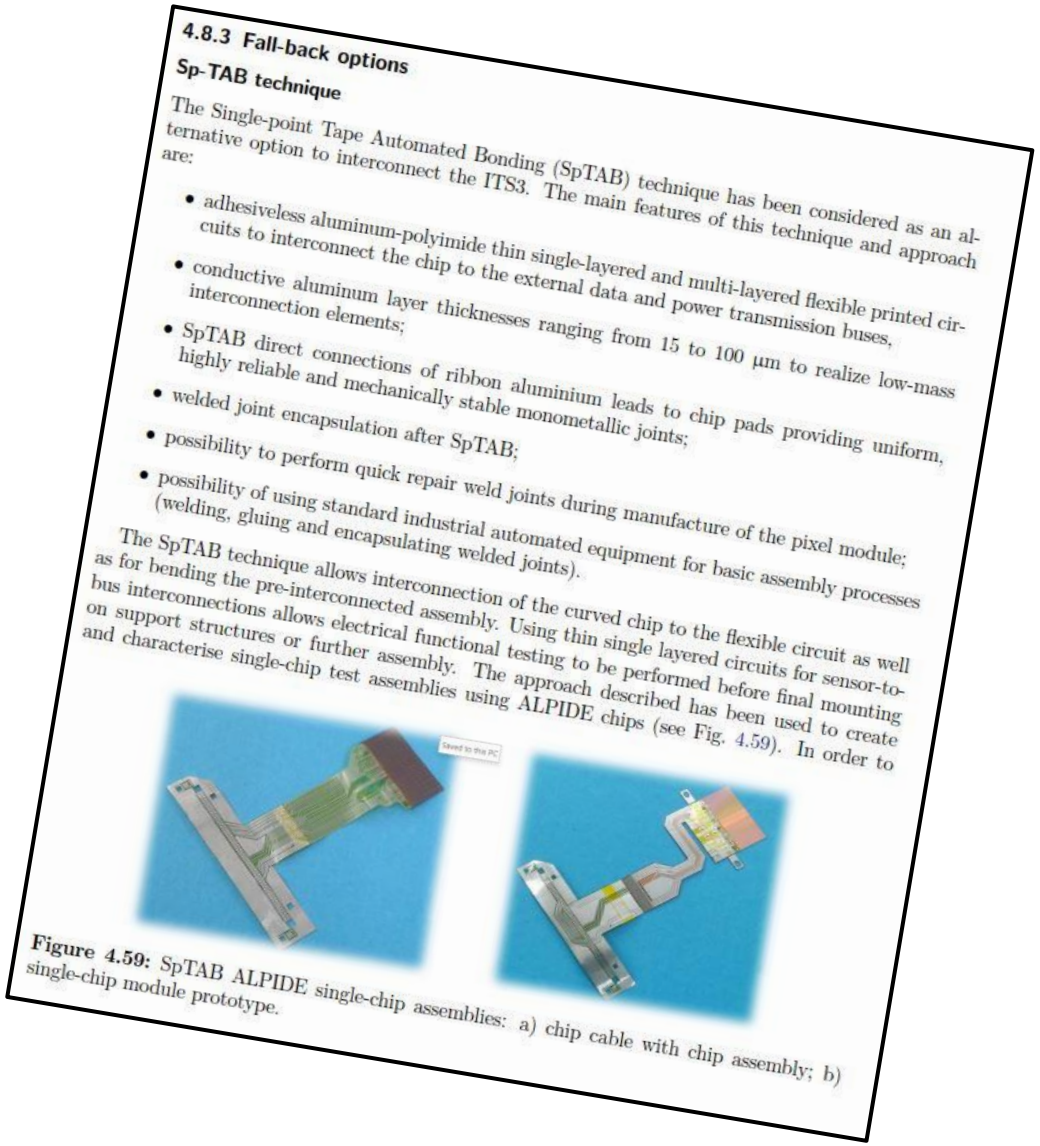
LTU contribution to ITS3





4.8.3 Fall-back options

Sp-TAB technique

The Single-point Tape Automated Bonding (SpTAB) technique has been considered as an alternative option to interconnect the ITS3. The main features of this technique and approach are:

- adhesiveless aluminum-polyimide thin single-layered and multi-layered flexible printed circuits to interconnect the chip to the external data and power transmission buses,
- conductive aluminum layer thicknesses ranging from 15 to 100 µm to realize low-mass interconnection elements;
- SpTAB direct connections of ribbon aluminium leads to chip pads providing uniform, highly reliable and mechanically stable monometallic joints;
- welded joint encapsulation after SpTAB;
- possibility to perform quick repair weld joints during manufacture of the pixel module;
- possibility of using standard industrial automated equipment for basic assembly processes (welding, gluing and encapsulating welded joints).

The SpTAB technique allows interconnection of the curved chip to the flexible circuit as well as for bending the pre-interconnected assembly. Using thin single layered circuits for sensor-to-bus interconnections allows electrical functional testing to be performed before final mounting on support structures or further assembly. The approach described has been used to create and characterise single-chip test assemblies using ALPIDE chips (see Fig. 4.59). In order to

Figure 4.59: SpTAB ALPIDE single-chip assemblies: a) chip cable with chip assembly; b) single-chip module prototype.

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LTU presented at the WP3 meeting their idea for FPCs proposed for the ALICE ITS3

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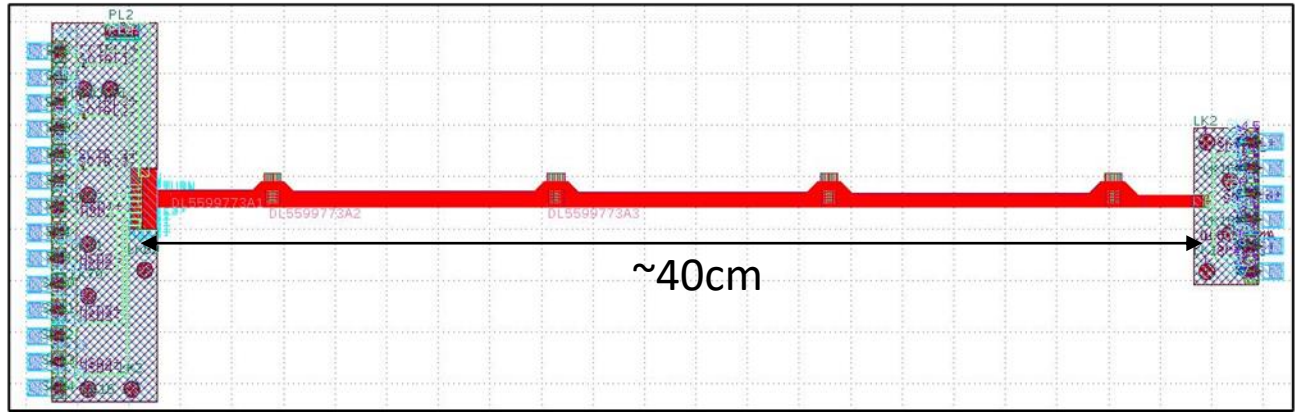
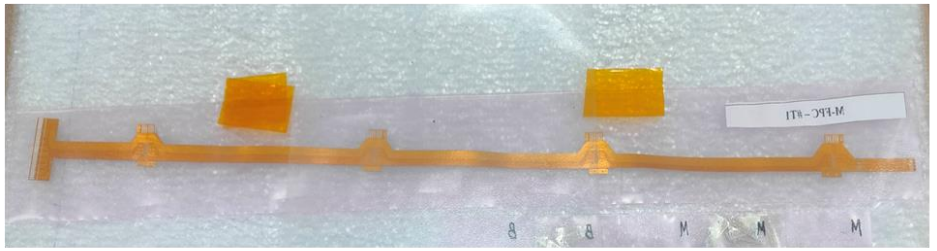
Testing FPCs for IB

- Planning to send to INFN Trieste a stand-alone M-FPC & interface cards.
- INFN Trieste will test signal propagation as a function of bending radii.
- To procure ad-hoc FPGA development board to perform these tests.

Sketch of the main FPC (M-FPC) to interconnected to interface cards





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Next steps:

- To clarify/define a target supplier: LTU(baseline) or CERN?
- To design an FPC with representative length to test signal propagation with selected supplier;
- To practice interconnection related to selected supplier;

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Outer barrel

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Low TRL OB L4 prototypes: time-line

- Defined requirements:
  - 18/03/2024
- Design review:
  - 16/05/2024
- Prototypes delivery:
  - 08/10/2024
- Testing:
  - To assemble to interface cards;
  - To distribute and test;

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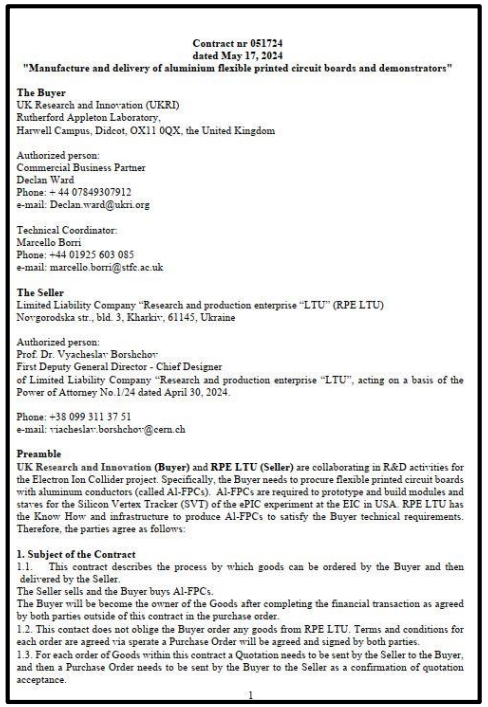
- Issue so far:
  - RPE LTU customer contract ☑

Administrative issue



Contract nr 051724
dated May 17, 2024
"Manufacture and delivery of aluminium flexible printed circuit boards and demonstrators"

The Buyer
UK Research and Innovation (UKRI)
Rutherford Appleton Laboratory,
Harwell Campus, Didcot, OX11 0QX, the United Kingdom

Authorized person:
Commercial Business Partner
Declan Ward
Phone: + 44 07849307912
e-mail: Declan.ward@ukri.org

Technical Coordinator:
Marcello Borri
Phone: +44 01925 603 085
e-mail: marcello.borri@stfc.ac.uk

The Seller
Limited Liability Company "Research and production enterprise "LTU" (RPE LTU)
Novgorodska str., bld. 3, Kharkiv, 61145, Ukraine

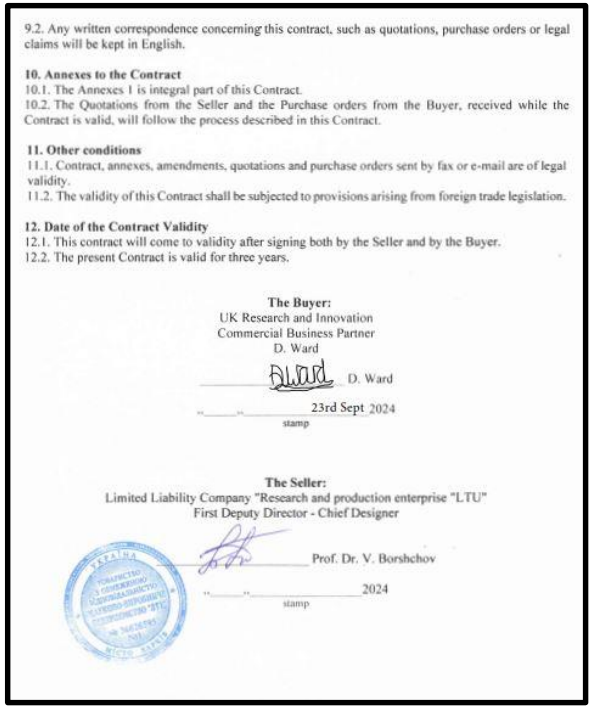
Authorized person:
Prof. Dr. Vyacheslav Borshchov
First Deputy General Director - Chief Designer
of Limited Liability Company "Research and production enterprise "LTU", acting on a basis of the Power of Attorney No.1/24 dated April 30, 2024.

Phone: +38 099 311 37 51
e-mail: viacheslav.borshchov@cern.ch

Preamble
UK Research and Innovation (Buyer) and **RPE LTU (Seller)** are collaborating in R&D activities for the Electron Ion Collider project. Specifically, the Buyer needs to procure flexible printed circuit boards with aluminum conductors (called Al-FPCs). Al-FPCs are required to prototype and build modules and staves for the Silicon Vertex Tracker (SVT) of the ePIC experiment at the EIC in USA. RPE LTU has the Know How and infrastructure to produce Al-FPCs to satisfy the Buyer technical requirements. Therefore, the parties agree as follows:

1. Subject of the Contract
1.1. This contract describes the process by which goods can be ordered by the Buyer and then delivered by the Seller.
The Seller sells and the Buyer buys Al-FPCs.
The Buyer will be become the owner of the Goods after completing the financial transaction as agreed by both parties outside of this contract in the purchase order.
1.2. This contact does not oblige the Buyer order any goods from RPE LTU. Terms and conditions for each order are agreed via sperate a Purchase Order will be agreed and signed by both parties.
1.3. For each order of Goods within this contract a Quotation needs to be sent by the Seller to the Buyer, and then a Purchase Order needs to be sent by the Buyer to the Seller as a confirmation of quotation acceptance.

1



9.2. Any written correspondence concerning this contract, such as quotations, purchase orders or legal claims will be kept in English.

10. Annexes to the Contract
10.1. The Annexes 1 is integral part of this Contract.
10.2. The Quotations from the Seller and the Purchase orders from the Buyer, received while the Contract is valid, will follow the process described in this Contract.

11. Other conditions
11.1. Contract, annexes, amendments, quotations and purchase orders sent by fax or e-mail are of legal validity.
11.2. The validity of this Contract shall be subjected to provisions arising from foreign trade legislation.

12. Date of the Contract Validity
12.1. This contract will come to validity after signing both by the Seller and by the Buyer.
12.2. The present Contract is valid for three years.

The Buyer:
UK Research and Innovation
Commercial Business Partner
D. Ward
D. Ward
23rd Sept 2024
stamp

The Seller:
Limited Liability Company "Research and production enterprise "LTU"
First Deputy Director - Chief Designer
Prof. Dr. V. Borshchov
2024
stamp

Issued on 17/05/2024
Signed on 23/09/2024

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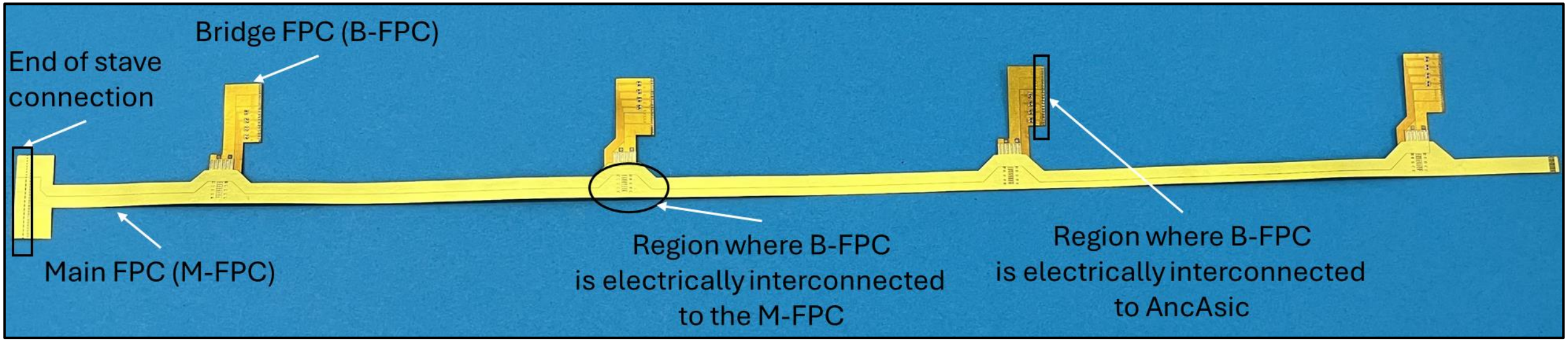
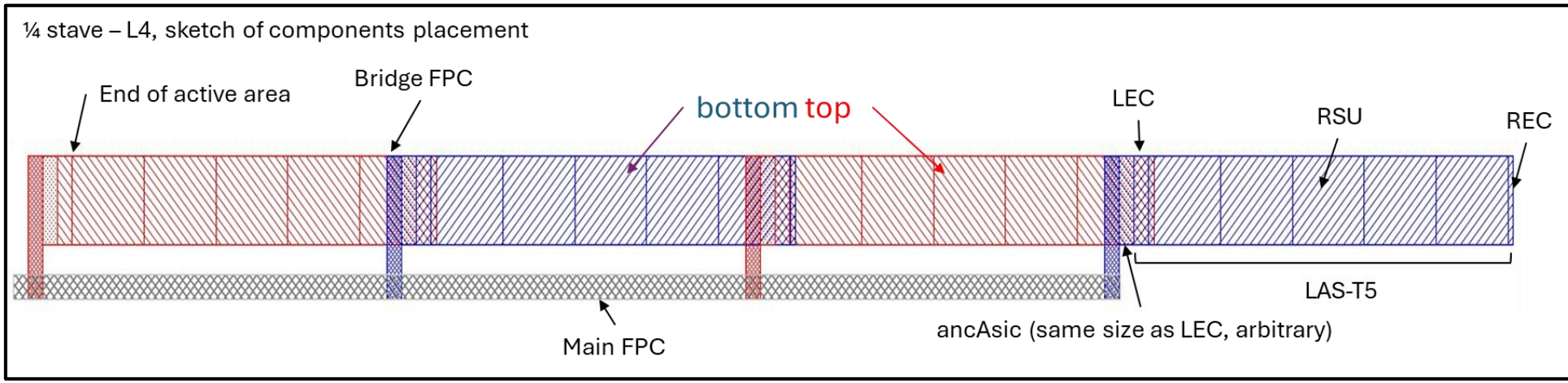
Design recap 1





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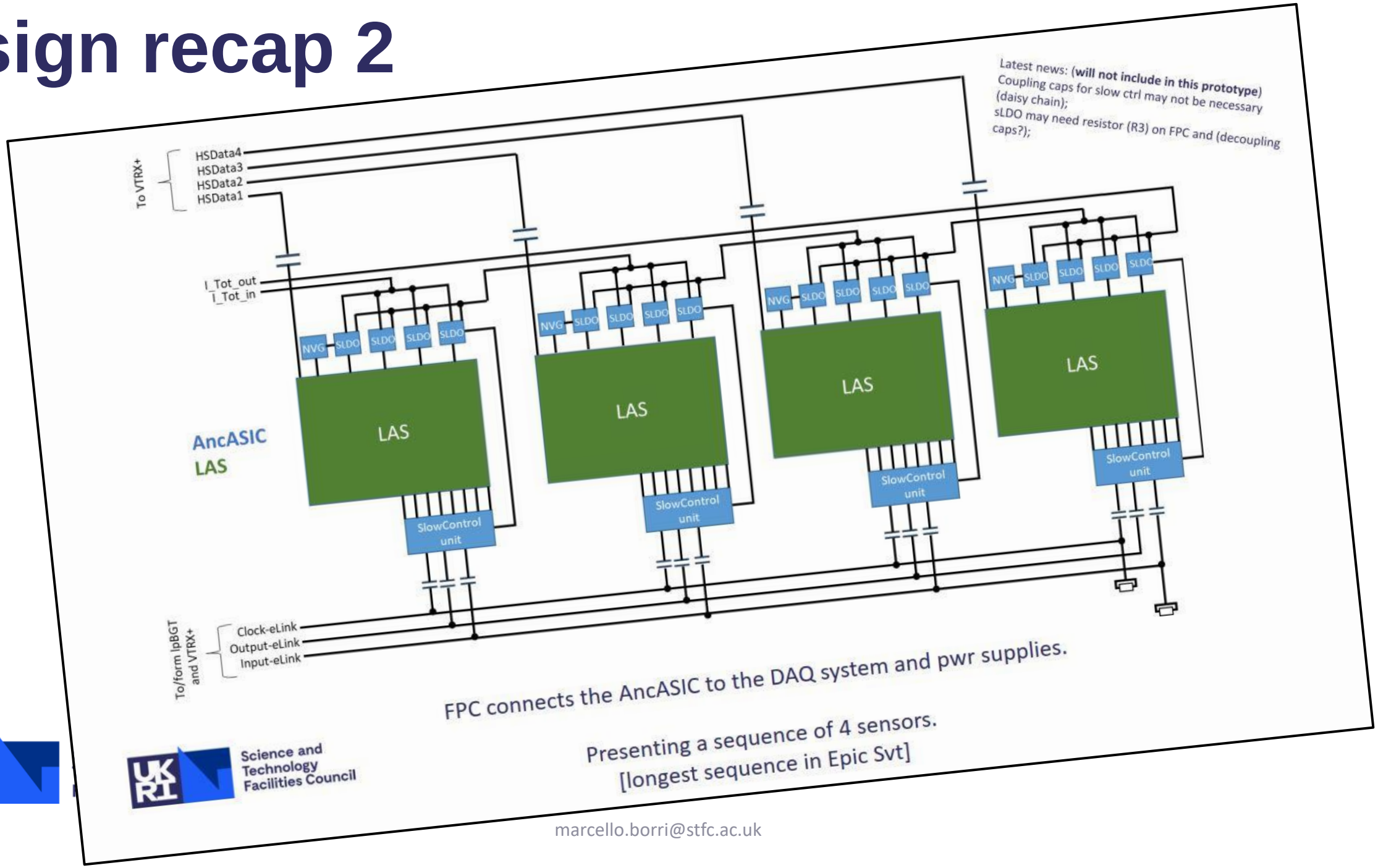
Design recap 2



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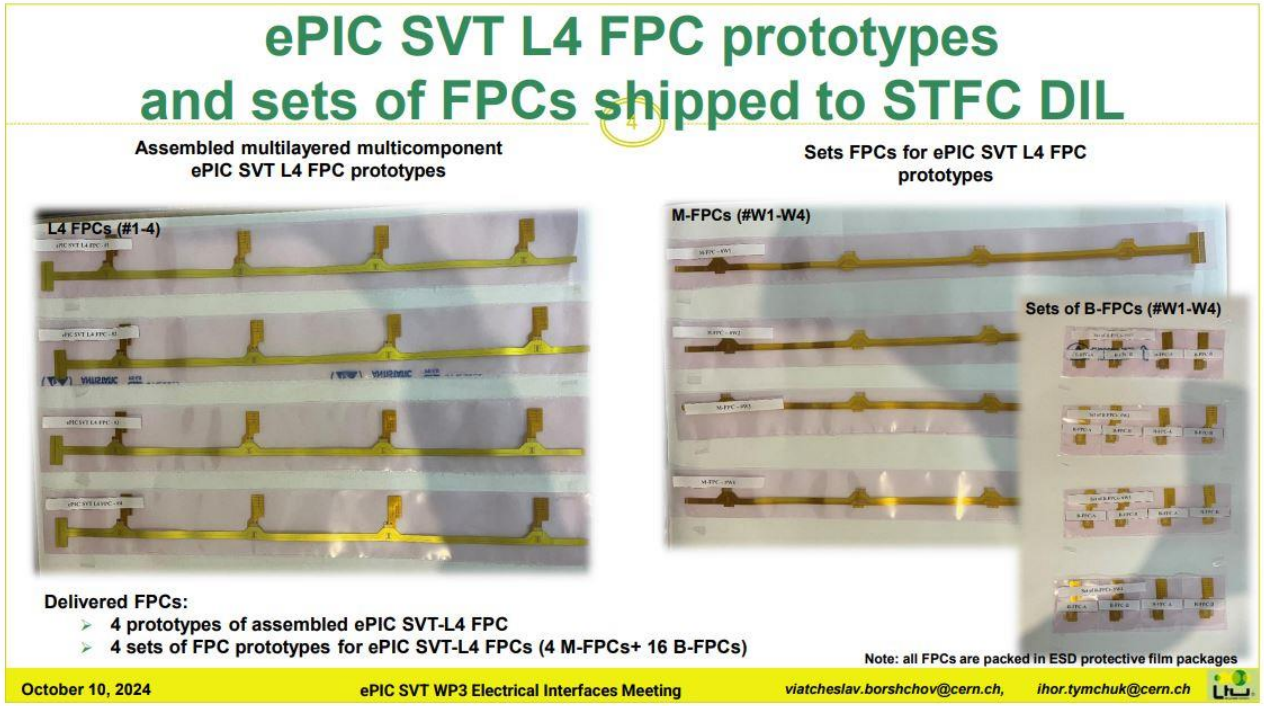
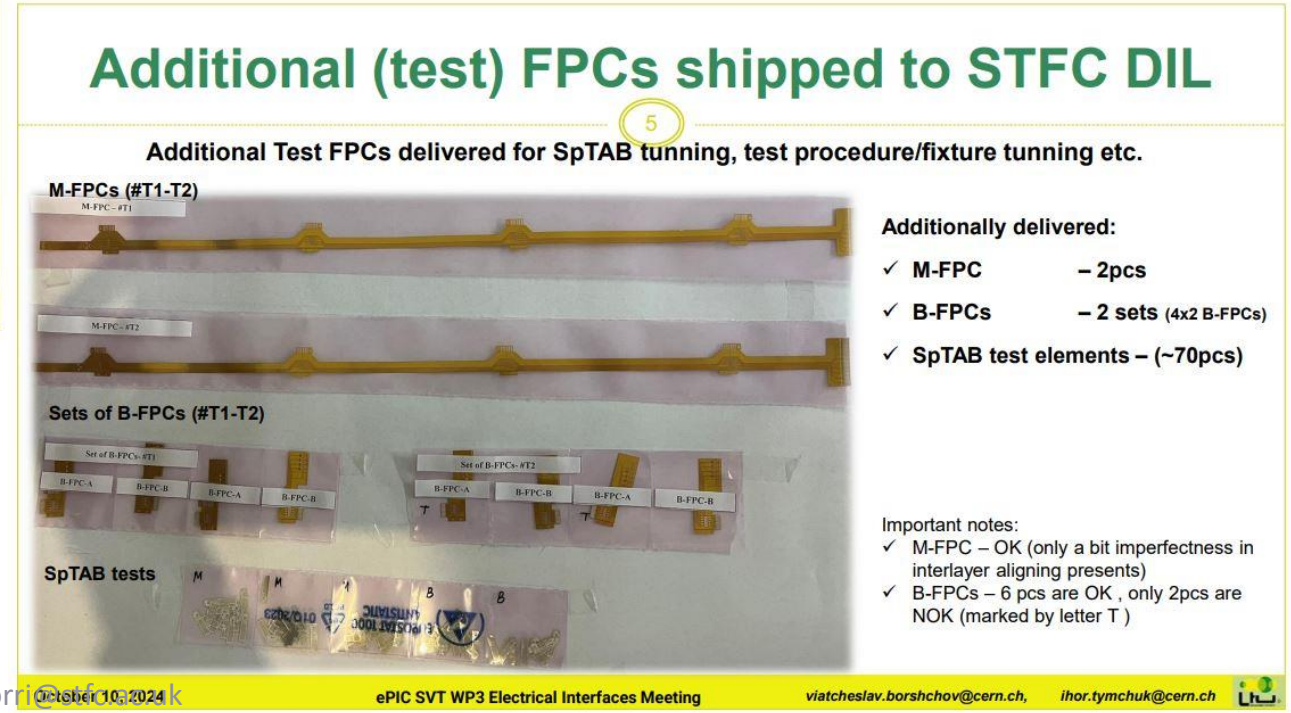
Low TRL OB L4 prototypes: LTU delivery

A lot of details in the design…

I.Tymchuk:
30 masks in total were required for M-FPC & B-FPC-A & B-FPC-B;
i.e. 10 photomasks for each FPC were required;
(usually a 2 layer FPC requires up to 6 masks)





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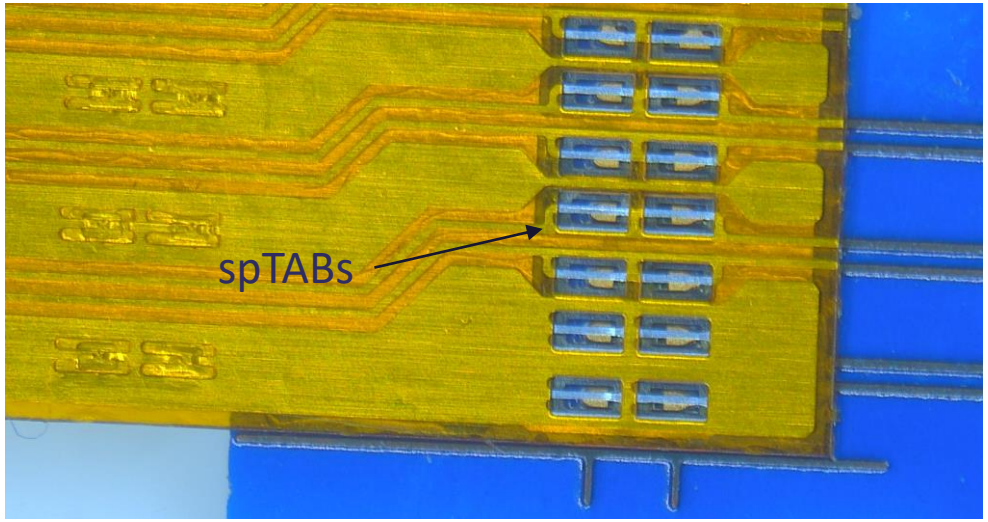
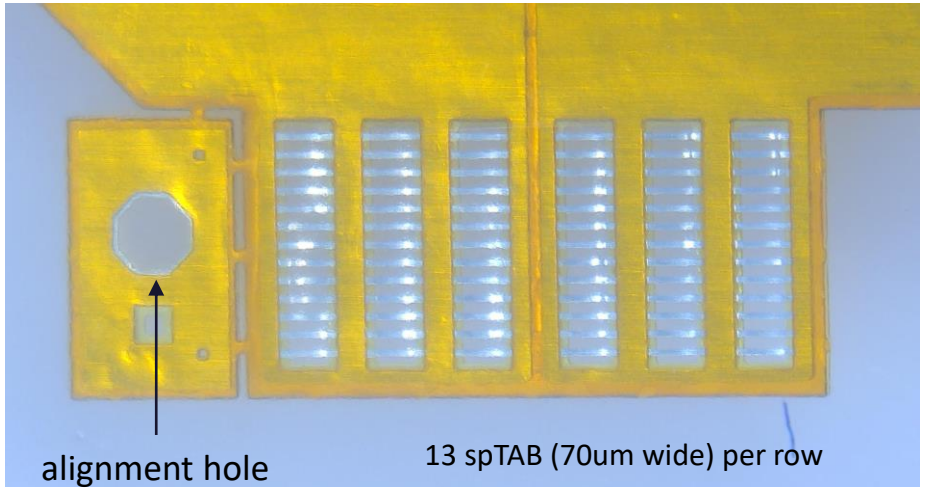
Visual inspection 1

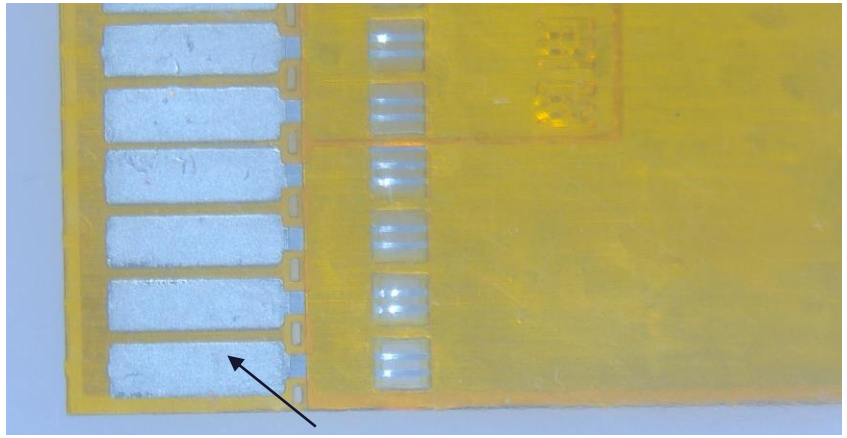
Alignment of FPC to interface PCB

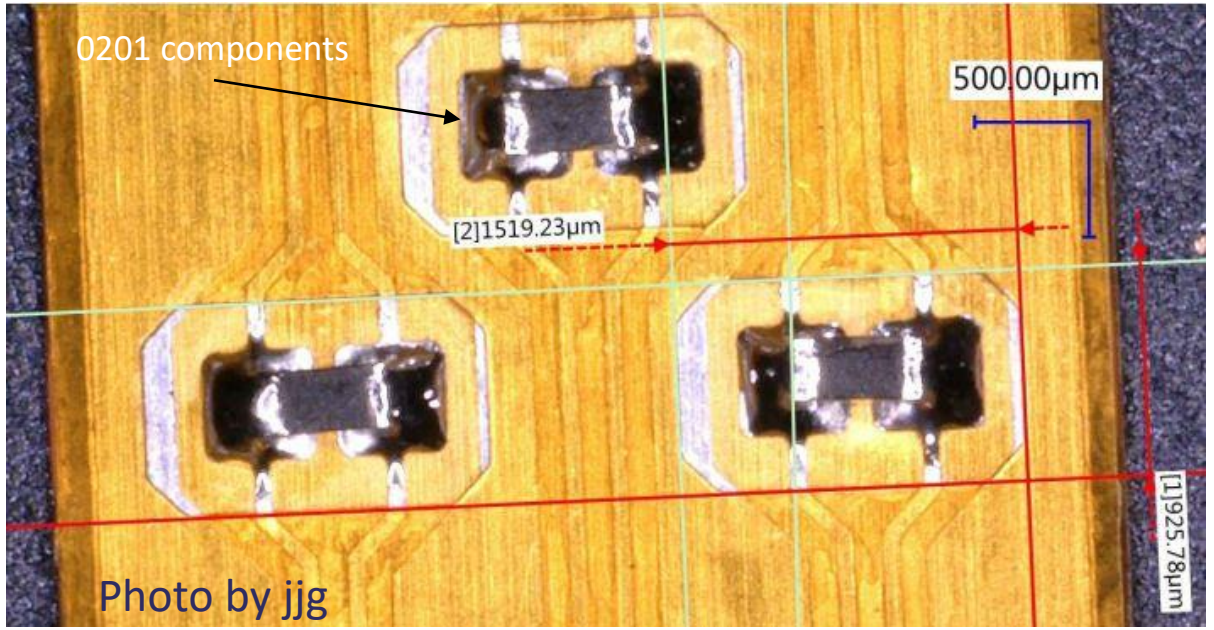


Current in/out spTABs at joint with bridge FPC



Probe pads and perforated area





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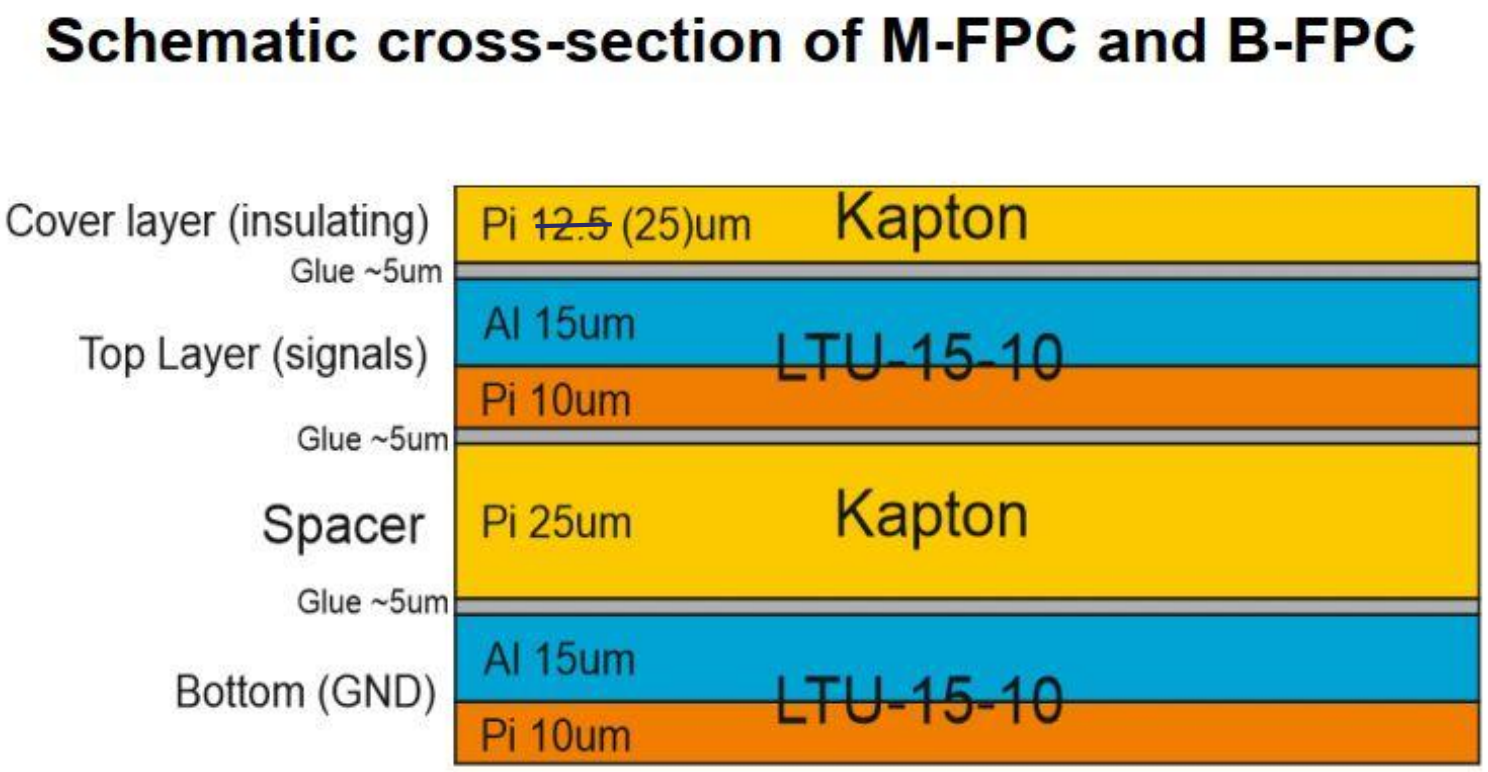
Visual inspection 2



Total = ~115um

Difference ~3.6um

Measured 111.4um

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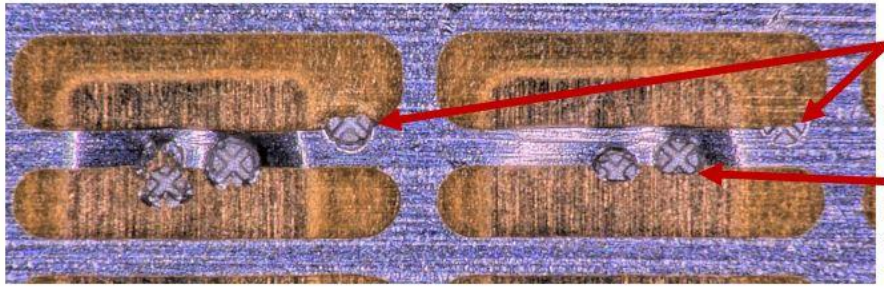
spTAB

Initial bonds

Bond machine was set up with the general 25 µm wire bonding settings:

Ultrasonic power (US): 20% Bondforce (BF): 20 cN

Deformation: 35 µm Duration: 70 ms



Initial bond position calibration needed work.

Uncentred due to Z-axis offset (movement of foil as it is pushed through the Kapton window).

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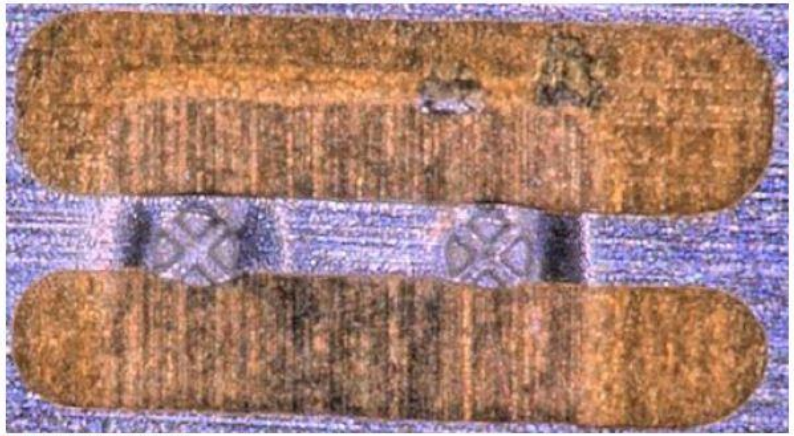
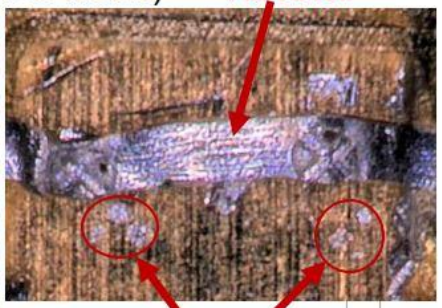
06 January 2025 OB module: ad-hoc meeting 4

Adjusting settings (US18|BF18)

Bonds look good, only slight foil breaks (likely too weak)





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06 January 2025 OB module: ad-hoc meeting 7

… components also sent to the University of Liverpool.

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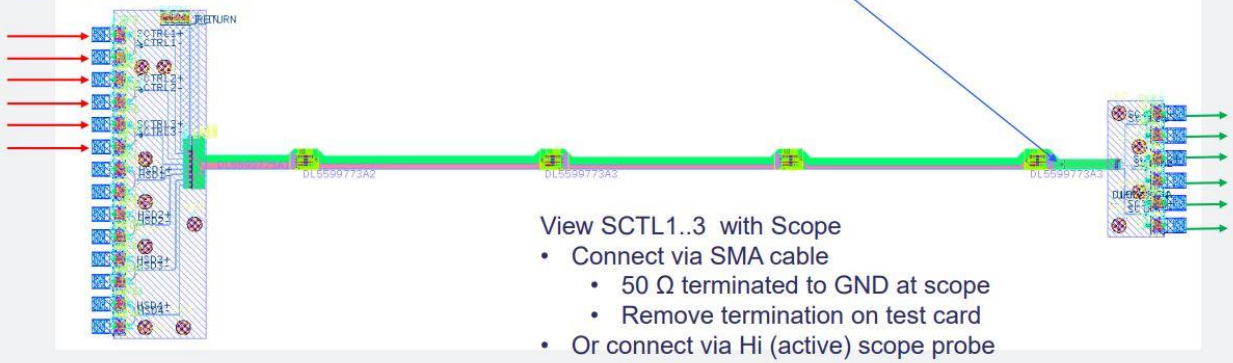
Test plan 1

- Step 1: to test stand-alone M-FPC with interface cards

Main FPC only, slow control

Inject Data or Clock and data into SCTL1…3 from KCU105 via SMA cables

Remove termination from Main FPC



View SCTL1..3 with Scope

- Connect via SMA cable
  - 50 Ω terminated to GND at scope
  - Remove termination on test card
- Or connect via Hi (active) scope probe
  - With termination on test card.
- Also consider test in reverse direction.
- Additionally test these lines at > 1 Gbits/s using iBert bitstreams and MGT.

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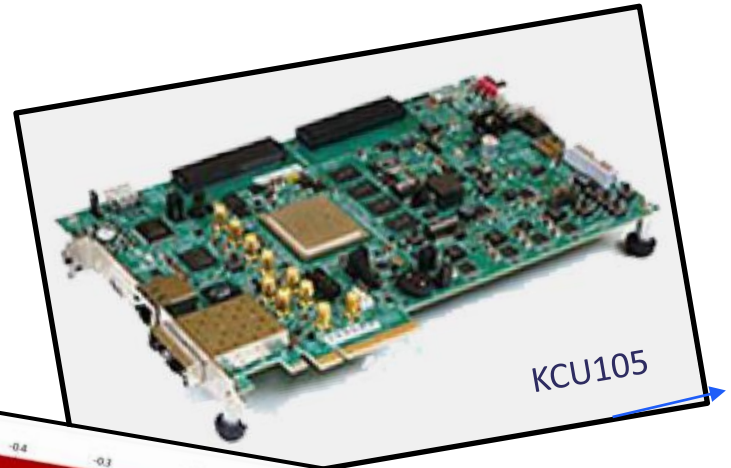

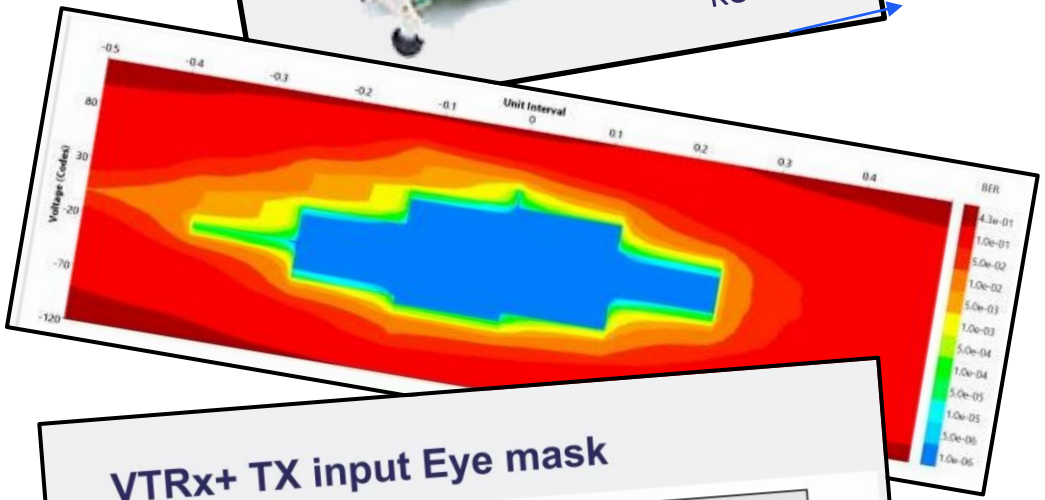

VTRx+ TX input Eye mask

Specification	Value
X1 @ UI=97.66ps	10.7 ps
X2	30.3 ps
Y1	95 mV
Y2	350 mV

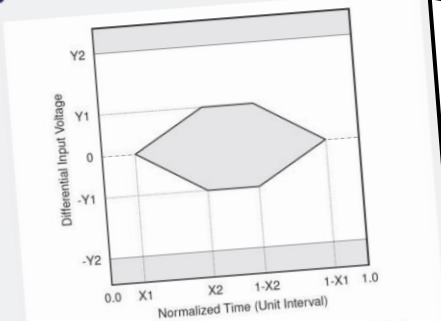

Figure 6: Electrical Eye Mask for 4.2.5 Tx Input & 4.4.5 Rx Output

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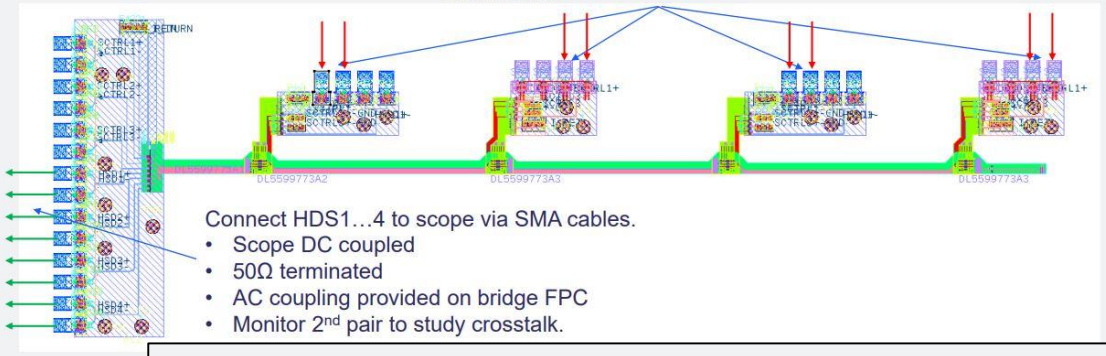
Test plan 2

High speed signals

Inject Data into HSD1..4 from KCU105 via SMA cables.



Connect HDS1…4 to scope via SMA cables.

- Scope DC coupled
- 50Ω terminated
- AC coupling provided on bridge FPC
- Monitor 2nd pair to study crosstalk.

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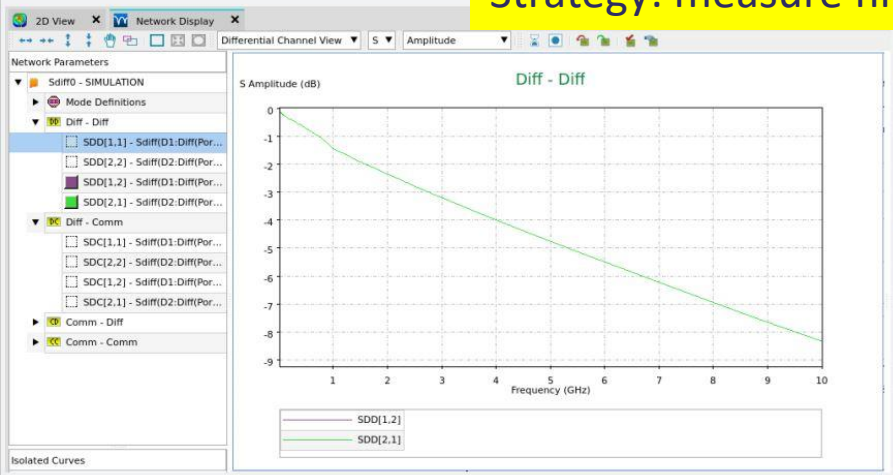
Clarity3d layout simulations of 100 mm pair

Strategy: measure first, simulate after



- -0.076 dB at 10 MHz
- = 0.99 transmission
- expect 0.97 at DC
- -8.4 dB @ 10 GHz
- Predicted -4.23
- Explained by different values of Df.
- Clarity material: Df= 0.035 @ 10 GHz

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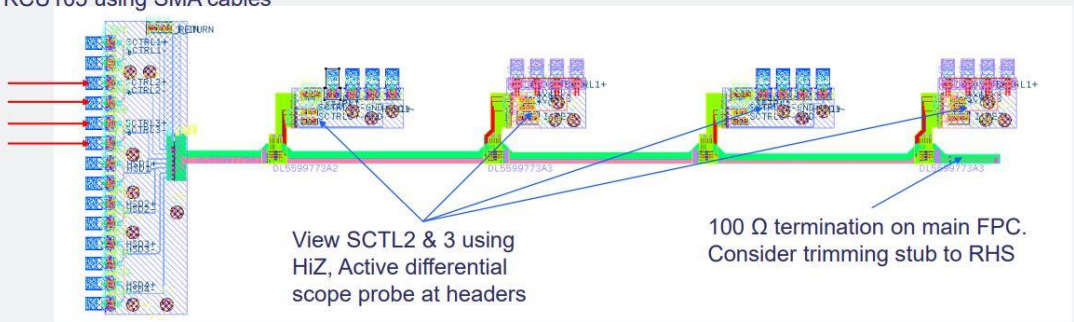
Slow Control Clock and TX data SCTL2 & 3

Inject Data or Clock and data into SCTL2…3 from KCU105 using SMA cables



View SCTL2 & 3 using HiZ, Active differential scope probe at headers

100 Ω termination on main FPC. Consider trimming stub to RHS

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- Equipment:
  - Higher spec oscilloscopes & TDR available at RAL (accessed via Oxford)
  - DL to rent similar equipment
- DUT:
  - Assembly of M-FPC & B-FPC is in progress

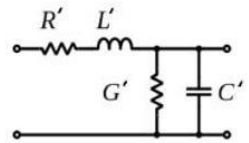
What do we test for: signal and pwr integrity

- Signal integrity.
  - The ability to propagate signals without distortions
- Factors that contribute to signal integrity degradation:
  - Reflections
    - Impedance discontinuities
  - Cross talk
    - Mutual parasitic capacitance & inductance
  - Skew
    - Propagation delays
  - Jitter
    - Non-uniform impedance, crosstalk, interference, and power supply noise
  - Signal attenuation
    - Losses caused by conductive and dielectric energy dissipation.

- Power integrity
  - Reduced Noise pick up
    - Decoupling capacitors (Equivalent Series Resistor)
    - Coherent grounding strategy over the Power Distribution Network
  - Acceptable IR drop (and related FPC power consumption)

https://www.microwaves101.com/encyclopedias/transmission-line-loss

Transmission lines – signal attenuation



Infinitesimal portion of transmission line

KCL + KVL

$$\frac{\partial v(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t}$$
$$\frac{\partial i(z,t)}{\partial z} = -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t}$$

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}$$
$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z}$$

Schematic cross-section of M-FPC and B-FPC

Let γ = α + jβ or α + j(2π/λ)

γ = complex propagation constant
α = attenuation constant (nepers/unit length)
β = phase constant (radians/unit length)
λ = wavelength
ω = angular frequency (radians/second)

$\alpha = \alpha_C + \alpha_D + \alpha_G + \alpha_R$
α_C = loss due to metal conductivity
α_D = loss due to dielectric loss tangent
α_G = loss due to conductivity of dielectric
α_R = loss due to radiation

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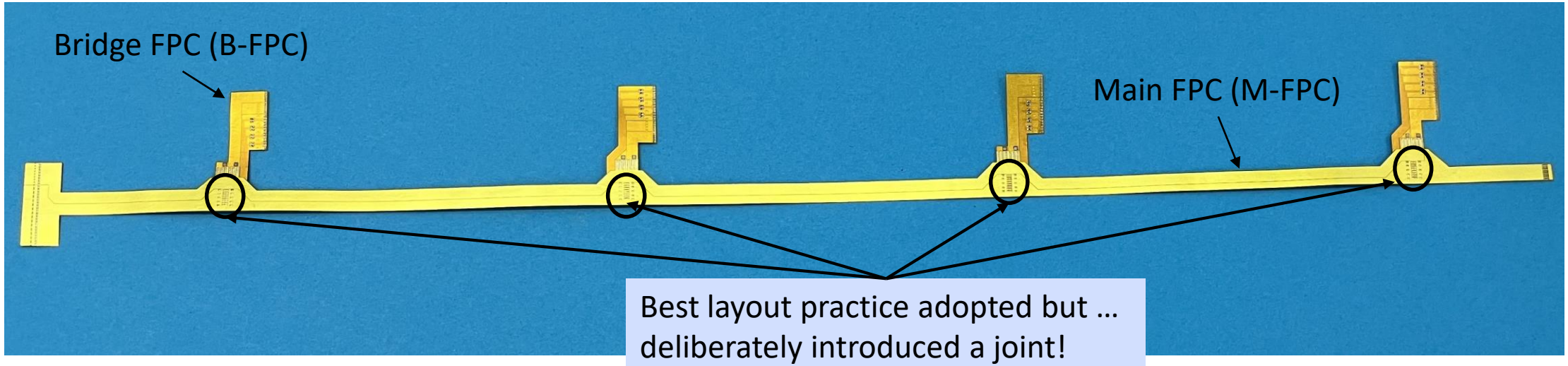
Signal integrity: layout dependent



The most important cause of signal integrity issues in a PCB is faster signal rise times.

Signal name	Type	Comment	Coupling	Standard	lpGBT eLink	Rate
slow ctrl clk (down)	AC	from lpGBT to AncASIC	Capacitive	CERN Low Powering Signal (CLPS)	clock-eLink	80 Mb/s
slow ctrl write (down)	AC	from lpGBT to AncASIC	Capacitive	CERN Low Powering Signal (CLPS)	output-eLink	80 Mb/s
slow ctrl read (up)	AC	from AncAsic to lpGBT	Capacitive	CERN Low Powering Signal (CLPS)	input-eLink	160 Mb/s
data	AC	from AncAsic to VTRX+ (1 diff line/AncASIC)	Capacitive	CERN Low Powering Signal (CLPS)	N/A	5.12 Gb/s (o 10Gb/s)
voltage supply	DC	Max: (2.5V/AncASIC) * (4 AncASIC)	Direct	10% Vdrop for 2.5V/LAS, is it OK?	N/A	N/A
current	DC	2.5 A (total per AnASIC)	Direct		N/A	N/A

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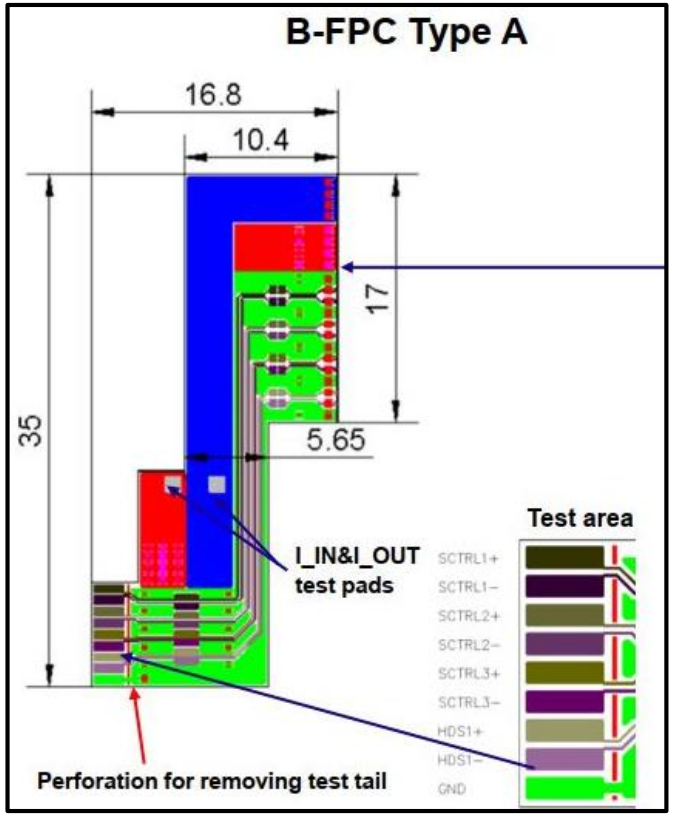
Q-flex

LANL ordered a copy of the B-FPC (type A) via Q-flex.

- To be delivered;

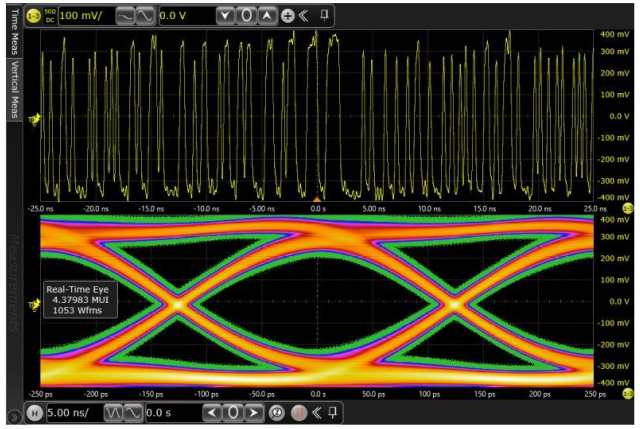
Q-flex compromised on several features of the original design:

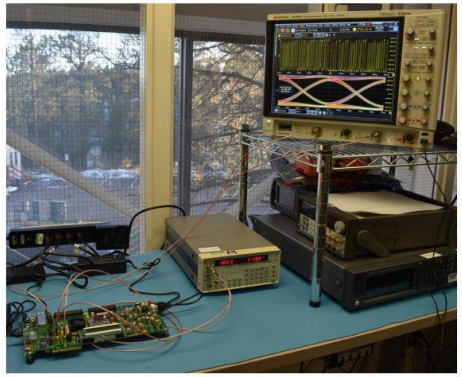
- ❖ mounting of passive components;
- ❖ surface finish;
- ❖ differential tracks impedance changed to 150 Ohm;



Test setup: available

Results from 4Gbps PRBS generate by KC705





Stack-up

	12um polyimide	Top Coverlay
	25um adhesive	
	L1 17um Aluminium	0.7mil Aluminium with Kapton
	12um adhesive	
	12um Polyimide	
	25um adhesive	Bondply
	25um polyimide	
	25um adhesive	
	12um Polyimide	0.7mil Aluminium with Kapton
	12um adhesive	
	L2 17um Aluminium	
	25um adhesive	Bottom Coverlay
	12um polyimide	
Flex Thickness	~233um +/-10%	

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Next steps

- To start ASAP the electrical characterization of Low TRL OB L4 prototypes;
- To perform comparative interconnection test between wire-bonding and spTAB bonding via ad-hoc daisy chain structures from LTU;
- To complete evaluation of Q-flex;
- Design the next iteration of OB prototypes, in progress (linked to module design).

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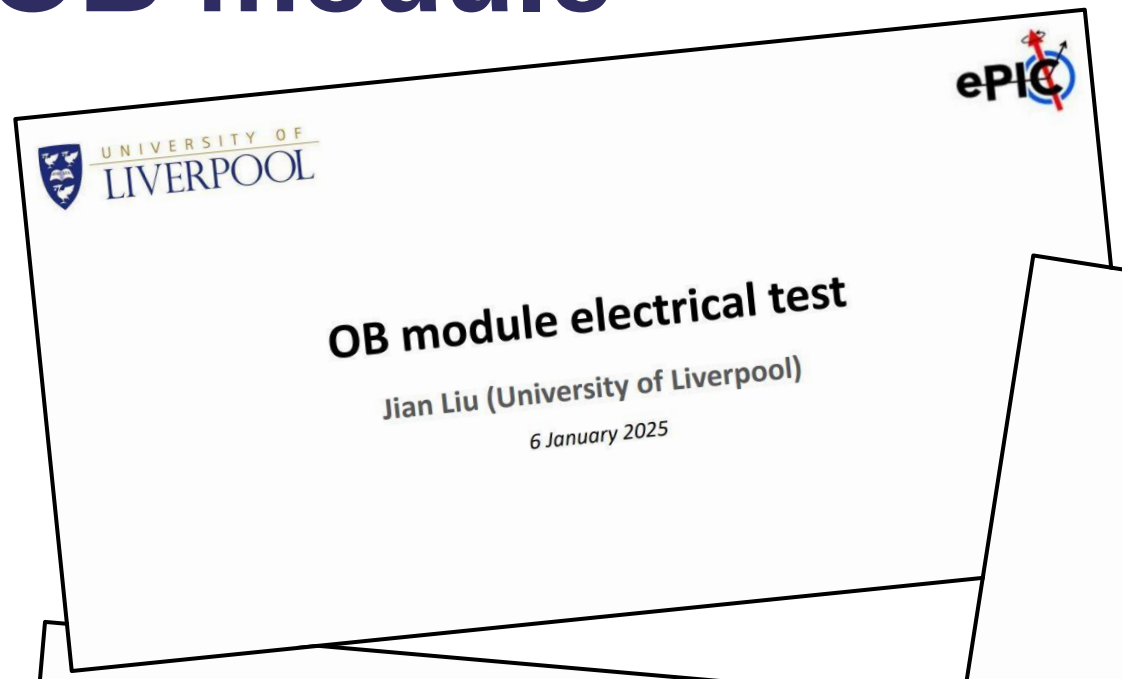
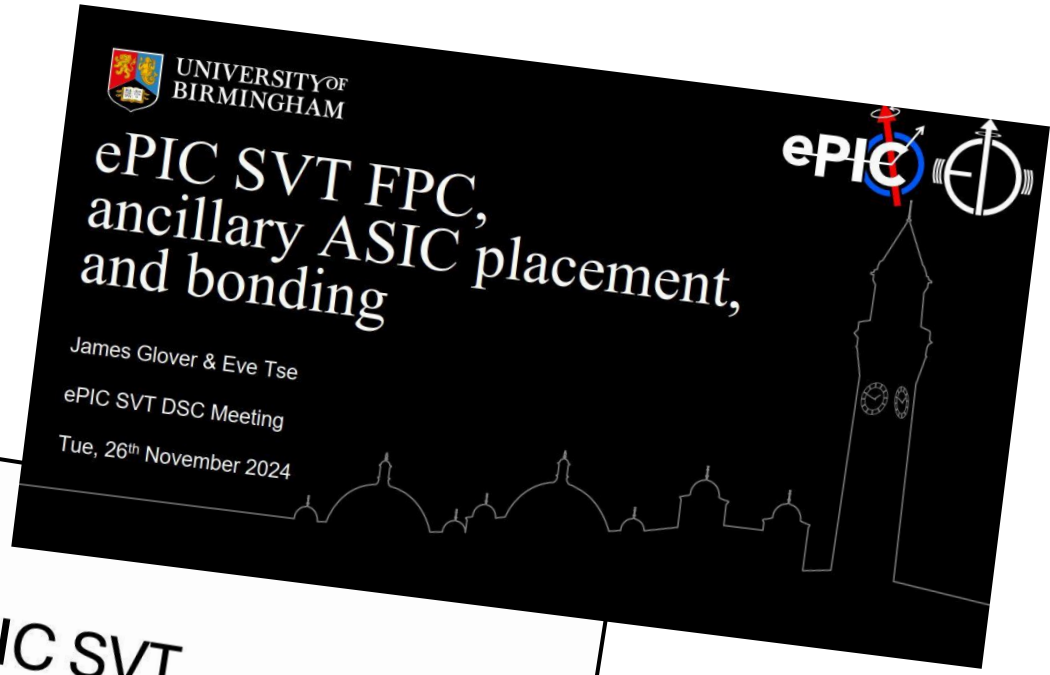
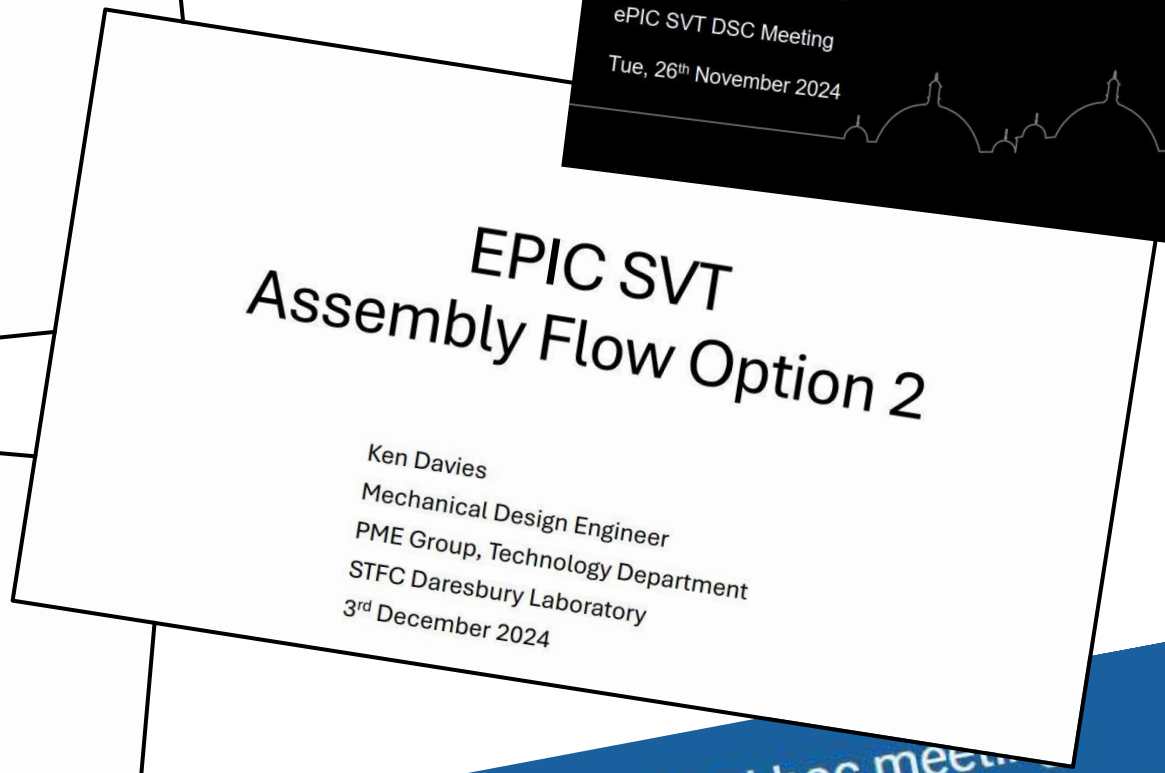
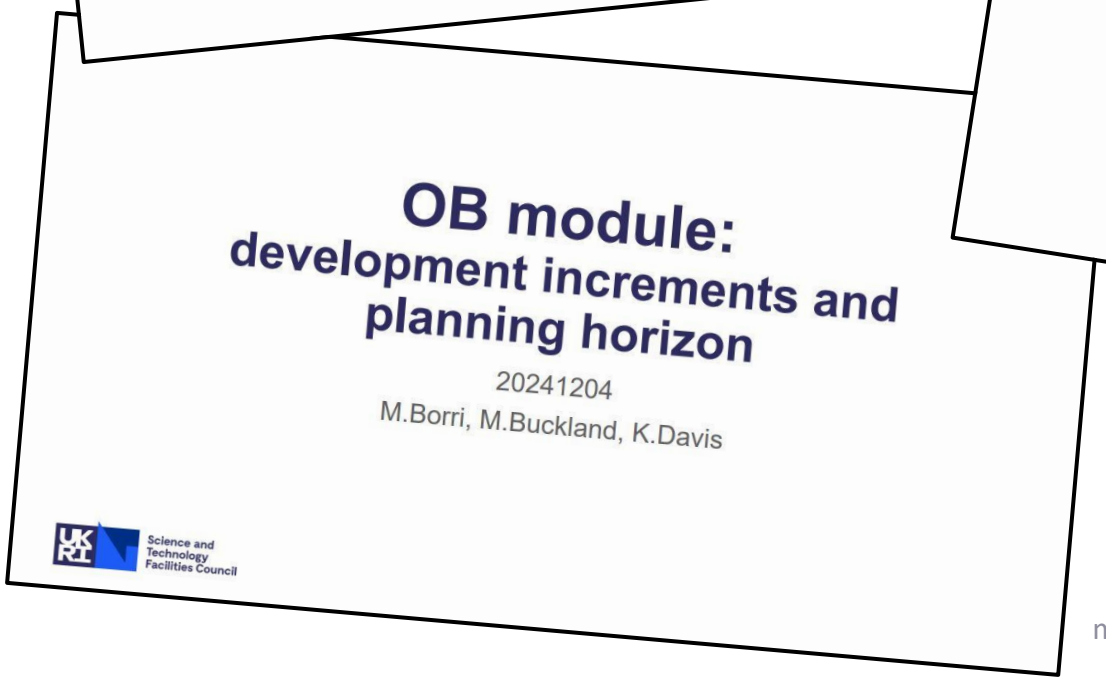
OB module









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Disks

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Overview

- LBNL progressing prototyping with Omni Circuit Boards (CA);
- Two iterations completed with supplier;
- A third iteration under development;

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1st iteration

- Design based on a PCB from another project;
- Pads were OK for wire-bonding, not for soldering
- Significant signal loss was measured

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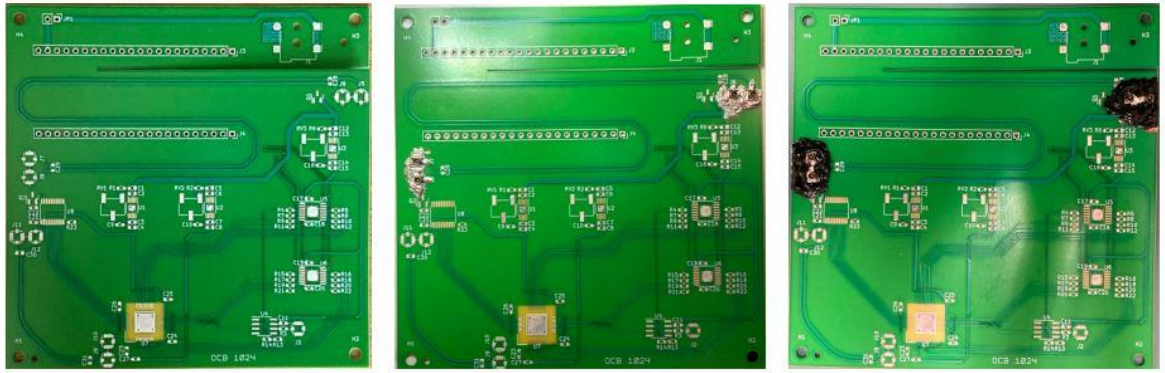
First Low TRL Prototypes



- Connectors were mounted via non-standard methods (removing the soldermask, epoxies).

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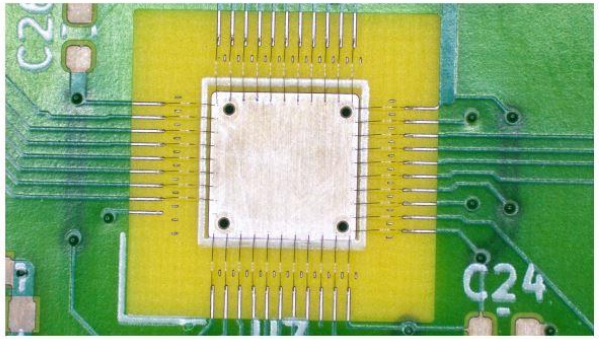
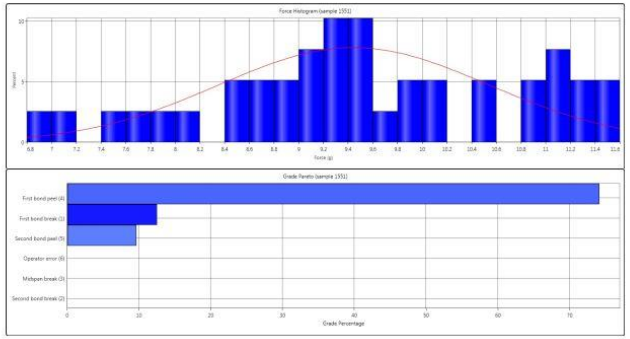
Wire-bonding and Pull Tests





- Number of tests: 39
- Mean - 3 * standard deviation: 5.7782 g
- Minimum load: 6.9011 g
- Maximum load: 11.570 g
- Mean: 9.5195 g
- Standard Deviation: 1.2471 g

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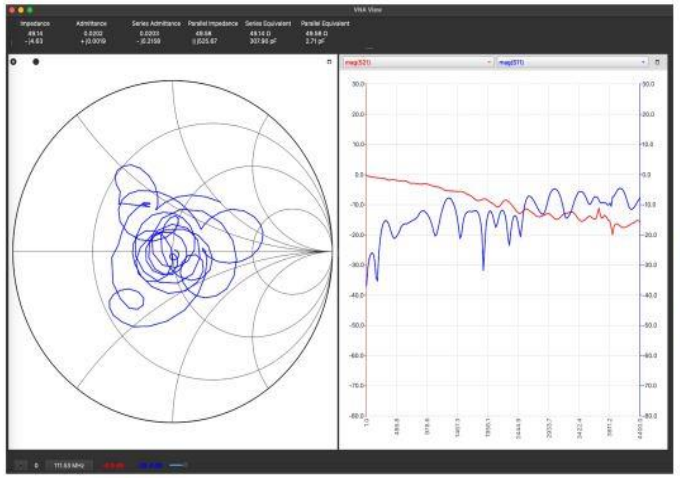
Single-ended VNA Measurements



$$\alpha_d = 0.9106 \times \sqrt{\epsilon_R} \times F_{GHz} \times tan\delta \quad \text{(dB/cm)}$$

	polyimide	ArlonEMD	soldermask
Dk	0.9106	0.9106	0.9106
	3.76	4.3	3.6
	1	1	1
Df	0.017	0.0036	0.025
dB/cm	0.030017	0.006798	0.043194

- More signal loss than expected

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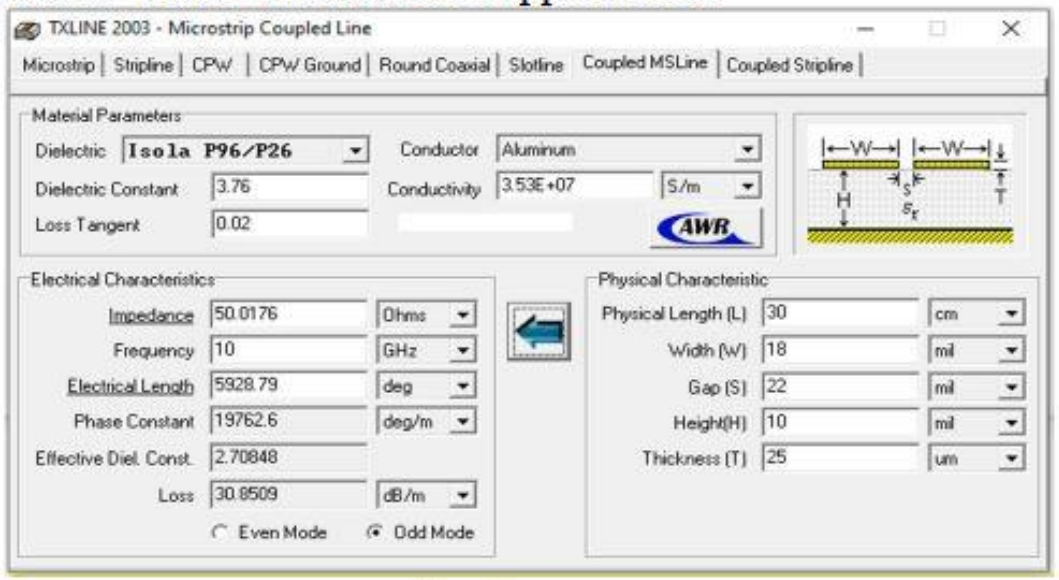
Al-based FPC (Yuan Mei)

Constraints from vendor

- Prefer 1mil thick Polyimide-fiber glass substrate (Isola);
- Prefer 20μm Al - 8μm Cu - Polyimide stack. Can be without Cu, but Al - Polyimide adhesion is weak.
- Prefer burying traces between substrates for added strength. 5mil/5mil width/spacing in small area, 7mil/7mil for long traces.
- Not support SMD soldering. Al in a few small places can be plated with 5μm copper for solder.
- 0.016" wide (minimum) cutout. Plated vias must be copper based.



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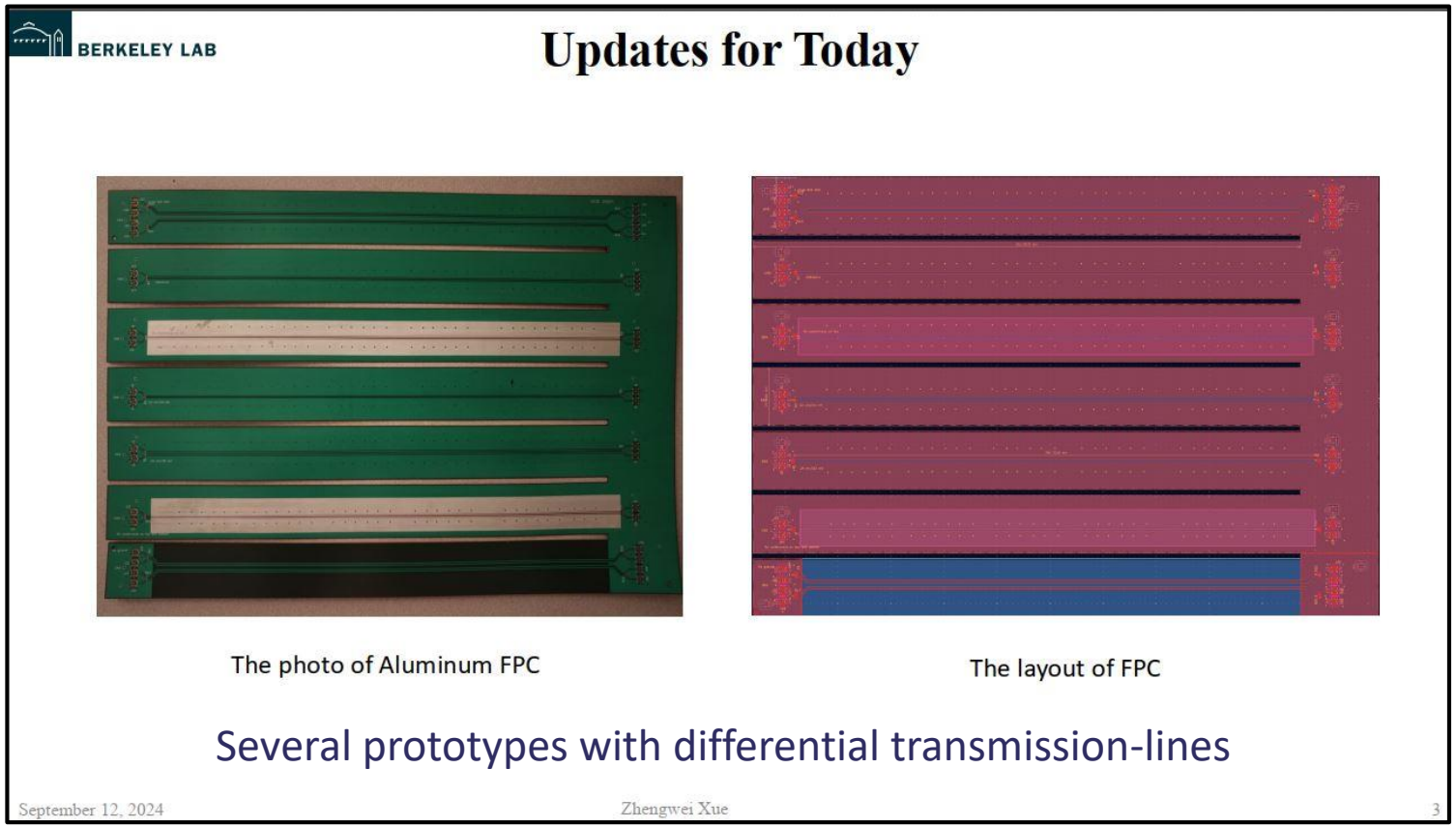
2nd iteration

- Dedicated to signal transmission investigation:
  - understand and improve signal losses: different substrate materials, different width/pitch, with and without soldering mask;
- Use of selective Cu plating for soldering
- Make plated-thru holes in an all-aluminium stack



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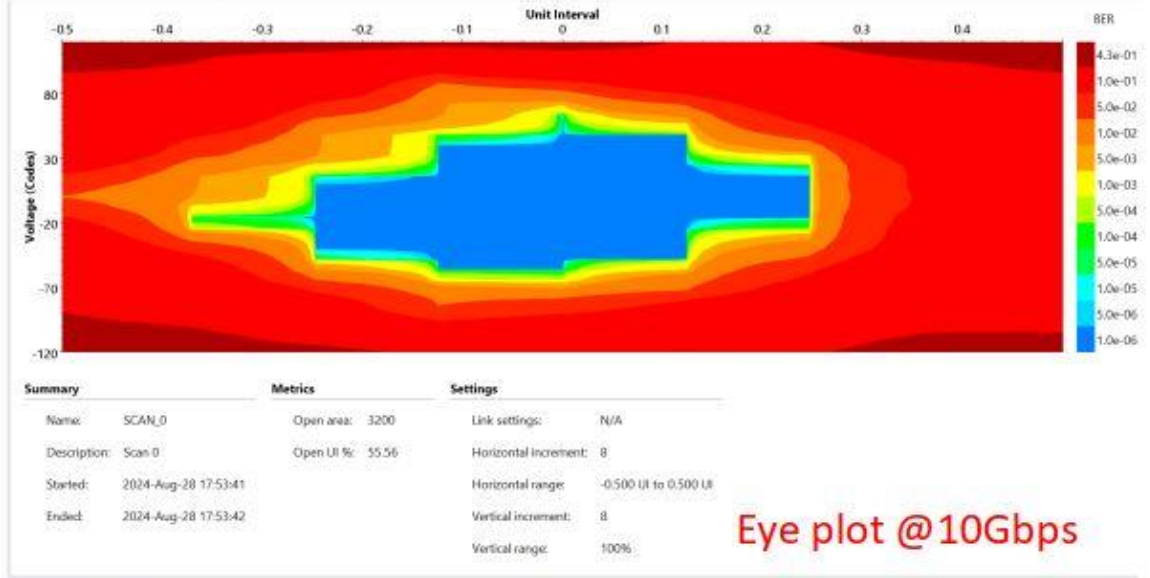
Updates for Today

- Received a 2nd set of Al-based FPC prototypes from OMNI.
  - Double metal layer with 25 cm long differential lines for high-speed data transmission
- Improvements compared to the previous set
  - Soldering and vias facilitated by selective Cu plating
  - Improved high frequency signal transmission property based on S21 measured up to 4 GHz
  - IBERT test done with FPGA suggests that these FPC support GTY communication @10Gbps
- Questions to follow up:
  - Check the mechanical properties of the FPC
  - 2 out of 36 connector pads detached from the FPC when disconnecting the cable
  - Total material budget of the FPC is 0.136% X_0 (TBC), with dominant contribution from dielectrics. Can this be reduced
- Plan:
  - Manufacture FPC based on LTU/STFC design but modified to be consistent with vendor's design rules if there is no objection.



Eye plot @10Gbps

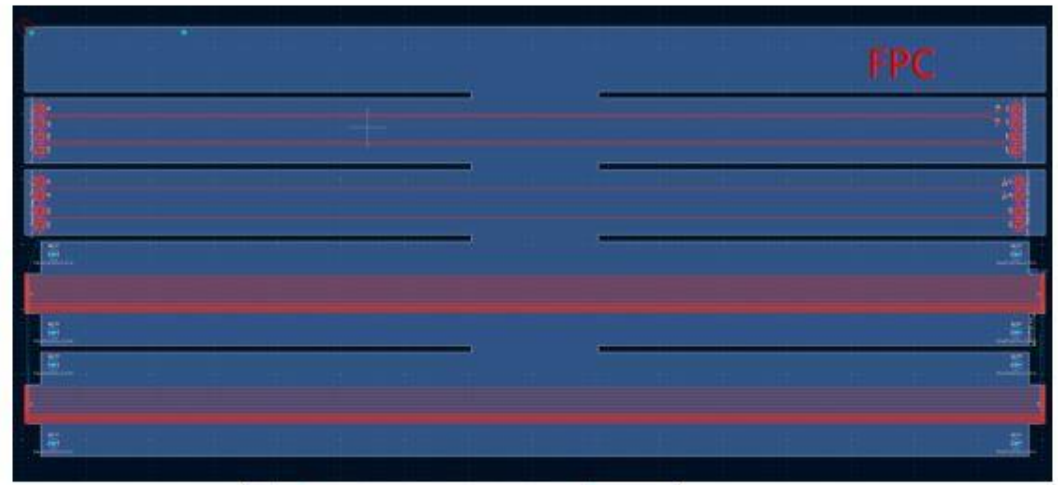
*Dielectric substrate is ArlonEmd

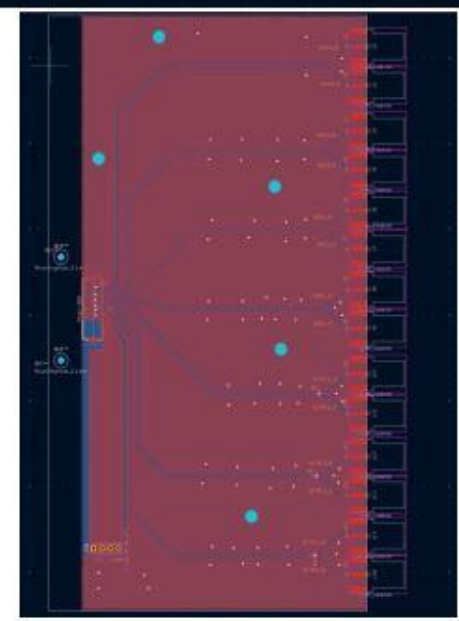
Updates for Today

- The 3rd set of FPC is still under design:
  - Discussing with OMNI about the plan to optimize material budget (in progress);
  - Two strips have interface pins that share the same structure as the LTU/STFC design;
  - Corresponding interface board;
  - Two strips are used to test the effect of AC coupling on the signal;
  - One strip for the physical property test;
  - No spTAB bonding;
  - Minimum trace width/distance is 6/6 mil.

(150/150 µm)

- Plan:
  - Manufacture FPC and interface board as soon as we confirm the material budget optimization plan.





Interface board

Conclusion

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Conclusion

- Prototyping of FPCs for IB, OB and disks in progress.
- WP3 community active and engaged.
- Key questions to data transmission Vs fabrication technologies to be fully assessed.

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Thank you

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